AD1989A
High Definition Audio SoundMAX Codec

Data Sheet

DSH-202088A
March 2009

CONEXANT

Ordering Information

Device Set Order ID	Package Type	Package	Operating Temperature
AD1989AJCPZ*	QFN	48-Lead QFN, 7x7 mm	0°C to 70°C
*Lead-free (Pb Free) and RoHS compliant			

Revision History

Revision	Date	Description
A	March 2, 2009	Initial release

AD1989A

High Definition Audio SoundMAX Codec

The AD1989A audio codec and SoundMAX® software provide superior HD audio quality that exceeds Vista Premium performance. The AD1989A has eight 101 dB DACs and six 92 dB ADCs, three stereo headphone ports, C/LFE swapping, a 2-channel digital microphone interface, digital and analog PCBeep, two independent S/PDIF outputs, and a S/PDIF input, making the AD1989A the right choice for PCs where performance is the primary consideration.

The jack retasking feature on this product supports various configurations including 5.1 on 3 jacks, and front panel jack retasking.

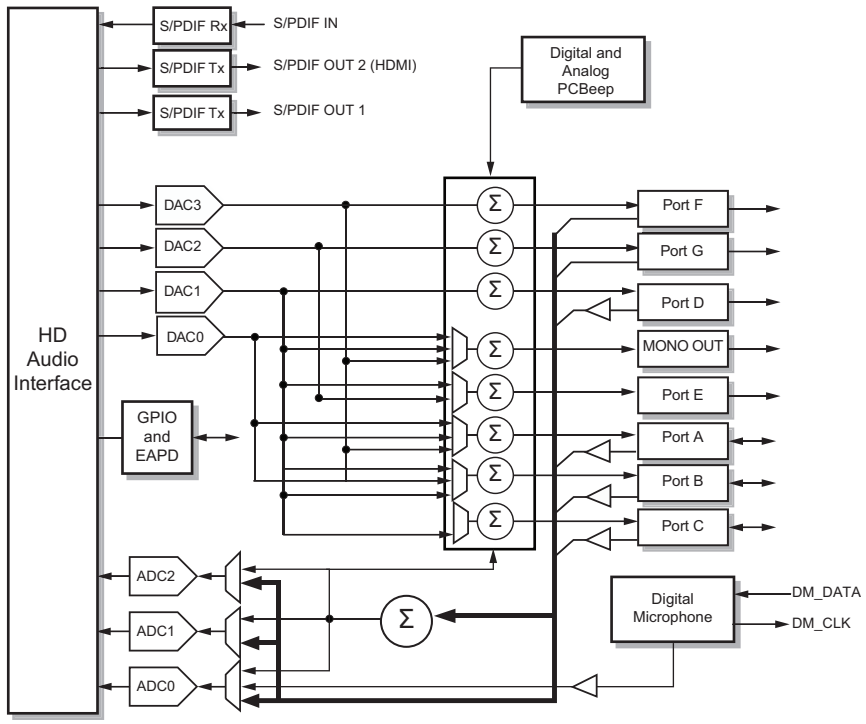
The AD1989A is available in a 48-lead RoHS compliant lead frame chip scale package in both reels and trays. See the Ordering Information table on the previous page.

Special Software Features

The AD1989A audio codec also supports the following additional software features:

- Supports WaveRT (Vista) and WDM, 32-/64-bit
- BlackHawk® and SoundMAX GUI contain all user audio controls
- Voice input enhancements: Andrea Electronics best-in-class noise reduction, beam forming, and echo cancellation
- Output enhancements: Sensaura/Sonic Focus, spreading/downmixing, MP3 refinement, adaptive dynamics, compressor/limiter, speaker/graphic EQ, Voice Clarity/X-MatrixTM, AGC, UI tuning tools
- DTS®, SRS®, EAX for gaming

Functional Block Diagram



Distinguishing Features

- Eight 192 kHz, 101 dB DACs
  - 5.1 surround sound plus independent headphone
  - All independent sample rates, 8 kHz through 192 kHz
  - Selectable stereo mixer on outputs
  - 16-, 20-, and 24-bit resolution
- Six 192 kHz, 92 dB ADCs
  - Simultaneous record of up to 3 stereo channels
  - All independent sample rates, 8 kHz through 192 kHz
  - 16-, 20-, and 24-bit resolution
- S/PDIF output
  - 2 independent transmitters, second S/PDIF can support external HDMI interface
  - Supports 44.1 kHz through 192 kHz sample rates
  - 16-, 20-, and 24-bit data; PCM, and AC3 formats
  - Digital PCM gain control
- S/PDIF input
  - Supports 44.1 kHz through 192 kHz sample rates
  - 16-, 20-, and 24-bit data; PCM, and AC3 formats
  - Digital PCM gain control
  - Auto synchronizes to source sample rate
- Stereo digital microphone
  - Two 192 kHz digital microphone channels
  - Supports 1 or 2 microphones on 1 pin
  - Selectable bit clock rates of 1.5 MHz, 2.0 MHz, and 3.0 MHz
  - All sample rates, 8 kHz through 192 kHz
  - 16-, 20-, and 24-bit resolution
- Dedicated auxiliary pins
  - Stereo CD/auxiliary I/O port w/ GND sense
  - MONO_OUT pin for internal speaker with EAPD support
- Microsoft Vista Premium® logo
- Presence detection up to 9 jacks
- Three stereo headphones
- Impedance and presence detection; retasking
- 5 adjustable microphone bias pins
- 3 general-purpose digital I/O (GPIO) pins

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- Digital and analog PCBeep
- Multiple EAPD pins for external circuit control
- 3.3 V analog and digital supply voltages
- 1.5 V and 3.3 V HD Audio link signaling
- Advanced power management modes

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High Definition Audio SoundMAX Codec

This data sheet provides a general overview of the AD1989A SoundMAX codec's architecture and functionality. Additional information on the AD1989A is available in the *AD1989A Programmers Reference Manual*. Please contact your local Conexant sales representative for more information.

1.1 Jack Configuration

Use the guidelines shown in Tables 1 through 3 when selecting ports for particular functions.

Table 1. Typical Desktop Applications with Discreet Jacks (Default Configuration)

Port	Function
Port A	Front Panel Headphone
Port B	Front Panel Microphone
Port C	Rear Line-In
Port D	Rear Line-Out
Port E	Rear Microphone
Port F	Rear Surround (5.1)
Port G	Rear C/LFE

Table 2. Typical Desktop Retasking to Support Shared Input/5.1 Jacks

Port	Function
Port A	Front Panel Headphone
Port B	Front Panel Microphone
Port C	Rear Line-In/Surround Out
Port D	Rear Line-Out
Port E	Rear Microphone/C/LFE

Table 3. Typical Notebook Application

Port	Function
Port A	Headphone Jack
Port B	Microphone Jack
Port C	Internal Analog Microphone (optional)
Port D	Dock Line-Out/Headphone
Port E	Dock Line-In
Port F	Internal Speakers
Digital Microphone	Internal Digital Microphone

1.2 Specifications

Table 4. Test Conditions

Parameter	Test Condition
Temperature Digital Supply Analog Supply MIC_BIAS_IN (via Low-Pass Filter) Sample Rate f_S Input Signal (Frequency Sine Wave) Amplitude for THD + N Analog Output Pass Band	25°C 3.3 V 3.3 V 5.0 V 48 kHz 1008 Hz –3.0 dB Full Scale 20 Hz to 20 kHz
DAC	10 kΩ Output Load: Line-Out Tests 32 Ω Output Load: Headphone Tests
ADC	0 dB Gain

Table 5. Performance

Parameter	Min	Typ	Max	Unit
Line-Out Drive (10 kΩ loads—DAC to Pin) Total Harmonic Distortion (THD + N) Dynamic Range (–60 dB in ref to f_S A-Weighted) Signal-to-Noise Ratio		 –86 101 101		 dB dB dB
Headphone Drive (32 Ω loads—DAC to Pin) Total Harmonic Distortion (THD + N) Dynamic Range (–60 dB in ref to f_S A-Weighted) Signal-to-Noise Ratio		 –84 101 101		 dB dB dB
Input Ports (Mic Boost = 0 dB) Total Harmonic Distortion (THD + N) Dynamic Range (–60 dB in ref to f_S A-Weighted) Signal-to-Noise Ratio		 –80 92 92		 dB dB dB

***Table 6. General Specifications** (1 of 4)*

Parameter	Min	Typ	Max	Unit
Digital Decimation And Interpolation Filters—f_S = 8 kHz to 96 kHz[1]				
Pass Band	0		0.4 f_S	Hz
Pass-Band Ripple			±0.005	dB
Stop Band	0.6 f_S			Hz
Stop-Band Rejection			–110	dB
Group Delay		20		$1/f_S$
Group Delay Variation Over Pass Band		0		µs
Analog-to-Digital Converters				
Resolution		24		Bits
Gain Error (Full-Scale Span Relative to Nominal Input Voltage)[2]			±10	%
Interchannel Gain Mismatch (Difference of Gain Errors)		±0.2	±0.5	dB
ADC Offset Error[1]			±5	mV
ADC Crosstalk[1]				
Line Inputs (Input L, Ground R, Read R; Input R, Ground L, Read L)		–94		dB
Line Inputs to Other		–100	–80	dB
Digital-to-Analog Converters				
Resolution		24		Bits
Gain Error (Full-Scale Span Relative to Nominal Input Voltage)[1]			±10	%
Interchannel Gain Mismatch (Difference of Gain Errors)			±0.5	dB
DAC Crosstalk (Input L, Zero R, Measure R_OUT; Input R, Zero L, Measure L_OUT)[1]		–104		dB
DAC Volumes				
Step Size		1.5		dB
Output Gain/Attenuation Range	–58.5		0	dB
Mute Attenuation of 0 dB Fundamental[1]		–80		dB
ADC Volumes				
Step Size		1.5		dB
PGA Gain/Attenuation Range	–58.5		+22.5	dB
Mute Attenuation of 0 dB Fundamental[1]		–80		dB

***Table 6. General Specifications** (2 of 4)*

Parameter		Min	Typ	Max	Unit
Analog Mixer					
Signal-to-Noise Reduction (SNR) Input to Output			95		dB
Step Size: All Mixer Inputs			1.5		dB
Input Gain/Attenuation Range: All Mixer Inputs		–34.5		+12.0	dB
Analog Line Level Outputs					
Full-Scale Output Voltage: Line-Out Drive Enabled		1.0			Vrms(3)
Ports A, D, E, F, and Mono Out		2.83			V p-p
	Output Impedance(1)		190		Ω
	External Load Impedance(1)	10			kΩ
	Output Capacitance(1)		15		pF
	External Load Capacitance(1)			1000	pF
Analog HP Drive Outputs					
Full-Scale Output Voltage: Line-Out Drive Enabled		1.0			Vrms(3)
	Output Impedance(1)			0.5	Ω
	External Load Impedance(1)	32			Ω
	Output Capacitance(1)		15		pF
	External Load Capacitance(1)			1000	pF
Analog Inputs					
Input Voltages—Ports A, B, C, or E					
	Mic Boost = 0 dB		1 2.83		Vrms(3) V p-p
Input Voltages—Microphone Boost Amplifier, Ports B, C, or E	Mic Boost = +10 dB		0.316 0.894		Vrms(3) V p-p
	Mic Boost = +20 dB		0.1 0.283		Vrms(3) V p-p
	Mic Boost = +30 dB		0.032 0.089		Vrms(3) V p-p
Input Impedance PCBEEP Ports A, B, C, E (Mic Boost = 0 dB)			 23 150		 kΩ kΩ
Input Capacitance(1)			5	7.5	pF

***Table 6. General Specifications** (3 of 4)*

Parameter		Min	Typ	Max	Unit
Microphone Bias					
MIC_BIAS-B, MIC_BIAS-C					
MIC_BIAS_IN (Pin 33) = +5 V or +3.3 V	V_{REF} Setting = High-Z		High-Z		
	V_{REF} Setting = 0 V		0		V dc
	V_{REF} Setting = 50%		1.65		V dc
MIC_BIAS_IN (Pin 33) = +5 V	V_{REF} Setting = 80%		3.7		V dc
	V_{REF} Setting = 100%		3.9		V dc
MIC_BIAS_IN (Pin 33) = +3.3 V	V_{REF} Setting = 80%		2.86		V dc
	V_{REF} Setting = 100%		3.0		V dc
MIC_BIAS-E (When enabled as BIAS)	V_{REF} Setting = High-Z		High-Z		
	V_{REF} Setting = 0 V		0		V dc
	V_{REF} Setting = 50%		1.65		V dc
	V_{REF} Setting = 80%		2.86		V dc
	V_{REF} Setting = 100%		3.0		V dc
Output Drive Current	V_{REF} Setting = 50%, 80%, or 100%		1.6		mA
GPIO_0, GPIO_1, and GPIO_2					
Input Signal High (V_{IH})		$DV_{GPIO} \times 0.60$		DV_{GPIO}	V
Input Signal Low (V_{IL})		0		$DV_{GPIO} \times 0.24$	V
Output Signal High (V_{OH})	I_{OUT} = –500 µA	$DV_{GPIO} \times 0.72$		DV_{GPIO}	V
Output Signal Low (V_{OL})	I_{OUT} = +1500 µA	0		$DV_{GPIO} \times 0.10$	V
Input Leakage Current (Signal High) (I_{IH})			–150		nA
Input Leakage Current (Signal Low) (I_{IL})			–50		µA
DM_Clock					
Output Signal High (V_{OH})	I_{OUT} = –500 µA	$DV_{GPIO} \times 0.72$		DV_{GPIO}	V
Output Signal Low (V_{OL})	I_{OUT} = +1500 µA	0		$DV_{GPIO} \times 0.10$	V

***Table 6. General Specifications** (4 of 4)*

Parameter		Min	Typ	Max	Unit
DM_DATA					
Input Signal High (V_{IH})		$DV_{GPIO} \times 0.60$		DV_{GPIO}	V
Input Signal Low (V_{IL})		0		$DV_{GPIO} \times 0.24$	V
Input Leakage Current (Signal High) (I_{IH})			–150		nA
Input Leakage Current (Signal Low) (I_{IL})			–50		nA
S/PDIF-Out_1, S/PDIF-Out_2					
Output Signal High (V_{OH})	I_{OUT} = –500 µA	$DV_{GPIO} \times 0.72$		DV_{GPIO}	V
Output Signal Low (V_{OL})	I_{OUT} = +1500 µA	0		$DV_{GPIO} \times 0.10$	V
S/PDIF_IN					
Input Signal High (V_{IH})		$DV_{GPIO} \times 0.60$		DV_{GPIO}	V
Input Signal Low (V_{IL})		0		$DV_{GPIO} \times 0.24$	V
Input Leakage Current (Signal High) (I_{IH})			150		nA
Input Leakage Current (Signal Low) (I_{IL})			–50		µA
Power Supply					
Analog (AV_{DD}) 3.3 V ± 5% Power Supply Range Power Dissipation Supply Current		3.13	3.30 76 23	3.46	V mW mA
Digital (DV_{DD}) 3.3 V ± 10% Power Supply Range Power Dissipation Supply Current		2.97	3.30 142 43	3.63	V mW mA
Digital I/O (DV_{IO}) 3.3 V ± 10% Power Supply Range Power Dissipation Supply Current		2.97	3.30 0.66 0.20	3.63	V mW mA
Digital I/O (DV_{IO}) 1.5 V ± 5.5% Power Supply Range Power Dissipation Supply Current		1.42	1.50 0.03 0.20	1.58	V mW mA
Digital GPIO (DV_{GPIO}) 3.3 V ± 10% Power Supply Range Power Dissipation Supply Current		2.97	3.30 3.63 1.10	3.63	V mW mA
Power Supply Rejection (Reference to f_S 100 mV p-p Signal @ 1 kHz)(1)			80		dB

FOOTNOTES:
(1) Guaranteed but not tested.
(2) Measurements reflect main ADC.
(3) RMS values assume sine wave input.

1.3 HD Audio Link Specification

HD Audio signals comply with the High Definition Audio Specifications. Please refer to these specifications at: *http://www.intel.com/standards/hdaudio/*

Table 7. Power-Down States

Parameter	IDV_{DD} Typ	IAV_{DD} Typ	Unit
Function Node in D0, All Nodes Active	73	49	mA
Function Node in D3	24	1	mA
Codec in $\overline{RESET}$	3	3	mA
Individual Block Power Savings			
DAC Pair Powered Down Saves (Each)	6	5	mA
ADC Pair Powered Down Saves (Each)	6	3	mA
Mixer Power Control (and Associated Amps) Saves	0	2	mA
MIC_BIAS Powered Down Saves[1] [2]	0	0.1	mA

FOOTNOTES:

(1) Powering down the MIC_BIAS powers down all port MIC_BIAS pins. This disables all microphone bias circuits, setting them to the high-Z state.

(2) Test conditions: 30 pF load, 2.0 MHz frequency, 3.3 V AV_{DD}.

1.4 Absolute Maximum Ratings

Stresses greater than those listed below may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute Maximum Ratings

Parameter	Rating
Digital (DV_{DD})	–0.30 V to +3.65 V
Digital I/O (DV_{IO})	–0.30 V to +3.65 V
Digital GPIO (DV_{GPIO})	–0.30 V to +3.65 V
Analog (AV_{DD})	–0.30 V to +3.65 V
Input Current (Except Supply Pins)	±10.0 mA
Analog Input Voltage (Signal Pins)	–0.30 V to AV_{DD} + 0.3 V
Digital Input Voltage (Signal Pins)	–0.30 V to DV_{IO} + 0.3 V
Ambient Temperature (Operating)	0°C to +70°C
Storage Temperature	–65°C to +150°C

CAUTION

Electrostatic Discharge Device (ESD)

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

1.5 Environmental Conditions

Ambient Temperature Rating

$T_{AMB} = T_{CASE} – (PD \times \theta_{CA})$
T_{CASE} = Case Temperature in °C
PD = Power Dissipation in W
θ_{CA} = Thermal Resistance (Case-to-Ambient)
θ_{JA} = Thermal Resistance (Junction-to-Ambient)
θ_{JC} = Thermal Resistance (Junction-to-Case)

All measurements per EIA-JESD51 with 2S2P test board per EIA-JESD51-7.

Table 9. Thermal Resistance

Package	θ_{JA}	θ_{JC}	θ_{CA}	Unit
QFN	47	15	32	°C/W

1.6 Pin Configuration and Function Descriptions

Figure 1. AD1989A Pinout

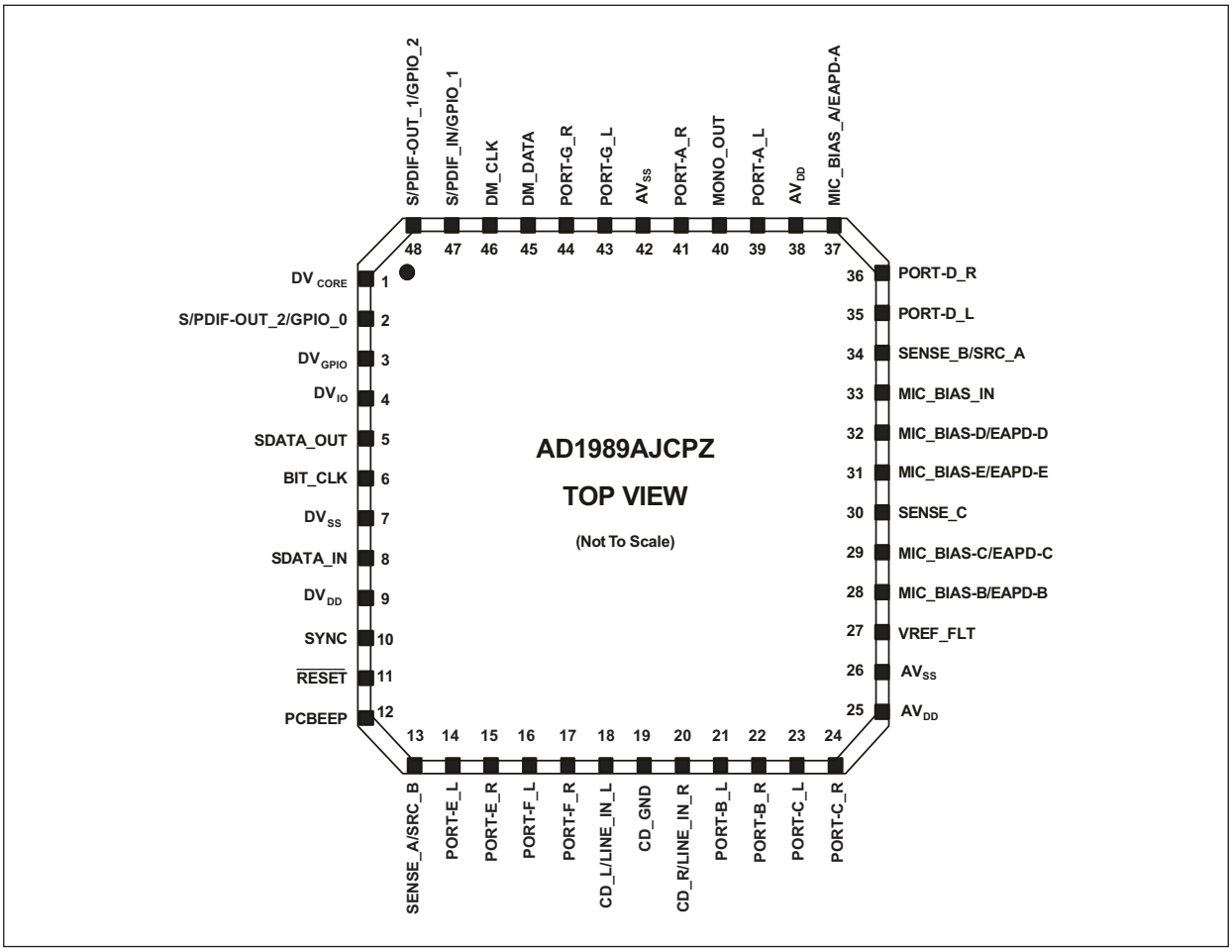


Table 10. Pin Descriptions *(1 of 3)*

Mnemonic	Pin No.	Function	Description
Digital Interface			
SDATA_OUT	5	I	Link Serial Data Output. Clocked on both edges of the BIT_CLK.
BIT_CLK	6	I	Link Bit Clock. 24.000 MHz serial data clock.
SDATA_IN	8	I/O	Link Serial Data Input. AD1989A output stream clocked only on one edge of BIT_CLK.
SYNC	10	I	Link Frame Sync.
$\overline{\text{RESET}}$	11	I	Link Reset. Master hardware reset
Digital I/O			
S/PDIF-OUT_2/GPIO_0	2	I/O	S/PDIF Out or GPIO. Supports S/PDIF output as primary function.
S/PDIF_IN/GPIO_1	47	I/O	S/PDIF Input/General-Purpose Input/Output Pin. Supports S/PDIF input as primary function.
SPDIF_OUT_1/GPIO_2	48	I/O	S/PDIF_OUT or GPIO. Supports S/PDIF output as primary function.
DM_DATA	45	DMIC	Digital Microphone Data Input. Support for two digital microphones.
DM_CLK	46	DMIC_CLK	Digital Microphone Clock Output.
JACK SENSE			
SENSE_A/SRC_B	13	I/O	JACK SENSE A-D Input/Sense B Drive.
SENSE_B/SRC_A	34	1/O	JACK SENSE E-H Input/Sense A Drive.
SENSE_C	30	I	JACK Sense CD/Line inputs.
Analog I/O			
PCBEEP	12	LI	Monaural Input from System for Analog PCBeep.
PORT-E_L	14	LI, MIC, LO, SWAP	Auxiliary Input/Output Left Channel.
PORT-E_R	15	LI, MIC, LO, SWAP	Auxiliary Input/Output Right Channel.
PORT-F_L	16	LO	Auxiliary Input/Surround Rear (5.1) Left Channel.
PORT-F_R	17	LO	Auxiliary Input/Surround Rear (5.1) Right Channel.
CD_L/LINE_IN_L	18	LL	CD Audio Left Channel.
CD_GND	19	LI	CD Audio Analog Ground Reference (for Differential CD Input). Must be connected to AGND via 0.1 mF capacitor if not in use as CD_GND.
CD_R/LINE_IN_R	20	LI	CD Audio Right Channel.
PORT-B_L	21	LI, MIC, HP, LO	Front Panel Stereo MIC/Line-In.

Table 10. Pin Descriptions *(2 of 3)*

Mnemonic	Pin No.	Function	Description
Analog I/O (continued)			
PORT-B_R	22	LI, MIC, HP, LO	Front Panel Stereo MIC/Line-In.
PORT-C_L	23	LI, MIC, LO	Rear Panel Stereo MIC/Line-In.
PORT-C_R	24	LI, MIC, LO	Rear Panel Stereo MIC/Line-In.
PORT-D_L	35	LI, HP, LO	Rear Panel Headphone/Line-Out.
PORT-D_R	36	LI, HP, LO	Rear Panel Headphone/Line-Out.
PORT-A_L	39	LI, MIC, HP, LO	Front Panel Headphone/Line-Out.
MONO_OUT	40	LO	Monaural Output to Internal Speaker or Telephony Subsystem Speakerphone.
PORT-A_R	41	LI, MIC, HP, LO	Front Panel Headphone/Line-Out.
PORT-G_L	43	LO, SWAP	Rear Panel C/LFE Output.
PORT-G_R	44	LO, SWAP	Rear Panel C/LFE Output.
Filter/Reference			
MIC_BIAS-B/EAPD-B MIC_BIAS-C/EAPD-C MIC_BIAS-E/EAPD-E MIC_BIAS-D/EAPD-D MIC_BIAS-A/EAPD-A	28 29 31 32 37	O O O O O	Switchable Microphone Bias. For use with Port B (Pins 21, 22). Switchable Microphone Bias. For use with Port C (Pins 23, 24). Switchable Microphone Bias. For use with Port E (Pins 14, 15). Switchable Microphone Bias. For use with Port D (Pins 35, 36) Switchable Microphone Bias. For use with Port A (Pins 39, 41) All MIC_BIAS pins are capable of: High-Z, 0 V, 1.65 V, 3.78 V, and 3.95 V (with 5.0 V on Pin 33) High-Z, 0 V, 1.65 V, 2.86 V, and 3.00 V (with 3.3 V on Pin 33).
VREF_FILT	27	O	Voltage Reference Filter.
DV_{CORE}	1	O	CAUTION: DO NOT APPLY 3.3 V TO THIS PIN! Filter connection for internal core voltage regulator. This pin must be connected to filter caps: 10 µF, 1.0 µF, and 0.1 µF connected in parallel between Pin 1 and DV_{SS} (Pin 4).

Table 10. Pin Descriptions *(3 of 3)*

Mnemonic	Pin No.	Function	Description
Power and Ground			
DV_{GPIO} 3.3 V ± 10%	3	I	GPIO and S/PDIF Out (1 and 2) Signal Level (independent of DV_{IO}). Connect to 3.3 V ±10%.
DV_{IO} 3.3 V ± 10% or DV_{IO} 1.5 V ± 5.5%	4	I	Connect to the I/O voltage used for the HD Audio controller signals.
DV_{SS}	7	I	Digital Supply Return (Ground).
DV_{DD} 3.3 V ± 10%	9	I	Digital Supply Voltage 3.3 V. This is regulated down to Pin 1 to supply the internal digital core.
AV_{DD} 3.3 V ± 5%	25, 38	I	CAUTION: DO NOT APPLY 5.0 V TO THESE PINS! Analog Supply Voltage 3.3 V ONLY. Note: AV_{DD} supplies should be well regulated and filtered as supply noise degrades audio performance.
MIC_BIAS_IN	33	I	Source for Microphone Bias Circuitry. Connect this pin to 5.0 V via a low-pass filter. When connected this way the AD1989A is capable of providing +3.95 V as a mic bias to all of the MIC_BIAS pins. If 5 V is not available, connect this pin to +3.3 V (AV_{DD}) via a low-pass filter. The AD1989A produces a mic bias voltage relative to the AV_{DD} supply (typically 3.0 V @ AV_{DD} = 3.3 V).
AV_{SS}	26, 42	I	Analog Supply Return (Ground). AV_{SS} should be connected to DV_{SS} using a conductive trace under, or close to, the AD1989A.

GENERAL NOTES:

1. The symbols used in this table are defined as follows:
   I = Input
   O = Output
   LI = Line level input
   LO = Line level output
   HP = Output capable of driving headphone load
   MIC = Input supports microphones with MIC bias and boost amplifier
   SWAP = Outputs can swap L/R channels (typically used to support C/LFE or shared C/LFE function).

1.7 Digital Microphone Interface Timing Specifications

The digital microphone interface can support one or two digital microphones using two or three codec pins. Both uniplex (one microphone per data pin) and multiplex (two microphones sharing the same data pin) are supported. The timing for these configurations is shown in Figures 2 and 3. The interface can generate a microphone clock at 1.5 MHz, 2.0 MHz, or 3.0 MHz to suit quality and power requirements

Table 11. Microphone Timing Parameters

Parameter		Minimum	Typical	Maximum	Unit
Timing Requirements					
t_0	DM_CLK (1.5 MHz) Period Duty Cycle		667 50/50		ns %
t_0	DM_CLK (2.0 MHz) Period Duty Cycle		500 50/50		ns %
t_0	DM_CLK (3.0 MHz) Period Duty Cycle		333 50/50		ns %
t_1	DM_CLK Rise Time			5	ns
t_2	DM_CLK Fall Time			5	ns
t_3	Data Setup to DM_CLK Edge	100			ns
t_4	Data Hold from DM_CLK Edge	5			ns

Figure 2. Uniplex Microphone Timing

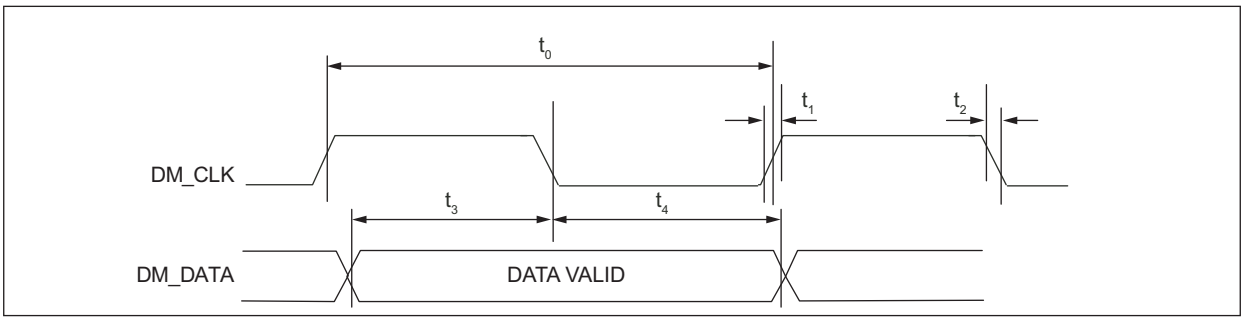
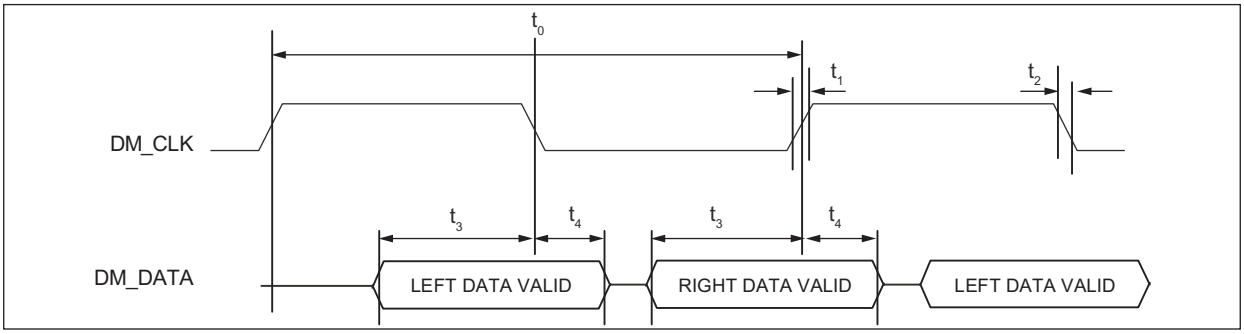


Figure 3. Multiplex Microphone Timing



1.8 HD Audio Widgets

Table 12. HD Audio Widgets[1] *(1 of 2)*

Node ID	Name	Type ID	Type	Description
00	ROOT	x	Root	Device identification
01	FUNCTION	x	Function	Designates this device as an audio codec
02	S/PDIF_1 DAC	0	Audio Output	S/PDIF-1 digital stream output interface
03	DAC_0	0	Audio Output	Headphone/surround side (7.1) channel digital/audio converters
04	DAC_1	0	Audio Output	Stereo front channel digital/audio converters
05	DAC_2	0	Audio Output	Stereo C/LFE channel digital/audio converters
06	DAC_3	0	Audio Output	Stereo surround-back (5.1) channel digital/audio converters
07	S/PDIF ADC	1	Audio Input	S/PDIF digital stream input interface
08	ADC_0	1	Audio Input	Stereo record Channel 1 audio/digital converters
09	ADC_1	1	Audio Input	Stereo record Channel 2 audio/digital converters
0A	DAC_4	1	Audio Output	Stereo surround side (7.1) channel digital/audio converters
0B	S/PDIF_2 DAC	0	Audio Output	S/PDIF-2 output (typically used for HDMI)
0C	ADC Selector 0	3	Audio Selector	Selects and amplifies/attenuates the input to ADC0
0D	ADC Selector 1	3	Audio Selector	Selects and amplifies/attenuates the input to ADC1
0E	ADC Selector 2	3	Audio Selector	Selects and amplifies/attenuates the input to ADC2
0F	ADC_2	3	Audio Input	Stereo record channel 2 audio/digital converters
10	Digital Beep	7	Beep Generator	Internal digital PCBeep signal
11	Port A (Headphone)	4	Pin Complex	Front panel headphone/microphone jack
12	Port D (Front L/R)	4	Pin Complex	Rear panel output/headphone output
13	Mono Out	4	Pin Complex	Monaural output pin (internal speakers or telephony system)
14	Port B (Front Mic)	4	Pin Complex	Front panel microphone/headphone jack
15	Port C (Line In)	4	Pin Complex	Line-in jack (rear or front)
16	Port F (Surr Back)	4	Pin Complex	Rear panel surround-rear (5.1) jack
17	Port E (Rear Mic)	4	Pin Complex	Rear panel mic jack
18	CD In/Line In	4	Pin Complex	Analog CD input or line input
19	Mixer Power Down	5	Power Widget	Powers down the analog mixer and associated amps
1A	Analog PCBeep	4	Pin Complex	External analog PCBeep signal input
1B	S/PDIF Out_1	4	Pin Complex	S/PDIF_1 output pin
1C	S/PDIF In	4	Pin Complex	S/PDIF input pin
1D	S/PDIF Out_2	4	Audio Mixer	S/PDIF_2 output pin

Table 12. HD Audio Widgets[1] *(2 of 2)*

Node ID	Name	Type ID	Type	Description
1E	Mono Out Mixer	2	Audio Mixer	Selects which source drives the mono out signal
1F	Digital Miicrophone	4	Pin Complex	Digital microphone input pin
20	Analog Mixer	2	Audio Mixer	Mixes individually gainable analog inputs
21	Mixer Output Atten	3	Audio Selector	Attenuates the mixer output to drive the port mixers
22	Port A Mixer	2	Audio Mixer	Mixes the Port A Selected DAC and mixer output amps to drive Port A
23	V_{REF} Power Down	F	Vendor Defined	Powers down the Internal and external V_{REF} circuitry
24	Port G (C/LFE)	4	Pin Complex	Rear panel C/LFE jack
26	Port E Mixer	2	Audio Mixer	Mixes DAC2 and mixer output amps to drive Port E
27	Port G Mixer	2	Audio Mixer	Mixes DAC2 and mixer output amps to drive Port G
29	Port D Mixer	2	Audio Mixer	Mixes DAC1 and mixer output amps to drive Port D
2A	Port F Mixer	2	Audio Mixer	Mixes DAC3 and mixer output amps to drive Port F
2B	Port B Mixer	2	Audio Mixer	Mixes the Port B selected DAC and mixer output amps to drive Port B
2C	Port C Mixer	2	Audio Mixer	Mixes the Port C selected DAC and mixer output amps to drive Port C
2D	Stereo Mix Down	2	Audio Mixer	Mixes the stereo L/R channels to drive mono output
2F	BIAS Power Down	F	Vendor Defined	Powers down the internal MIC_BIAS_FILT and all MIC_BIAS Pins
30	Port B Out Selector	3	Audio Selector	Selects the Port B DAC (0, 1)
31	Port C Out Selector	3	Audio Selector	Selects the Port C DAC (0, 3)
32	Port E Out Selector	3	Audio Selector	Selects the Port E DAC (2, 4)
33	Port C In Selector	3	Audio Selector	Selects from the Port C and G inputs to drive the mixer input
34	Port E In Selector	3	Audio Selector	Selects from the Port E and G inputs to drive the mixer input
36	Mono Out Selector	3	Audio Selector	Selects the mono out DAC (0, 1, 3)
37	Port A Selector	3	Audio Selector	Selects the Port A DAC (0, 1, 3)
38	Port A Boost	3	Audio Selector	Microphone boost amp for Port A
39	Port B Boost	3	Audio Selector	Microphone boost amp for Port B
3A	Port C Boost	3	Audio Selector	Microphone boost amp for Port C
3C	Port E Boost	3	Audio Selector	Microphone boost amp for Port E
3D	Port D Boost	3	Audio Selector	Microphone boost amp for Port D

FOOTNOTES:

[1] All Node IDs (NIDs) are sequential in the codec. Any NIDs missing from this table are vendor defined.

1.9 HD Audio Parameters

Table 13. Root and Function Node Parameters

Node ID	Name	Vendor ID 00	01	Revision ID 02[(1)]	03	Sub Node Count 04	Func. Group Type 05	Audio F.G. Caps 08	GPIO Caps 11
00	ROOT	11D4989A		0010 0300		0001 0001			
01	FUNCTION					0002 003C	0000 0001	0001 0C0C	4000 0003

FOOTNOTES:
(1) Subject to change with silicon stepping.

Table 14. SubSystem ID

Node ID	Name	Value	31:16 SSID	15:8 SKU	7:0 ASM ID
01	FUNCTION	BFD80000	BFD8	00	00

GENERAL NOTES:
1. The default SSID is overwritten by platform BIOS after power on. It is preserved across HD Audio link reset and verb reset.

1.10 Default Configuration Bytes

In Table 15, default configuration values are set on codec power-up only. Default configuration values are not reset by link or soft reset to preserve modifications by BIOS control.

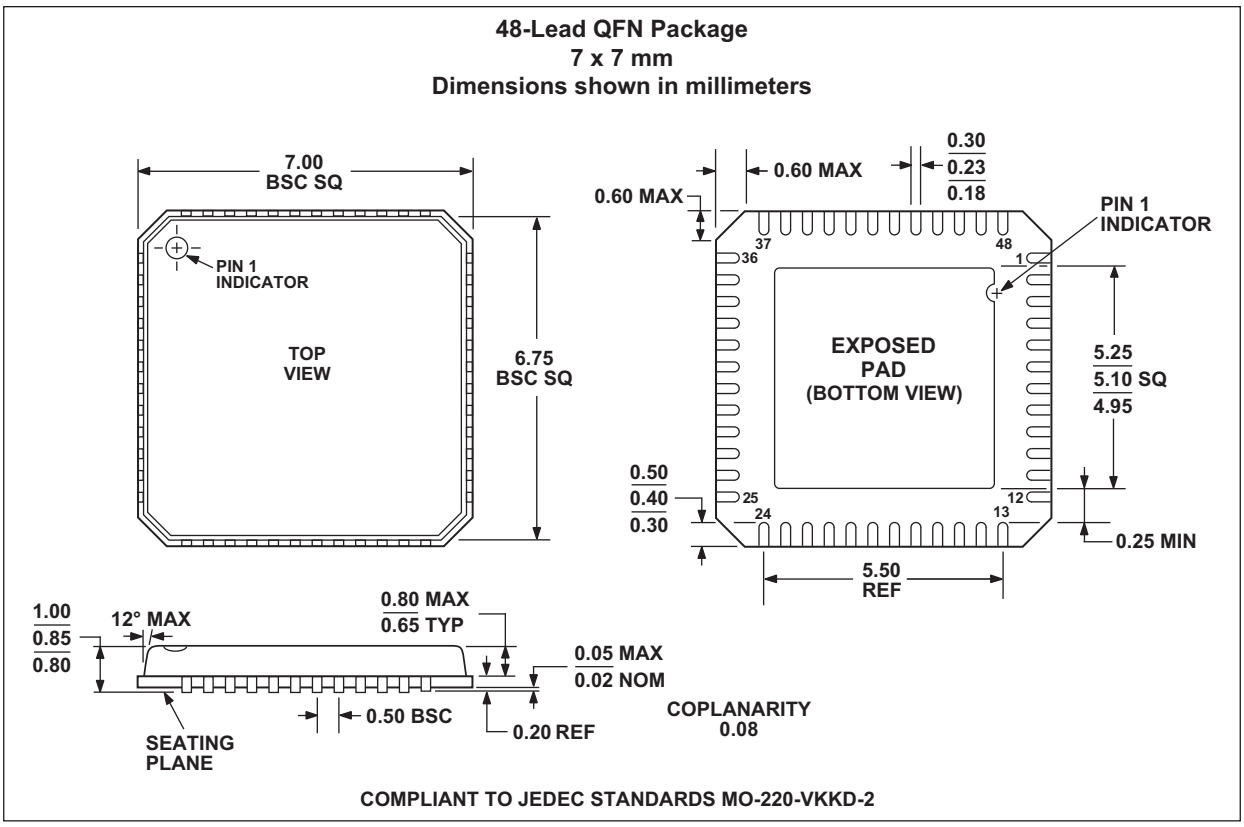
Table 15. Default Configuration Bytes

Node ID	Name	Value	31:30	29:28	27:24	23:20	19:16	15:12	8	7:4	3:0
			Connectivity	Location		Def Device	Connector Type	Color	JD	Def Assn	Sequence
				Chassis	Position						
11	Port A (Headphone)	0x0221 4030	Jack	External	Front	HP Out	1/8" Jack	Green	0	3	0
12	Port D (Front L/R)	0x0101 4010	Jack	External	Rear	Line Out	1/8" Jack	Green	0	1	0
13	Mono Out	0x9913 01F0	Fixed	Internal	Special 3	Speaker	ATAPI	Unknown	1	F	0
14	Port B (Front Mic)	0x02A1 9040	Jack	External	Front	Mic In	1/8" Jack	Pink	0	4	0
15	Port C (Line In)	0x0181 3021	Jack	External	Rear	Line In	1/8" Jack	Blue	0	2	1
16	Port F (Surr Back)	0x0101 1012	Jack	External	Rear	Line Out	1/8" Jack	Black	0	1	2
17	Port E (Rear Mic)	0x01A1 9020	Jack	External	Rear	Mic In	1/8" Jack	Pink	0	2	0
18	CD IN/ Line In	0x9933 012E	Fixed	Internal	Special 3	CD	ATAPI	Unknown	1	2	E
1A	Analog PCBeep	0x99F3 01F0	Fixed	Internal	Special 3	Other	ATAPI	Unknown	1	F	0
1B	S/PDIF_1 Out	0x0145 11F0	Jack	External	Rear	S/PDIF Out	Optical	Black	1	F	0
1C	S/PDIF In	0x01C5 11F0	Jack	External	Rear	S/PDIF In	Optical	Black	1	F	0
1D	S/PDIF_2 Out	0x9856 01F0	Fixed	Internal	Special 2	Digital Out	Other Digital	Unknown	1	F	0
1F	Digital Mic	0x97A6 01F0	Fixed	Internal	Special 1	Mic In	Other Digital	Unknown	1	F	0
24	Port G (C/LFE)	0x0101 6011	Jack	External	Rear	Line Out	1/8" Jack	Orange	0	1	1

1.11 Package Dimensions

Dimensions are shown in millimeters.

Figure 4. 48-Lead QFN Package



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