High Definition Audio SoundMAX® Codec

AD1988A/AD1988B

FEATURES

Ten 192 kHz DACs
- Five independent stereo DAC pairs
- 7.1 surround sound plus independent headphone
- Independent 8 kHz, 11.025 kHz, 16 kHz, 22.05 kHz, 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz sample rates
- Selectable stereo mixer on outputs
- 16-, 20-, and 24-bit PCM resolution

Six 192 kHz ADCs
- Three independent stereo ADC pairs
- Simultaneous record of up to three stereo channels
- Support for quad microphone arrays plus independent capture channel
- Independent 8 kHz, 11.025 kHz, 16 kHz, 22.05 kHz, 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz sample rates
- 16-, 20-, and 24-bit resolution

S/PDIF output
- 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz sample rates
- 16-, 20-, and 24-bit data widths
- PCM, WMA/PRO, Dolby®, AC3, and DTS® formats
- Digital PCM gain control
- Digital PCM ADC/stream mixer

S/PDIF input
- 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz sample rates
- 16-, 20-, and 24-bit data widths
- PCM, WMA/PRO, Dolby, AC3, and DTS formats
- Digital PCM gain control
- Auto synchronizes to source

High quality stereo CD input with GND sense

MONO_OUT pin for internal speakers or telephony

Retasking jack support

ENHANCED FEATURES

Three stereo headphone amps

AD1988A: Windows Vista™ Operating System Premium Logo compliant
- 95 dB outputs
- 90 dB audio inputs

AD1988B: Windows Vista Premium Logo compliant and Dolby Master Studio™ compliant
- 101 dB outputs
- 92 dB audio inputs

Internal 32-bit arithmetic for greater accuracy

Impedance and presence detection on all jacks

Analog PCBEEP and digital synthesis BEEP

C/LFE channel swap

Two general-purpose digital I/O (GPIO) pins

3.3 V analog and digital supplies

Reduced support components

Advanced power management modes

48-pin LQFP and LFCSP_VQ package options, Pb-free

Supports Andrea Active Noise Reduction headphones

Hardware volume control

Built-in microphone gain amps

Adjustable microphone bias pins

Rev. 0

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REVISION HISTORY

10/06—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

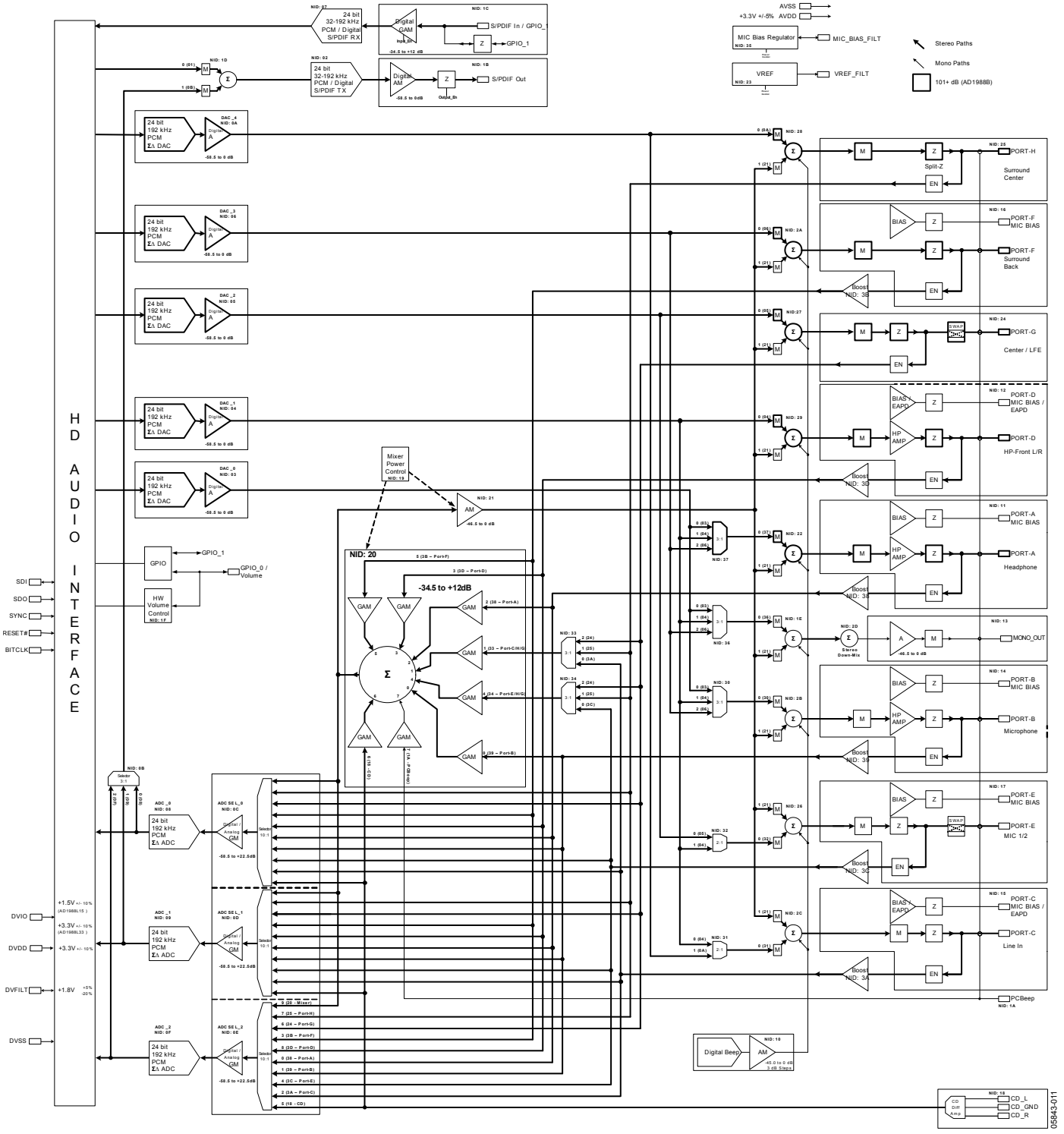


Figure 1. Block Diagram

SPECIFICATIONS

TEST CONDITIONS

Test Conditions for the AD1988A and AD1988B are as follows, unless otherwise noted.

Analog Input/Output Conditions

Temperature at 25°C
Digital supply (DV_{DD}) at 3.3 V ±10%
Analog supply (AV_{DD}) at 3.3 V ±5%
MIC_BIAS_FILT at 5.0 V ±5%
Sample rate (F_S) at 48 kHz
Input signal at 1008 Hz
Analog output pass band at 20 Hz to 20 kHz

DAC Conditions

Calibrated
Output −3 dB relative to full scale
10 kΩ output load: line out tests
32 Ω output load: headphone tests

ADC Conditions

Calibrated
0 db PGA gain
Input −3.0 dB relative to full scale

Table 1.

Parameter	Conditions/Comments	Min	Typ AD1988A/ AD1988B	Max	Unit
DIGITAL DECIMATION AND INTERPOLATION FILTERS[1]	f_S 8 kHz ~ 192 kHz				
Pass Band		0		0.40 f_S	Hz
Pass-Band Ripple				±0.005	dB
Stop Band		0.60 f_S			Hz
Stop Band Rejection				−100	dB
Group Delay			20		$1/f_S$
Group Delay Variation over Pass Band			0		µs
ANALOG-TO-DIGITAL CONVERTERS					
Resolution[1]			24		Bits
Gain Error	Full-scale span relative to nominal input voltage			±10	%
Interchannel Gain Mismatch	Difference of gain errors		±0.2	±0.5	dB
ADC Offset Error				±5	mV
ADC Crosstalk[1]					
Line Inputs	Input L, Ground R, Read R; Input R, Ground L, Read L		−85		dB
LINE_IN to Other			−100	−80	dB
DIGITAL-TO-ANALOG CONVERTERS					
Resolution[1]			24		Bits
Gain Error	Full-scale span relative to nominal input voltage			±10	%
Interchannel Gain Mismatch	Difference of gain errors		±0.2	±0.5	dB
Total Out-of-Band Energy [1]	To 100 kHz		−85		dB
DAC Crosstalk[1]	Input L, Zero R, Read R; Input R, Zero L, Read L		−95		dB
DAC VOLUMES—PROGRAMMABLE GAIN ATTENUATOR					
Step Size	DAC_0, DAC_1, DAC_2, DAC_3, DAC_4		+1.5		dB
Output Gain/Attenuation Range		−58.5		0	dB
ADC VOLUMES—PROGRAMMABLE GAIN AMPLIFIER/ATTENUATOR					
Step Size	ADCSEL_0, ADCSEL_1, ADCSEL_2		+1.5		dB
PGA Gain/Attenuation Range		−58.5		+22.5	dB
ANALOG MIXER—PROGRAMMABLE GAIN AMPLIFIER/ATTENUATOR					
Signal-to-Noise Ratio (SNR)[1, 2]	Input to output (including CD in)		95/96		
Step Size	All mixer inputs		+1.5		dB
Input Gain/Attenuation Range	All mixer inputs	−34.5		+12.0	dB

Parameter	Conditions/Comments	Min	Typ AD1988A/ AD1988B	Max	Unit
ANALOG LINE LEVEL OUTPUTS					
Full-Scale Output Voltage	Line out drive enabled	1.0			V rms[3]
PORT-C, PORT-E, PORT-F, PORT-G, PORT-H, and MONO_OUT	When ports are used as line level outputs	2.83			V p-p
Output Impedance[1]			300		Ω
External Total Load Impedance		10			kΩ
Output Capacitance[1]			15		pF
External Load Capacitance[1]				1000	pF
Total Harmonic Distortion (THD+N)[1]			−85/−85		dB
Dynamic Range[1]	−60 dB reference to f_S A-weighted		+95/+101		dB
ANALOG HP DRIVE OUTPUTS					
Full-Scale Output Voltage	Output drive enabled	1.0			V rms[3]
PORT-A, PORT-B, and PORT-D	When ports are used as outputs	2.83			V p-p
Output Impedance[1]				0.5	Ω
External Load Impedance[1]		32			Ω
Output Capacitance[1]			15		pF
External Load Capacitance[1]				1000	pF
Total Harmonic Distortion (THD+N)[1]	10 kΩ load		−83/−84		dB
	32 Ω load		−83/−84		dB
Dynamic Range[1]	−60 dB reference to f_S A-weighted, 10 kΩ or 32 Ω loads		+95/+101		dB
ANALOG INPUTS	When ports are used as inputs				
PORT-G, PORT-H, or CD			1		V rms[3]
			2.83		V p-p
Microphone Boost Amplifiers					
PORT-A, PORT-B, PORT-C, PORT-D, PORT-E, or PORT-F	0 dB boost		1		V rms[3]
			2.83		V p-p
	+10 dB boost		0.316		V rms[3]
			0.894		V p-p
	+20 dB boost		0.1		V rms[3]
			0.283		V p-p
	+30 dB boost		0.032		V rms[3]
			0.089		V p-p
Input Impedance[1]					
PCBEEP			23		kΩ
PORT-G, PORT-H			60		kΩ
All others (with 0 dB boost)			150		kΩ
Input Capacitance[1]			5	7.5	pF
ANALOG INPUT PERFORMANCE					
Total Harmonic Distortion Plus Noise (THD+N)[1]			−81/−82		dB
Dynamic Range	−60 dB in reference to f_S A-weighted		+90/+92		dB
Signal-to-Noise Ratio (SNR)[2]			+90/+92		dB
STATIC DIGITAL SPECIFICATIONS					
Digital I/O (DV_{IO})	DV_{IO} @ 3.3 V ± 10%	2.97	3.3	3.63	V
V_{IH}			2.0		V
V_{IL}			0.8		V
V_{OH}			2.4		V
V_{OL}			0.6		V

Parameter	Conditions/Comments	Min	Typ AD1988A/ AD1988B	Max	Unit
POWER SUPPLY					
Analog (AV_{DD})	3.3 V ± 5%				
Power Supply Range		3.13	3.30	3.46	V
Power Dissipation			155/172		mW
Supply Current			47/52		mA
Digital (DV_{DD})	3.3 V ± 10%				
Power Supply Range		2.97	3.30	3.63	V
Power Dissipation			247.5/238		mW
Supply Current			75/75		mA
Digital I/O (DV_{IO})	3.3 V ± 10%				
Power Supply Range		2.97	3.30	3.63	V
Power Dissipation			3.96		mW
Supply Current			1.20		mA
Power Supply Rejection[1] (AV_{DD})	100 mV p-p signal @ 1 kHz		80		dB V

[1] Guaranteed, not tested.
[2] SNR measurement defined as "the difference in level between a reference output signal and the device output with no signal applied." This definition is taken from B. Metzler, *Audio Measurement Handbook*, 1st edition, Audio Precision, Inc., 1993, p. 165.
[3] RMS values assume sine wave input.

Table 2. Power-Down States

Parameter	Comments	D-State	AD1988A/AD1988B DI_{DD} Typ	AD1988A/AD1988B AI_{DD} Typ	Unit
POWER-DOWN STATES					
FUNCTION Node		D3	21/20	1.2/1.7	mA
DAC Pair	Powered down saves (each)	D3	6/6	5/5.6	mA
ADC Pair	Powered down saves (each)	D3	5.3/5.4	3.2/3.1	mA
Mixer Power Control (and Associated Amps)	Saves	D3	0/0	2.0/2.4	mA
MIC_BIAS	Powered down saves	D3	0/0	0.5/0.5	mA
RESET	Low (active) state		2.9/2.7	3.1/3.4	mA

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Digital (DV_{DD})	−0.30 V to +3.65 V
Digital I/O (DV_{IO})	−0.30 V to +3.65 V
Analog (AV_{DD})	−0.30 V to +3.65 V
Input Current (Except Supply Pins)	±10.0 mA
Analog Input Voltage (Signal Pins)	−0.30 V to AV_{DD} + 0.3 V
Digital Input Voltage (Signal Pins)	−0.30 V to DV_{IO} + 0.3 V
Ambient Temperature (Operating)	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Ambient temperature ratings are as follows:

$$T_{AMB} = T_{CASE} - (P_D \times \theta_{CA})$$

where:

T_{CASE} = case temperature in °C.
P_D = power dissipation in W.
θ_{CA} = thermal resistance (case-to-ambient).

Table 4. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}[2]	θ_{CA}[3]	Unit
LQFP	48	17	31	°C/W
LFCSP_VQ[4]	47	15	32	°C/W

[1] θ_{JA} = thermal resistance: junction-to-ambient.
[2] θ_{JC} = thermal resistance: junction-to-case.
[3] θ_{CA} = thermal resistance: case-to-ambient.
[4] VQ = very thin quad.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

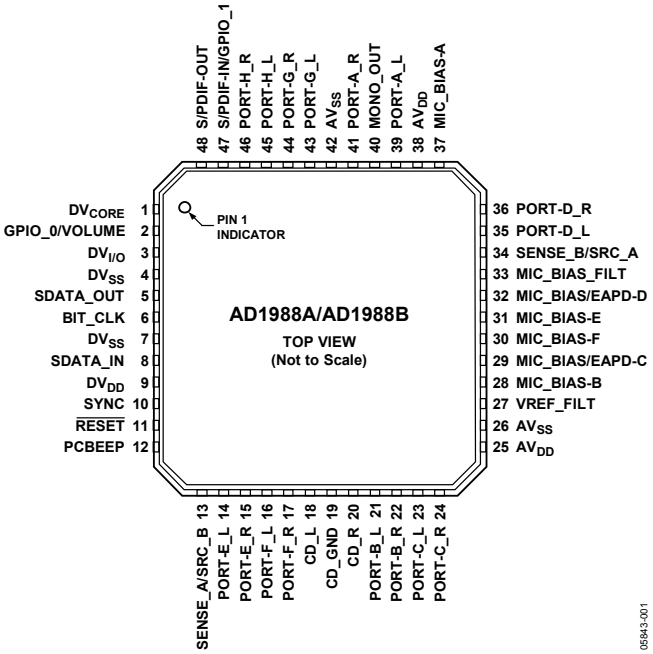


Figure 2. LFCSP_VQ Pin Configuration

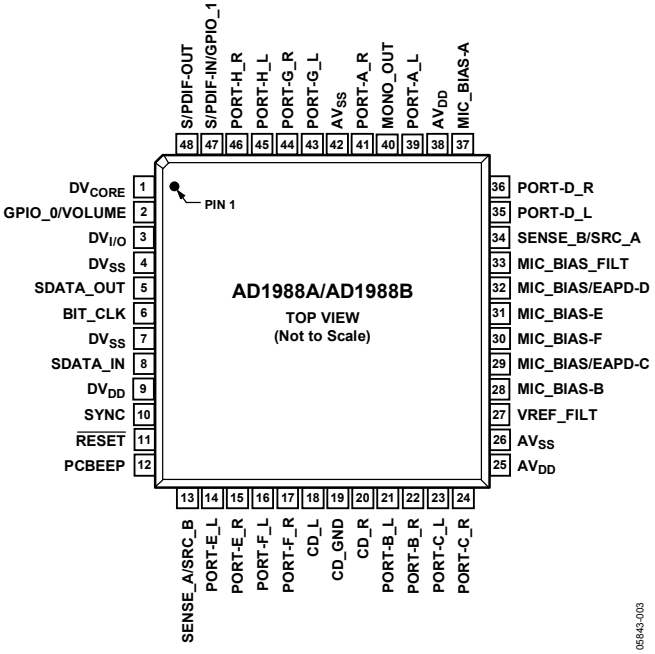


Figure 3. LFQP Pin Configuration

Table 5. Pin Function Descriptions

Mnemonic	Pin Number	I/O	Description
DV_{CORE}	1	O	Filter Connection for Internal Core Voltage Regulator. This pin must be connected to filter capacitors: 10 µF, 1.0 µF, and 0.1 µF connected in parallel between Pin 1 and DV_{SS} (Pin 4 and Pin 7).
GPIO_0/VOLUME	2	I/O	General-Purpose Input/Output Pin (Digital I/O). Digital signal used to control external circuitry. Volume Control. When enabled, it can be used as an external volume control
DV_{IO}	3	I	Link Digital I/O Voltage Reference. 3.3 V (±10%).
DV_{SS}	4, 7	I	Digital Supply Return (Ground).
SDATA_OUT	5	I	Link Serial Data Output (Digital Interface). AD1988 input stream. Clocked on both edges of the BIT_CLK.
BIT_CLK	6	O	Link Bit Clock (Digital Interface). 24.000 MHz serial data clock.
SDATA_IN	8	I/O	Link Serial Data Input (Digital Interface). AD1988 output stream. Clocked only on one edge of BIT_CLK.
DV_{DD}	9	I	Digital Supply Voltage 3.3 V ± 10%. This is regulated down to 1.9 V on Pin 1 to supply the internal digital core internal to the AD1988.
SYNC	10	I	Link Frame Sync (Digital Interface). 48 kHz frame sync plus SDI stream IDs.
$\overline{\text{RESET}}$	11	I	Link Reset (Digital Interface). AD1988 master hardware reset.
PCBEEP	12	I	Monaural Input from System for PCBEEP. Line level input.
SENSE_A/SRC_B	13	I/O	Jack Sense A to Jack Sense D Input/Sense B Drive.
PORT-E_L, PORT-E_R	14, 15	I/O	Left and Right Rear Panel Stereo Mic In/C/LFE (Analog Input/Output). Input: line level input, supports microphones with MIC_BIAS and boost amplifiers. Output: line level output.
PORT-F_L, PORT-F_R	16, 17	I/O	Left and Right Rear Panel Stereo Mic In/Surround Rear (Analog Input/Output). Input: line level input, supports microphones with MIC_BIAS and boost amplifiers. Output: line level output only.
CD_L, CD_R	18, 20	I	CD Audio Left Channel, CD Audio Right Channel.
CD_GND	19	I	CD Audio Analog Ground Reference (for Analog CD Input). Line level input only.
PORT-B_L, PORT-B_R	21, 22	I/O	Front Panel Stereo Mic In/Front Panel Headphones. Analog input/output. Input: line level input, supports microphones with MIC Bias and boost amplifiers. Output: line level output, capable of driving headphone load and power.

Mnemonic	Pin Number	I/O	Description
PORT-C_L, PORT-C_R	23, 24	I/O	Rear Panel Line-In/Surround Back Output. Analog input/output. Input: line level input, supports microphones with MIC Bias and boost amplifiers. Output: line level output only.
AV_{DD}	25, 38	I	Analog Supply Voltage. 3.3 V only. Caution: Do not apply 5.0 V to this pin. AV_{DD} supplies should be well regulated and filtered because supply noise degrades audio performance.
AV_{SS}	26, 42	I	Analog Supply Return (Ground). AV_{SS} should be connected to DV_{SS} using a conductive trace under, or close to, the AD1988A/AD1988B.
VREF_FILT	27	O	Voltage Reference Filter. This pin must be connected to filter capacitors: 1.0 µF and 0.1 µF connected in parallel between Pin 27 and AV_{SS} (Pin 26).
MIC_BIAS-B	28	O	Switchable Microphone Bias for PORT-B. Capable of: High-Z, 0 V, 1.65 V, 3.78 V, and 3.95 V (with 5.0 V on Pin 33). High-Z, 0 V, 1.65 V, 2.86 V, and 3.10 V (with 3.3 V on Pin 33).
MIC_BIAS-C	29	O	Switchable Microphone Bias for PORT-C. This pin has the same function as MIC_BIAS-B.
MIC_BIAS-F	30	O	Switchable Microphone Bias for PORT-F. This pin has the same function as MIC_BIAS-B.
MIC_BIAS-E	31	O	Switchable Microphone Bias for PORT-E. This pin has the same function as MIC_BIAS-B.
MIC_BIAS-D	32	O	Switchable Microphone Bias for PORT-D. This pin has the same function as MIC_BIAS-B.
MIC_BIAS_FILT	33	I	Filter for Microphone Bias Boost Circuitry. Connect this pin to 5.0 V via a low-pass filter. When connected in this way, the AD1988A/AD1988B are each capable of providing 3.95 V as a microphone bias to all of the MIC_BIAS pins. If 5 V is not available, connect this pin to 3.3 V (AV_{DD}) via a low-pass filter. The AD1988A/AD1988B produce a MIC_BIAS voltage relative to the AV_{DD} supply (typically 3.1 V @ AV_{DD} = 3.3 V).
SENSE_B/SRC_A	34	I/O	Jack Sense E to Jack Sense H Input/Sense A Drive.
PORT-D_L, PORT-D_R	35, 36	I/O	Left and Right Rear Panel Headphone (Front Line Out)/Stereo MIC In. Analog input/output. Input: line level input, supports microphones with MIC_BIAS and boost amplifiers. Output: line level output, capable of driving headphone load and power.
MIC_BIAS-A	37	O	Switchable Microphone Bias for PORT-A. This pin has the same function as MIC_BIAS-B.
PORT-A_L, PORT-A_R	39, 41	I/O	Left and Right Front Panel Headphone Output/Stereo MIC In. Analog input/output. Input: line level input, supports microphones with MIC_BIAS and boost amplifiers. Output: line level output, capable of driving headphone load and power.
MONO_OUT	40	O	Monaural Output to Internal Speaker or Telephony Subsystem. Line level output only.
PORT-G_L, PORT-G_R	43, 44		Left and Right Rear Panel C/LFE Output/Line Input. Input: line level input. Output: line level output.
PORT-H_L, PORT-H_R	45, 46		Left and Right Rear Panel Surround Center/Side Output/Line Input. Analog input/output. Input: line level input. Output: line level output.
S/PDIF_IN/GPIO_1	47	I/O	S/PDIF_IN/GPIO Pin. S/PDIF_IN supports S/PDIF input. When enabled, GPIO_1 can be used as a GPIO pin.
S/PDIF_OUT	48	O	S/PDIF_OUT. Supports S/PDIF output.

Table 6. Pins Grouped by Function

Function	Pin No.	Mnemonic
Digital Interface	5	SDATA_OUT
	6	BIT_CLK
	8	SDATA_IN
	10	SYNC
	11	$\overline{\text{RESET}}$
Digital Input/Output	48	S/PDIF_OUT
	47	S/PDIF_IN/GPIO_1
	2	GPIO_0/VOLUME
Jack Sense	13	SENSE_A/SRC_B
	34	SENSE_B/SRC_A
Filter/Reference	1	DV_{CORE}
	27	VREF_FILT
	33	MIC_BIAS_FILT
Microphone Bias	28	MIC_BIAS-B
	29	MIC_BIAS-C
	30	MIC_BIAS-F
	31	MIC_BIAS-E
	32	MIC_BIAS-D
	37	MIC_BIAS-A
Power and Ground	9	DV_{DD}
	3	DV_{IO}
	4, 7	DV_{SS}
	25, 38	AV_{DD}
	26, 42	AV_{SS}
Analog Input/Output	12	PCBEEP
	14	PORT-E_L
	15	PORT-E_R
	16	PORT-F_L
	17	PORT-F_R
	18	CD_L
	20	CD_R
	21	PORT-B_L
	22	PORT-B_R
	23	PORT-C_L
	24	PORT-C_R
	35	PORT-D_L
	36	PORT-D_R
	39	PORT-A_L
	40	MONO_OUT
	41	PORT-A_R
	43	PORT-G_L
	44	PORT-G_R
	45	PORT-H_L
	46	PORT-H_R

CLARIFICATION OF OUTPUT CONFIGURATIONS

DAC, ADC, and port assignments are arbitrary; however, ports are optimized for certain configurations. Use the guidelines in Table 7, Table 8, and Table 9 when selecting ports for particular functions. Note the following for each of these tables:

- HP is the output capable of driving headphone load and power
- MIC is input that supports microphones with MIC Bias and boost amplifiers
- LO is the line level output
- LI is the line level input

In desktop applications with discreet jacks (the default configuration), assign the ports as listed in Table 7.

Table 7. Discreet Jacks (Default Configuration)

Port	Function	HP	MIC	LO	LI
PORT-A	Front Panel Headphone	x	x	x	x
PORT-B	Front Panel Microphone	x	x	x	x
PORT-C	Rear Panel Line-In		x	x	x
PORT-D	Rear Panel Front/Headphone	x	x	x	x
PORT-E	Rear Panel Microphone		x	x	x
PORT-F	Rear Panel Surround-Rear (5.1)		x	x	x
PORT-G	Rear Panel C/LFE			x	x
PORT-H	Rear Panel Surround-Center/Side (7.1)			x	x
MONO_OUT	Internal Mono Speaker (use GPIO as EAPD)			x	

In desktop applications with shared input/5.1 jacks, assign the ports as listed in Table 8.

Table 8. Shared Input/5.1 Jacks

Port	Function	HP	MIC	LO	LI
PORT-A	Front Panel Headphone	x	x	x	x
PORT-B	Front Panel Microphone	x	x	x	x
PORT-C	Rear Panel Line-In/Surround-Rear (5.1)		x	x	x
PORT-D	Rear Panel Front/Headphone	x	x	x	x
PORT-E	Rear Panel Microphone/C/LFE		x	x	x
MONO_OUT	Internal Mono Speaker (use GPIO as EAPD)			x	

In notebook applications, to support fully retasking jacks, assign the ports as listed in Table 9.

Table 9.

Port	Function	HP	MIC	LO	LI
PORT-A	Headphone Jack	x	x	x	x
PORT-B	Microphone Jack	x	x	x	x
PORT-D	Line-In Jack	x	x	x	x
PORT-C	Internal Stereo Speakers (use GPIO as EAPD)		x	x	x
PORT-E/PORT-F	Internal Quad Microphone Array (Optional)		x	x	x

HD AUDIO WIDGETS

Table 10.

Node ID	Name	Type	Description
00	ROOT	Root	Device identification
01	FUNCTION	Function	Designates this device as an audio codec
02	S/PDIF DAC	Audio output	S/PDIF digital stream output interface
03	DAC_0	Audio output	Stereo headphone channel digital/audio converters
04	DAC_1	Audio output	Stereo front channel digital/audio converters
05	DAC_2	Audio output	Stereo C/LFE channel digital/audio converters
06	DAC_3	Audio output	Stereo surround-back (5.1) channel digital/audio converters
07	S/PDIF ADC	Audio input	S/PDIF digital stream input interface
08	ADC_0	Audio input	Stereo record Channel 0 audio/digital converters
09	ADC_1	Audio input	Stereo record Channel 1 audio/digital converters
0A	DAC_4	Audio output	Stereo surround-side (7.1) channel digital/audio converters
0B	S/PDIF Mix Selector	Audio selector	Selects the ADC to drive the S/PDIF mixer
0C	ADC Selector 0	Audio selector	Selects and amplifies/attenuates the input to ADC_0
0D	ADC Selector 1	Audio selector	Selects and amplifies/attenuates the input to ADC_1
0E	ADC Selector 2	Audio selector	Selects and amplifies/attenuates the input to ADC_2
0F	ADC_2	Audio input	Stereo record Channel 2 audio/digital converters
10	Digital Beep	Beep generator	Internal digital PCBEEP signal
11	PORT-A	Pin complex	Front panel headphone jack
12	PORT-D	Pin complex	Rear panel front speaker jack
13	MONO_OUT	Pin complex	Monaural output pin (internal speakers or telephony system)
14	PORT-B	Pin complex	Front panel microphone jack
15	PORT-C	Pin complex	Rear panel line-in jack
16	PORT-F	Pin complex	Rear panel surround-back (5.1) jack
17	PORT-E	Pin complex	Rear panel microphone jack
18	CD IN	Pin complex	Analog CD input
19	Mixer Power-Down	Power widget	Powers down the analog mixer and associated amps
1A	Analog PCBEEP	Pin complex	External analog PCBEEP signal input
1B	S/PDIF Out	Pin complex	S/PDIF output pin
1C	S/PDIF In	Pin complex	S/PDIF input pin
1D	S/PDIF Mixer	Audio mixer	Mixes the selected ADC with the digital stream to drive S/PDIF out
1E	MONO_OUT Mixer	Audio mixer	Selects the source that drives the MONO_OUT signal
1F	Volume Knob	Vendor defined	Hardware volume knob
20	Analog Mixer	Audio mixer	Mixes individual gain analog inputs
21	Mixer Output Attenuator	Audio selector	Attenuates the mixer output to drive the port mixers
22	PORT-A Mixer	Audio mixer	Mixes the DAC_0 and mixer output amps to drive PORT-A
23	VREF Power-Down	Vendor defined	Powers down the internal and external VREF circuitry
24	PORT-G	Pin complex	Rear panel C/LFE jack
25	PORT-H	Pin complex	Rear panel surround-side (7.1) jack
26	PORT-E Mixer	Audio mixer	Mixes the PORT-E selected DAC and mixer output amps to drive PORT-E
27	PORT-G Mixer	Audio mixer	Mixes the DAC_3 and mixer output amps to drive PORT-G
28	PORT-H Mixer	Audio mixer	Mixes the DAC_4 and mixer output amps to drive PORT-H
29	PORT-D Mixer	Audio mixer	Mixes the DAC_1 and mixer output amps to drive PORT-D
2A	PORT-F Mixer	Audio mixer	Mixes the DAC_2 and mixer output amps to drive PORT-F
2B	PORT-B Mixer	Audio mixer	Mixes the PORT-B selected DAC and mixer output amps to drive PORT-B
2C	PORT-C Mixer	Audio mixer	Mixes the PORT-C selected DAC and mixer output amps to drive PORT-C
2D	Stereo Mix-Down	Audio mixer	Mixes the stereo L/R channels to drive MONO_OUT
2F	BIAS Power-Down	Vendor defined	Powers down the internal MIC_BIAS_FILT and all MIC_BIAS pins
30	PORT-B Out Selector	Audio selector	Selects DAC_0, DAC_1, and DAC_3 for PORT-B
31	PORT-C Out Selector	Audio selector	Selects DAC_2 and DAC_4 for PORT-C
32	PORT-E Out Selector	Audio selector	Selects DAC_2 and DAC_4 for PORT-E
33	PORT-C In Selector	Audio selector	Selects from the PORT-C, PORT-G, and PORT-H inputs to the mixer input

Node ID	Name	Type	Description
34	PORT-E In Selector	Audio selector	Selects from the PORT-E, PORT-G, and PORT-H inputs to the mixer input
36	MONO_OUT Selector	Audio selector	Selects DAC_0, DAC_1, and DAC_3 for MONO_OUT
37	PORT-A Out Selector	Audio selector	Selects DAC_0, DAC_1, and DAC_3 for PORT-A
38	PORT-A Boost	Audio selector	Microphone boost amp for PORT-A
39	PORT-B Boost	Audio selector	Microphone boost amp for PORT-B
3A	PORT-C Boost	Audio selector	Microphone boost amp for PORT-C
3B	PORT-F Boost	Audio selector	Microphone boost amp for PORT-F
3C	PORT-E Boost	Audio selector	Microphone boost amp for PORT-E
3D	PORT-D Boost	Audio selector	Microphone boost amp for PORT-D

Table 11. AD1988A Device Root and Function Node Parameters

Node ID	Name	Vendor ID 0x00	Revision ID[1] 0x02	Sub Node Count 0x04	Function Group Type 0x05	Audio Function Group Capabilities 0x08	GPIO Capabilities 0x11
00	ROOT	11D41988	00100400	00010001			
01	FUNCTION			0002003C	00000001	00010C0C	40000002

[1] Silicon revision number may change without prior notice. Number shown is current at the publication date of this document.

Table 12. AD1988B Device Root and Function Node Parameters

Node ID	Name	Vendor ID 0x00	Revision ID[1] 0x02	Sub Node Count 0x04	Function Group Type 0x05	Audio Function Group Capabilities 0x08	GPIO Capabilities 0x11
00	ROOT	11D4198B	00100300	00010001			
01	FUNCTION			0002003C	00000001	00010C0C	40000002

[1] Silicon revision number may change without prior notice. Number shown is current at the publication date of this document.

Table 13. Widget Parameters

Node ID	Type ID	Widget Capabilities	PCM Size, Rate	Stream Formats	Pin Capabilities	Input Amp Capabilities	Con. List Length	Power States	Output Amp Capabilities	Volume Knob Capabilities
		09	0A	0B	0C	0D	0E	0F	12	13
01	X	000004C0	000E07FF	00000001		80000000		00000009	00052727	
02	0	00030311	000E07E0	00000005			00000001			
03	0	00000405	000E07FF	00000001			00000000	00000009	00052727	
04	0	00000405	000E07FF	00000001			00000000	00000009	00052727	
05	0	00000405	000E07FF	00000001			00000000	00000009	00052727	
06	0	00000405	000E07FF	00000001			00000000	00000009	00052727	
07	1	00130391	000E07E0	00000005			00000001			
08	1	00100501	000E07FF	00000001			00000001	00000009		
09	1	00100501	000E07FF	00000001			00000001	00000009		
0A	0	00000405	000E07FF	00000001			00000000	00000009	00052727	
0B	3	00300301					00000003			
0C	3	0030010D					00000007		80053627	
0D	3	0030010D					00000007		80053627	
0E	3	0030010D					00000007		80053627	
0F	1	00100501	000E07FF	00000001			00000001	00000009		
10	7	0070000C					00000000		800B0F0F	
11	4	0040018D			0000373F		00000001		80000000	
12	4	0040018D			0000373F		00000001		80000000	
13	4	0040010C			00000010		00000001		80051F1F	
14	4	0040018D			0000373F		00000001		80000000	
15	4	0040018D			00003737		00000001		80000000	
16	4	0040018D			00003737		00000001		80000000	
17	4	0040098D			00003737		00000001		80000000	
18	4	00400001			00000020		00000000			
19	5	00500500					00000002	00000009		
1A	4	00400000			00000020		00000000			
1B	4	0040030D			00000010		00000001		80052727	
1C	4	0040020B			00000020	80051F17	00000000			
1D	2	00200303				80000000	00000002			
1E	2	00200103				80000000	00000002			
1F	6	00600080					00000000			000000BF
20	2	0020010B				80051F17	00000008			
21	3	0030010D					00000001		80051F1F	
22	2	00200103				80000000	00000002			
23	F	00F00100					00000008			
24	4	0040098D			00000037		00000001		80000000	
25	4	0040018D			00000037		00000001		80000000	
26	2	00200103				80000000	00000002			
27	2	00200103				80000000	00000002			
28	2	00200103				80000000	00000002			
29	2	00200103				80000000	00000002			
2A	2	00200103				80000000	00000002			
2B	2	00200103				80000000	00000002			
2C	2	00200103				80000000	00000002			
2D	2	00200100					00000001			
2F	F	00F00100					00000006			
30	3	00300101					00000003			
31	3	00300101					00000002			

Node ID	Type ID	Widget Capabilities 09	PCM Size, Rate 0A	Stream Formats 0B	Pin Capabilities 0C	Input Amp Capabilities 0D	Con. List Length 0E	Power States 0F	Output Amp Capabilities 12	Volume Knob Capabilities 13
32	3	00300101					00000002			
33	3	00300101					00000003			
34	3	00300101					00000003			
36	3	00300101					00000003			
37	3	00300101					00000003			
38	3	0030010D					00000001		00270300	
39	3	0030010D					00000001		00270300	
3A	3	0030010D					00000001		00270300	
3B	3	0030010D					00000001		00270300	
3C	3	0030010D					00000001		00270300	
3D	3	0030010D					00000001		00270300	

Table 14. Connection List

Node	Connections			0		1		2		3		4		5		6		7	
ID	0 to 3	4 to 7	Length	NID	I	NID	I	NID	I	NID	I	NID	I	NID	I	NID	I	NID	I	NID
02	0000001D		1	1D																
03			0																	
04			0																	
05			0																	
06			0																	
07	0000001C		1	1C																
08	0000000C		1	0C																
09	0000000D		1	0D																
0A			0																	
0B	000F0908		3	08		09		0F												
0C	2418BC38	00203D25	7	38	1	3C		18		24		25		3D		20				
0D	2418BC38	00203D25	7	38	1	3C		18		24		25		3D		20				
0E	2418BC38	00203D25	7	38	1	3C		18		24		25		3D		20				
0F	0000000E		1	0E																
10			0																	
11	00000022		1	22																
12	00000029		1	29																
13	0000002D		1	2D																
14	0000002B		1	2B																
15	0000002C		1	2C																
16	0000002A		1	2A																
17	00000026		1	26																
18			0																	
19	00002120		2	20		21														
1A			0																	
1B	00000002		1	02																
1C			0																	
1D	00000B01		2	01		0B														
1E	00002136		2	36		21														
1F			0																	
20	3D383339	1A183B34	8	39		33		38		3D		34		3B		18		1A		
21	00000020		1	20																
22	00002137		2	37		21														
23	25249811	2120BD38	8	11	1	18		24		25		38	1	3D		20		21		
24	00000027		1	27																
25	00000028		1	28																
26	00002132		2	32		21														
27	00002105		2	05		21														
28	0000210A		2	0A		21														
29	00002104		2	04		21														
2A	00002106		2	06		21														
2B	00002130		2	30		21														
2C	00002131		2	31		21														
2D	0000001E		1	1E																
2F	15141211	00001716	6	11		12		14		15		16		17						
30	00060403		3	03		04		06												
31	00000A04		2	04		0A														
32	00000405		2	05		04														
33	0024253A		3	3A		25		24												
34	0024253C		3	3C		25		24												

Node	Connections			0		1		2		3		4		5		6		7	
ID	0 to 3	4 to 7	Length		NID	I	NID	I	NID	I	NID	I	NID	I	NID	I	NID	I	NID
36	00060403		3		03		04		06										
37	00060403		3		03		04		06										
38	00000011		1		11														
39	00000014		1		14														
3A	00000015		1		15														
3B	00000016		1		16														
3C	00000017		1		17														
3D	00000012		1		12														

Table 15. Default Configuration Bytes[1]

	MSB	31	29	27	23	19	15	8	7	3
	LSB	30	28	24	20	16	12	8	4	0
Node			Location		Default	Conn		Misc	Def	
ID	Value	Connectivity	Chassis	Position	Device	Type	Color	JD Ovrrd	Assn	Seq
11	02214030	Jack	External	Front	HP out	⅛" jack	Green	0	3	0
12	01014010	Jack	External	Rear	Line out	⅛" jack	Green	0	1	0
13	9913011F	Fixed	Internal	Special 3	Speaker	ATAPI	Unknown	1	1	F
14	02A19040	Jack	External	Front	Mic in	⅛" jack	Pink	0	4	0
15	01813021	Jack	External	Rear	Line in	⅛" jack	Blue	0	2	1
16	01011012	Jack	External	Rear	Line out	⅛" jack	Black	0	1	2
17	01A19020	Jack	External	Rear	Mic in	⅛" jack	Pink	0	2	0
18	9933012E	Fixed	Internal	Special 3	CD	ATAPI	Unknown	1	2	E
1A	99F301F0	Fixed	Internal	Special 3	Other	ATAPI	Unknown	1	F	0
1B	014511F0	Jack	External	Rear	S/PDIF out	Optical	Black	1	F	0
1C	01C511F0	Jack	External	Rear	S/PDIF in	Optical	Black	1	F	0
24	01016011	Jack	External	Rear	Line out	⅛" jack	Orange	0	1	1
25	01012014	Jack	External	Rear	Line out	⅛" jack	Gray	0	1	4

[1] Default configuration values are set on codec power-up only. To preserve modifications by BIOS control, default configuration values do not change by reset operations.

JACK PRESENCE DETECTION

HD AUDIO STYLE JACK PRESENCE DETECTION

The AD1988 uses two jack sense pins for presence detection on up to eight audio jacks. This, combined with the device identification engine, enables software to determine if there is a device plugged into the circuit, and the type of device it is. Allowing software to configure jacks and amplifiers, as necessary, ensures proper audio operation.

Detect jack presence by using a resistor tree arrangement detailed by the HD audio specification, allowing up to four jacks per sense line. Jacks must have normally open, isolated switches to use this method of jack presence detection.

For proper operation, there must be a 2.67 kΩ 1% resistor connected between SENSE_A and AV_{DD}, and another 2.67 kΩ 1% resistor between SENSE_B and AV_{DD}.

The specific resistor values for each jack are listed in Table 16. Use 1% tolerance resistors to ensure accurate detection.

Table 16. Jack Sense Mapping

Resistor Value	SENSE_A			SENSE_B		
(1% Tolerance)	Name	Port	Node ID	Name	Port	Node ID
2.67 kΩ	Pull-up to AV_{DD}			Pull-up to AV_{DD}		
5.10 kΩ	FRONT	D	0x12	SURR_SIDE (7.1)	H	0x25
10.0 kΩ	LINE IN	C	0x15	C/LFE	G	0x24
20.0 kΩ	FRONT_MIC	B	0x14	SURR_BACK (5.1)	F	0x16
39.2 kΩ	HP_OUT	A	0x11	REAR_MIC	E	0x17

HARDWARE VOLUME CONTROL

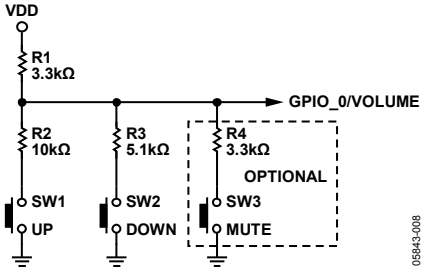


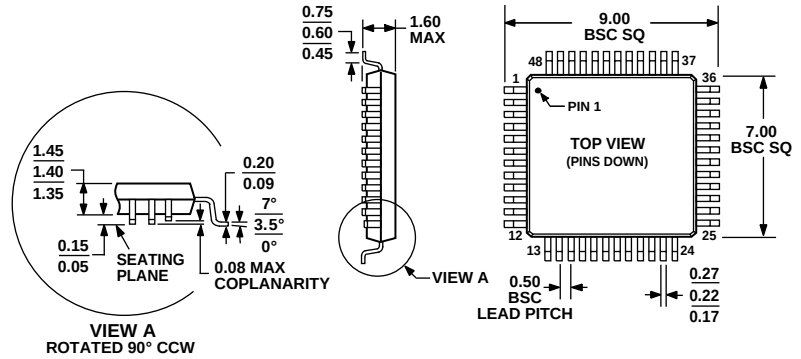
Figure 4 . Volume Control Circuitry

The AD1988A/AD1988B support external volume control on Pin 2 (GPIO_0/VOLUME). The circuit diagram in Figure 4 allows up/down/mute control using only three switches and four resistors external to the codec. The up/down switches can also be replaced by a center-position-off SPDT toggle switch. The mute switch is optional, but desirable, for a satisfactory user interface.

To use the GPIO_0/VOLUME pin (Pin 2) as a GPIO pin, it is recommended to pull it down using a 10 kΩ resistor (Pin 2 to DV_{SS}). In the GPIO configuration, the volume control widget has no effect.

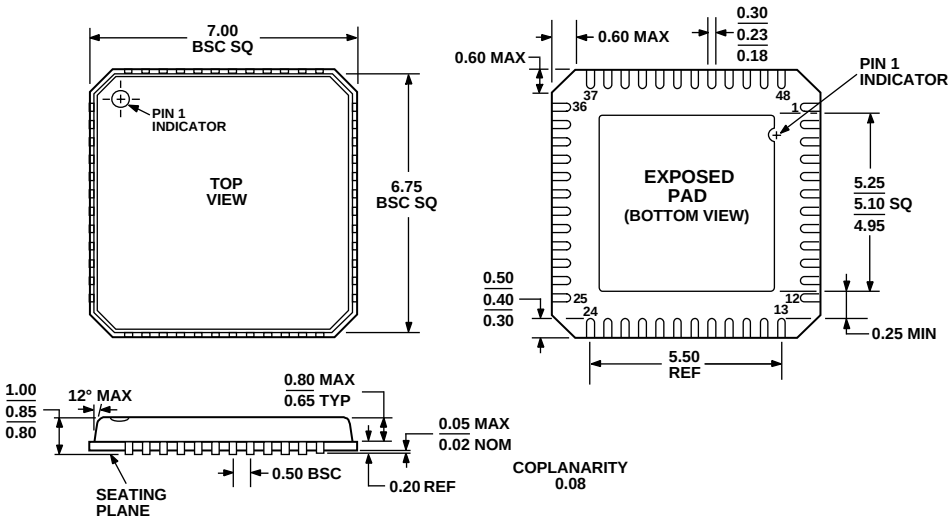
When the GPIO_0/VOLUME pin (Pin 2) is used as a volume control, pull-up Pin 2 to AV_{DD}. The volume control widget operates the codec volumes only under software control. If one of the buttons is pressed, the control volume setting is incremented (up), decremented (down), or set Bit 7 (mute). The volume control supports 40 steps (other than mute) and uses a range of 0 (0x00, minimum volume) to 63 (0x3F, maximum volume). Pressing the mute switch (or both up and down simultaneously) toggles Bit 7 which indicates mute on/off.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BBC

Figure 5. 48-Lead Low Profile Quad Flat Package [LQFP]
(ST-48)
Dimension shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VKKD-2

Figure 6. 48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
7 mm × 7 mm Body, Very Thin Quad
(CP-48-1)
Dimension shown in millimeters

ORDERING GUIDE

Model	Audio Output Performance	Temperature Range	Package Description	Package Option
AD1988AJSTZ[1]	95 dB	0°C to 70°C	48-Lead LQFP, Tray	ST-48
AD1988AJSTZ-RL[1]	95 dB	0°C to 70°C	48-Lead LQFP, Reel	ST-48
AD1988AJCPZ[1]	95 dB	0°C to 70°C	48-Lead LFCSP_VQ, Tray	CP-48-1
AD1988AJCPZ-RL[1]	95 dB	0°C to 70°C	48-Lead LFCSP_VQ, Reel	CP-48-1
AD1988BJSTZ[1]	101 dB	0°C to 70°C	48-Lead LQFP, Tray	ST-48
AD1988BJSTZ-RL[1]	101 dB	0°C to 70°C	48-Lead LQFP, Reel	ST-48
AD1988BJCPZ[1]	101 dB	0°C to 70°C	48-Lead LFCSP_VQ, Tray	CP-48-1
AD1988BJCPZ-RL[1]	101 dB	0°C to 70°C	48-Lead LFCSP_VQ, Reel	CP-48-1

[1] Z = Pb-free part.