D/A Converter Series for Electronic Adjustments

Standard 8bit 4ch・6ch Type D/A Converters

BH2227FV, BH2228FV

●Description

The BH2227FV and BH2228FV ICs are 8bit R-2R-type D/A converters with 4 and 6 channels, respectively. Optimized circuitry allows two output voltages to be supplied (3V/5V). Furthermore, the built-in RESET function ensures that the output voltage at all channels is Low during power up. A broad power supply voltage range is available (2.7V-5.5V), providing design flexibility.

●Features

1) Suitable for 2 independent power sources (3V/5V)
2) Built-in RESET function
3) High speed output response characteristics
4) 3-line serial interface
5) Broad power supply voltage range: 2.7V-5.5V

●Applications

DVCs, DSCs, DVDs, CD-Rs, CD-RWs

●Lineup

Parameter	BH2227FV	BH2228FV
Power source voltage range	2.7 to 5.5V	2.7 to 5.5V
Number of channels	4ch	6ch
Current consumption	0.9mA	0.9mA
Differential non linearity error	±1.0LSB	±1.0LSB
Integral non linearity error	±1.5LSB	±1.5LSB
Output current performance	±1.0mA	±1.0mA
Settling time	100µs	100µs
Data transfer frequency	10MHz	10MHz
Input method	CMOS	CMOS
Data latch method	CSB method	CSB method
Package	SSOP-B14	SSOP-B14

Apr.2008

●Absolute Maximum Ratings

(Ta=25℃)

Parameter	Symbol	Limits	Unit	Remarks
Power source voltage	VCC	-0.3 to 7.0	V	-
Terminal voltage	VIN	-0.3 to VCC	V	-
Storage temperature range	TSTG	-55 to 125	℃	-
Power dissipation	PD	400*1	mW	-

*1 Derated at 4.0mW/ ℃ at Ta>25℃

*2 This product is not robust against radiation.

●Recommended Operating Conditions

(Ta=25℃)

Parameter	Symbol	Limits			Unit	Remarks
		Min.	Typ.	Max.		
VDD power source voltage	VDD	2.7	-	5.5	V	-
VFS voltage to be impressed	VFS	2.7	-	5.5	V	-
Terminal input voltage range	VIN	0	-	VDD	V	-
Analog output current	IO	-1.0	-	1.0	mA	-
Action temperature range	TOPR	-20	-	85	℃	-
Serial clock frequency	FCLK	-	1.0	10.0	MHz	-
Limit load capacity	CL	-	-	0.1	μF	-

●Electrical Characteristics

(Unless otherwise specified, VDD=VFS=3.0V, RL=OPEN, CL=0pF, Ta=25℃)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
<Current consumption>						
VDD system	IDD	-	0.5	1.5	mA	VDD=5V, CLK=1MHz
VFS system	IFS	-	0.3	0.9	mA	
<Logic interface>						
L input voltage	VIL	VSS	-	0.6	V	VDD=5.0V
H input voltage	VIH	2.4	-	VDD	V	VDD=5.0V
Input current	IIN	-10	-	10	μA	
<Buffer amplifier>						
Output zero scale voltage	ZS	VSS	-	0.1	V	00h setting, at no load
		VSS	-	0.3	V	00h setting, IOL=1.0mA
Output full scale voltage	FS1	VDD-0.1	-	VDD	V	FFh setting, at no load
		VDD-0.3	-	VDD	V	FFh setting,IOH=1.0mA
	FS2	VFS-0.1	-	VFS	V	FFh setting, at no load
		VFS-0.3	-	VFS	V	FFh setting,IOH=1.0mA
<D/A converter precision>						
Differential non linearity error	DNL	-1.0	-	1.0	LSB	Input code 02H to FDH
Integral non linearity error	INL	-1.5	-	1.5	LSB	Input code 02H to FDH
VDD power source voltage rise time	trVDD	100	-	-	μs	VDD=0→2.7
Power ON reset release voltage	VPOR	-	1.9	-	V	

●Timing Chart

(Unless otherwise specified, VDD = VFS = 3.0V, RL = OPEN, CL = 0pF, Ta = 25℃)

Parameter	Symbol	Limits			Unit	Conditions
		MIN.	TYP.	MAX.		
CLK L level time	tCLKL	50	-	-	ns	
CLK H level time	tCLKH	50	-	-	ns	
DI setup time	tsDI	20	-	-	ns	
DI hold time	thDI	40	-	-	ns	
CSB setup time	tsCSB	50	-	-	ns	
CSB hold time	thCSB	50	-	-	ns	
CSB H level time	tCSBH	50	-	-	ns	
D/A Output settling time	tOUT	-	-	100	μs	CL=50pF,RL=10kΩ

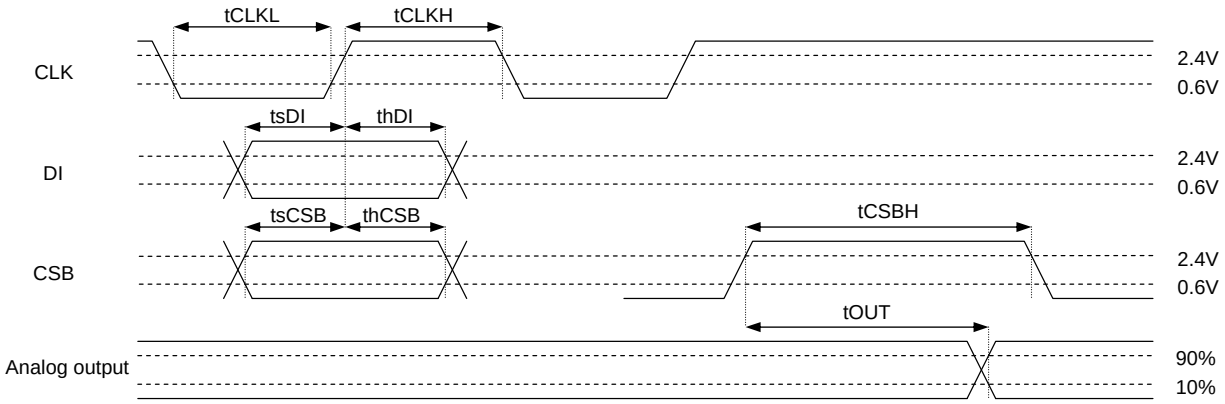
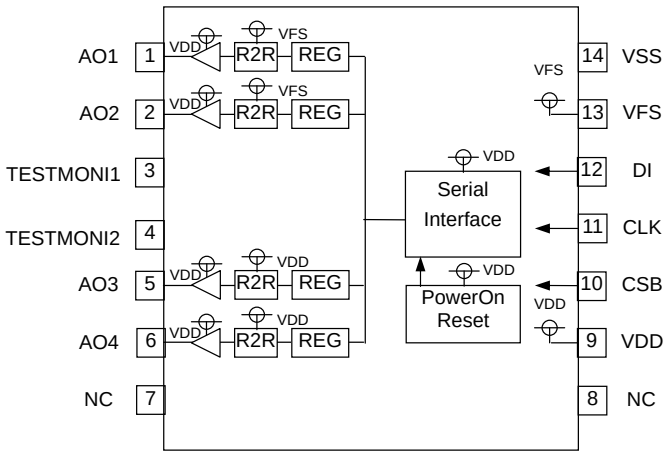


Fig.1

● Terminal Description / Block Diagrams

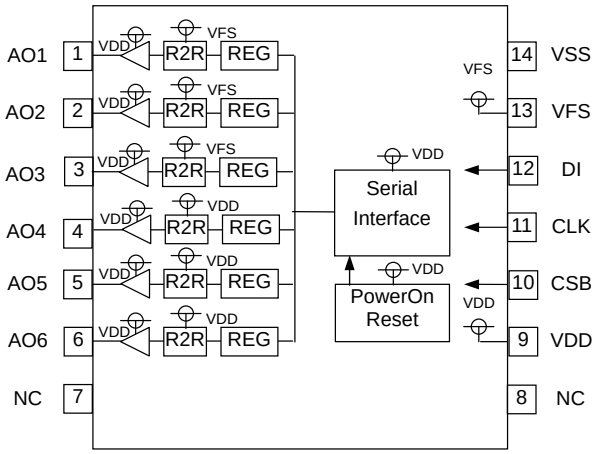
(BH2227FV)

Terminal	Terminal name	Function
1	AO1	Analog output terminal
2	AO2	
3	TESTMONI1	Test terminal (OPEN at normal use)
4	TESTMONI2	
5	AO3	Analog output terminal
6	AO4	
7	NC	Internally not connected yet
8	NC	
9	VDD	Power source terminal (AO3, 4 full scale voltage use in common)
10	CSB	Chip select signal input terminal
11	CLK	Serial clock input terminal
12	DI	Serial data input terminal
13	VFS	AO1,2 full scale Voltage setting terminal
14	VSS	Ground terminal



(BH2228FV)

Terminal	Terminal name	Function
1	AO1	Analog output terminal
2	AO2	
3	AO3	
4	AO4	
5	AO5	
6	AO6	
7	NC	Internally not connected yet
8	NC	
9	VDD	Power source terminal (AO4~6 full scale voltage use in common)
10	CSB	Chip select signal input terminal
11	CLK	Serial clock input terminal
12	DI	Serial data input terminal
13	VFS	AO1,2,3 full scale Voltage setting terminal
14	VSS	Ground terminal



●Equivalent Circuits

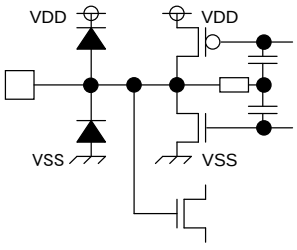
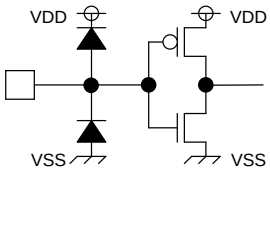
Terminal	Equivalent circuit	Terminal	Equivalent circuit
AO1 AO2 AO3 AO4 AO5 AO6		DI CLK CSB	

Fig.4 Equivalent circuit

●Operation Description

· Command Transmission

The Control command consists of 3-lines of 12bit serial input data (MSB first).

Data is read at the rise edge of CLK, and data becomes valid in the CSB Low area (before the CSB rise for 12bit data).

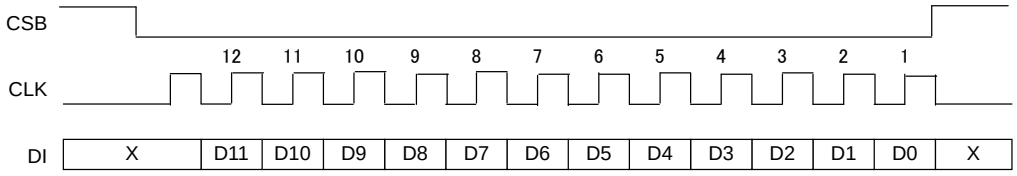


Fig.5

Data Settings

D0	D1	D2	D3	D4	D5	D6	D7	Setting
0	0	0	0	0	0	0	0	GND
1	0	0	0	0	0	0	0	(VDD or VFS-GND)/256x1
0	1	0	0	0	0	0	0	(VDD or VFS-GND)/256x2
1	1	0	0	0	0	0	0	(VDD or VFS-GND)/256x3
0	0	1	0	0	0	0	0	(VDD or VFS-GND)/256x4
~								~
0	1	1	1	1	1	1	1	(VDD or VFS-GND)/256x254
1	1	1	1	1	1	1	1	(VDD or VFS-GND)/256x255

Note: Initial status D[7:0]=00h

Channel Settings

D8	D9	D10	D11	BH2227FV	BH2228FV
0	0	0	0	Inconsequential	Inconsequential
0	0	0	1	AO1	AO1
0	0	1	0	AO2	AO2
0	0	1	1	Inconsequential	AO3
0	1	0	0	Inconsequential	AO4
0	1	0	1	AO3	AO5
0	1	1	0	AO4	AO6
0	1	1	1	Inconsequential	Inconsequential
1	0	0	0	Inconsequential	Inconsequential
1	0	0	1	Inconsequential	Inconsequential
1	0	1	0	Inconsequential	Inconsequential
1	0	1	1	Inconsequential	Inconsequential
1	1	0	0	Inconsequential	Inconsequential
1	1	0	1	Inconsequential	Inconsequential
1	1	1	0	Inconsequential	Inconsequential
1	1	1	1	Inconsequential	Inconsequential

●Electrical Characteristics Curves

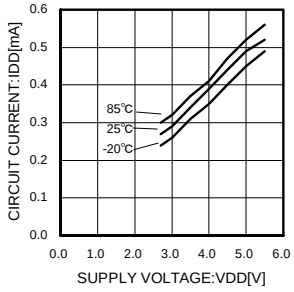


Fig.6 VDD current consumption

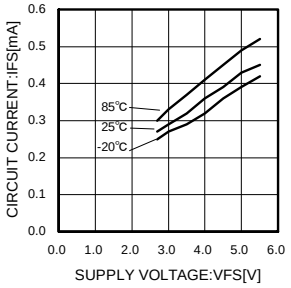


Fig.7 VFS current consumption

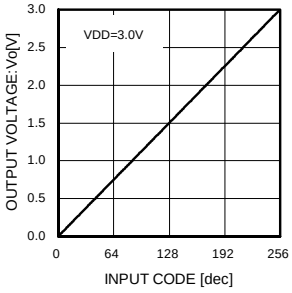


Fig.8 Output voltage characteristic

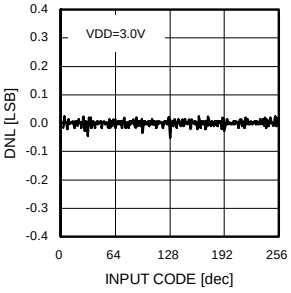


Fig.9 Differential non linearity error

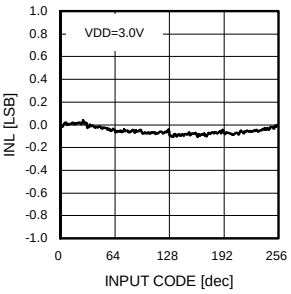


Fig.10 Integral non linearity error

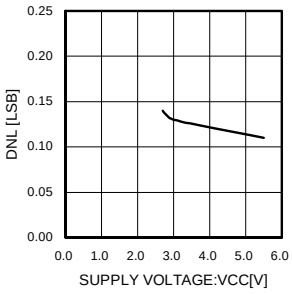


Fig.11 Power source voltage to differential non linearity error

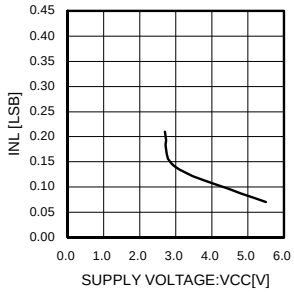


Fig.12 Power source voltage to integral non linearity error

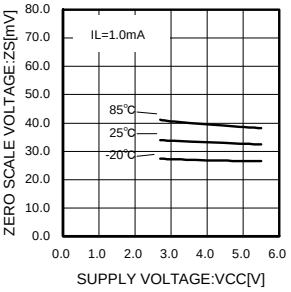


Fig.13 Output zero scale voltage

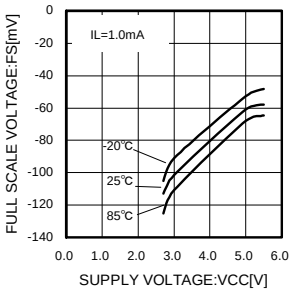


Fig.14 Output full scale voltage

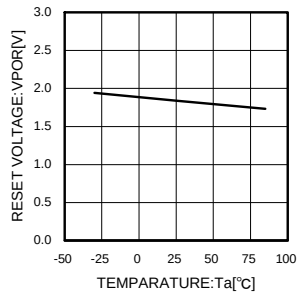


Fig.15 Reset release voltage

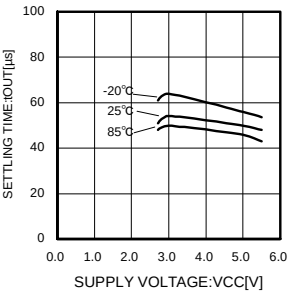


Fig.16 Settling time

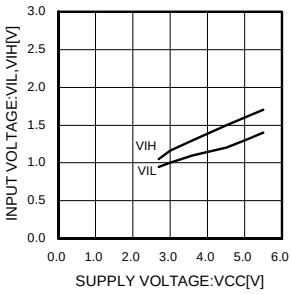


Fig.17 Input voltage

● Operation Notes

(1) Absolute maximum ratings

Operating or testing the device over the maximum specifications may damage the part itself as well as peripheral components. Therefore, please ensure that the specifications are not exceeded.

(2) GND potential

Ensure that the GND terminal is at the lowest potential under all operating conditions.

(3) Thermal design

Use a thermal design that allows for a sufficient margin regarding power dissipation (Pd) under actual operating conditions.

(4) Terminal shorts and mis-mounting

Incorrect orientation or misalignment of the IC when mounting to the PCB may damage part. Short-circuits caused by The introduction of foreign matter between the output terminals or across the output and power supply or GND may also result in destruction.

(5) Operation in a strong magnetic field

Operation in a strong electromagnetic field may cause malfunction.

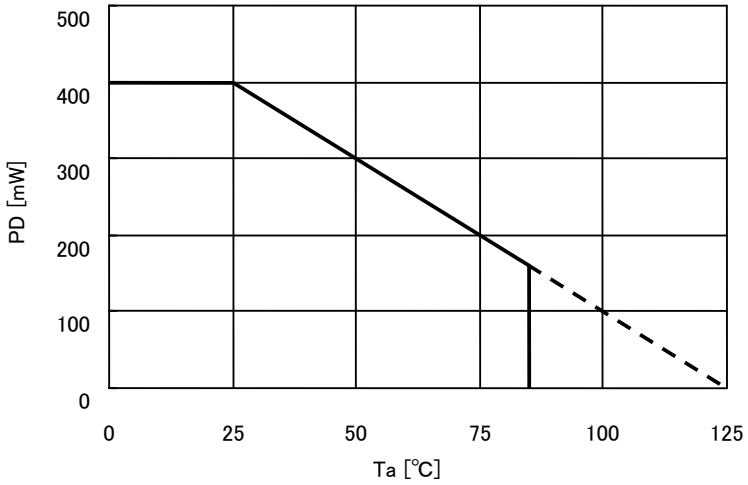
(6) Set the power source voltage so that VDD ≧ VFS.

(7) Reset function

The power on reset circuit, which initializes internal settings, may malfunction during abrupt power ons. Therefore, set the time constant so as to satisfy the power source rise time.

● Thermal Derating Curve

・SSOP-B14



Board size : 70 x 70 x 1.6mm　Material : FR4 glass epoxy board (copper foil area less than 3%)

Fig.18

●Part Number Explanation

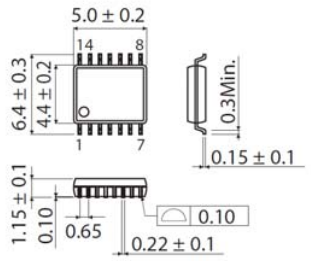
B	H	2	2	2	7	F	V	-	E	2

Part No.
BH2227FV
BH2228FV

Package and forming specification

SSOP-B14

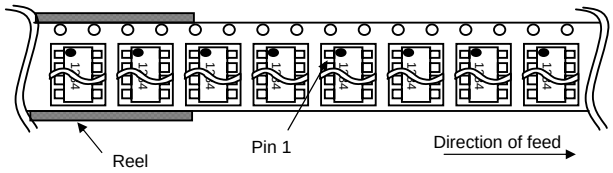
<Dimensions>



(Unit:mm)

<Tape and Reel Information>

Tape	Embossed carrier tape
Quantity	2,500pcs
Direction of feed	E2 (Pin 1 at the upper left when holding the reel with the left hand while pulling the tape out towards the right)



※Please order in multiples of the minimum quantity

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