Quad Digitally-Controlled (XDCP™) Potentiometer

The X9252 integrates 4 digitally controlled potentiometers (XDCP) on a monolithic CMOS integrated circuit.

The digitally controlled potentiometers are implemented using 255 resistive elements in a series array. Between each pair of elements are tap points connected to wiper terminals through switches. The position of each wiper on the array is controlled by the user through the Up/Down (U/$\overline{D}$) or 2-wire bus interface. The wiper of each potentiometer has an associated volatile Wiper Counter Register (WCR) and four non-volatile Data Registers (DRs) that can be directly written to and read by the user. The contents of the WCR controls the position of the wiper on the resistor array through the switches. At power-up, the device recalls the contents of the default data registers DR00, DR10, DR20, DR30, to the corresponding WCR.

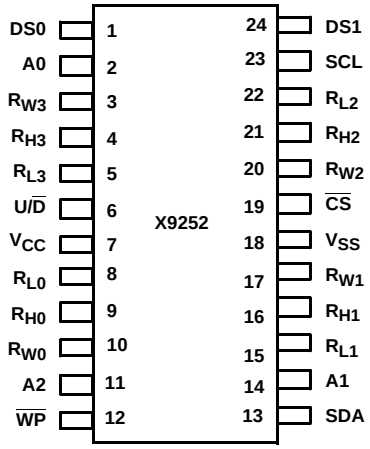
Each DCP can be used as a three-terminal potentiometer or as a two terminal variable resistor in a wide variety of applications including the programming of bias voltages, the implementation of ladder networks, and three resistor programmable networks.

Features

- Quad Solid State Potentiometer
- 256 Wiper Tap Points-0.4% Resolution
- 2-Wire Serial Interface for Write, Read, and Transfer Operations of the Potentiometer
- Up/Down Interface for Individual Potentiometers
- Wiper Resistance: 40Ω Typical
- Non-Volatile Storage of Wiper Positions
- Power On Recall. Loads Saved Wiper Position on Power-Up.
- Standby Current < 100µA Max
- Maximum Wiper Current: 3mA
- V_{CC}: 2.7V to 5.5V Operation
- 2.8kΩ,10kΩ, 50kΩ, 100kΩ Version of Total Pot Resistance
- Endurance: 100,000 Data Changes per Bit per Register
- 100 yr. Data Retention
- 24 Ld SOIC, 24 Ld TSSOP
- Pb-Free Plus Anneal Available (RoHS Compliant)

Pinout

X9252
(24 LD SOIC/TSSOP)
TOP VIEW

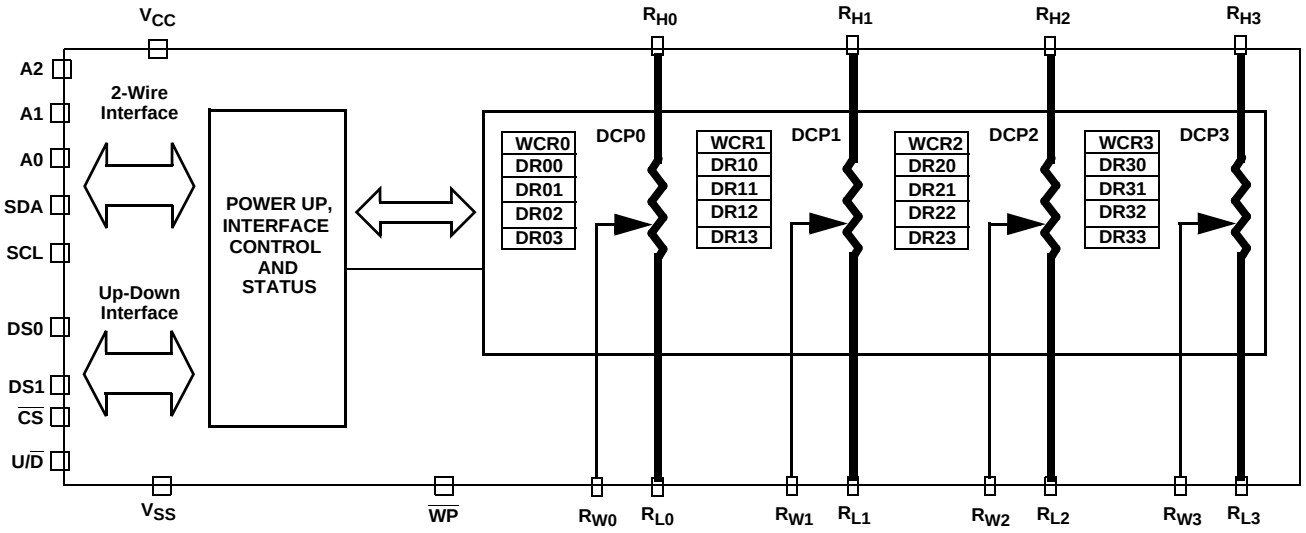


Ordering Information

PART NUMBER	PART MARKING	R_{TOTAL} (kΩ)	TEMP RANGE (°C)	PACKAGE
X9252YS24I-2.7		2.8	-40 to 85	24 Ld SOIC (300 mil)
X9252YS24IZ-2.7 (Note)			-40 to 85	24 Ld SOIC (300 mil) (Pb-Free)
X9252YV24I-2.7	X9252YV G		-40 to 85	24 Ld TSSOP (4.4mm)
X9252YV24IZ-2.7 (Note)	X9252YV Z G		-40 to 85	24 Ld TSSOP (4.4mm) (Pb-free)
X9252WS24I-2.7	X9252WS G	10	-40 to 85	24 Ld SOIC (300 mil)
X9252WS24IZ-2.7 (Note)	X9252WS Z G		-40 to 85	24 Ld SOIC (300 mil) (Pb-Free)
X9252WV24I-2.7	X9252WV G		-40 to 85	24 Ld TSSOP (4.4mm)
X9252WV24IZ-2.7 (Note)	X9252WV Z G		-40 to 85	24 Ld TSSOP (4.4mm) (Pb-free)
X9252US24I-2.7	X9252US G	50	-40 to 85	24 Ld SOIC (300 mil)
X9252US24IZ-2.7 (Note)	X9252US Z G		-40 to 85	24 Ld SOIC (300 mil) (Pb-Free)
X9252UV24I-2.7	X9252UV G		-40 to 85	24 Ld TSSOP (4.4mm)
X9252UV24IZ-2.7 (Note)	X9252UV Z G		-40 to 85	24 Ld TSSOP (4.4mm) (Pb-free)
X9252TS24I-2.7	X9252TS G	100	-40 to 85	24 Ld SOIC (300 mil)
X9252TS24IZ-2.7 (Note)	X9252TS Z G		-40 to 85	24 Ld SOIC (300 mil) (Pb-Free)
X9252TV24I-2.7	X9252TV G		-40 to 85	24 Ld TSSOP (4.4mm)
X9252TV24IZ-2.7 (Note)	X9252TV Z G		-40 to 85	24 Ld TSSOP (4.4mm) (Pb-free)

Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Functional Diagram



Pin Descriptions

SOIC/TSSOP PIN	SYMBOL	BRIEF DESCRIPTION
1	DS0	DCP select for Up/Down interface.
2	A0	Device address for 2-wire bus.
3	RW3	Wiper terminal of DCP3.
4	RH3	High terminal of DCP3.

Pin Descriptions (Continued)

SOIC/TSSOP PIN	SYMBOL	BRIEF DESCRIPTION
5	RL3	Low terminal of DCP3.
6	U/$\overline{D}$	Increment/decrement for up/down interface.
7	VCC	System supply voltage
8	RL0	Low terminal of DCP0.
9	RH0	High terminal of DCP0.
10	RW0	Wiper terminal of DCP0.
11	A2	Device address for 2-wire bus.
12	$\overline{WP}$	Hardware write protect
13	SDA	Serial data input/output for 2-wire bus.
14	A1	Device address for 2-wire bus.
15	RL1	Low terminal of DCP1.
16	RH1	High terminal of DCP1.
17	RW1	Wiper terminal DCP1.
18	VSS	System ground
19	$\overline{CS}$	Chip select for Up/Down interface.
20	RW2	Wiper terminal of DCP2.
21	RH2	High terminal of DCP2.
22	RL2	Low terminal of DCP2.
23	SCL	Serial clock for 2-wire bus.
24	DS1	DCP select for up/down interface.

Pin Descriptions

Bus Interface Pins

Serial Data Input/Output (SDA)

The SDA is a bidirectional serial data input/output pin for the 2-wire interface. It receives device address, operation code, wiper register address and data from a 2-wire external master device at the rising edge of the serial clock SCL, and it shifts out data after each falling edge of the serial clock SCL.

SDA requires an external pull-up resistor, since it's an open drain output.

Serial Clock (SCL)

This input is the serial clock of the 2-wire and Up/Down interface.

Device Address (A2-A0)

The Address inputs are used to set the least significant 3 bits of the 8-bit 2-wire interface slave address. A match in the slave address serial data stream must be made with the Address input pins in order to initiate communication with the X9252. A maximum of 8 devices may occupy the 2-wire serial bus.

Chip Select ($\overline{CS}$)

When the $\overline{CS}$ pin is low, increment or decrement operations are possible using the SCL and U/$\overline{D}$ pins. The 2-wire interface is disabled at this time. When $\overline{CS}$ is high, the 2-wire interface is enabled.

Up or Down Control (U/$\overline{D}$)

The U/$\overline{D}$ input pin is held HIGH during increment operations and held LOW during decrement operations.

DCP Select (DS1-DS0)

The DS1-DS0 select one of the four DCPs for an Up/Down interface operation.

Hardware Write Protect Input ($\overline{WP}$)

When the $\overline{WP}$ pin is set low, "write" operations to non volatile DCP Data Registers are disabled. This includes both 2-wire interface non-volatile "Write", and Up/Down interface "Store" operations.

DCP Pins

R_{H0}, R_{L0}, R_{H1}, R_{L1}, R_{H2}, R_{L2}, R_{H3}, and R_{L3}

These pins are equivalent to the terminal connections on mechanical potentiometers. Since there are 4 DCPs, there is one set of R_H and R_L for each DCP.

R_{W0}, R_{W1}, R_{W2}, and R_{W3}

The wiper pins are equivalent to the wiper terminal of mechanical potentiometers. Since there are four DCPs, there are 4 R_W pins.

Absolute Maximum Ratings

Junction Temperature under bias. . . . . .-65°C to +135°C
Storage temperature . . . . . .-65°C to +150°C
Voltage at any digital interface pin
with respect to V_{SS} . . . . . -1V to +7V
V_{CC} . . . . . -1V to +7V
Voltage at any DCP pin with
respect to V_{SS} . . . . . -1V to V_{CC}
Lead temperature (soldering, 10s). . . . . .300°C
I_W (10s) . . . . . ±6mA

Recommended Operating Conditions

Commercial . . . . . 0°C to +70°C
Industrial . . . . . .-40°C to +85°C
Supply Voltage (V_{CC})(Note 4) Limits . . . . . 2.7V to 5.5V

CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Analog Specifications

Over recommended operating conditions unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 4)	MAX	UNIT
R_{TOTAL}	End to end resistance	Y, W, U, T versions respectively		2.8, 10, 50, 100		kΩ
	End to end resistance tolerance		-20		+20	%
	Power rating	25°C, each DCP			50	mW
R_{TOTAL} Matching	DCP to DCP resistance matching			0.75	2.0	%
I_W (Note 5)	Wiper current	See test circuit	-3.0		+3.0	mA
R_W	Wiper resistance	Wiper current = $\frac{V_{CC}}{R_{TOTAL}}$		50	150	Ω
V_{TERM}	Voltage on any DCP pin		Vss		Vcc	V
	Noise (Note 5)	Ref: 1kHz		-120		dBV
	Resolution			0.4		%
	Absolute linearity (Note 1)	$V(R_{H0})=V(R_{H1})=V(R_{H2})=V(R_{H3})=V_{CC}$ $V(R_{L0})=V(R_{L1})=V(R_{L2})=V(R_{L3})=V_{SS}$	-1		+1	MI (Note 3)
	Relative linearity (Note 2)		-0.3		+0.3	MI (Note 3)
	Temperature coefficient of resistance (Note 5)			±300		ppm/°C
	Ratiometric Temperature (Note 5) Coefficient		-20		+20	ppm/°C
$C_H/C_L/C_W$	Potentiometer Capacitance (Note 5)	See equivalent circuit		10/10/25		pF
I_{OL}	Leakage on DCP pins	Voltage at pin from V_{SS} to V_{CC}		0.1	10	µA

DC Electrical Specifications

Over the recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNITS
I_{CC1}	V_{CC} supply current (Volatile write/read)	f_{SCL} = 400kHz;SDA = Open; (for 2-Wire, Active, Read and Volatile Write States only)		3	mA
I_{CC2}	V_{CC} supply current (active)	f_{SCL} = 200kHz; (for $\overline{U/D}$ interface, increment, decrement)		3	mA
I_{CC3}	V_{CC} supply current (nonvolatile write)	f_{SCL} = 400kHz; SDA = Open; (for 2-Wire, Active, Nonvolatile Write State only)		5	mA
I_{SB}	V_{CC} current (standby)	V_{CC} = +5.5V; V_{IN} = V_{SS} or V_{CC}; SDA = V_{CC}; (for 2-Wire, Standby State only)		100	µA

DC Electrical Specifications Over the recommended operating conditions unless otherwise specified. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNITS
I_L	Leakage current, bus interface pins	Voltage at pin from V_{SS} to V_{CC}	-10	10	µA
V_{IH}	Input HIGH voltage		V_{CC} x 0.7	V_{CC} + 1	V
V_{IL}	Input LOW voltage		-1	V_{CC} x 0.3	V
V_{OL}	SDA pin output LOW voltage	I_{OL} = 3mA		0.4	V

Endurance and Data Retention

PARAMETER	MIN	UNITS
Minimum endurance	100,000	Data changes per bit
Data retention	100	Years

Capacitance

Symbol	Test	Test Conditions	Max.	Units
$C_{IN/OUT}$ (Note 5)	Input / Output capacitance (SDA)	V_{OUT} = 0V	8	pF
C_{IN} (Note 5)	Input capacitance (SCL, $\overline{WP}$, DS0, DS1, $\overline{CS}$, U/$\overline{D}$, A2, A1 and A0)	V_{IN} = 0V	6	pF

Power-Up Timing

SYMBOL	PARAMETER	MAX	UNITS
t_D (Notes 5, 9)	Power Up Delay from V_{CC} power up (V_{CC} above 2.7V) to wiper position recall completed, and communication interfaces ready for operation.	2	ms

A.C. Test Conditions

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input rise and fall times	10ns
Input and output timing threshold level	V_{CC} x 0.5
External load at pin SDA	2.3kΩ to V_{CC} and 100pF to V_{SS}

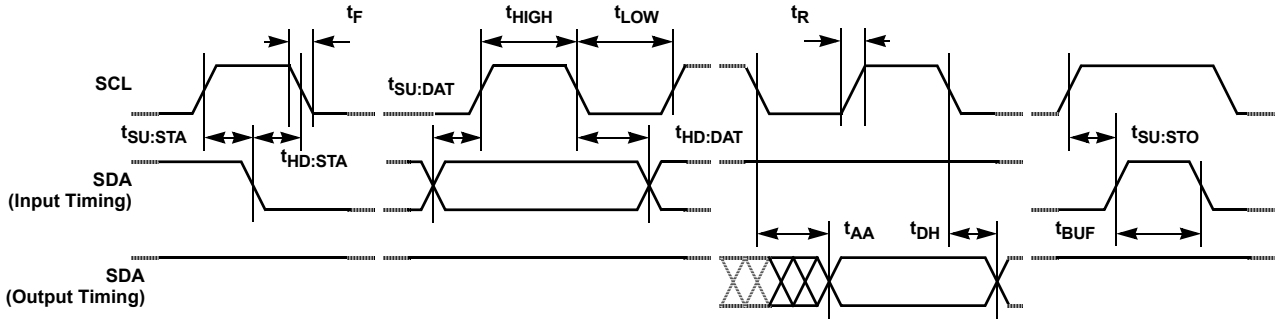
2-Wire Interface timing (s)

SYMBOL	PARAMETER	MIN	MAX	UNITS
f_{SCL}	Clock Frequency		400	kHz
t_{HIGH}	Clock High Time	600		ns
t_{LOW}	Clock Low Time	1300		ns
$t_{SU:STA}$	Start Condition Setup Time	600		ns
$t_{HD:STA}$	Start Condition Hold Time	600		ns
$t_{SU:STO}$	Stop Condition Setup Time	600		ns
$t_{SU:DAT}$	SDA Data Input Setup Time	100		ns
$t_{HD:DAT}$	SDA Data Input Hold Time	30		ns
t_R (Note 5)	SCL and SDA Rise Time		300	ns
t_F (Note 5)	SCL and SDA Fall Time		300	ns
t_{AA} (Note 5)	SCL Low to SDA Data Output Valid Time		0.9	µs
t_{DH}	SDA Data Output Hold Time	0		ns
t_{IN} (Note 5)	Pulse Width Suppression Time at SCL and SDA inputs		50	ns

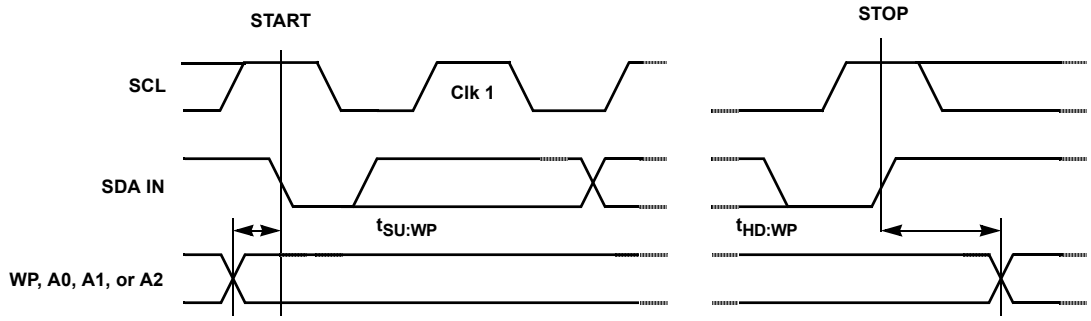
2-Wire Interface timing (s) (Continued)

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{BUF} (Note 5)	Bus Free Time (Prior to Any Transmission)	1200		ns
$t_{SU:WPA}$ (Note 5)	A0, A1, A2 and $\overline{WP}$ Setup Time	600		ns
$t_{HD:WPA}$ (Note 5)	A0, A1, A2 and $\overline{WP}$ Hold Time	600		ns

SDA vs SCL Timing



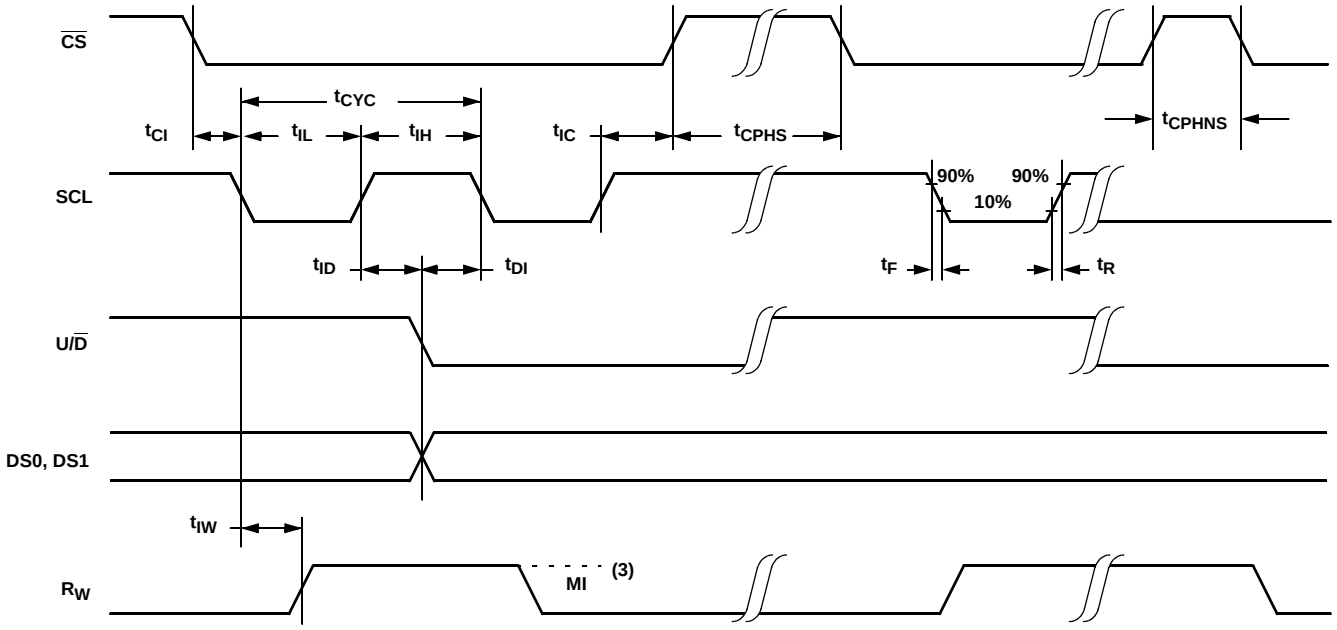
$\overline{WP}$, A0, A1, and A2 Pin Timing



Increment/Decrement Timing

SYMBOL	PARAMETER	MIN	TYP (Note 4)	MAX	UNITS
t_{CI}	$\overline{CS}$ to SCL Setup	600			ns
t_{ID} (Note 5)	SCL HIGH to U/$\overline{D}$, DS0 or DS1 change	600			ns
t_{DI} (Note 5)	U/$\overline{D}$, DS0 or DS1 to SCL setup	600			ns
t_{IL}	SCL LOW period	2.5			µs
t_{IH}	SCL HIGH period	2.5			µs
t_{IC}	SCL inactive to $\overline{CS}$ inactive (Nonvolatile Store Setup Time)	1			µs
t_{CPHS}	$\overline{CS}$ deselect time (STORE)	10			ms
t_{CPHNS} (Note 5)	$\overline{CS}$ deselect time (NO STORE)	1			µs
t_{IW} (Note 5)	SCL to R_W change		100	500	µs
t_{CYC}	SCL cycle time	5			µs
t_R, t_F (Note 5)	SCL input rise and fall time			500	µs

Increment/Decrement Timing



High-Voltage Write Cycle Timing

SYMBOL	PARAMETER	TYP	MAX	UNITS
t_{WC} (Notes 5, 8)	Non-volatile write cycle time	5	10	ms

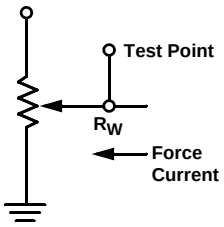
XDCP Timing

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{WRL} (Note 5)	SCL rising edge to wiper code changed, wiper response time after instruction issued (all load instructions)	5	20	µs

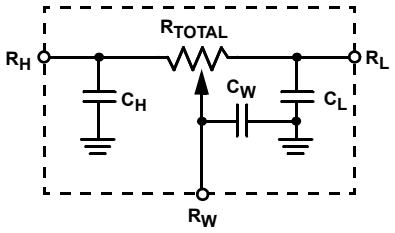
NOTES:

1. Absolute linearity is utilized to determine actual wiper voltage versus expected voltage = $[V(R_{W(n)(actual)})-V(R_{W(n)(expected)})]/MI$ $V(R_{W(n)(expected)}) = n(V(R_H)-V(R_L))/255 + V(R_L)$, with n from 0 to 255.
2. Relative linearity is a measure of the error in step size between taps = $[V(R_{W(n+1)})-(V(R_{W(n)}) + MI)]/MI$, with n from 0 to 254
3. 1 MI = Minimum Increment = $[V(R_H)-V(R_L)]/255$.
4. Typical values are for T_A = 25°C and nominal supply voltage.
5. This parameter is not 100% tested.
6. Ratiometric temperature coefficient = $(V(R_W)_{T1(n)}-V(R_W)_{T2(n)})/[V(R_W)_{T1(n)}(T1-T2)] \times 10^6$, with T1 & T2 being 2 temperatures, and n from 0 to 255.
7. Measured with wiper at tap position 255, R_L grounded, using test circuit.
8. t_{WC} is the minimum cycle time to be allowed for any nonvolatile write by the user, unless Acknowledge Polling is used. It is the time from a valid STOP condition at the end of a write sequence of a 2-wire interface write operation, or from the rising edge of $\overline{CS}$ of a valid “Store” operation of the Up/Down interface, to the end of the self-timed internal nonvolatile write cycle.
9. The recommended power up sequence is to apply V_{CC}/V_{SS} first, then the potentiometer voltages. During power up, the data sheet parameters for the DCP do not fully apply until t_D after V_{CC} reaches its final value. In order to prevent unwanted tap position changes, or an inadvertant store, bring the $\overline{CS}$ pin high before or concurrently with the V_{CC} pin on power up.

Test Circuit



Equivalent Circuit



Principles of Operation

The X9252 is an integrated circuit incorporating four resistor arrays, their associated registers and counters, and the serial interface logic providing direct communication between the host and the digitally controlled potentiometers. This section provides detail description of the following:

- Resistor Array
- Up/Down Interface
- 2-wire Interface

Resistor Array Description

The X9252 is comprised of four resistor arrays. Each array contains 255 discrete resistive segments that are connected in series. The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer (R_{Hi} and R_{Li} inputs) (See Figure 1.)

At both ends of each array and between each resistor segment is a switch connected to the wiper (R_{Wi}) pin.

Within each individual array only one switch may be turned on at a time.

These switches are controlled by a Wiper Counter Register (WCR). The 8-bits of the WCR (WCR[7:0]) are decoded to select and enable one of 256 switches (see Table 1). Note that each wiper has a dedicated WCR. When all bits of a WCR are zeroes, the switch closest to the corresponding R_L pin is selected. When all bits of a WCR are ones, the switch closest to the corresponding R_H pin is selected.

The WCR is volatile and may be written directly. There are four non-volatile Data Registers (DR) associated with each WCR. Each DR can be loaded into WCR. All DRs and WCRs can be read or written.

Power Up and Down Requirements

During power up, $\overline{CS}$ must be high, to avoid inadvertant “store” operations. At power up, the contents of Data Registers DR00, DR10, DR20, and DR30, are loaded into the corresponding wiper counter register.

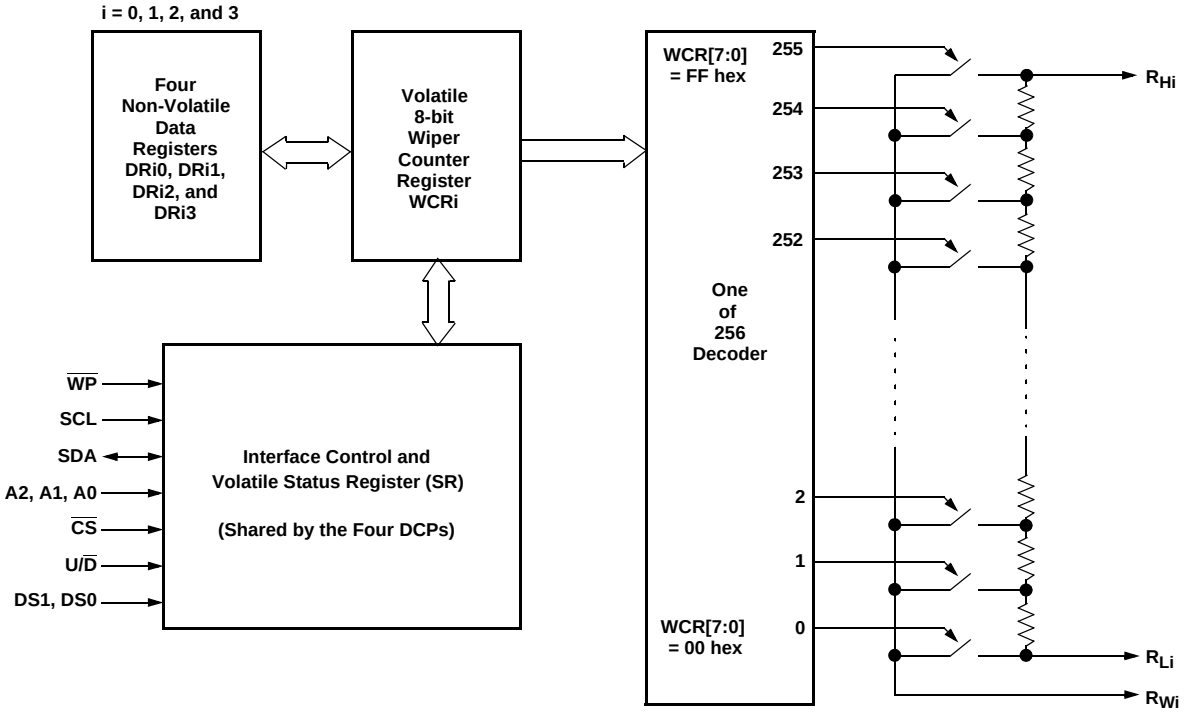


FIGURE 1. DETAILED BLOCK DIAGRAM OF ONE DCP

Up/Down Interface Operation

The SCL, U/$\overline{D}$, $\overline{CS}$, DS0 and DS1 inputs control the movement of the wiper along the resistor array. With $\overline{CS}$ set LOW the device is selected and enabled to respond to the U/$\overline{D}$ and SCL inputs. HIGH to LOW transitions on SCL will increment or decrement (depending on the state of the U/$\overline{D}$ input) a wiper counter register selected by DS0 and DS1. The output of this counter is decoded to select one of 256 wiper positions along the resistor array.

The value of the counter is stored in nonvolatile Data Registers DRi0 whenever $\overline{CS}$ transitions HIGH while the SCL and $\overline{WP}$ inputs are HIGH. “i” indicates the DCP number selected with pins DS1 and DS0. During a “Store” operation bits DRSel1 and DRSel0 in the Status Register must be both “0”, which is their power up default value. Other combinations are reserved and must not be used.

The system may select the X9252, move the wiper, and deselect the device without having to store the latest wiper position in nonvolatile memory. After the wiper movement is performed as described above and once the new position is reached, the system must keep SCL LOW while taking $\overline{CS}$ HIGH. The new wiper position will be maintained until changed by the system or until a power-down/up cycle recalled the previously stored data.

This procedure allows the system to always power-up to a preset value stored in nonvolatile memory; then during system operation minor adjustments could be made. The adjustments might be based on user preference, system parameter changes due to temperate drift, etc.

The state of U/$\overline{D}$ may be changed while $\overline{CS}$ remains LOW. This allows the host system to enable the device and then move the wiper up and down until the proper trim is attained. The 2-wire interface is disabled while $\overline{CS}$ remains LOW.

TABLE 1. DCP SELECTION FOR UP/DOWN CONTROL

DS1	DS0	SELECTED DCP
0	0	DCP0
0	1	DCP1
1	0	DCP2
1	1	DCP3

Mode Selection for Up/Down Control

$\overline{CS}$	SCL	U/$\overline{D}$	MODE
L	↘	H	Wiper Up
L	↘	L	Wiper Down
↗	H	X	Store Wiper Position to nonvolatile memory if $\overline{WP}$ pin is high. No store, return to standby, if $\overline{WP}$ pin is low.
H	X	X	Standby
↗	L	X	No Store, Return to Standby
↘	L	H	Wiper Up (not recommended)
↘	L	L	Wiper Down (not recommended)

2-Wire Serial Interface

Protocol Overview

The device supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is called the master and the device being controlled is called the slave. The master always initiates data transfers, and provides the clock for both transmit and receive operations. The X9252 operates as a slave in all applications.

All 2-wire interface operations must begin with a START, followed by a Slave Address byte. The Slave Address selects the X9252, and specifies if a Read or Write operation is to be performed.

All Communication over the 2-wire interface is conducted by sending the MSB of each byte of data first.

Serial Clock and Data

Data states on the SDA line can change only while SCL is LOW. SDA state changes while SCL is HIGH are reserved for indicating START and STOP conditions (See Figure 2). On power up of the X9252, the SDA pin is in the input mode.

Serial Start Condition

All commands are preceded by the START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The device continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition has been met (See Figure 2).

Serial Stop Condition

All communications must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH. The STOP condition is also used to place the device into the Standby power mode after a read sequence. A STOP condition can only be issued after the transmitting device has released the bus (See Figure 2).

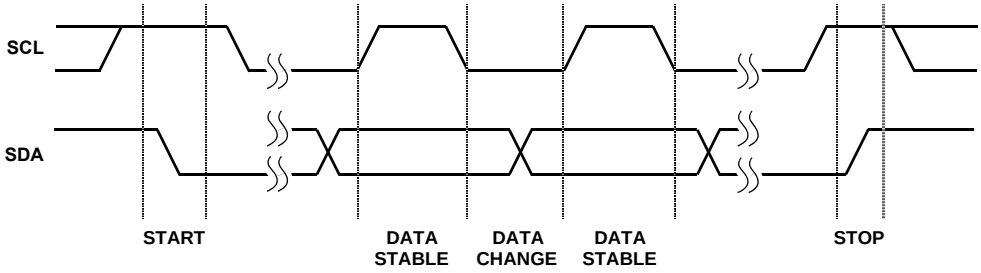


FIGURE 2. VALID DATA CHANGES, START, AND STOP CONDITIONS

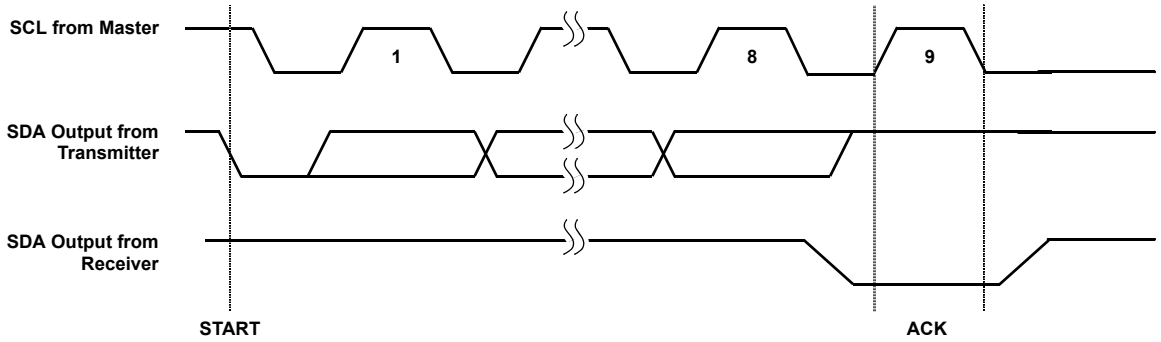


FIGURE 3. ACKNOWLEDGE RESPONSE FROM RECEIVER

Serial Acknowledge

An ACK (Acknowledge), is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (See Figure 3).

The device responds with an ACK after recognition of a START condition followed by a valid Slave Address byte. A valid Slave Address byte must contain the Device Type Identifier 0101, and the Device Address bits matching the logic state of pins A2, A1, and A0 (See Figure 4).

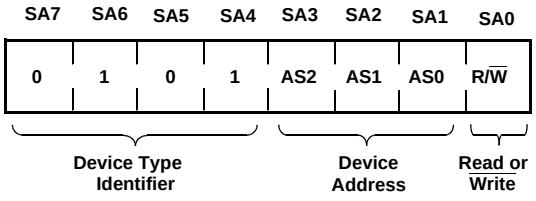
If a write operation is selected, the device responds with an ACK after the receipt of each subsequent eight-bit word.

In the read mode, the device transmits eight bits of data, releases the SDA line, and then monitors the line for an ACK. The device continues transmitting data if an ACK is detected. The device terminates further data transmissions if an ACK is not detected. The master must then issue a STOP condition to place the device into a known state.

Slave Address Byte

Following a START condition, the master must output a Slave Address Byte (Refer to figure 4.). This byte includes three parts:

- The four MSBs (SA7-SA4) are the Device Type Identifier, which must always be set to 0101 in order to select the X9252.
- The next three bits (SA3-SA1) are the Device Address bits (AS2-AS0). To access any part of the X9252's memory, the value of bits AS2, AS1, and AS0 must correspond to the logic levels at pins A2, A1, and A0 respectively.
- The LSB (SA0) is the R/$\overline{W}$ bit. This bit defines the operation to be performed on the device being addressed. When the R/$\overline{W}$ bit is "1", then a Read operation is selected. A "0" selects a Write operation.



SLAVE ADDRESS BIT(S)	DESCRIPTION
SA7-SA4	Device Type Identifier
SA3-SA1	Device Address
SA0	Read or Write Operation Select

FIGURE 4. SLAVE ADDRESS (SA) FORMAT

Nonvolatile Write Acknowledge Polling

After a nonvolatile write command sequence is correctly issued (including the final STOP condition), the X9252 initiates an internal high voltage write cycle. This cycle typically requires 5ms. During this time, any Read or Write command is ignored by the X9252. Write Acknowledge Polling is used to determine whether a high voltage write cycle is completed.

During acknowledge polling, the master first issues a START condition followed by a Slave Address Byte. The Slave Address Byte contains the X9252's Device Type Identifier and Device Address. The LSB of the Slave Address (R/$\overline{W}$) can be set to either 1 or 0 in this case. If the device is busy within the high voltage cycle, then no ACK is returned. If the high voltage cycle is completed, an ACK is returned and the master can then proceed with a new Read or Write operation. (Refer to figure 5.)

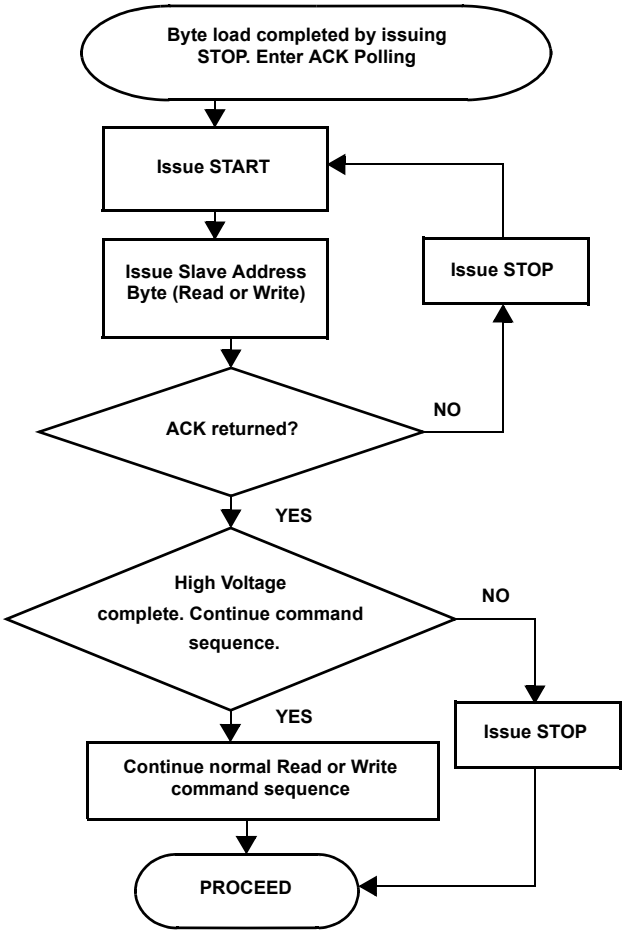


FIGURE 5. ACKNOWLEDGE POLLING SEQUENCE

2-Wire Serial Interface Operation

X9252 Digital Potentiometer Register Organization

Refer to the Functional Diagram on page 2. There are four Digitally Controlled Potentiometers, referred to as DCPi, i=0,1,2,3. Each potentiometer has one volatile Wiper Control Register (WCR) with the corresponding number, WCRi, i=0,1,2,3. Each potentiometer also has four nonvolatile registers to store wiper position or general data, these are numbered DRi0, DRi1, DRi2 and DRi3, i=0,1,2,3.

The registers are organized in five pages of four, with one page consisting of the WCRi (i=0-3), a second page containing the DRi0 (i=0-3), a third page containing the DRi1, and so forth. These pages can be written to four bytes at time. In this manner all four potentiometer WCRs can be updated in a single serial write (see "Page Write Operation"), as well as all four registers of a given page in the DR array.

The unique feature of the X9252 device is that writing or reading to a Data Register of a given DCP automatically updates/moves the WCR of that DCP with the content of the DR. In this manner data can be moved from a particular DCP register to that DCP's WCR just by performing a 2-wire read operation. Simultaneously, that data byte can be utilized by the host.

Status Register Organization

The Status Register (SR) is used in read and write operations to select the appropriate DCP register. Before any DCP register can be accessed, the SR must be set to the correct value. It is accessed by setting the Address Byte to 07h (See Table 3). Do this by Writing the Slave Address followed by a Byte Address of 07h. The SR is volatile and defaults to 00h on power up. It is an 8-bit register containing three control bits in the 3 LSBs as follows:

7	6	5	4	3	2	1	0
Reserved					DRSel1	DRSel0	NVEnable

Bits DRSel1 and DRSel0 determine which Data Register of a DCP is selected for a given operation. NVEnable is used to select the volatile WCR if "0", and one of the nonvolatile DCP registers if "1". Table 2 shows this register organization. "Store" operations using the Up/Down interface require that bits DRSel1 and DRSel0 are set to "0".

TABLE 2. REGISTER NUMBERING

STATUS REG (Note 1) (Addr: 07H)				REGISTERED SELECTED (Note 2)			
RESERVED BITS 7-3	DRSel1 bit 2	DRSel0 bit 1	NVEnable bit 0	DCP0 (Addr: 00h)	DCP1 (Addr: 01h)	DCP2 (Addr: 02h)	DCP3 (Addr: 03h)
Reserved	X	X	0	**WCR0**	**WCR1**	**WCR2**	**WCR3**
	0	0	1	DR00	DR10	DR20	DR30
	0	1	1	DR01	DR11	DR21	DR31
	1	0	1	DR02	DR12	DR22	DR32
	1	1	1	DR03	DR13	DR23	DR33

To read or write the contents of a single Data Register or Wiper Register:

1. **Load the status register (using a write command) to select the row** (See Figure 6)
   Writing a 1, 3, 5, or 7 to the Status Register specifies that the subsequent read or write command will access a Data Register. This Status Register operation also initiates a transfer of the contents of the selected data register to its associated WCR for all DCPs. So, for example, writing '03h' to the status register causes the value in DR01 to move to WCR0, DR11 to move to WCR1, DR21 to move to WCR2, and DR31 to move to WCR3.

   Writing a 0 to bit '0' of the Status Register specifies that the subsequent read or write command will access a Wiper Counter Register. Each WCR can be written to individually, without affecting the contents of any other.

2. **Access the desired DR or WCR using a new write or read command** (see Figure 7 for write and Figure 9 for read.)
   Specify the desired column (DCP number) by sending the DCP address as part of this read or write command.

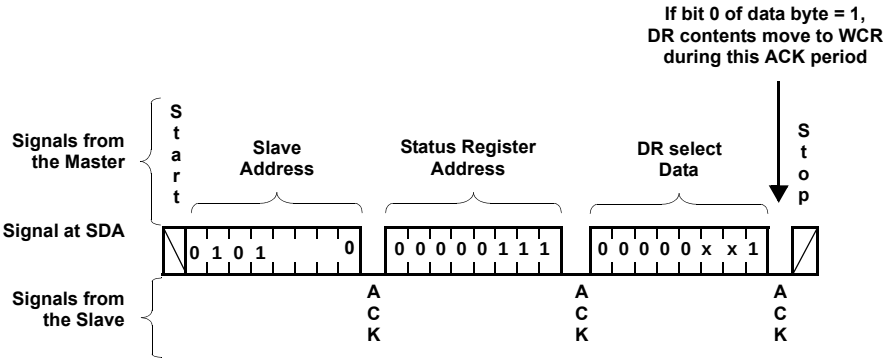


FIGURE 6. STATUS REGISTER WRITE (USES STANDARD BYTE WRITE SEQUENCE TO SET UP ACCESS TO A DATA REGISTER)

DCP Addressing for 2-Wire Interface

Once the register number has been selected by a 2-wire instruction, then the DCP number is determined by the Address Byte of the following instruction. Note again that this enables a complete page write of the DRs of all four potentiometers at once. The register addresses accessible in the X9252 include:

TABLE 3. 2-WIRE INTERFACE ADDRESS BYTE

ADDRESS (HEX)	CONTENTS
0	DCP 0
1	DCP 1
2	DCP 2
3	DCP 3
4	Not Used
5	Not Used
6	Not Used
7	Status Register

All other address bits in the Address Byte must be set to “0” during 2-wire write operations and their value should be ignored when read.

Byte Write Operation

For any Byte Write operation, the X9252 requires the Slave Address byte, an Address Byte, and a Data Byte (See Figure 7). After each of them, the X9252 responds with an ACK. The master then terminates the transfer by generating a STOP condition. At this time, if the write operation is to a volatile register (WCR, or SR), the X9252 is ready for the next read or write operation. If the write operation is to a nonvolatile register (DR), and the $\overline{WP}$ pin is high, the X9252 begins the internal write cycle to the nonvolatile memory. During the internal nonvolatile write cycle, the X9252 does not respond to any requests from the master. The SDA output is at high impedance.

The SR bits and $\overline{WP}$ pin determine the register being accessed through the 2-wire interface (See Table 2).

As noted before, any write operation to a Data Register (DR), also transfers the contents of all the data registers in that row to their corresponding WCR.

For example, to write 3Ahex to the Data Register 1 of DCP2 the following sequence is required:

START		
Slave Address	0101 0000	(Hardware Address = 000, and a Write command)
ACK		
Address Byte	0000 0111	(Indicates Status Register address)
ACK		
Data Byte	0000 0011	(Data Register 1 and NVEnable selected)
ACK		
note: at this ACK, the WCRs are all updated with their respective DR.		
STOP		
START		
Slave Address	0101 0000	(Hardware address = 000, Write command)
ACK		
Address Byte	0000 0010	(Access DCP2)
ACK		
Data Byte	0011 1010	(Write Data Byte 3Ah)
ACK		
STOP		

During the sequence of this example, $\overline{WP}$ pin must be high, and A0, A1, and A2 pins must be low. When completed, the DR21 register and the WCR2 will be set to 3Ah and the other Data Register in Row 1 will transfer their other contents to the respective WCR’s.

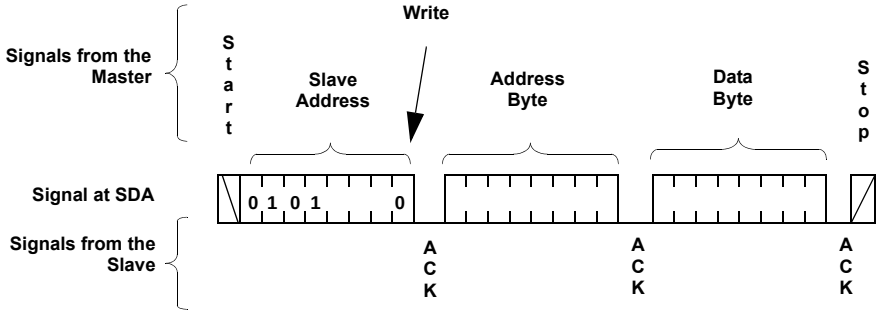


FIGURE 7. BYTE WRITE SEQUENCE

Page Write Operation

As stated previously, the memory is organized as a single Status Register (SR), and four pages of four registers each. Each page contains one Data Register for each DCP. The order of the bytes within a page is DR0i, followed by DR1i, followed by DR2i, and then DR3i, with i being the Data Register number (0, 1, 2, or 3). Normally a page write operation will be used to efficiently update all four data registers and WCR in a single write command, starting at DCP0 and finishing with DCP3.

In order to perform a Page Write operation to the memory array, the NVEnable bit in the SR must first be set to “1”.

A Page Write operation is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data byte is transferred, the master can transmit up to 4 bytes (See Figure 8). After the receipt of each byte, the X9252 responds with an ACK, and the internal DCP address counter is incremented by one. The page address remains constant. When the counter reaches the end of the page (DR3i, 03hex), it “rolls over” and goes back to the first byte of the same page (DR0i, 00hex).

For example, if the master writes 3 bytes to a page starting at location DR22, the first 2 bytes are written to locations DR22 and DR32, while the last byte is written to locations DR02. Afterwards, the DCP counter would point to location DR12. If the master supplies more than 4 bytes of data, then new data overwrites the previous data, one byte at a time.

The master terminates the loading of Data Bytes by issuing a STOP condition, which initiates the nonvolatile write cycle. As with the Byte Write operation, all inputs are disabled until completion of the internal write cycle. If the $\overline{WP}$ pin is low, the nonvolatile write cycle doesn’t start and the bytes are discarded.

Notice that the Data Bytes are also written to the WCR of the corresponding DCPs, therefore in the above example, WCR2, WCR3, and WCR0 are also written and WCR1 is updated with the contents of DR12.

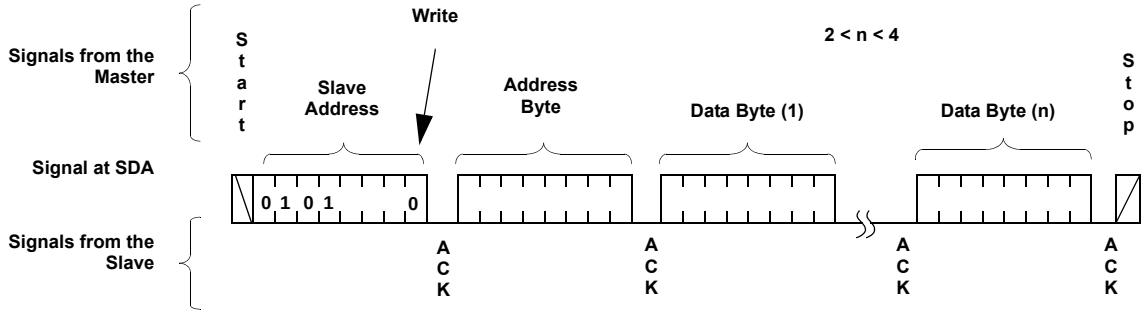


FIGURE 8. PAGE WRITE OPERATION

Move/Read Operation

The Move/Read operation simultaneously reads the contents of a Data Register (DR) and moves the contents into the corresponding DCP's WCR and the WCRs of all DCPs are updated with the content of their corresponding DR. Move/Read operation consists of a one byte, or three byte instruction followed by one or more Data Bytes (See Figure 9). To read an arbitrary byte, the master initiates the operation issuing the following sequence: a START, the Slave Address byte with the R/$\overline{W}$ bit set to "0", an Address Byte, a second START, and a second Slave Address byte with the R/$\overline{W}$ bit set to "1". After each of the three bytes, the X9252 responds with an ACK. Then the X9252 transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eight bit of each byte. The master terminates the Move/Read operation (issuing a STOP condition) following the last bit of the last Data Byte.

The first byte being read is determined by the current DCP address and by the Status Register bits, according to Table 2. If more than one byte is read, the DCP address is incremented by one after each byte, in the same way as during a Page Write operation. After reaching DCP3, the DCP address "rolls over" to DCP0.

On power up, the Address pointer is set to the Data Register 0 of DCP0.

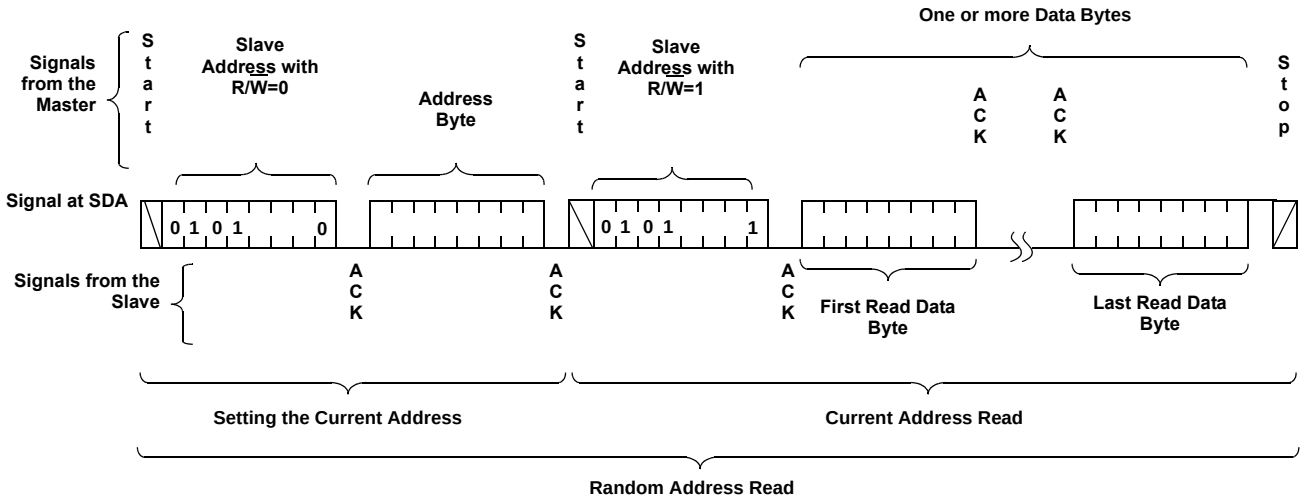
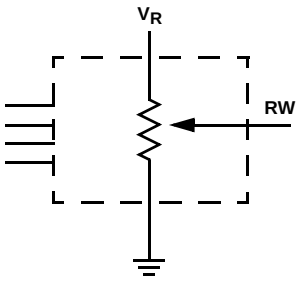


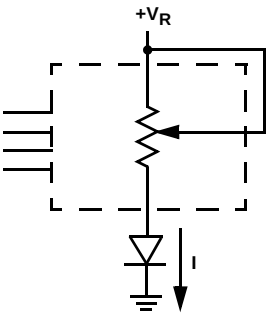
FIGURE 9. MOVE/READ SEQUENCE

Applications Information

Basic Configurations of Electronic Potentiometers



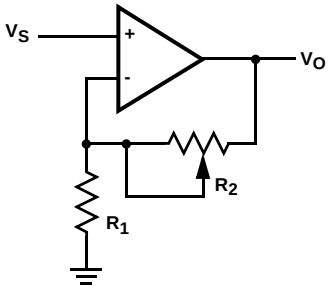
Three terminal
Potentiometer;
Variable voltage divider



Two terminal Variable
Resistor;
Variable current

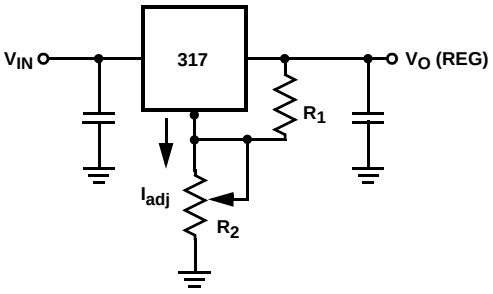
Application Circuits

NONINVERTING AMPLIFIER



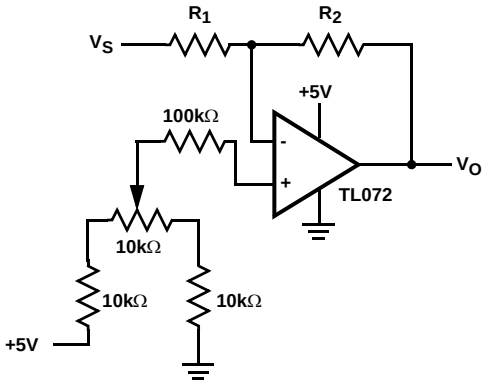
$V_O = (1+R_2/R_1)V_S$

VOLTAGE REGULATOR

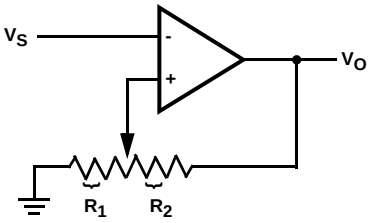


V_O (REG) = 1.25V $(1+R_2/R_1)+I_{adj}$ R_2

OFFSET VOLTAGE ADJUSTMENT



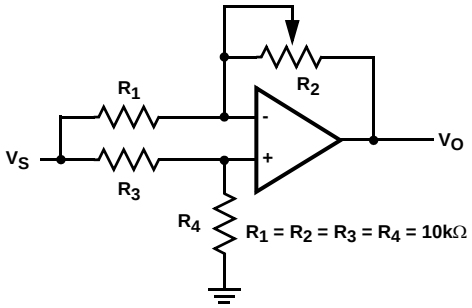
COMPARATOR WITH HYSTERISIS



$V_{UL} = \{R_1/(R_1+R_2)\}\ V_O(max)$
$RL_L = \{R_1/(R_1+R_2)\}\ V_O(min)$

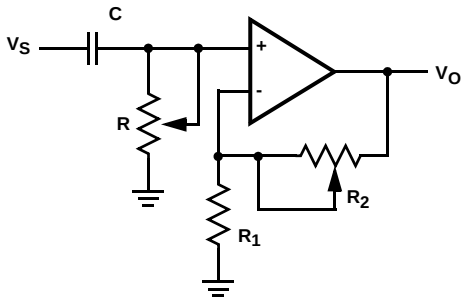
Application Circuits (Continued)

ATTENUATOR



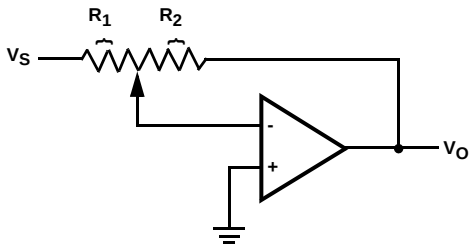
$V_O = G\ V_S$
$-1/2 \leq G \leq +1/2$

FILTER



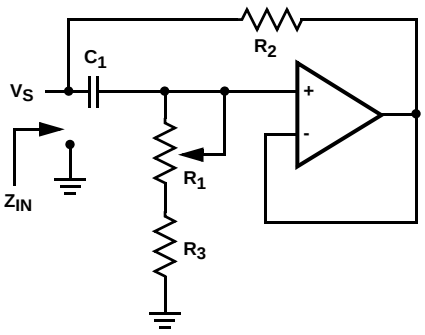
$G_O = 1 + R_2/R_1$
$fc = 1/(2\pi RC)$

INVERTING AMPLIFIER



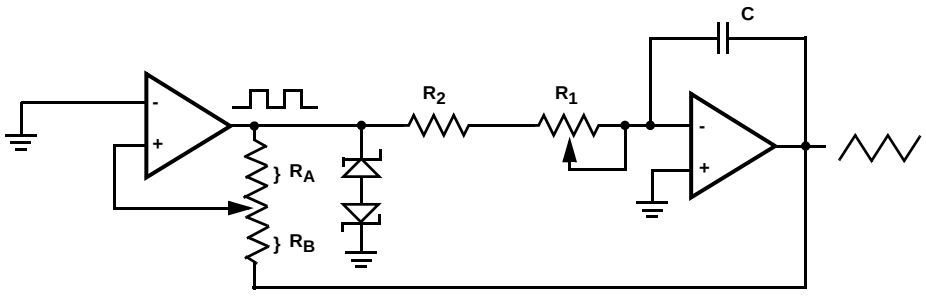
$V_O = G\ V_S$
$G = -R_2/R_1$

EQUIVALENT L-R CIRCUIT



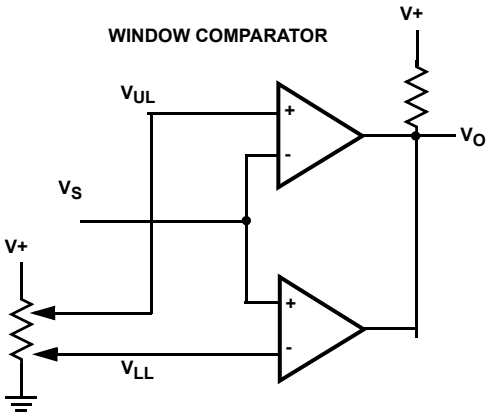
$Z_{IN} = R_2 + s\ R_2\ (R_1 + R_3)\ C_1 = R_2 + s\ Leq$
$(R_1 + R_3) >> R_2$

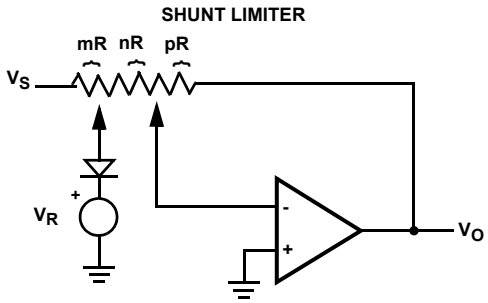
FUNCTION GENERATOR

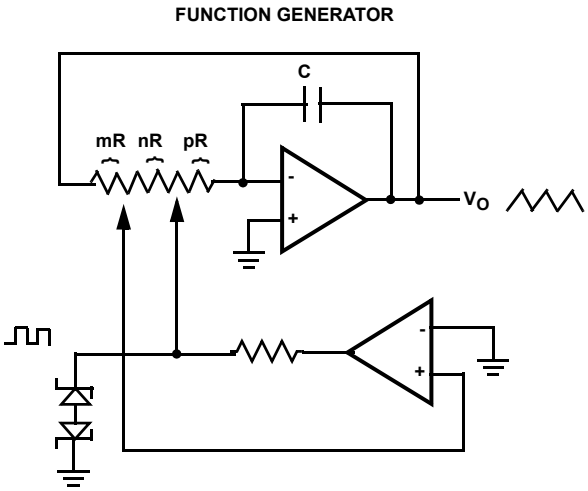


frequency ∝ R_1, R_2, C
amplitude ∝ R_A, R_B

Application Circuits (Continued)

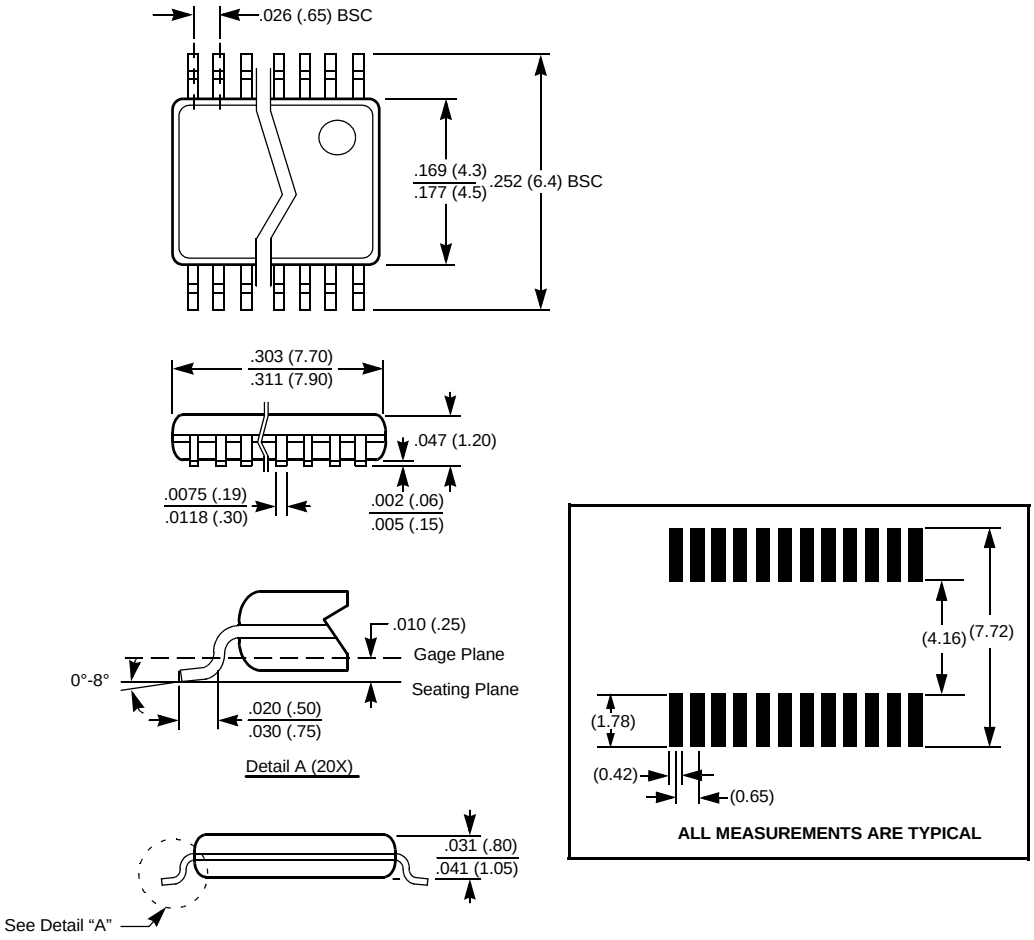






Packaging Information

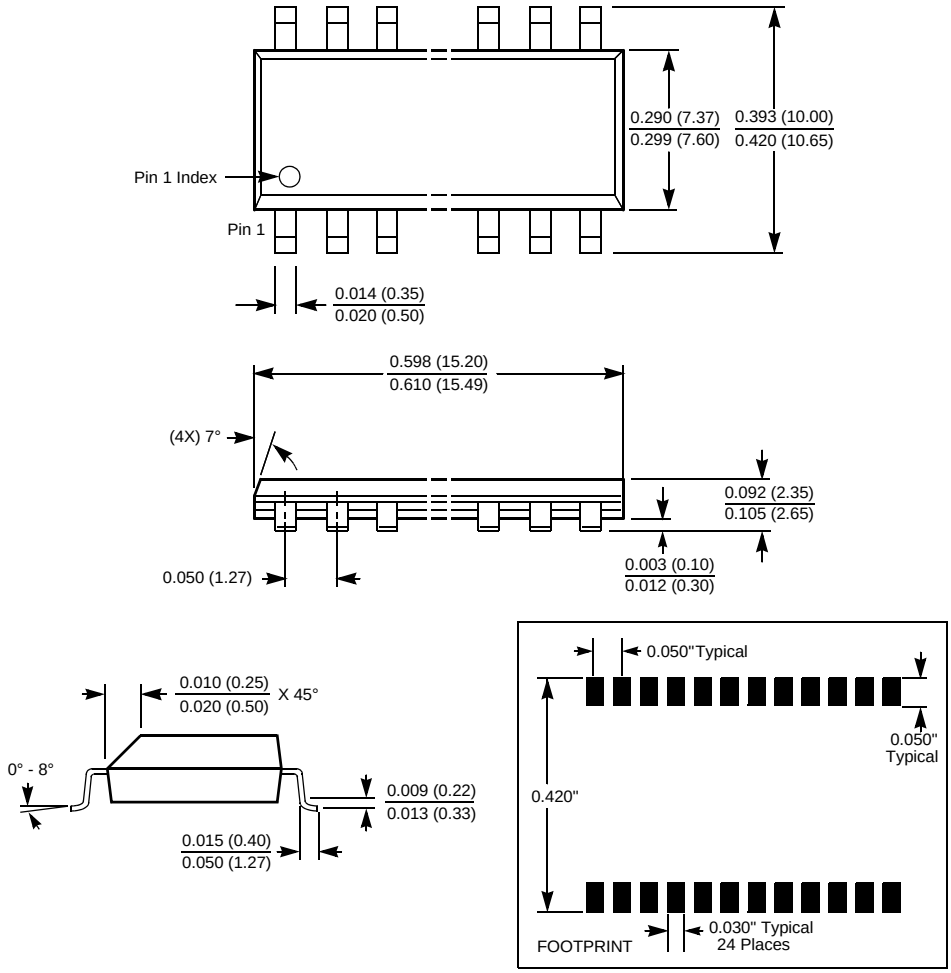
24-Lead Plastic, TSSOP, Package Code V24



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

Packaging Information

24-Lead Plastic, SOIC, Package Code S24



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)