

**Quad Digitally-Controlled (XDCP™) Potentiometers**

The X9259 integrates four digitally controlled potentiometers (XDCP) on a monolithic CMOS integrated circuit.

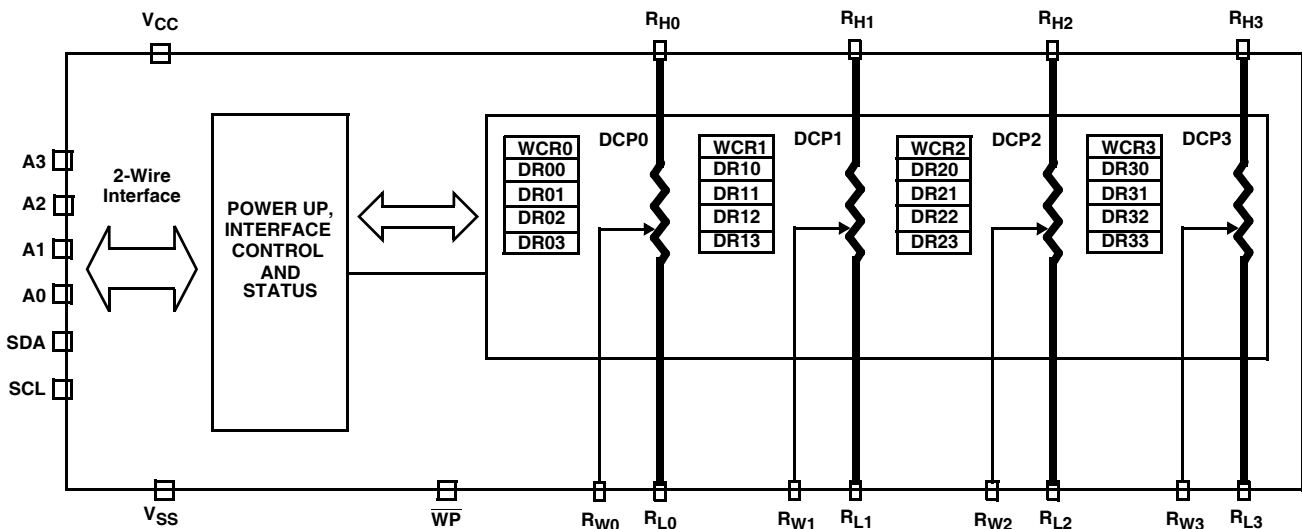
The digitally controlled potentiometers are implemented with a combination of resistor elements and CMOS switches. The position of the wipers are controlled by the user through the 2-wire bus interface. Each potentiometer has associated with it a volatile Wiper Counter Register (WCR) and four non-volatile Data Registers that can be directly written to and read by the user. The content of the WCR controls the position of the wiper. At power-up, the device recalls the content of the default Data Registers of each DCP (DR00, DR10, DR20, and DR30) to the corresponding WCR.

The XDCP can be used as a three-terminal potentiometer or as a two terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

**Features**

- Four Separate Potentiometers in One Package
- 256 Resistor Taps–0.4% Resolution
- 2-Wire Serial Interface for Write, Read, and Transfer Operations of the Potentiometer
- Wiper Resistance: 100Ω typical @ V<sub>CC</sub> = 5V
- 4 Non-volatile Data Registers for Each Potentiometer
- Non-volatile Storage of Multiple Wiper Positions
- Standby Current <5μA Max
- V<sub>CC</sub>: 2.7V to 5.5V Operation
- 50kΩ, 100kΩ versions of Total Resistance
- Endurance: 100,000 Data Changes per Bit per Register
- 100 year Data Retention
- Single Supply Version of X9258
- 24 Ld SOIC, 24 Ld TSSOP
- Low Power CMOS
- Pb-Free Plus Anneal Available (RoHS Compliant)

**Functional Diagram**



## Ordering Information

PART NUMBER	PART MARKING	V <sub>CC</sub> LIMITS (V)	R <sub>TOTAL</sub> (kΩ)	TEMPERATURE RANGE (°C)	PACKAGE	PKG. DWG. #		
X9259TS24	X9259TS	5 ±10%	100	0 to +70	24 Ld SOIC	M24.3		
X9259TS24Z (Note)	X9259TS Z			0 to +70	24 Ld SOIC (Pb-free)	M24.3		
X9259TS24I	X9259TS I			-40 to +85	24 Ld SOIC	M24.3		
X9259TS24IZ (Note)	X9259TS ZI			-40 to +85	24 Ld SOIC (Pb-free)	M24.3		
X9259TV24I	X9259TV I			-40 to +85	24 Ld TSSOP	MDP0044		
X9259TV24IZ (Note)	X9259TV ZI			-40 to +85	24 Ld TSSOP (Pb-free)	MDP0044		
X9259US24*	X9259US			2.7 to 5.5	100	0 to +70	24 Ld SOIC	M24.3
X9259US24Z* (Note)	X9259US Z		0 to +70			24 Ld SOIC (Pb-free)	M24.3	
X9259US24I	X9259US I		-40 to +85			24 Ld SOIC	M24.3	
X9259US24IZ (Note)	X9259US ZI		-40 to +85			24 Ld SOIC (Pb-free)	M24.3	
X9259UV24I*	X9259UV I		-40 to +85			24 Ld TSSOP	MDP0044	
X9259UV24IZ* (Note)	X9259UV Z I		-40 to +85			24 Ld TSSOP (Pb-free)	MDP0044	
X9259TS24-2.7*	X9259TS F		50			100	0 to +70	24 Ld SOIC
X9259TS24Z-2.7* (Note)	X9259TS ZF				0 to +70		24 Ld SOIC (Pb-free)	M24.3
X9259TS24I-2.7	X9259TS G	-40 to +85			24 Ld SOIC		M24.3	
X9259TS24IZ-2.7 (Note)	X9259TS ZG	-40 to +85			24 Ld SOIC (Pb-free)		M24.3	
X9259TV24-2.7	X9259TV F	0 to +70			24 Ld TSSOP		MDP0044	
X9259TV24Z-2.7 (Note)	X9259TV ZF	0 to +70			24 Ld TSSOP (Pb-free)		MDP0044	
X9259US24-2.7	X9259US F	50			50		0 to +70	24 Ld SOIC
X9259US24Z-2.7 (Note)	X9259US ZF					0 to +70	24 Ld SOIC (Pb-free)	M24.3
X9259US24I-2.7	X9259US G			-40 to +85		24 Ld SOIC	M24.3	
X9259US24IZ-2.7 (Note)	X9259US ZG			-40 to +85		24 Ld SOIC (Pb-free)	M24.3	
X9259UV24-2.7*	X9259UV F			0 to +70		24 Ld TSSOP	MDP0044	
X9259UV24Z-2.7 (Note)	X9259UV ZF			0 to +70		24 Ld TSSOP (Pb-free)	MDP0044	
X9259UV24I-2.7*	X9259UV G			-40 to +85		24 Ld TSSOP	MDP0044	
X9259UV24IZ-2.7* (Note)	X9259UV ZG	-40 to +85		24 Ld TSSOP (Pb-free)	MDP0044			

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

\*Add "T1" suffix for tape and reel.

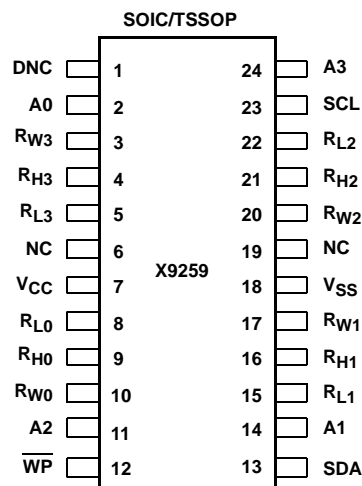
### Circuit Level Applications

- Vary the gain of a voltage amplifier
- Provide programmable dc reference voltages for comparators and detectors
- Control the volume in audio circuits
- Trim out the offset voltage error in a voltage amplifier circuit
- Set the output voltage of a voltage regulator
- Trim the resistance in Wheatstone bridge circuits
- Control the gain, characteristic frequency and Q-factor in filter circuits
- Set the scale factor and zero point in sensor signal conditioning circuits
- Vary the frequency and duty cycle of timer ICs
- Vary the dc biasing of a pin diode attenuator in RF circuits
- Provide a control variable (I, V, or R) in feedback circuits

### System Level Applications

- Adjust the contrast in LCD displays
- Control the power level of LED transmitters in communication systems
- Set and regulate the DC biasing point in an RF power amplifier in wireless systems
- Control the gain in audio and home entertainment systems
- Provide the variable DC bias for tuners in RF wireless systems
- Set the operating points in temperature control systems
- Control the operating point for sensors in industrial systems
- Trim offset and gain errors in artificial intelligent systems

### Pin Configuration



### Pin Assignments

PIN (SOIC/TSSOP)	SYMBOL	FUNCTION
2	A0	Device Address for 2-Wire bus. (See Note 1)
3	R <sub>W3</sub>	Wiper Terminal of DCP3
4	R <sub>H3</sub>	High Terminal of DCP3
5	R <sub>L3</sub>	Low Terminal of DCP3
6	NC1	Must be left unconnected
7	V <sub>CC</sub>	System Supply Voltage
8	R <sub>L0</sub>	Low Terminal of DCP0
9	R <sub>H0</sub>	High Terminal of DCP0
10	R <sub>W0</sub>	Wiper Terminal of DCP0
11	A2	Device Address for 2-Wire bus. (See Note 1)
12	$\overline{WP}$	Hardware Write Protect – Active Low
13	SDA	Serial Data Input/Output for 2-Wire bus.
14	A1	Device Address for 2-Wire bus. (See Note 1)
15	R <sub>L1</sub>	Low Terminal of DCP1
16	R <sub>H1</sub>	High Terminal of DCP1
17	R <sub>W1</sub>	Wiper Terminal of DCP1
18	V <sub>SS</sub>	System Ground
20	R <sub>W2</sub>	Wiper Terminal of DCP2
21	R <sub>H2</sub>	High Terminal of DCP2
22	R <sub>L2</sub>	Low Terminal of DCP2
23	SCL	Serial Clock for 2-Wire bus.
24	A3	Device Address for 2-Wire bus. (See Note 1)
6, 19	NC	No Connect
1	DNC	Do Not Connect

**Note 1:** A0 through A3 Device address pins must be tied to a logic level.

## Pin Descriptions

### Bus Interface Pins

#### SERIAL DATA INPUT/OUTPUT (SDA)

The SDA is a bidirectional serial data input/output pin for a 2-Wire slave device and is used to transfer data into and out of the device. It receives device address, opcode, wiper register address and data sent from a 2-Wire master at the rising edge of the serial clock SCL, and it shifts out data after each falling edge of the serial clock SCL.

It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs. An open drain output requires the use of a pull-up resistor.

#### SERIAL CLOCK (SCL)

This input is used by 2-Wire master to supply 2-Wire serial clock to the X9259.

#### DEVICE ADDRESS (A3 THROUGH A0)

The Address inputs are used to set the least significant 4 bits of the 8-bit slave address. A match in the slave address serial data stream must be made with the Address input in order to initiate communication with the X9259. A maximum of 16 devices may occupy the 2-Wire serial bus. Device pins A3 through A0 must be tied to a logic level which specifies the external address of the device, see Figures 3, 4, and 5.

### Potentiometer Pins

#### R<sub>H</sub>, R<sub>L</sub>

The R<sub>H</sub> and R<sub>L</sub> pins are equivalent to the terminal connections on a mechanical potentiometer. Since there are 4 potentiometers, there are 4 sets of R<sub>H</sub> and R<sub>L</sub> such that R<sub>H0</sub> and R<sub>L0</sub> are the terminals of DCP0 and so on.

#### R<sub>W</sub>

The wiper pin are equivalent to the wiper terminal of a mechanical potentiometer. Since there are 4 potentiometers, there are 4 sets of R<sub>W</sub> such that R<sub>W0</sub> is the terminal of DCP0 and so on.

### Bias Supply Pins

#### SYSTEM SUPPLY VOLTAGE (V<sub>CC</sub>) AND SUPPLY GROUND (V<sub>SS</sub>)

The V<sub>CC</sub> pin is the system supply voltage. The V<sub>SS</sub> pin is the system ground.

### Other Pins

#### NO CONNECT

No connect pins should be left open. This pins are used for Intersil manufacturing and testing purposes.

#### HARDWARE WRITE PROTECT INPUT ( $\overline{WP}$ )

The  $\overline{WP}$  pin when LOW prevents non-volatile writes to the Data Registers.

### One of Four Potentiometers

#: 0, 1, 2, or 3

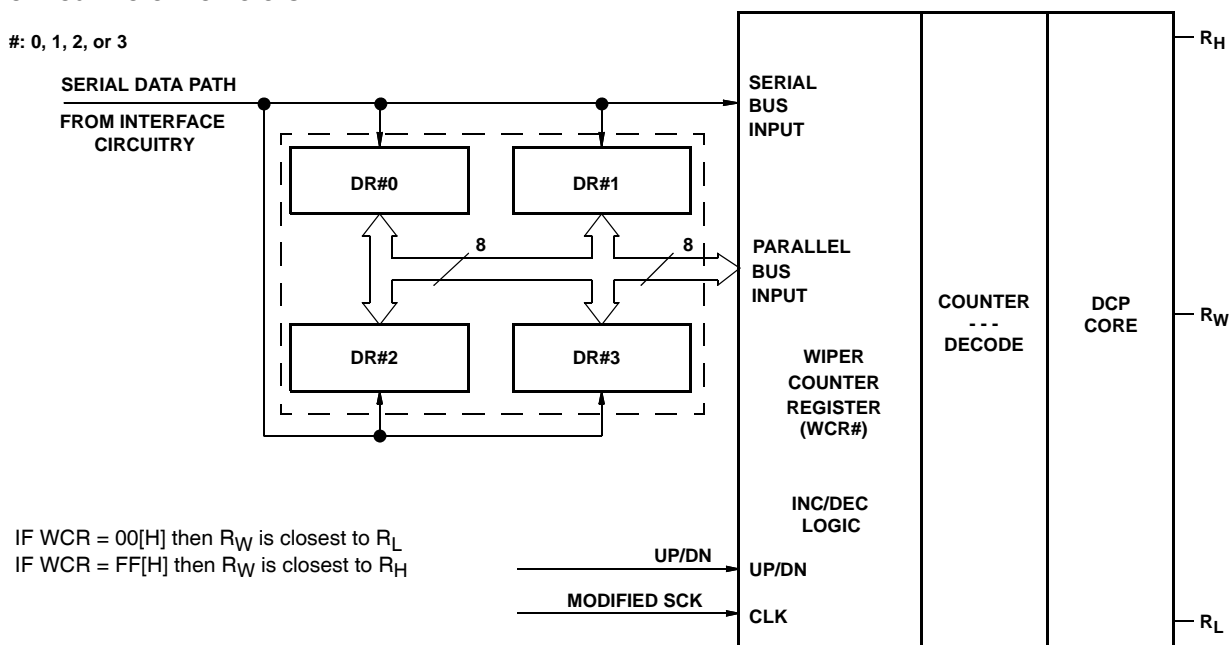


FIGURE 1. DETAILED POTENTIOMETER BLOCK DIAGRAM

**Principles of Operation**

The X9259 is an integrated circuit incorporating four DCPs and their associated registers and counters, and the serial interface providing direct communication between a host and the potentiometers.

**DCP Description**

Each DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of each DCP are equivalent to the fixed terminals of a mechanical potentiometer ( $R_H$  and  $R_L$  pins). The RW pin is an intermediate node, equivalent to the wiper terminal of a mechanical potentiometer.

The position of the wiper terminal within the DCP is controlled by an 8-bit volatile Wiper Counter Register (WCR).

**Power Up and Down Recommendations**

There are no restrictions on the power-up or power-down conditions of  $V_{CC}$  and the voltages applied to the potentiometer pins provided that  $V_{CC}$  is always more positive than or equal to  $V_H$ ,  $V_L$ , and  $V_W$ , i.e.,  $V_{CC} \geq V_H, V_L, V_W$ . The  $V_{CC}$  ramp rate specification is always in effect.

**Wiper Counter Register (WCR)**

The X9259 contains four Wiper Counter Registers, one for each potentiometer. The Wiper Counter Register can be envisioned as a 8-bit parallel and serial load counter with its outputs decoded to select one of 256 wiper positions along its resistor array. The contents of the WCR can be altered in four ways: it may be written directly by the host via the Write Wiper Counter Register instruction (serial load); it may be

written indirectly by transferring the contents of one of four associated data registers via the XFR Data Register instruction (parallel load); it can be modified one step at a time by the Increment/Decrement instruction (see Instruction section for more details). Finally, it is loaded with the contents of its data register zero (DR#0) upon power-up. (See Figure 1)

The Wiper Counter Register is a volatile register; that is, its contents are lost when the X9259 is powered-down. Although the register is automatically loaded with the value in DR#0 upon power-up, this may be different from the value present at power-down. Power-up guidelines are recommended to ensure proper loadings of the DR#0 value into the WCR# (See Design Considerations Section).

**Data Registers (DR)**

Each of the four DCPs has four 8-bit non-volatile Data Registers. These can be read or written directly by the host. Data can also be transferred between any of the four data registers and the associated Wiper Counter Register. All operations changing data in one of the data registers is a non-volatile operation and takes a maximum of 10ms.

If the application does not require storage of multiple settings for the potentiometer, the Data Registers can be used as regular memory locations for system parameters or user preference data.

Bit [7:0] are used to store one of the 256 wiper positions (0 ~ 255).

**TABLE 1. WIPER COUNTER REGISTER, WCR (8-bit), WCR[7:0]:** Used to store the current wiper position (Volatile).

WCR7	WCR6	WCR5	WCR4	WCR3	WCR2	WCR1	WCR0
(MSB)							(LSB)

**TABLE 2. DATA REGISTER, DR (8-BIT), BIT [7:0]:** Used to store wiper positions or data (Non-volatile).

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
(MSB)							(LSB)

## **Serial Interface**

The X9259 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master always initiates data transfers and provide the clock for both transmit and receive operations. Therefore, the X9259 operates as a slave device in all applications.

All 2-wire interface operations must begin with a START, followed by an Identification Byte, that selects the X9259. All communication over the 2-wire interface is conducted by sending the MSB of each byte of data first.

### **Clock and Data Conventions**

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions. See Figure 2. On power up of the X9259 the SDA pin is in the input mode.

### **START Condition**

All commands to the X9259 are preceded by the start condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The X9259 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met. See Figure 2.

### **STOP Condition**

All communications must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH. See Figure 2. The STOP condition is also used to place the device into the Standby Power mode after a Read sequence. A STOP condition can only be issued after the transmitting device has released the bus.

## **Acknowledge**

An ACK, Acknowledge, is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data. See Figure 3.

The X9259 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Instruction Byte. The X9259 also responds with an ACK after receiving a Data Byte after a Write Instruction.

A valid Identification Byte contains the Device Type Identifier 0101, as the four MSBs, and the Device Address bits matching the logic states of pins A3, A2, A1, and A0, as the four LSBs. See Figure 4.

In the Read mode, the device transmits eight bits of data, releases the SDA line, and then monitors the line for an ACK. The device continues transmitting data if an ACK is detected. The device terminates further data transmissions if an ACK is not detected. The master must then issue a STOP condition to place the device into a known state.

During the internal non-volatile Write operation, the X9259 ignores the inputs at SDA and SCL, and does not issue an ACK after Identification bytes.

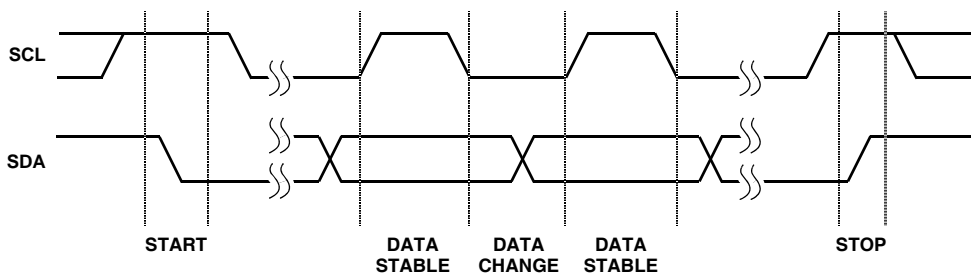


FIGURE 2. VALID DATA CHANGES, START, AND STOP CONDITIONS

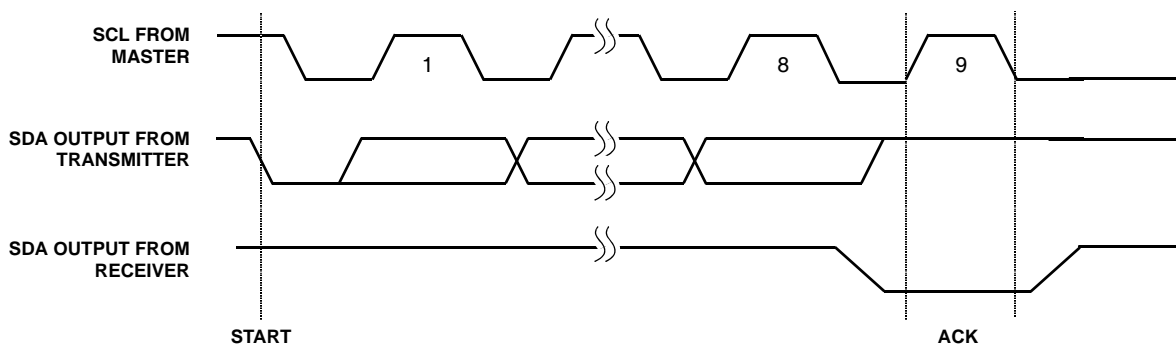


FIGURE 3. ACKNOWLEDGE RESPONSE FROM RECEIVER

**Identification Byte**

The first byte sent to the X9259 from the host is called the Identification Byte. The most significant four bits are a Device Type Identifier, ID[3:0] bits, which must be 0101. Refer to Table 3.

Only the device which Slave Address matches the incoming device address sent by the master executes the instruction. The A3 - A0 inputs can be actively driven by CMOS input signals or tied to V<sub>CC</sub> or V<sub>SS</sub>.

**INSTRUCTION BYTE (I)**

The next byte sent to the X9259 contains the instruction and register pointer information. The four most significant bits are used provide the instruction opcode I [3:0]. The RB and RA bits point to one of the four data registers of each associated XDCCP. The least two significant bits point to one of four Wiper Counter Registers or DCPs. The format is shown in Table 4.

**Data Register Selection**

REGISTER	RB	RA
DR#0	0	0
DR#1	0	1
DR#2	1	0
DR#3	1	1

#: 0, 1, 2, or 3

The least significant four bits of the Identification Byte are the Slave Address bits, AD[3:0]. To access the X9259, these four bits must match the logic values of pins A3, A2, A1, and A0.

TABLE 3. IDENTIFICATION BYTE FORMAT

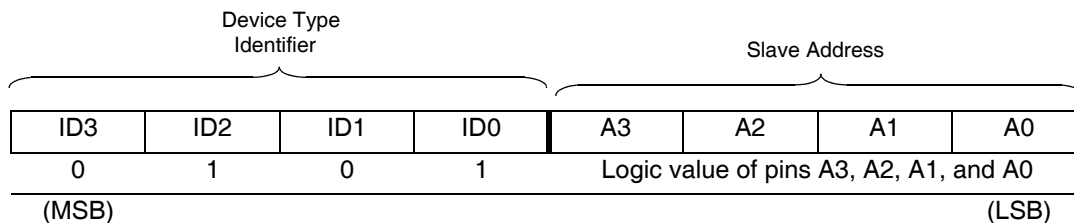


TABLE 4. INSTRUCTION BYTE FORMAT

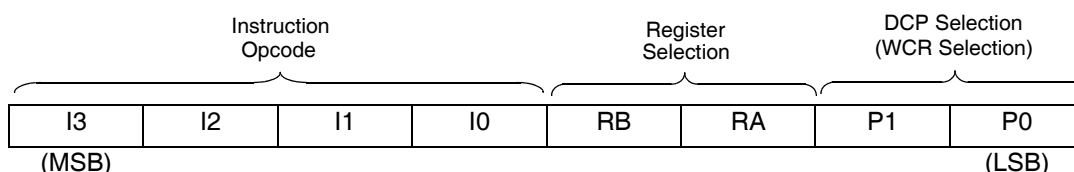


TABLE 5. INSTRUCTION SET

INSTRUCTION	INSTRUCTION SET								OPERATION
	I3	I2	I1	I0	RB	RA	P1	P0	
Read Wiper Counter Register	1	0	0	1	0	0	1/0	1/0	Read the contents of the Wiper Counter Register pointed to by P1 - P0
Write Wiper Counter Register	1	0	1	0	0	0	1/0	1/0	Write new value to the Wiper Counter Register pointed to by P1 - P0
Read Data Register	1	0	1	1	1/0	1/0	1/0	1/0	Read the contents of the Data Register pointed to by P1 - P0 and RB - RA
Write Data Register	1	1	0	0	1/0	1/0	1/0	1/0	Write new value to the Data Register pointed to by P1 - P0 and RB - RA
XFR Data Register to Wiper Counter Register	1	1	0	1	1/0	1/0	1/0	1/0	Transfer the contents of the Data Register pointed to by P1 - P0 and RB - RA to its associated Wiper Counter Register
XFR Wiper Counter Register to Data Register	1	1	1	0	1/0	1/0	1/0	1/0	Transfer the contents of the Wiper Counter Register pointed to by P1 - P0 to the Data Register pointed to by RB - RA
Global XFR Data Registers to Wiper Counter Registers	0	0	0	1	1/0	1/0	0	0	Transfer the contents of the Data Registers pointed to by RB - RA of all four pots to their respective Wiper Counter Registers
Global XFR Wiper Counter Registers to Data Register	1	0	0	0	1/0	1/0	0	0	Transfer the contents of both Wiper Counter Registers to their respective data Registers pointed to by RB - RA of all four DCPs
Increment/Decrement Wiper Counter Register	0	0	1	0	0	0	1/0	1/0	Enable Increment/decrement of the Control Latch pointed to by P1 - P0

Note: 1/0 = data is one or zero



**Instructions**

Four of the nine instructions are three bytes in length. These instructions are:

- **Read Wiper Counter Register** – read the current wiper position of the selected potentiometer,
- **Write Wiper Counter Register** – change current wiper position of the selected potentiometer,
- **Read Data Register** – read the contents of the selected Data Register;
- **Write Data Register** – write a new value to the selected Data Register.

The basic sequence of the three byte instructions is illustrated in Figure 5. These three-byte instructions exchange data between the WCR and one of the Data Registers. A transfer from a Data Register to a WCR is essentially a write to a static RAM, with the static RAM controlling the wiper position. The response of the wiper to this action is delayed by  $t_{WRL}$ . A transfer from the WCR (current wiper position), to a Data Register is a write to non-volatile memory and takes a minimum of  $t_{WR}$  to complete. The transfer can occur between one of the four potentiometer's WCR, and one of its associated registers, DRs; or it may occur globally, where the transfer occurs between all potentiometers and one associated register.

Four instructions require a two-byte sequence to complete. These instructions transfer data between the host and the X9259; either between the host and one of the data registers

or directly between the host and the Wiper Counter Register. These instructions are:

- **XFR Data Register to Wiper Counter Register** – This transfers the contents of one specified Data Register to the associated Wiper Counter Register.
- **XFR Wiper Counter Register to Data Register** – This transfers the contents of the specified Wiper Counter Register to the specified associated Data Register.
- **Global XFR Data Register to Wiper Counter Register** – This transfers the contents of all specified Data Registers to the associated Wiper Counter Registers.
- **Global XFR Wiper Counter Register to Data Register** – This transfers the contents of all Wiper Counter Registers to the specified associated Data Registers.

**Increment/Decrement Command**

The final command is Increment/Decrement (Figure 6 and 7). The Increment/Decrement command is different from the other commands. Once the command is issued and the X9259 has responded with an Acknowledge, the master can clock the selected wiper up and/or down in one segment steps; thereby, providing a fine tuning capability to the host. For each SCL clock pulse ( $t_{HIGH}$ ) while SDA is HIGH, the selected wiper moves one wiper position towards the  $R_H$  terminal. Similarly, for each SCL clock pulse while SDA is LOW, the selected wiper moves one resistor wiper position towards the  $R_L$  terminal.

See Instruction format for more details.

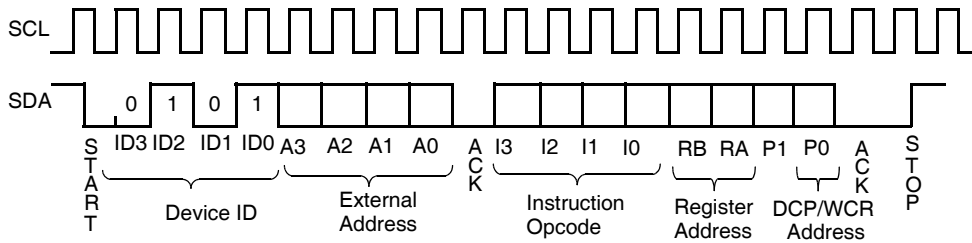


FIGURE 4. TWO-BYTE INSTRUCTION SEQUENCE

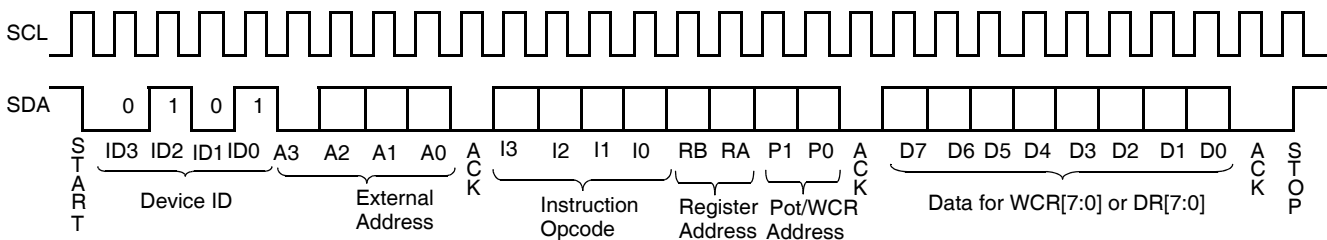


FIGURE 5. THREE-BYTE INSTRUCTION SEQUENCE 2-WIRE INTERFACE

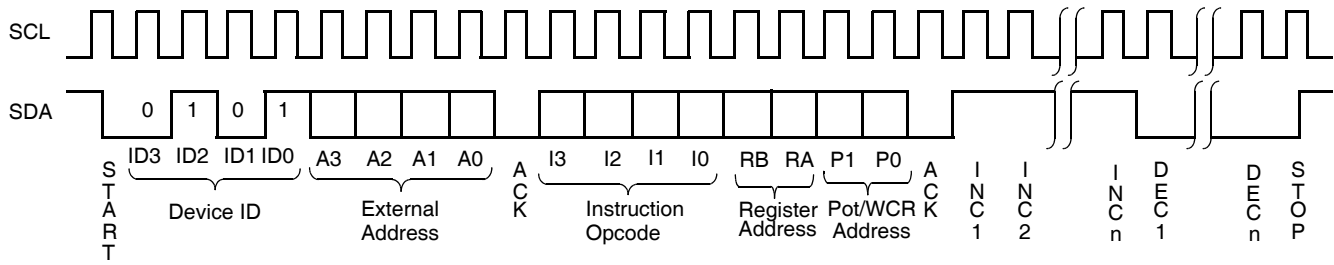


FIGURE 6. INCREMENT/DECREMENT INSTRUCTION SEQUENCE 2-WIRE INTERFACE

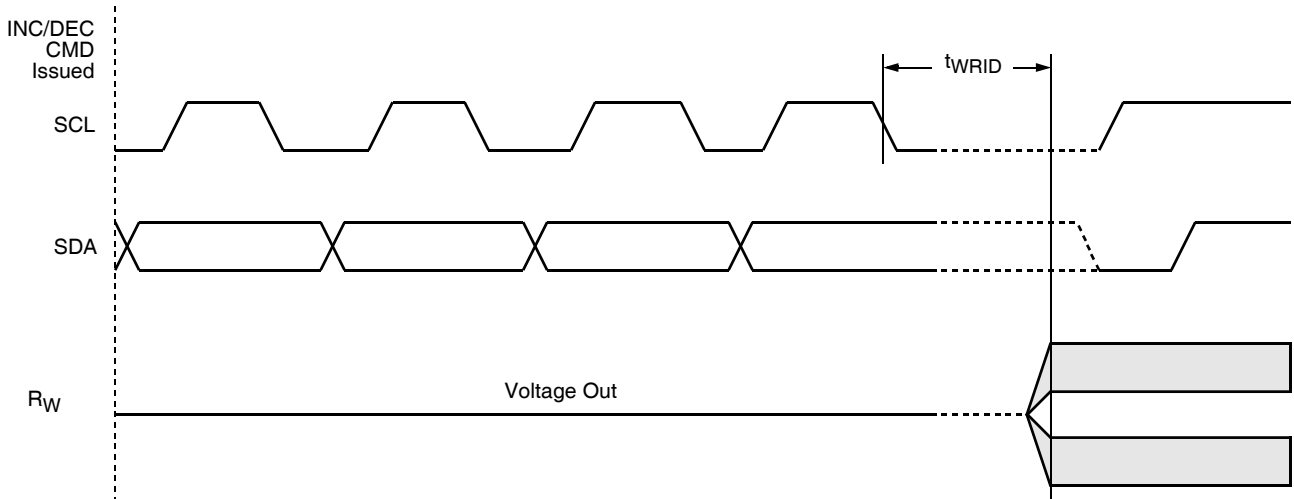


FIGURE 7. INCREMENT/DECREMENT TIMING SPEC

**Instruction Format**

**Read Wiper Counter Register (WCR)**

S T A R T	Device Type Identifier				Device Addresses				S A C K	Instruction Opcode				DR/WCR Addresses				S A C K	Wiper Position (Sent by X9259 on SDA)								M A C K	S T O P
	0	1	0	1	A3	A2	A1	A0		1	0	0	1	0	0	P1	P0		W C R 7	W C R 6	W C R 5	W C R 4	W C R 3	W C R 2	W C R 1	W C R 0		
	0	1	0	1	A3	A2	A1	A0		1	0	0	1	0	0	P1	P0		W C R 7	W C R 6	W C R 5	W C R 4	W C R 3	W C R 2	W C R 1	W C R 0		

**Write Wiper Counter Register (WCR)**

S T A R T	Device Type Identifier				Device Addresses				S A C K	Instruction Opcode				DR/WCR Addresses				S A C K	Wiper Position (Sent by Master on SDA)								S A C K	S T O P
	0	1	0	1	A3	A2	A1	A0		1	0	1	0	0	0	P1	P0		W C R 7	W C R 6	W C R 5	W C R 4	W C R 3	W C R 2	W C R 1	W C R 0		
	0	1	0	1	A3	A2	A1	A0		1	0	1	0	0	0	P1	P0		W C R 7	W C R 6	W C R 5	W C R 4	W C R 3	W C R 2	W C R 1	W C R 0		

**Read Data Register (DR)**

S T A R T	Device Type Identifier				Device Addresses				S A C K	Instruction Opcode				DR/WCR Addresses				S A C K	Wiper Position (Sent by X9259 on SDA)								M A C K	S T O P
	0	1	0	1	A3	A2	A1	A0		1	0	1	1	RB	RA	P1	P0		W C R 7	W C R 6	W C R 5	W C R 4	W C R 3	W C R 2	W C R 1	W C R 0		
	0	1	0	1	A3	A2	A1	A0		1	0	1	1	RB	RA	P1	P0		W C R 7	W C R 6	W C R 5	W C R 4	W C R 3	W C R 2	W C R 1	W C R 0		

**Write Data Register (DR)**

S T A R T	Device Type Identifier				Device Addresses				S A C K	Instruction Opcode				DR/WCR Addresses				S A C K	Wiper Position (Sent by Master on SDA)								S A C K	S T O P	H I G H- V O L T A G E  W R I T E C Y C L E
	0	1	0	1	A3	A2	A1	A0		1	1	0	0	RB	RA	P1	P0		W C R 7	W C R 6	W C R 5	W C R 4	W C R 3	W C R 2	W C R 1	W C R 0			
	0	1	0	1	A3	A2	A1	A0		1	1	0	0	RB	RA	P1	P0		W C R 7	W C R 6	W C R 5	W C R 4	W C R 3	W C R 2	W C R 1	W C R 0			

**Global XFR Data Register (DR) to Wiper Counter Register (WCR)**

S T A R T	Device Type Identifier				Device Addresses				S A C K	Instruction Opcode				DR/WCR Addresses				S A C K	S T O P
	0	1	0	1	A3	A2	A1	A0		0	0	0	1	RB	RA	0	0		
	0	1	0	1	A3	A2	A1	A0		0	0	0	1	RB	RA	0	0		

- Notes: (1) "MACK"/"SACK": stands for the acknowledge sent by the Master/Slave.  
 (2) "A3 ~ A0": stands for the device addresses sent by the master.  
 (3) "X": indicates that it is a "0" for testing purpose but physically it is a "don't care" condition.  
 (4) "I": stands for the increment operation, SDA held high during active SCL phase (high).  
 (5) "D": stands for the decrement operation, SDA held low during active SCL phase (high).

**Global XFR Wiper Counter Register (WCR) to Data Register (DR)**

S T A R T	Device Type Identifier				Device Addresses				S A C K	Instruction Opcode				DR/WCR Addresses				S A C K	S T O P	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	A3	A2	A1	A0		1	0	0	0	RB	RA	0	0			

**Transfer Wiper Counter Register (WCR) to Data Register (DR)**

S T A R T	Device Type Identifier				Device Addresses				S A C K	Instruction Opcode				DR/WCR Addresses				S A C K	S T O P	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	A3	A2	A1	A0		1	1	1	0	RB	RA	P1	P0			

**Transfer Data Register (DR) to Wiper Counter Register (WCR)**

S T A R T	Device Type Identifier				Device Addresses				S A C K	Instruction Opcode				DR/WCR Addresses				S A C K	S T O P
	0	1	0	1	A3	A2	A1	A0		1	1	0	1	RB	RA	P1	P0		

**Increment/Decrement Wiper Counter Register (WCR)**

S T A R T	Device Type Identifier				Device Addresses				S A C K	Instruction Opcode				DR/WCR Addresses				Increment/Decrement (Sent by Master on SDA)						S T O P
	0	1	0	1	A3	A2	A1	A0		0	0	1	0	0	0	P1	P0	I/D	I/D	.	.	.	.	

- Notes: (1) "MACK"/"SACK": stands for the acknowledge sent by the Master/Slave.  
 (2) "A3 ~ A0": stands for the device addresses sent by the master.  
 (3) "X": indicates that it is a "0" for testing purpose but physically it is a "don't care" condition.  
 (4) "I": stands for the increment operation, SDA held high during active SCL phase (high).  
 (5) "D": stands for the decrement operation, SDA held low during active SCL phase (high).

**Absolute Maximum Ratings**

Temperature under bias . . . . . -65°C to +135°C  
 Storage temperature . . . . . -65°C to +150°C  
 Voltage on SCL, SDA, any address input, V<sub>CC</sub>  
 with respect to V<sub>SS</sub> . . . . . -1V to +7V  
 $\Delta V = | (V_H - V_L) |$  . . . . . 5.5V  
 Lead temperature (soldering, 10 seconds) . . . . . 300°C  
 I<sub>W</sub> (10 seconds) . . . . . ±6mA

**Recommended Operating Conditions**

Temperature (Commercial) . . . . . 0°C to +70°C  
 Temperature (Industrial) . . . . . -40°C to +85°C  
 Supply Voltage (V<sub>CC</sub>) (Note 4) Limits  
 X9259 . . . . . 5V ± 10%  
 X9259-2.7 . . . . . 2.7V to 5.5V  
 Wiper current . . . . . ±3mA  
 Power rating (each pot) . . . . . 50mW

*CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; the functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

**Analog Specifications** Over recommended industrial (2.7V) operating conditions unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			
			MIN	TYP	MAX	UNITS
R <sub>TOTAL</sub>	End to End Resistance	T version		100		kΩ
R <sub>TOTAL</sub>	End to End Resistance	U version		50		kΩ
	End to End Resistance Tolerance				±20	%
R <sub>W</sub>	Wiper Resistance	$I_W = \frac{V(V_{CC})}{R_{TOTAL}} @ V_{CC} = 3V$			300	Ω
		$I_W = \frac{V(V_{CC})}{R_{TOTAL}} @ V_{CC} = 5V$			220	Ω
V <sub>TERM</sub>	Voltage on any R <sub>H</sub> or R <sub>L</sub> Pin	V <sub>SS</sub> = 0V	V <sub>SS</sub>		V <sub>CC</sub>	V
	Noise (Note 6)	Ref: 1V		-120		dB/√Hz
	Resolution			0.4		%
	Absolute Linearity (Note 1)	R <sub>w(n)(actual)</sub> - R <sub>w(n)(expected)</sub> (Note 5)	-1		+1	MI (Note 3)
	Relative Linearity (Note 2)	R <sub>w(n+1)</sub> - [R <sub>w(n)</sub> + MI] (Note 5)	-0.6		+0.6	MI (Note 3)
	Temperature Coefficient of R <sub>TOTAL</sub> (Note 6)			±300		ppm/°C
	Ratiometric Temp. Coefficient (Note 6)			±20		ppm/°C
C <sub>H</sub> /C <sub>L</sub> /C <sub>W</sub>	Potentiometer Capacitances (Note 6)	See Macro model		10/10/25		pF

**NOTES:**

1. Absolute linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.
2. Relative linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.
3. MI = RTOT / 255 or (R<sub>H</sub> - R<sub>L</sub>) / 255, single pot
4. During power up V<sub>CC</sub> > V<sub>H</sub>, V<sub>L</sub>, and V<sub>W</sub>.
5. n = 0, 1, 2, ..., 255; m = 0, 1, 2, ..., 254.

**DC Electrical Specifications** Over the recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			
			MIN	TYP	MAX	UNITS
I <sub>CC1</sub>	V <sub>CC</sub> supply current (active)	f <sub>SCL</sub> = 400kHz; V <sub>CC</sub> = +6V; SDA = Open; (for 2-Wire, Active, Read and Volatile Write States only)			3	mA
I <sub>CC2</sub>	V <sub>CC</sub> supply current (non-volatile write)	f <sub>SCL</sub> = 400kHz; V <sub>CC</sub> = +6V; SDA = Open; (for 2-Wire, Active, Non-volatile Write State only)			5	mA
I <sub>SB</sub>	V <sub>CC</sub> current (standby)	V <sub>CC</sub> = +6V; V <sub>IN</sub> = V <sub>SS</sub> or V <sub>CC</sub> ; SDA = V <sub>CC</sub> ; (for 2-Wire, Standby State only)			5	μA
I <sub>LI</sub>	Input leakage current	V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>			10	μA
I <sub>LO</sub>	Output leakage current	V <sub>OUT</sub> = V <sub>SS</sub> to V <sub>CC</sub>			10	μA
V <sub>IH</sub>	Input HIGH voltage		V <sub>CC</sub> × 0.7			V
V <sub>IL</sub>	Input LOW voltage				V <sub>CC</sub> × 0.3	V
V <sub>OL</sub>	Output LOW voltage	I <sub>OL</sub> = 3mA			0.4	V
V <sub>OH</sub>	Output HIGH voltage	I <sub>OH</sub> = -1mA, V <sub>CC</sub> ≥ +3V	V <sub>CC</sub> - 0.8			V
V <sub>OH</sub>	Output HIGH voltage	I <sub>OH</sub> = -0.4mA, V <sub>CC</sub> ≤ +3V	V <sub>CC</sub> - 0.4			V

**Endurance and Data Retention**

PARAMETER	MIN	UNITS
Minimum endurance	100,000	Data changes per bit per register
Data retention	100	years

**Capacitance**

SYMBOL	TEST	MAX	UNITS	TEST CONDITIONS
C <sub>IN/OUT</sub> (Note 6)	Input / Output capacitance (SDA)	8	pF	V <sub>OUT</sub> = 0V
C <sub>IN</sub> (Note 6)	Input capacitance (SCL, $\overline{WP}$ , A2, A1 and A0)	6	pF	V <sub>IN</sub> = 0V

**Power-up Timing**

SYMBOL	PARAMETER	MIN	MAX	UNITS
t <sub>r VCC</sub> (Note 6)	V <sub>CC</sub> Power-up rate	0.2		V/ms
t <sub>PUR</sub> (Note 7)	Power-up to initiation of read operation		1	ms
t <sub>PUW</sub> (Note 7)	Power-up to initiation of write operation		50	ms

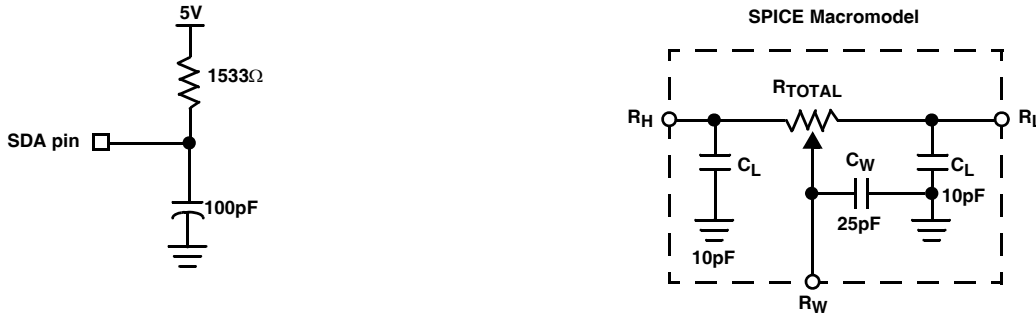
**A.C. Test Conditions**

Input Pulse Levels	V <sub>CC</sub> × 0.1 to V <sub>CC</sub> × 0.9
Input rise and fall times	10ns
Input and output timing level	V <sub>CC</sub> × 0.5

NOTES:

- This parameter is not 100% tested
- t<sub>PUR</sub> and t<sub>PUW</sub> are the delays required from the time the power supply (V<sub>CC</sub>) is stable until the specific instruction can be issued. These parameters are periodically sampled and not 100% tested.

**Equivalent A.C. Load Circuit**



**AC Timing**

SYMBOL	PARAMETER	MIN	MAX	UNITS
f <sub>SCL</sub>	Clock Frequency		400	kHz
t <sub>CYC</sub>	Clock Cycle Time	2500		ns
t <sub>HIGH</sub>	Clock High Time	600		ns
t <sub>LOW</sub>	Clock Low Time	1300		ns
t <sub>SU:STA</sub>	Start Setup Time	600		ns
t <sub>HD:STA</sub>	Start Hold Time	600		ns
t <sub>SU:STO</sub>	Stop Setup Time	600		ns
t <sub>SU:DAT</sub>	SDA Data Input Setup Time	100		ns
t <sub>HD:DAT</sub>	SDA Data Input Hold Time	30		ns
t <sub>R</sub>	SCL and SDA Rise Time		300	ns
t <sub>F</sub>	SCL and SDA Fall Time		300	ns
t <sub>AA</sub>	SCL Low to SDA Data Output Valid Time		0.9	μs
t <sub>DH</sub>	SDA Data Output Hold Time	0		ns
T <sub>I</sub>	Noise Suppression Time Constant at SCL and SDA inputs	50		ns
t <sub>BUF</sub>	Bus Free Time (Prior to Any Transmission)	1200		ns
t <sub>SU:WPA</sub>	A0, A1 Setup Time	0		ns
t <sub>HD:WPA</sub>	A0, A1 Hold Time	0		ns

**High-Voltage Write Cycle Timing**

SYMBOL	PARAMETER	TYP	MAX	UNITS
t <sub>WR</sub>	High-voltage write cycle time (store instructions)	5	10	ms

**XDCP Timing**

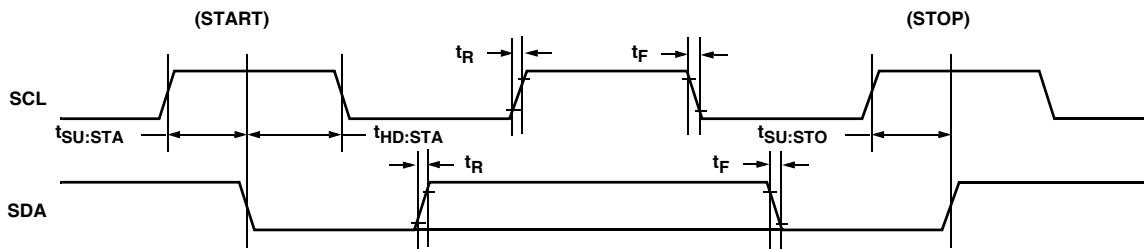
SYMBOL	PARAMETER	MIN	MAX	UNITS
t <sub>WRPO</sub>	Wiper response time after the third (last) power supply is stable	5	10	μs
t <sub>WRL</sub>	Wiper response time after instruction issued (all load instructions)	5	10	μs

**Symbol Table**

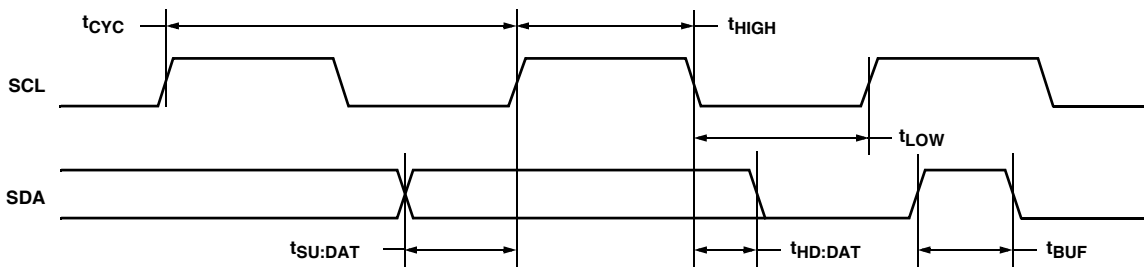
WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

**Timing Diagrams**

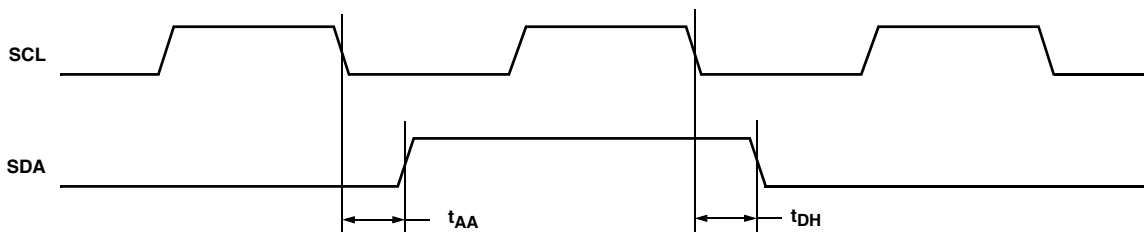
**Start and Stop Timing**



**Input Timing**

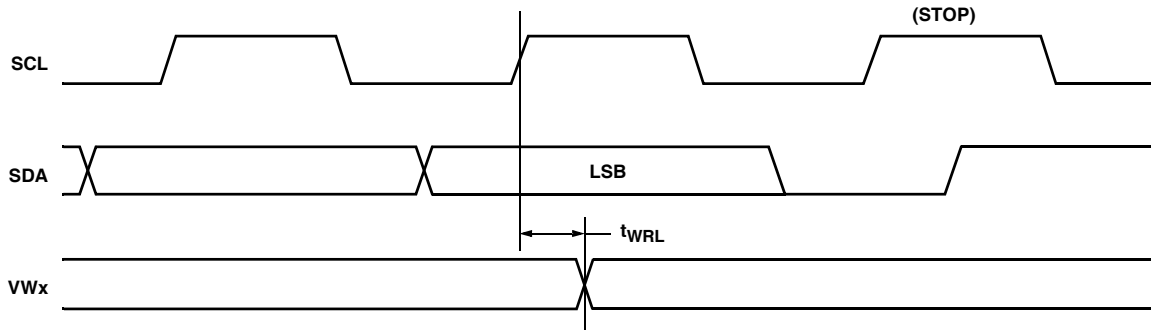


**Output Timing**

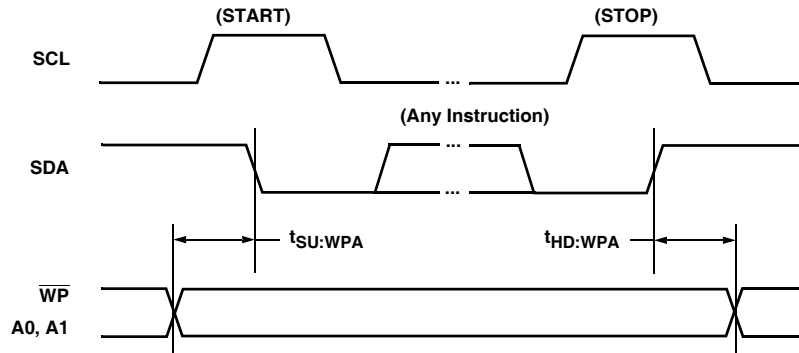




**XDCP Timing (for All Load Instructions)**

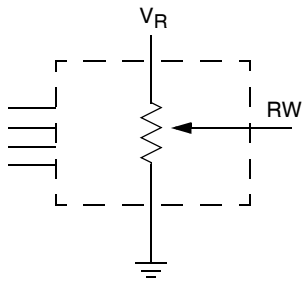


**Write Protect and Device Address Pins Timing**

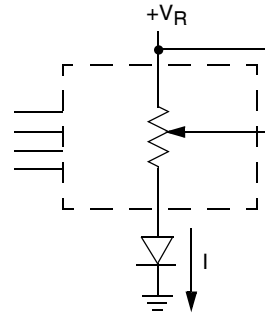


**Applications Information**

**Basic Configurations of Electronic Potentiometers**



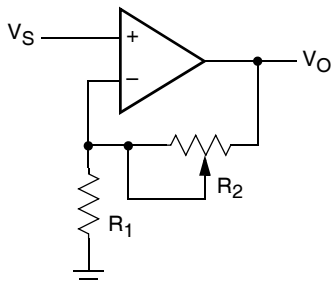
Three terminal Potentiometer; Variable voltage divider



Two terminal Variable Resistor; Variable current

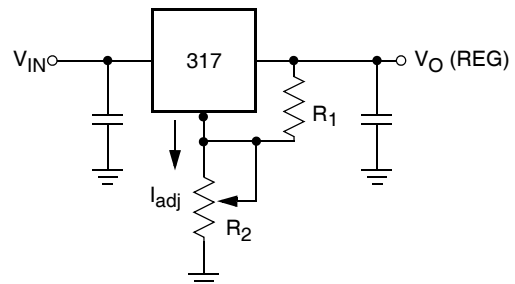
**Application Circuits**

**Non inverting Amplifier**



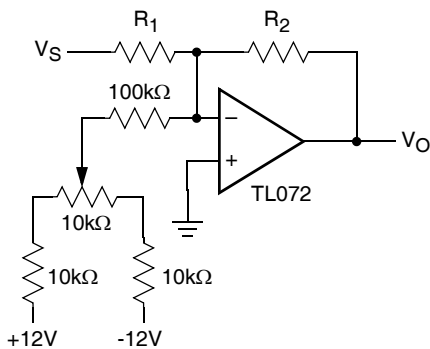
$$V_O = (1 + R_2/R_1)V_S$$

**Voltage Regulator**

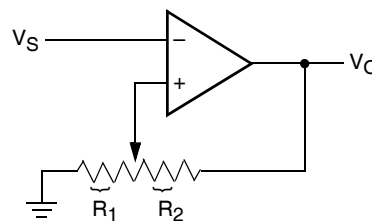


$$V_O (\text{REG}) = 1.25V (1 + R_2/R_1) + I_{\text{adj}} R_2$$

**Offset Voltage Adjustment**



**Comparator with Hysteresis**

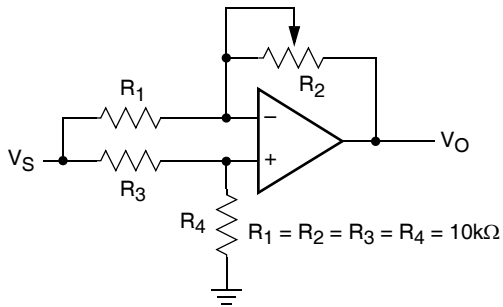


$$V_{UL} = \{R_1/(R_1+R_2)\} V_O(\text{max})$$

$$V_{LL} = \{R_1/(R_1+R_2)\} V_O(\text{min})$$

Application Circuits (continued)

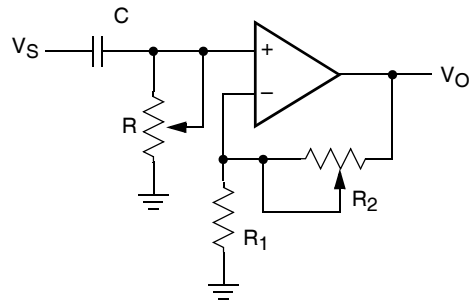
Attenuator



$V_O = G V_S$   
 $-1/2 \leq G \leq +1/2$

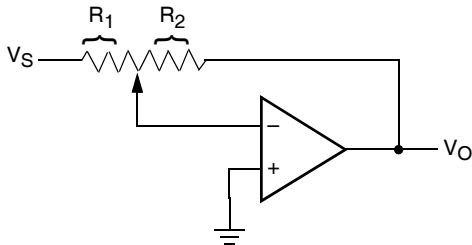
$R_1 = R_2 = R_3 = R_4 = 10k\Omega$

Filter



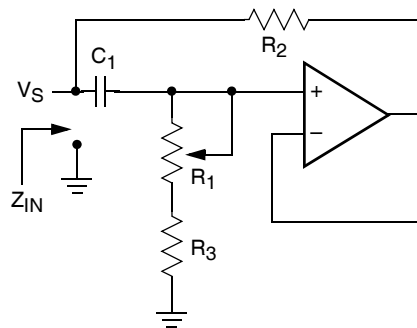
$G_O = 1 + R_2/R_1$   
 $f_c = 1/(2\pi RC)$

Inverting Amplifier



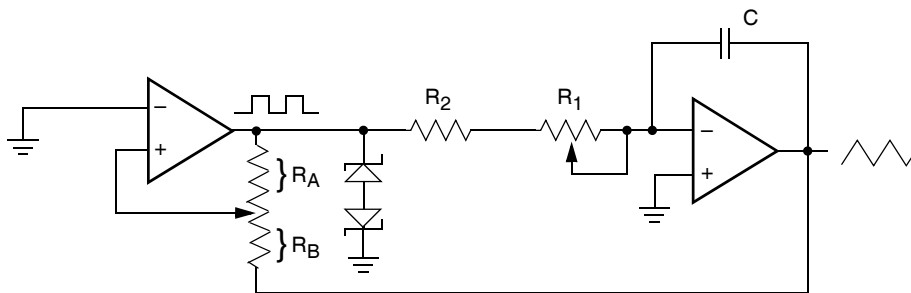
$V_O = G V_S$   
 $G = -R_2/R_1$

Equivalent L-R Circuit



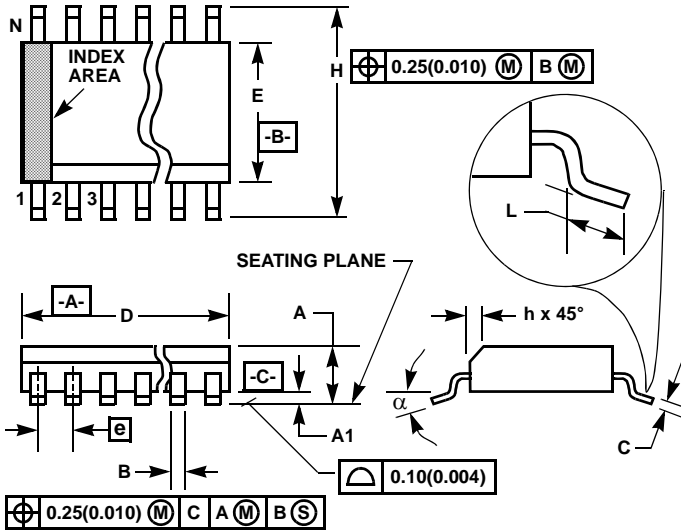
$Z_{IN} = R_2 + s R_2 (R_1 + R_3) C_1 = R_2 + s L_{eq}$   
 $(R_1 + R_3) \gg R_2$

Function Generator



frequency  $\propto R_1, R_2, C$   
 amplitude  $\propto R_A, R_B$

**Small Outline Plastic Packages (SOIC)**



**M24.3 (JEDEC MS-013-AD ISSUE C)**  
**24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE**

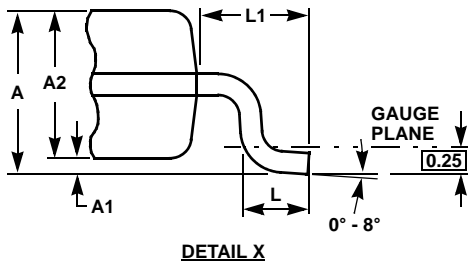
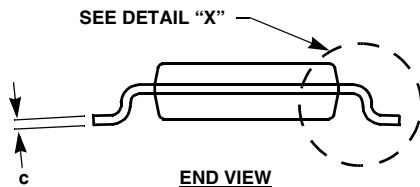
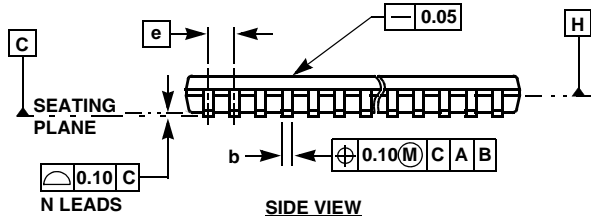
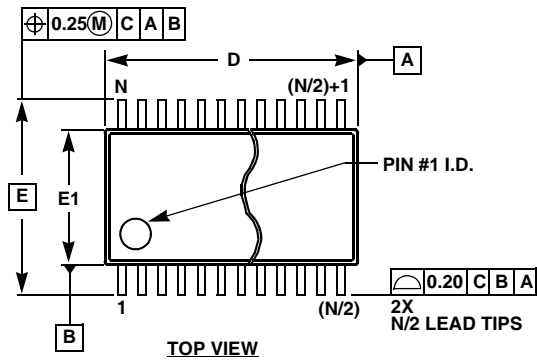
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.020	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.5985	0.6141	15.20	15.60	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
$\alpha$	0°	8°	0°	8°	-

**NOTES:**

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Rev. 1 4/06

Thin Shrink Small Outline Package Family (TSSOP)



MDP0044

THIN SHRINK SMALL OUTLINE PACKAGE FAMILY

SYMBOL	MILLIMETERS					TOLERANCE
	14 LD	16 LD	20 LD	24 LD	28 LD	
A	1.20	1.20	1.20	1.20	1.20	Max
A1	0.10	0.10	0.10	0.10	0.10	±0.05
A2	0.90	0.90	0.90	0.90	0.90	±0.05
b	0.25	0.25	0.25	0.25	0.25	+0.05/-0.06
c	0.15	0.15	0.15	0.15	0.15	+0.05/-0.06
D	5.00	5.00	6.50	7.80	9.70	±0.10
E	6.40	6.40	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	4.40	4.40	±0.10
e	0.65	0.65	0.65	0.65	0.65	Basic
L	0.60	0.60	0.60	0.60	0.60	±0.15
L1	1.00	1.00	1.00	1.00	1.00	Reference

Rev. F 2/07

NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm per side.
3. Dimensions "D" and "E1" are measured at dAtum Plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

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