X9448

Dual Digitally Controlled Potentiometer (XDCP™) & Voltage Comparator

FEATURES

- **Two digitally controlled potentiometers and two voltage comparators in one package**
- **2-wire serial interface**
- **Register oriented format**
  - **—Direct read/write wiper position**
  - **—Store as many as four positions per pot**
- **Fast response comparator**
- **Enable, latch, or shutdown comparator outputs through ACR**
- **Auto-recall of WCR and ACR data from R0**
- **Hardware write protection, $\overline{WP}$**
- **Separate analog and digital/system supplies**
- **Direct write cell**
  - **—Endurance–100,000 data changes per bit per register**
  - **—Register data retention–100 years**
- **16-bytes of EEPROM memory**
- **Power saving feature and low noise**
- **Two 10KΩ or two 2.5KΩ potentiometers**
- **Resolution: 64 taps each pot**
- **24-lead TSSOP and 24-lead SOIC packages**

DESCRIPTION

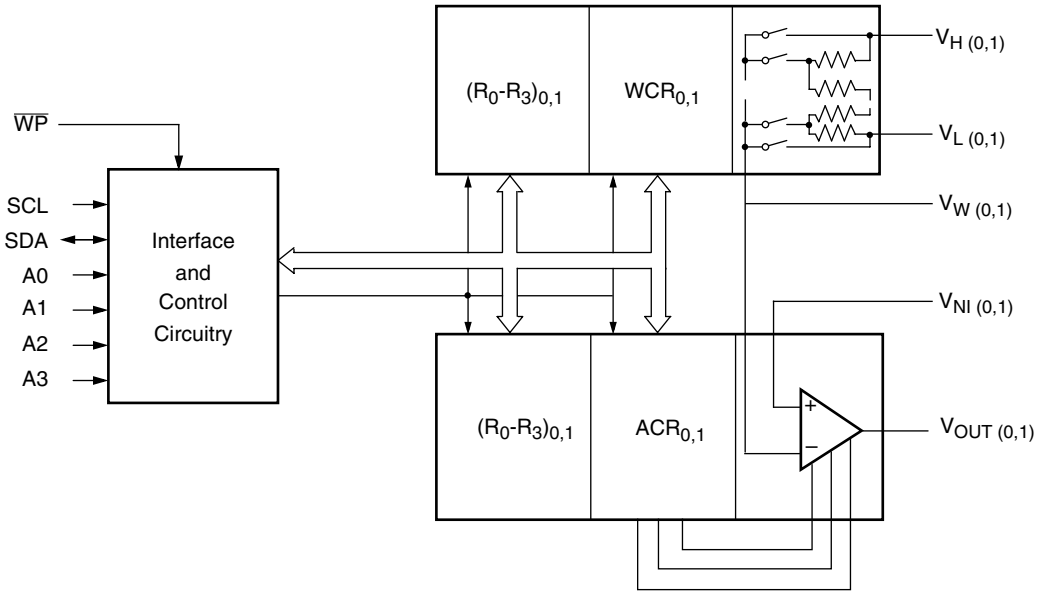
The X9448 integrates two nonvolatile digitally controlled potentiometers (XDCP) and two voltage comparators on a CMOS monolithic microcircuit.

The X9448 contains two resistor arrays, each composed of 63 resistive elements. Between each element and at either end are tap points accessible to the wiper elements. The position of the wiper element on the array is controlled by the user through the two wire serial bus interface.

Each potentiometer has an associated voltage comparator. The comparator compares the external input voltage V_{NI} with the wiper voltage V_W and sets the output voltage level to a logic high or low.

Each resistor array and comparator has associated with it a wiper counter register (WCR), analog control register (ACR), and eight 6-bit data registers that can be directly written and read by the user. The contents of the wiper counter register controls the position of the wiper on the resistor array. The contents of the analog control register controls the comparator and its output. The potentiometer is programmed with a 2-wire serial interface

BLOCK DIAGRAM



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PIN DESCRIPTIONS

Host Interface Pins

Serial Clock (SCL)

The SCL input is used to clock data into and out of the X9448.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs. An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the guidelines for calculating typical values on the bus pull-up resistors graph.

Device Address (A_0–A_3)

The address inputs are used to set the least significant 4 bits of the 8-bit slave address. A match in the slave address serial data stream must be made with the address input in order to initiate communication with the X9448. A maximum of 16 devices may share the same 2-wire serial bus.

Potentiometer Pins

V_H (V_{H0}–V_{H1}), V_L (V_{L0}–V_{L1})

The V_H and V_L inputs are equivalent to the terminal connections on either end of a mechanical potentiometer.

V_W (V_{W0}–V_{W1})

The wiper output is equivalent to the wiper output of a mechanical potentiometer and is connected to the inverting input of the voltage comparator.

Comparator and Device Pins

Voltage Input V_{NI0}, V_{NI1}

V_{NI0} and V_{NI1} are the input voltages to the plus (non-inverting) inputs of the two comparators.

Buffered Voltage Outputs V_{OUT0}, V_{OUT1}

The V_{OUT0}, and V_{OUT1} are the buffered voltage comparator outputs enabled by respective bits in the volatile analog control register.

Hardware Write Protect Input $\overline{WP}$

The $\overline{WP}$ pin when low prevents nonvolatile writes to the wiper counter and analog control registers.

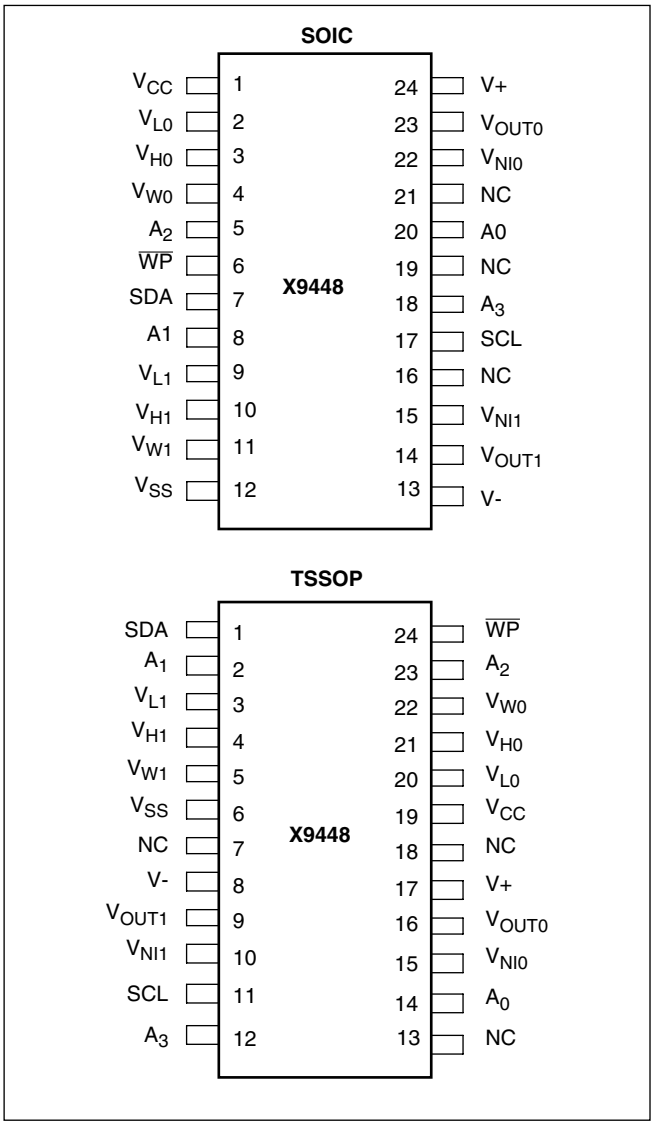
Analog Supplies V+, V-

The analog supplies V+, V- are the supply voltages for the XDCP analog section and the voltage comparators.

System Supply V_{CC} and Ground V_{SS}

The system supply V_{CC} and its reference V_{SS} is used to bias the interface and control circuits.

PIN CONFIGURATION



PIN NAMES

Symbol	Description
SCL	Serial Clock
SDA	Serial Data
A0-A3	Device Address
V_{H0}–V_{H1}, V_{L0}–V_{L1}	Potentiometers (terminal equivalent)
V_{W0}–V_{W1}	Potentiometers (wiper equivalent)
V_{NI0}, V_{NI1}	Comparator Input Voltages
V_{OUT0}, V_{OUT1}	Buffered Comparator Outputs
WP	Hardware Write Protection
V+,V-	Analog and Voltage Comparator Supplies
V_{CC}	System/Digital Supply Voltage
V_{SS}	System Ground
NC	No Connection

PRINCIPLES OF OPERATION

The X9448 is a highly integrated microcircuit incorporating two resistor arrays, two voltage comparators and their associated registers and counters; and the serial interface logic providing direct communication between the host and the digitally-controlled potentiometers and voltage comparators.

Serial Interface

The X9448 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X9448 will be considered a slave device in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW periods (t_{LOW}). SDA state changes during SCL HIGH are reserved for indicating start and stop conditions.

Start Condition

All commands to the X9448 are preceded by the start condition, which is a HIGH to LOW transition of SDA while SCL is HIGH (t_{HIGH}). The X9448 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition is met.

Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA while SCL is HIGH.

Acknowledge

Acknowledge is a software convention used to provide a positive handshake between the master and slave devices on the bus to indicate the successful receipt of data. The transmitting device, either the master or the slave, will release the SDA bus after transmitting eight bits. The master generates a ninth clock cycle and during this period the receiver pulls the SDA line LOW to acknowledge that it successfully received the eight bits of data.

The X9448 will respond with an acknowledge after recognition of a start condition and its slave address and once again after successful receipt of the command byte. If the command is followed by a data byte the X9448 will respond with a final acknowledge.

Array Description

The X9448 is comprised of two resistor arrays and two voltage comparators. Each array contains 63 discrete resistive segments that are connected in series. The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer (V_H and V_L inputs).

At both ends of each array and between each resistor segment is a CMOS switch connected to the wiper (V_W) output. Within each individual array only one switch may be turned on at a time. These switches are controlled by a volatile wiper counter register (WCR). The six bits of the WCR are decoded to select, and enable, one of sixty-four switches.

The WCR may be written directly, or it can be changed by transferring the contents of one of four associated data registers into the WCR. These data registers and the WCR can be read and written by the host system.

Voltage Comparator

The comparator compares the wiper voltage V_W with the external input voltage V_{NI}. The comparator and its logic level output are controlled by the Shutdown, Latch, and Enable bits of the analog control register (ACR). Enable connects the comparator output to the V_{OUT} pin, Latch memorizes the output logic state, and Shutdown removes the analog section supply voltages to save power. The analog control register is programmed using the two wire serial interface.

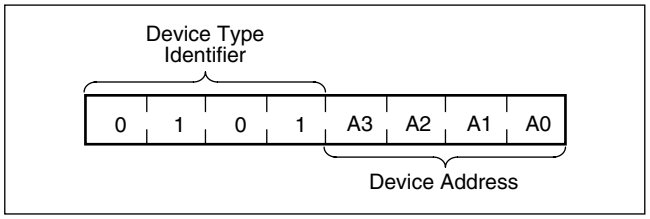
The ACR may be written directly, or it can be changed by transferring the contents of one of four associated data registers into the ACR. These data registers and the ACR may be read and written by the host system.

INSTRUCTIONS AND PROGRAMMING

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (refer to Figure 1 below). For the X9448 this is fixed as 0101[B].

Figure 1. Address/Identification Byte Format

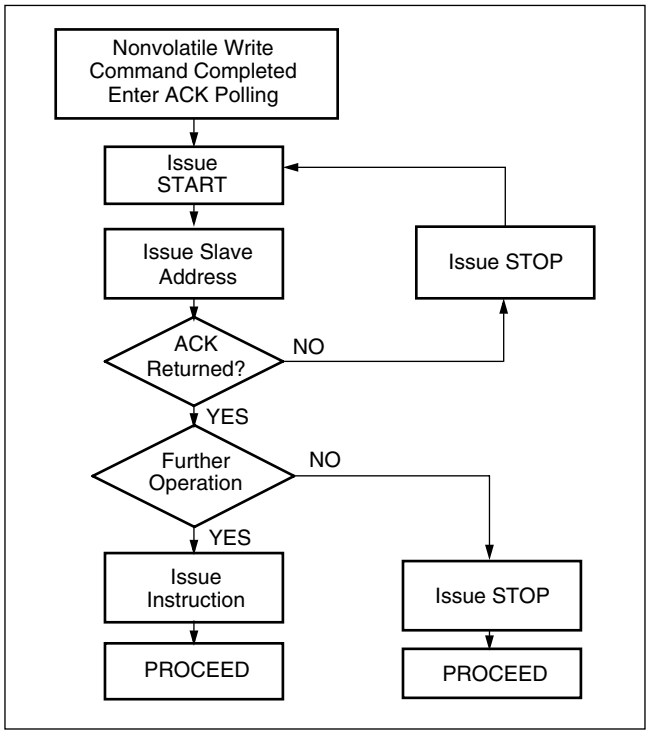


The next four bits of the slave address are the device address. The physical device address is defined by the state of the A0-A3 inputs. The X9448 compares the serial data stream with the address input state; a successful compare of all four address bits is required for the X9448 to respond with an acknowledge. The A_0–A_3 inputs can be actively driven by CMOS input signals or tied to V_{CC} or V_{SS}.

Acknowledge Polling

The disabling of the inputs, during the internal nonvolatile write operation, can be used to take advantage of the typical 5ms EEPROM write cycle time. Once the stop condition is issued to indicate the end of the nonvolatile write command the X9448 initiates the internal write cycle. ACK polling (Flow 1) can be initiated immediately. This involves issuing the start condition followed by the device slave address. If the X9448 is still busy with the write operation no ACK will be returned. If the X9448 has completed the write operation an ACK will be returned and the master can then proceed with the next operation.

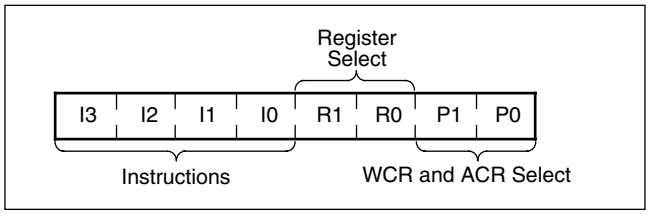
Flow 1. ACK Polling Sequence



Instruction Structure

The byte following the address contains the instruction and register pointer information. The four most significant bits are the instruction. The next four bits point to one of two pots or one of two voltage comparators and when applicable they point to one of four associated registers. The format is shown below in Figure 2.

Figure 2. Instruction Byte Format



The four high order bits define the instruction. The next two bits (R1 and R0) select one of the four registers that is to be acted upon when a register oriented instruction is issued. The last two bits (P1 and P0) select which one of the two potentiometers or which one of the two voltage comparators is to be affected by the instruction.

Four of the nine instructions end with the transmission of the instruction byte. The basic sequence is illustrated in Figure 3. These two-byte instructions exchange data between the wiper counter register or analog control register and one of the data registers. A transfer from a data register to a wiper counter register or analog control register is essentially a write to a static RAM. The response of the wiper to this action will be delayed t_{STPWV}. A transfer from the Wiper Counter Register current wiper position to a data register is a write to nonvolatile memory and takes a minimum of t_{WR} to complete. The transfer can occur between one of the two potentiometers or one of the two voltage comparators and one of its associated registers; or it may occur globally, wherein the transfer occurs between both of the potentiometers and voltage comparators and one of their associated registers.

Four instructions require a three-byte sequence to complete. The basic sequence is illustrated in Figure 4. These instructions transfer data between the host and the X9448; either between the host and one of the data registers or directly between the host and the wiper counter and analog control registers. These instructions are: read wiper counter register or analog control register, read the current wiper position of the selected pot or the comparator control bits, Write wiper counter register or analog control register, i.e. change current wiper position of the selected pot or control the voltage comparator; read data register, read the contents of the selected nonvolatile register; write data register, write a new value to the selected data register. The bit structures of the instructions are shown in Figure 6.

The increment/decrement command is different from the other commands. Once the command is issued and the X9448 has responded with an acknowledge, the master can clock the selected wiper up and/or down in one segment steps; thereby, providing a fine tuning capability to the host. For each SCL clock pulse (t_{HIGH}) while SDA is HIGH, the selected wiper will move one resistor segment towards the V_H terminal. Similarly, for each SCL clock pulse while SDA is LOW, the selected wiper will move one resistor segment towards the V_L terminal. A detailed illustration of the sequence for this operation is shown in Figure 5.

Figure 3. Two-Byte Command Sequence

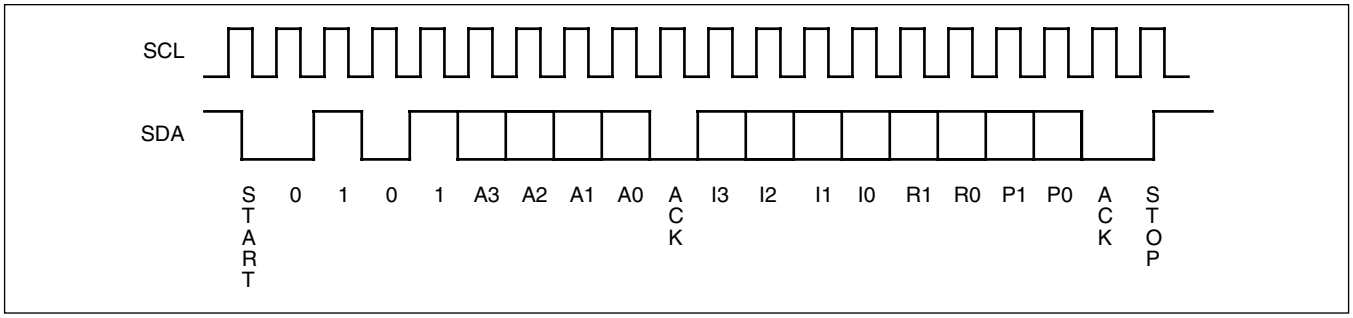


Figure 4. Three-Byte Command Sequence

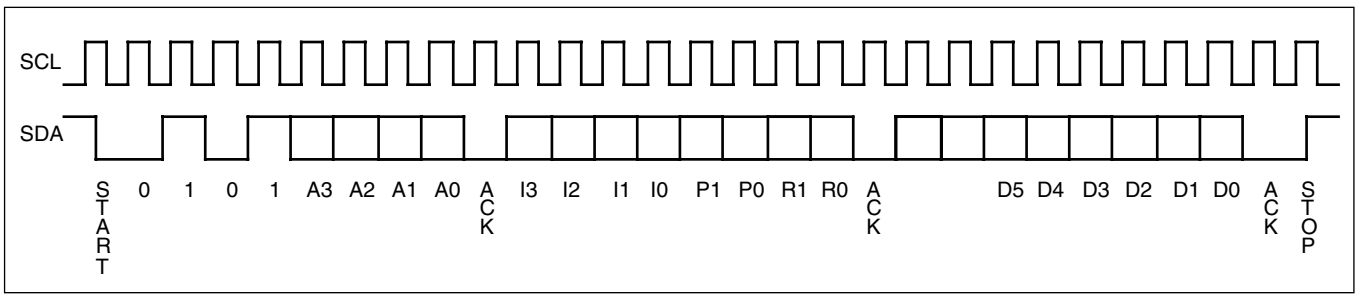
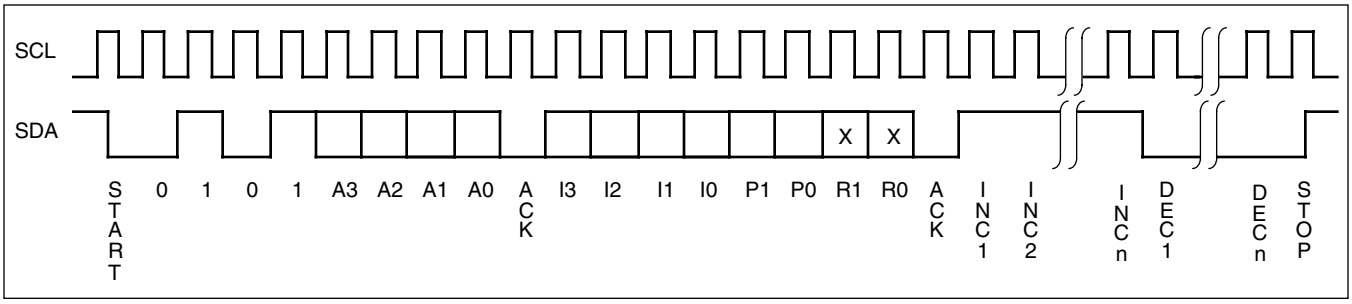


Figure 5. Increment/Decrement Command Sequence



INSTRUCTION SET

Read Wiper Counter Register (WCR) or Analog Control Register (ACR)

Read the contents of the Wiper Counter Register or Analog Control Register pointed to by P_1-P_0.

S	device type identifier				device addresses				S	instruction opcode				WCR/ACR addresses				S	register data (sent by slave on SDA)								M	S
T	0	1	0	1	A3	A2	A1	A0	A	1	0	0	1	0	0	P1	P0	A	0	0	D5	D4	D3	D2	D1	D0	A	T
A									C									C									C	O
R									K									K									K	P
T																												

P1 P0: 00-WCR0, 01 - WCR1
P1 P0: 10-ACR0, 11 - ACR1

Write Wiper Counter Register (WCR) or Analog Control Register (ACR)

Write new value to the Wiper Counter Register or Analog Control Register pointed to by P_1-P_0.

S	device type identifier				device addresses				S	instruction opcode				WCR/ACR addresses				S	register data (sent by master on SDA)								S	S
T	0	1	0	1	A3	A2	A1	A0	A	1	0	1	0	0	0	P1	P0	A	0	0	D5	D4	D3	D2	D1	D0	A	T
A									C									C									C	O
R									K									K									K	P
T																												

P1 P0: 00-WCR0, 01 - WCR1
P1 P0: 10-ACR0, 11 - ACR1

Read Data Register (DR)

Read the contents of the Register pointed to by P_1-P_0 and R_1-R_0.

S	device type identifier				device addresses				S	instruction opcode				WCR/ACR/DR addresses				S	register data (sent by master on SDA)								M	S
T	0	1	0	1	A3	A2	A1	A0	A	1	0	1	1	R1	R0	P1	P0	A	0	0	D5	D4	D3	D2	D1	D0	A	T
A									C									C									C	O
R									K									K									K	P
T																												

R1 R0: 00-R0, 10-R1
01-R2, 11-R3

Definitions:

SACK – Slave acknowledge, MACK – Master acknowledge, I/O – Increment/Decrement (I/O), R – Register, P – Potentiometer

Write Data Register (DR)

Write new value to the Register pointed to by P_1-P_0 and R_1-R_0.

S	device type identifier				device addresses				S	instruction opcode				WCR/ACR/DR addresses				S	register data (sent by master on SDA)								S	S	HIGH-VOLTAGE WRITE CYCLE
T	0	1	0	1	A3	A2	A1	A0	A	1	1	0	0	R1	R0	P1	P0	A	0	0	D5	D4	D3	D2	D1	D0	A	T	
A									C									C									C	O	
R									K									K									K	P	
T																													

Transfer Data Register to Wiper Counter Register or Analog Control Register

Transfer the contents of the Register pointed to by R_1-R_0 to the WCR or ACR pointed to by P_1-P_0.

S	device type identifier				device addresses				S	instruction opcode				WCR/ACR/DR addresses				S	S
T	0	1	0	1	A3	A2	A1	A0	A	1	1	0	1	R1	R0	P1	P0	A	T
A									C									C	O
R									K									K	P
T																			

Transfer Wiper Counter or Analog Control Register to Data Register

Transfer the contents of the WCR or ACR pointed to by P_1-P_0 to the Register pointed to by R_1-R_0.

S	device type identifier				device addresses				S	instruction opcode				WCR/ACR/DR addresses				S	S	HIGH-VOLTAGE WRITE CYCLE
T	0	1	0	1	A3	A2	A1	A0	A	1	1	1	0	R1	R0	P1	P0	A	T	
A									C									C	O	
R									K									K	P	
T																				

Global Transfer Data Register to Wiper Counter or Analog Control Register

Transfer the contents of all four Data Registers pointed to by R_1-R_0 to their respective WCR or ACR.

S	device type identifier				device addresses				S	instruction opcode				DR addresses				S	S
T	0	1	0	1	A3	A2	A1	A0	A	0	0	0	1	R1	R0	0	0	A	T
A									C									C	O
R									K									K	P
T																			

Global Transfer Wiper Counter or Analog Control Register to Data Register

Transfer the contents of all WCRs and ACRs to their respective data Registers pointed to by R_1-R_0.

S	device type identifier				device addresses				S	instruction opcode				DR addresses				S	S	HIGH-VOLTAGE WRITE CYCLE
T	0	1	0	1	A3	A2	A1	A0	A	1	0	0	0	R1	R0	0	0	A	T	
A									C									C	O	
R									K									K	P	
T																				

Increment/Decrement Wiper Counter Register

Enable Increment/decrement of the WCR pointed to by P_1-P_0.

S T A R T	device type identifier				device addresses				S A C K	instruction opcode				WCR addresses				S A C K	increment/decrement (sent by master on SDA)						S T O P
	0	1	0	1	A 3	A 2	A 1	A 0		0	0	1	0	0	0	P 1	P 0		I/ D	I/ D	. . . .		I/ D	I/ D	

P1 P0: 00 or 01 only.

REGISTERS OPERATION

Both XDCP potentiometers and voltage comparators share the serial interface and share a common architecture. Each potentiometer and voltage comparator is associated with wiper counter and analog control registers and eight data registers. A detailed discussion of the register organization and array operation follows.

Wiper Counter (WCR) and Analog Control Registers (ACR)

The X9448 contains two wiper counter registers one for each XDCP potentiometer and two analog control registers, one for each of the two voltage comparators. The wiper counter register is equivalent to a serial-in, parallel-out counter with its outputs decoded to select one of sixty-four switches along its resistor array. The contents of the wiper counter register and analog control register can be altered in four ways: it may be written directly by the host via the Write WCR instruction (serial load); it may be written indirectly by transferring the contents of one of four associated data registers (DR) via the XFR data register instruction (parallel load); it can be modified one step at a time by the increment/decrement instruction (WCR only). Finally, it is loaded with the contents of its data register zero (R0) upon power-up.

The wiper counter and analog control register are volatile registers; that is, their contents are lost when the X9448 is powered-down. Although the registers are automatically loaded with the value in R0 upon power-up, it should be noted this may be different from the value present at power-down.

Programming the ACR is similar to the WCR. However, the 6 bits in the WCR positions the wiper in the resistor array while 3 bits in the ACR control the comparator and its output.

Data Registers (DR)

Each potentiometer and each voltage comparator has four nonvolatile data registers (DR). These can be read or written directly by the host and data can be transferred between any of the four data registers and the WCR or ACR. It should be noted all operations changing data in one of these registers is a nonvolatile operation and will take a maximum of 10ms.

If the application does not require storage of multiple settings for the potentiometer or comparator, these registers can be used as regular memory locations that could store system parameters or user preference data.

REGISTER DESCRIPTIONS

Wiper Counter Register (WCR)

0	0	WP5	WP4	WP3	WP2	WP1	WP0
		(volatile)					(LSB)

WP0-WP5 identify wiper position.

Analog Control Register (ACR)

0	0	User -bit5	User -bit4	User -bit3	Latch	Enable	Shut- down
		(volatile)					(LSB)

Shutdown

"1" indicates power is connected to the voltage comparator.

"0" indicates power is not connected to the voltage comparator.

Enable

"1" indicates the output buffer of the voltage comparator is enabled.

"0" indicates the output buffer of the voltage comparator is disabled.

Latch

"1" indicates the output of the voltage comparator is memorized or latched.

"0" indicates the output of the voltage comparator is not latched.

Userbits—available for user applications

Data Registers (DR, R0-R3)

Wiper Position or Analog Control Data or User Data
(Nonvolatile)

Memory Map

WCRO	WCR1	ACR0	ACR1
R0	R0	R0	R0
R1	R1	R1	R1
R2	R2	R2	R2
R3	R3	R3	R3

ABSOLUTE MAXIMUM RATINGS

Temperature under bias .....–65°C to +135°C
Storage temperature .....–65°C to +150°C
Voltage on SDA, SCL or any
address input with respect to V_{SS} .....–1V to +7V
Voltage on any V+ (referenced to V_{SS} ..... +7V
Voltage on any V- (referenced to V_{SS} ..... -7V
(V+) – (V-) 10V
Any V_H ..... V+
Any V_L ..... V-
Lead temperature (soldering, 10 seconds) .....300°C

COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

Device	Supply Voltage (V_{CC}) Limits
X9448	5V ±10%
X9448-2.7	2.7V to 5.5V

POTENTIOMETER CHARACTERISTICS (Over recommended operating conditions unless otherwise stated.)

Symbol	Parameter		Limits Min.	Typ.	Max.	Unit	Test Conditions
R_{TOTAL}	End to end resistance		–20		+20	%	
	Power rating				50	mW	25°C, each pot
I_W	Wiper current		–3		+3	mA	
R_W	Wiper resistance			40	100	Ω	V_{CC} = 5V, Wiper Current = 3mA
				100	250	Ω	V_{CC} = 2.7-5V, Wiper Current = 3mA
Vv+	Voltage on V+ Pin	X9440	+4.5		+5.5	V	
		X9440-2.7	+2.7		+5.5		
Vv-	Voltage on V- Pin	X9440	-5.5		-4.5	V	
		X9440-2.7	-5.5		-2.7		
V_{TERM}	Voltage on any V_H or V_L pin		V-		V+	V	
	Noise			-120		dBv	Ref: 1V
	Resolution (4)			1.6		%	
	Absolute linearity (1)		–1		+1	MI(3)	$V_{w(n)(actual)}$–$V_{w(n)(expected)}$
	Relative linearity (2)		–0.2		+0.2	MI(3)	$V_{w(n+1)}$–[$V_{w(n)}$ + MI]
	Temperature Coefficient of R_{TOTAL}			±300		ppm/°C	

Notes: (1) Absolute linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.
(2) Relative linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.
(3) MI = RTOT/63 or (V_H–V_L)/63, single pot
(4) Individual array resolutions

COMPARATOR ELECTRICAL CHARACTERISTICS

(Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
V_{OS}	Input offset voltage	-1 -5		1 5	mV mV	V+/V- = ±3V V+/V- = ±5V
I_B	Input current		10		pA	
V_{IR}	Input voltage range	V-		V+	V	
t_R	Response time		200		ns	note 1
I_O	Output current	-1		1	mA	
A_V	Voltage gain				V/mV	
PSRR	Power supply rejection ratio		60		dB	
V_{OR}	Output voltage range	V_{SS}		V_{CC}	V	
T_CV_{OS}	Input offset voltage drift		6		µV/°C	
I_S	Supply current (V+ to V-)		1.2 .5		mA mA	V+/V- = ±5V V+/V- = ±3V
T_{ON}	Comparator enable time		1		µs	note 2
V_{OL}	Output low voltage			0.4	V	I_O = 1mA
V_{OH}	Output high voltage	V_{CC} – 0.8			V	I_O = 1mA

Notes: (1) 100mV step with 100mV overdrive, ZL = 10KΩ || 15pF, 10-90% risetime
(2) Time from leading edge of enable bit to valid V_{OUT}.

SYSTEM/DIGITAL D.C. OPERATING CHARACTERISTICS

(Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.	Max.	Unit	
I_{CC}	V_{CC} supply current (active)			400	µA	f_{SCL} = 400kHz, SDA = Open, Other Inputs = V_{SS}
I_{SB}	V_{CC} current (standby)			1	µA	SCL = SDA = V_{CC}, Addr. = V_{SS}
I_{LI}	Input leakage current			10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output leakage current			10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IH}	Input HIGH voltage	V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{IL}	Input LOW voltage	–0.5		V_{CC} x 0.1	V	
V_{OL}	Output LOW voltage			0.4	V	I_{OL} = 3mA

ENDURANCE AND DATA RETENTION

Parameter	Min.	Unit
Minimum endurance	100,000	Data changes per bit per register
Data retention	100	Years

CAPACITANCE

Symbol	Test	Typical	Unit	Test Conditions
$C_{I/O}$	Input/output capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input capacitance (A0, A1, A2, A3, and SCL)	6	pF	V_{IN} = 0V
C_L, C_H, C_W	Potentiometer capacitance	10/10/25	pF	

Power-Up Timing and Sequence

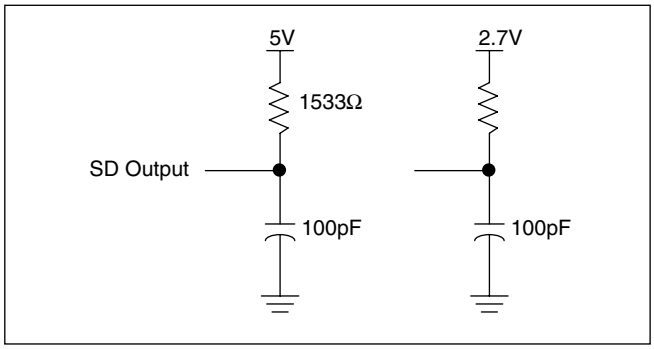
Power up sequence(1): (1) V_{CC} (2) V+ and V– {V+ ≤ V_{CC} at all times}
Power down sequence: no limitation

A.C. TEST CONDITIONS

Input pulse levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input rise and fall times	10ns
Input and output timing level	V_{CC} x 0.5

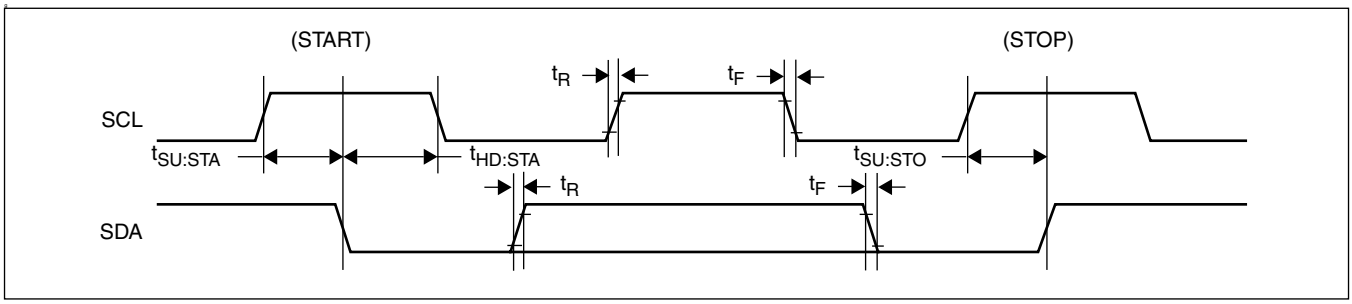
Note: (1) Applicable to recall and power consumption applications

EQUIVALENT A.C. LOAD CIRCUIT

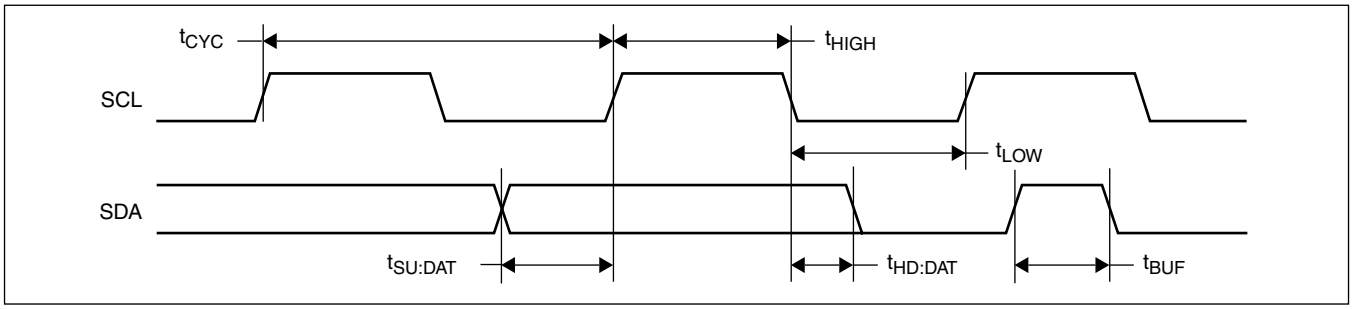


TIMING DIAGRAMS

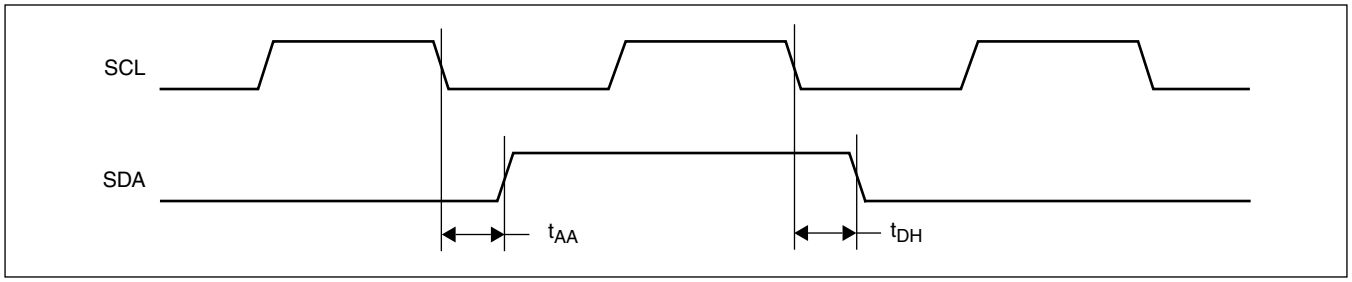
START and STOP Timing



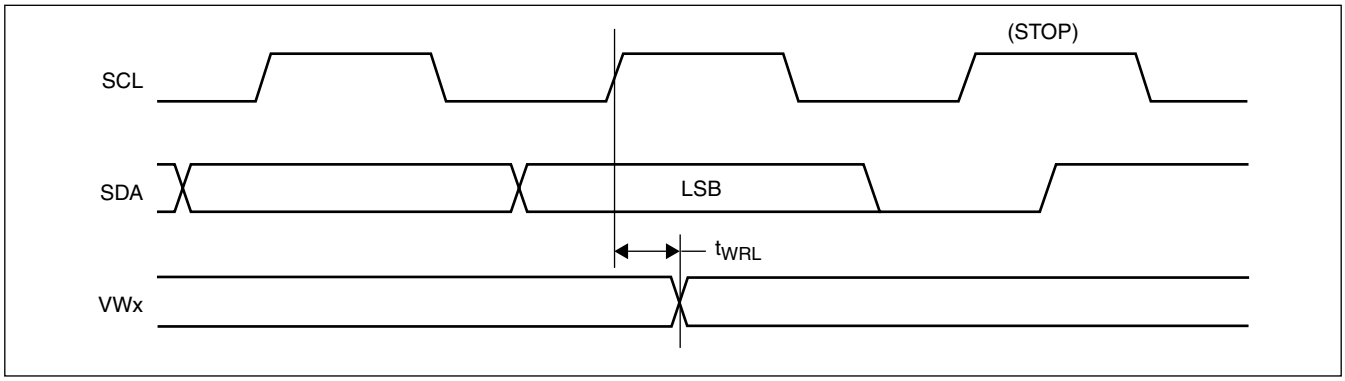
Input Timing



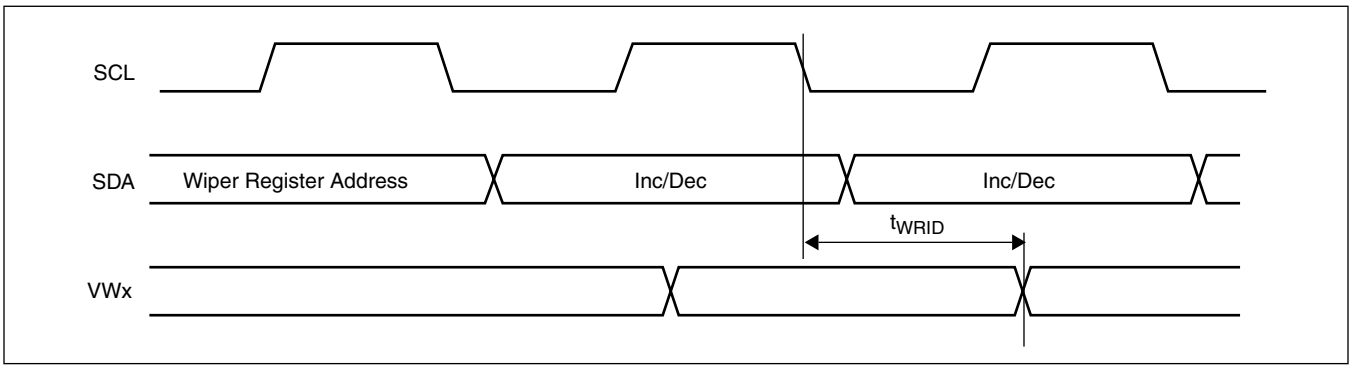
Output Timing



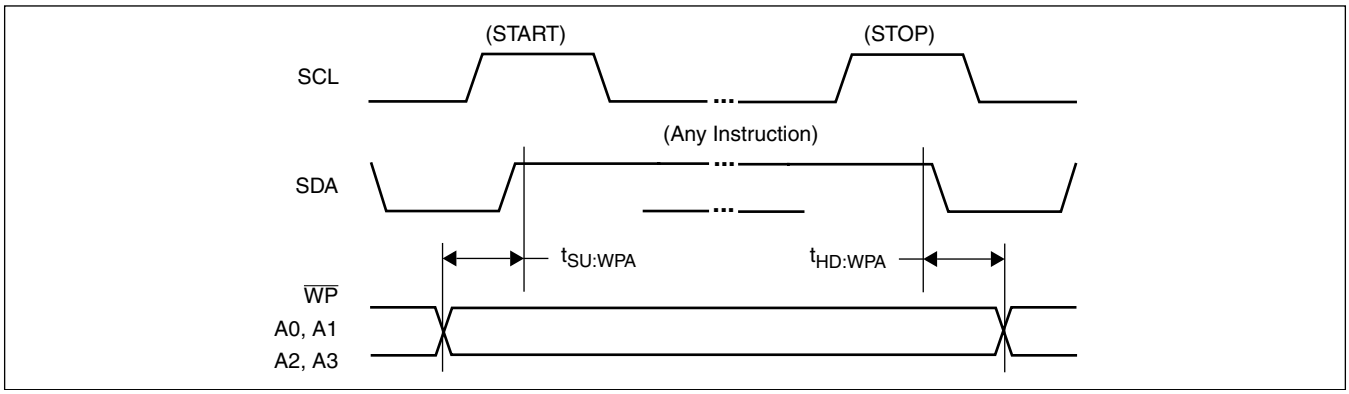
XDCP Timing (for All Load Instructions)



XDCP Timing (for Increment/Decrement Instruction)



Write Protect and Device Address Pins Timing



AC Timing

Symbol	Parameter	Min.	Max.	Unit
f_{SCL}	Clock frequency		400	kHz
t_{CYC}	Clock cycle time	2500		ns
t_{HIGH}	Clock high time	600		ns
t_{LOW}	Clock low time	1300		ns
$t_{SU:STA}$	Start setup time	600		ns
$t_{HD:STA}$	Start hold time	600		ns
$t_{SU:STO}$	Stop setup time	600		ns
$t_{SU:DAT}$	SDA data input setup time	100		ns
$t_{HD:DAT}$(4)	SDA data input hold time	0/30		ns
t_R	SCL and SDA rise time		300	ns
t_F	SCL and SDA fall time		300	ns
t_{AA}	SCL low to SDA data output valid time	100	900	ns
t_{DH}	SDA Data output hold time	50		ns
T_I	Noise suppression time constant at SCL and SDA inputs	50		ns
t_{BUF}	Bus free time (prior to any transmission)	1300		ns
$t_{SU:WPA}$	$\overline{WP}$, A0, A1, A2 and A3 setup time	0		ns
$t_{HD:WPA}$	$\overline{WP}$, A0, A1, A2 and A3 hold time	0		ns

High-Voltage Write Cycle Timing

Symbol	Parameter	Typ.	Max.	Unit
t_{WR}	High-voltage write cycle time (store instructions)	5	10	ms

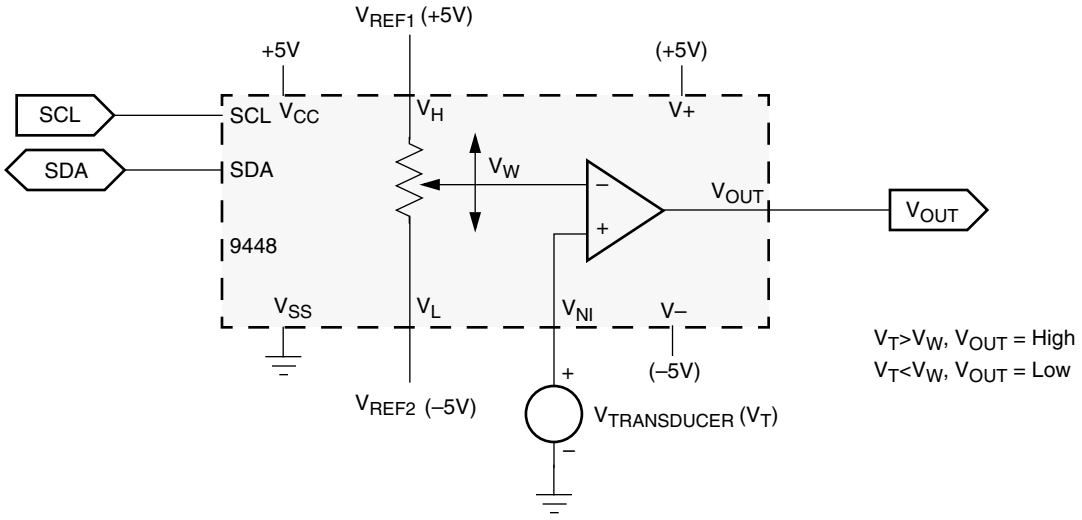
XDCP Timing

Symbol	Parameter	Min.	Max.	Unit
t_{WRL}	Wiper response time after instruction issued (all load instructions)		10	µs

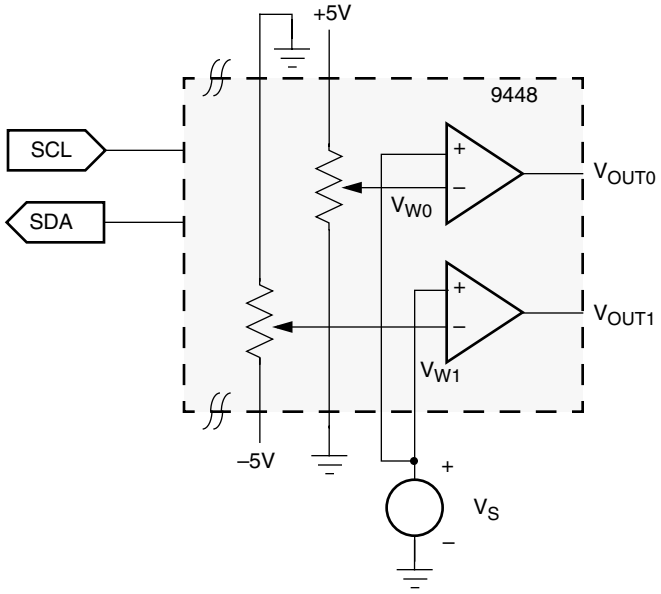
Note: (4) V_{CC} = 5V/2.7V

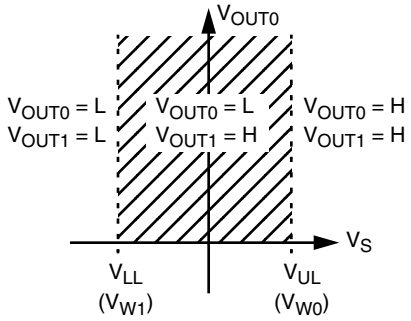
BASIC APPLICATIONS

Programmable Level Detector with Memory (typical bias conditions)



Programmable Window Detector with Memory



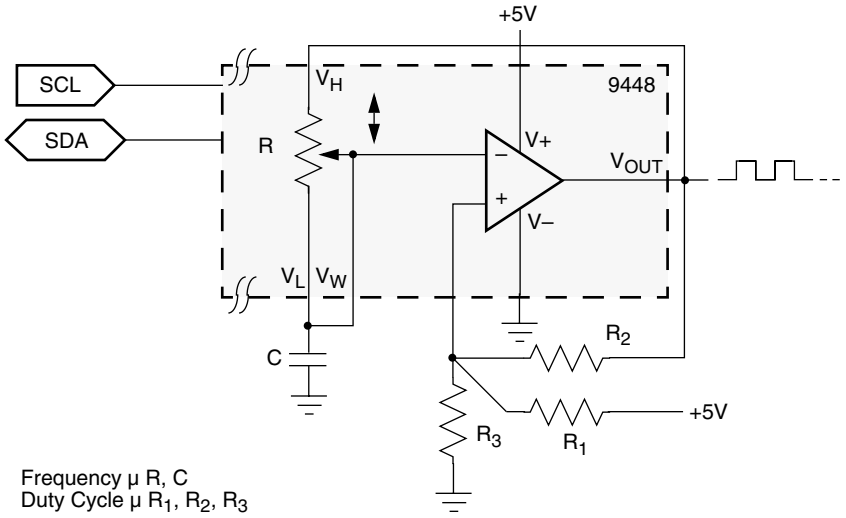


For the signal voltage V_S > the upper limit V_{UL}, (V_{OUT0} = H) • (V_{OUT1} = H)
V_S < the lower limit V_{LL}, (V_{OUT0} = L) • (V_{OUT1} = L)

For the window $V_{LL} \le V_S \le V_{UL}$, ($V_{OUT0}$ = L) • (V_{OUT1} = H)

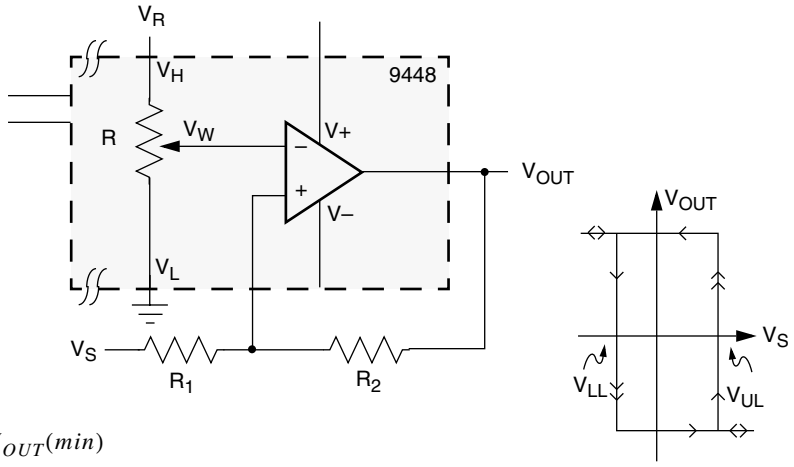
BASIC APPLICATION (continued)

Programmable Oscillator with Memory



Frequency µ R, C
Duty Cycle µ R_1, R_2, R_3

Programmable Schmitt Trigger with Memory

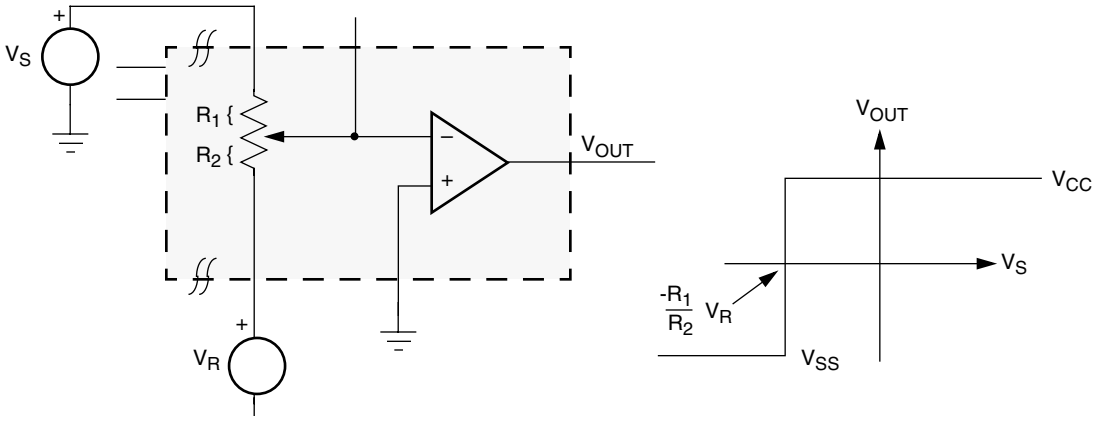


$$V_{UL} = \frac{R_1 + R_2}{R_2} V_W - \frac{R_1}{R_2} V_{OUT}(min)$$

$$V_{LL} = \frac{R_1 + R_2}{R_2} V_W - \frac{R_1}{R_2} V_{OUT}(max)$$

BASIC APPLICATION (continued)

Programmable Level Detector (alternate technique)

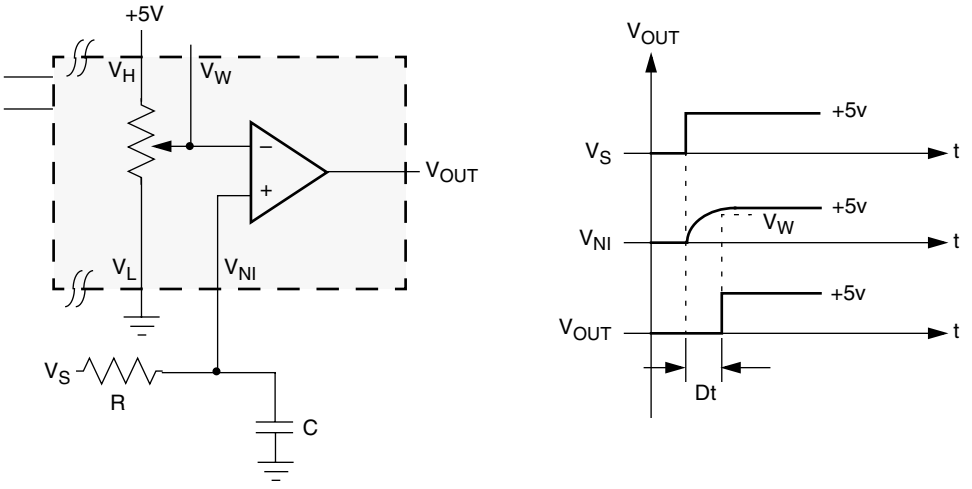


V_{OUT} = High for $V_S < -\frac{R_1}{R_2}V_R$

V_{OUT} = Low for $V_S > -\frac{R_1}{R_2}V_R$

$R_1 + R_2 = R_{POT}$

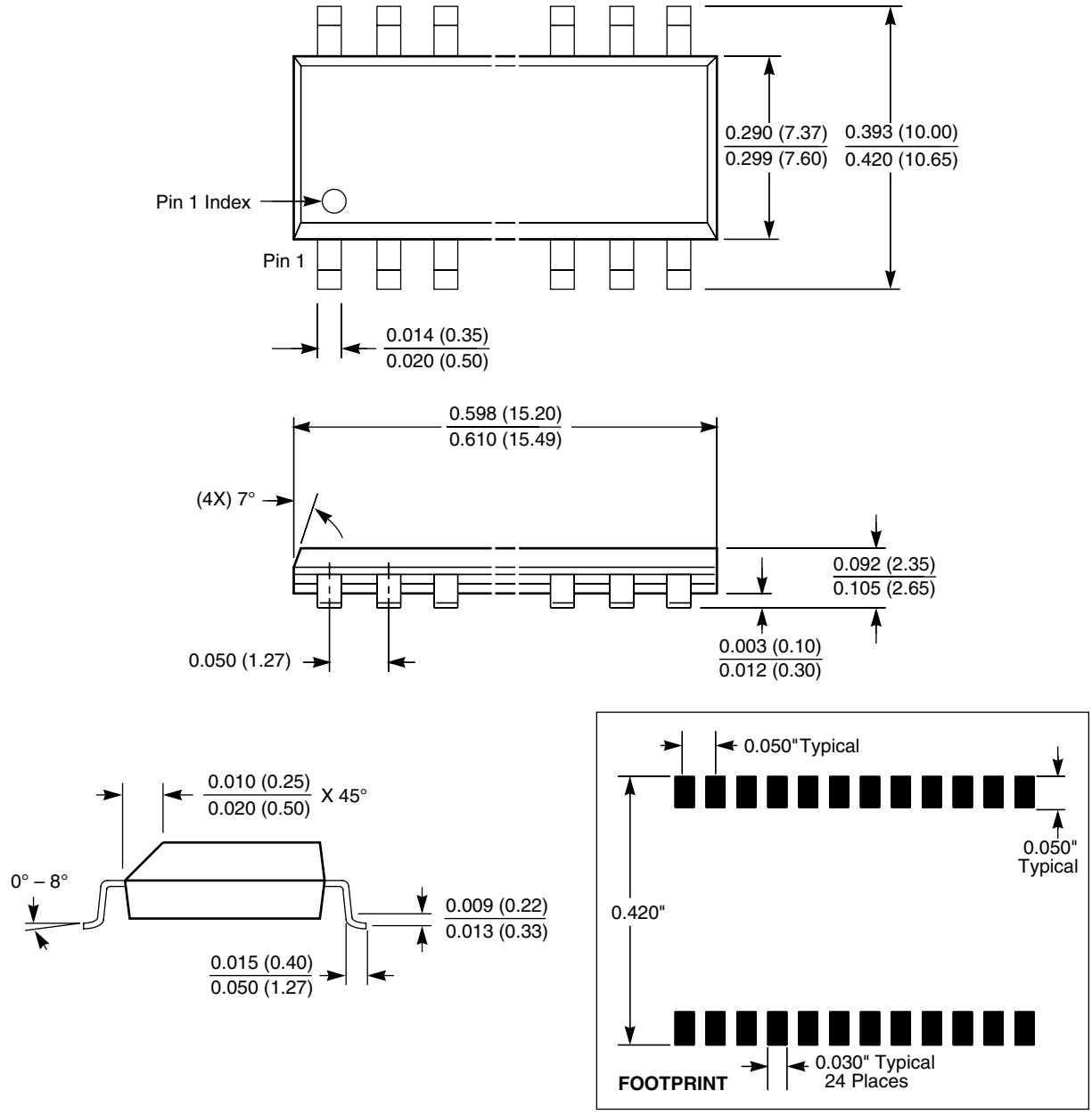
Programmable Time Delay with Memory



$\Delta t = RC \ln\left(\frac{5V}{5V - V_W}\right)$

PACKAGING INFORMATION

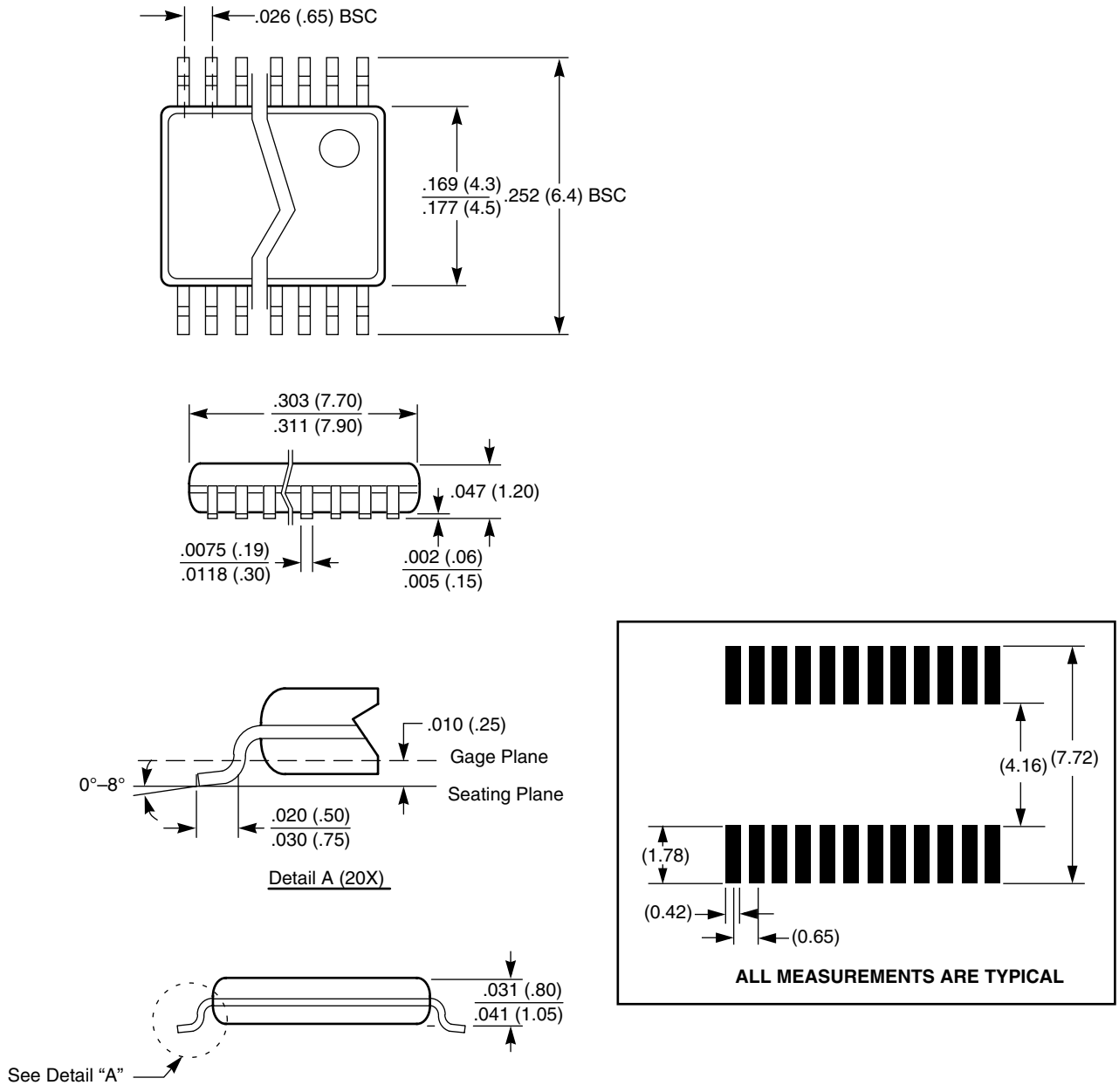
24-Lead Plastic Small Outline Gull Wing Package Type S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

24-Lead Plastic, TSSOP Package Type V



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

ORDERING INFORMATION