Dual LNA with Selectable Gain and Input Impedance

Preliminary Technical Data

# AD8432

## FEATURES

**Low noise**
- **Input voltage noise: 0.85 nV/√Hz**
- **Current noise: 2.0 pA/√Hz**

**Excellent ac specifications**
- **200 MHz bandwidth @ G = 4**
- **271 V/μs slew rate**

**Selectable Gain: ×4, ×8, ×12, ×16**
**Active input impedance matching**
**Single-ended input, differential output**
**Supply range: 4.5 V to 5.5 V**
**Low power: 60 mW/channel**

## APPLICATIONS

**Ultrasound front ends**
**Wideband A/D drivers**
**Low Noise Preamplification**
**Predriver for I/Q demodulators and phase shifters**

## FUNCTIONAL BLOCK DIAGRAM

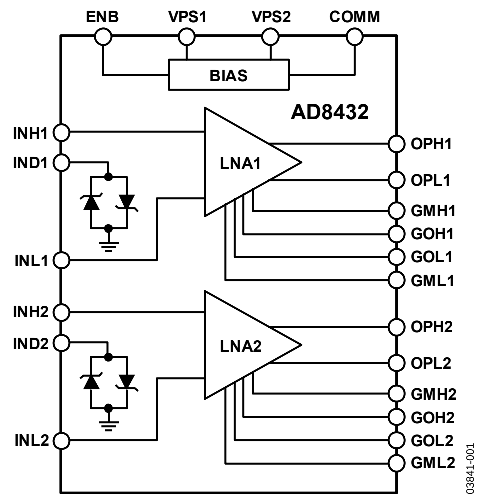


*Figure 1.*

## GENERAL DESCRIPTION

The AD8432 is a dual-channel, low power, ultralow noise amplifier with selectable gain and active impedance matching. Each amplifier has a single-ended input, differential output, and optional integrated input clamps. By pin strapping the gain setting pins, four accurate gains of G = ×4, ×8, ×12, and ×16 are possible. A bandwidth of 200 MHz at G = ×4 makes this amplifier well suited for many high speed applications.

The exceptional noise performance of the AD8432 is made possible by the active impedance matching. Using a feedback network, the input impedance of the amplifiers can be adjusted to match the signal source impedance without compromising the noise performance. Impedance matching and low noise of the AD8432 allow designers to create wider dynamic range systems that are able to detect even very low level signals.

The AD8432 achieves 0.85 nV/√Hz input referred voltage noise for a gain of ×4. The ultralow noise and low distortion of the AD8432, excellent gain accuracy, and active impedance matching is ideal for high performance ultrasound systems. Dual-channel and gain matching make it ideal for processing I/Q demodulator signals.

The AD8432 operates on a single supply of 5 V at 24 mA. It is available in a 4 mm × 4 mm, 24-lead LFSCP. The LFCSP features an exposed paddle that provides a low thermal resistance path to the PCB, which enables more efficient heat transfer and increases reliability. The operating temperature range is –40°C to +85°C.

**Rev. PrA**


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# SPECIFICATIONS

$V_S$ = 5 V, $T_A$ = 25°C, $R_S$ = $R_{IN}$ = 50 Ω, $R_{FB}$ =150 Ω, $C_{SH}$ = 47 pF, $R_{SH}$ = 15 Ω, $C_L$ = 5 pF, $R_L$ =500 Ω (per SE output), G = 12.04 dB (single-ended input to differential output), f = 10 MHz, unless otherwise specified.

**Table 1.**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE | | | | | |
| Gain Range | Single-ended input to differential output (selectable gain) | 12.04 | | 24.08 | dB |
| | Input to either of two outputs (selectable gain) | 6.02 | | 18.06 | dB |
| −3 dB Small Signal Bandwidth | $R_{IN}$ unterminated, $R_S$ = 50 Ω, $R_{FB}$ = ∞ | | | | |
| | G = 12.04 dB, $R_S$ = 50 Ω, $R_{FB}$ = ∞, $C_{SH}$ = 0 pF, $R_{SH}$ = 0 Ω | | 200 | | MHz |
| | G = 18.06 dB, $R_S$ = 50 Ω, $R_{FB}$ = ∞, $C_{SH}$ = 0 pF, $R_{SH}$ = 0 Ω | | 82 | | MHz |
| | G = 21.58 dB, $R_S$ = 50 Ω, $R_{FB}$ = ∞, $C_{SH}$ = 0 pF, $R_{SH}$ = 0 Ω | | 50 | | MHz |
| | G = 24.08 dB, $R_S$ = 50 Ω, $R_{FB}$ = ∞, $C_{SH}$ = 0 pF, $R_{SH}$ = 0 Ω | | 32 | | MHz |
| −3 dB Large Signal Bandwidth | $V_{OUT}$ = 2 V p-p | | 22 | | MHz |
| Slew Rate (Rising Edge) | $V_{OUT}$ = 2 V p-p, f = 10 MHz | | 271 | | V/µs |
| Slew Rate (Falling Edge) | $V_{OUT}$ = 2 V p-p, f = 10 MHz | | 170 | | V/µs |
| Overdrive Recovery Time | | | 10 | | ns |
| DISTORTION/NOISE PERFORMANCE | | | | | |
| Input Voltage Noise | $R_S$ = 0, $R_{FB}$ = ∞, f = 100 kHz | | 0.85 | | nV/√Hz |
| Input Current Noise | $R_{FB}$ = ∞, f = 100 kHz | | 2.0 | | pA/√Hz |
| Noise Figure | | | | | |
| Unterminated | $R_S$ = 50 Ω, $R_{FB}$ = ∞, f = 1 MHz | | 2.8 | | dB |
| Active Termination | $R_S$ = $R_{IN}$ = 50 Ω, $R_{FB}$ = 150Ω, f = 1 MHz | | 5.4 | | dB |
| | $R_S$ = 50 Ω, $R_{FB}$ = 226 Ω, $R_{IN}$ = 75 Ω f = 1 MHz | | 4.2 | | dB |
| | $R_S$ = 50 Ω, $R_{FB}$ = 301 Ω, $R_{IN}$ = 100 Ω f = 1 MHz | | 3.7 | | |
| | $R_S$ = 50 Ω, $R_{FB}$ = 619 Ω, $R_{IN}$ = 200 Ω, f = 1 MHz | | 3.1 | | dB |
| | $R_S$ = 50 Ω, $R_{FB}$ = 3.57 kΩ, $R_{IN}$ = 1 kΩ, f = 1 MHz | | 2.8 | | dB |
| Output Referred Noise | G = 12.04 dB, $R_S$ = 0 Ω, $R_{FB}$ = ∞, f = 100 kHz | | 3.4 | | nV/√Hz |
| | G = 18.06 dB, $R_S$ = 0 Ω, $R_{FB}$ = ∞, f = 100 kHz | | 6.8 | | nV/√Hz |
| | G = 21.58 dB, $R_S$ = 0 Ω, $R_{FB}$ = ∞, f = 100 kHz | | 10.2 | | nV/√Hz |
| | G = 24.08 dB, $R_S$ = 0 Ω, $R_{FB}$ = ∞, f = 100 kHz | | 13.6 | | nV/√Hz |
| Harmonic Distortion | | | | | |
| HD2 | $V_{OUT}$ = 1 V p-p, f = 1 MHz, $R_S$ = $R_{IN}$ = 50 Ω | | −102 | | dBc |
| HD3 | $V_{OUT}$ = 1 V p-p, f = 1 MHz, $R_S$ = $R_{IN}$ = 50 Ω | | −102 | | dBc |
| HD2 | $V_{OUT}$ = 1 V p-p, f = 10 MHz, $R_S$ = $R_{IN}$ = 50 Ω | | −64 | | dBc |
| HD3 | $V_{OUT}$ = 1 V p-p, f = 10 MHz, $R_S$ = $R_{IN}$ = 50 Ω | | −70 | | dBc |
| HD2 | $V_{OUT}$ = 1 V p-p, f = 1 MHz, $R_S$ = 50 Ω, $R_{FB}$ = ∞ $C_{SH}$ = 0 pF | | −99 | | dBc |
| HD3 | $V_{OUT}$ = 1 V p-p, f = 1 MHz, $R_S$ = 50 Ω, $R_{FB}$ = ∞ $C_{SH}$ = 0 pF | | −100 | | dBc |
| HD2 | $V_{OUT}$ = 1 V p-p, f = 10 MHz, $R_S$ = 50 Ω, $R_{FB}$ = ∞ $C_{SH}$ = 0 pF | | 63 | | dBc |
| HD3 | $V_{OUT}$ = 1 V p-p, f = 10 MHz, $R_S$ = 50 Ω, $R_{FB}$ = ∞ $C_{SH}$ = 0 pF | | 70 | | dBc |
| HD2 | $V_{OUT}$ = 2 V p-p, f = 1 MHz, $R_S$ = $R_{IN}$ = 50 Ω | | −95 | | dBc |
| HD3 | $V_{OUT}$ = 2 V p-p, f = 1 MHz, $R_S$ = $R_{IN}$ = 50 Ω | | −97 | | dBc |
| HD2 | $V_{OUT}$ = 2 V p-p, f = 10 MHz, $R_S$ = $R_{IN}$ = 50 Ω | | −57 | | dBc |
| HD3 | $V_{OUT}$ = 2 V p-p, f = 10 MHz, $R_S$ = $R_{IN}$ = 50 Ω | | −67 | | dBc |
| HD2 | $V_{OUT}$ = 2 V p-p, f = 1 MHz, $R_S$ = 50 Ω, $R_{FB}$ = ∞ $C_{SH}$ = 0 pF | | −93 | | dBc |
| HD3 | $V_{OUT}$ = 1 V p-p, f = 1 MHz, $R_S$ = 50 Ω, $R_{FB}$ = ∞ $C_{SH}$ = 0 pF | | −95 | | dBc |
| HD2 | $V_{OUT}$ = 1 V p-p, f = 10 MHz, $R_S$ = 50 Ω, $R_{FB}$ = ∞ $C_{SH}$ = 0 pF | | −56 | | dBc |
| HD3 | $V_{OUT}$ = 1 V p-p, f = 10 MHz, $R_S$ = 50 Ω, $R_{FB}$ = ∞ $C_{SH}$ = 0 pF | | −64 | | dBc |

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Two-Tone IMD3 Distortion | | | | | |
| 10 MHz | $V_{OUT}$ = 1 V p-p, f 1 = 9.5 MHz, f2 = 10.5 MHz, $R_S = R_{IN}$ = 50 Ω | | −90 | | dBc |
| | $V_{OUT}$ = 1 V p-p, f1 = 9.5 MHz, f2 = 10.5 MHz, $R_S$ = 50 Ω, $R_{FB}$ = ∞, $C_{SH}$ = 0 pF | | −72 | | dBc |
| | $V_{OUT}$ = 2 V p-p, f 1 = 9.5 MHz, f2 = 10.5 MHz, $R_S = R_{IN}$ = 50 Ω | | −73 | | dBc |
| | $V_{OUT}$ = 2 V p-p, f1 = 9.5 MHz, f2 = 10.5 MHz, $R_S$ = 50 Ω, $R_{FB}$ = ∞, $C_{SH}$ = 0 pF | | −63 | | dBc |
| 1 MHz | $V_{OUT}$ = 1 V p-p, f 1 = 0.9 MHz, f2 = 1.1 MHz, $R_S = R_{IN}$ = 50 Ω | | −110 | | dBc |
| | $V_{OUT}$ = 1 V p-p, f1 = 0.9 MHz, f2 = 1.1 MHz, $R_S$ = 50 Ω, $R_{FB}$ = ∞, $C_{SH}$ = 0 pF | | −102 | | dBc |
| | $V_{OUT}$ = 2 V p-p, f 1 = 0.9 MHz, f2 = 1.1 MHz, $R_S = R_{IN}$ = 50 Ω | | −103 | | dBc |
| | $V_{OUT}$ = 2 V p-p, f1 = 0.9 MHz, f2 = 1.1 MHz, $R_S$ = 50 Ω, $R_{FB}$ = ∞, $C_{SH}$ = 0pF | | −98 | | dBc |
| Input 1dB Compression Point | $V_{OUT}$ = 1 V p-p, f = 1 MHz to 10 MHz | | TBD | | dBm |
| Input 1dB Compression Point | $V_{OUT}$ = 2 V p-p, f = 1 MHz to 10 MHz | | TBD | | dBm |
| Output-Third Order Intercept | | | | | |
| | $V_{OUT}$ = 1 V p-p of composite tones, f = 1 MHz | | 36 | | dBV rms |
| | $V_{OUT}$ = 1 V p-p of composite tones, f = 10 MHz | | 27 | | dBV rms |
| | $V_{OUT}$ = 2 V p-p of composite tones, f = 1 MHz | | 41 | | dBV rms |
| | $V_{OUT}$ = 2 V p-p of composite tones, f = 10 MHz | | 26 | | dBV rms |
| | $V_{OUT}$ = 1 V p-p of composite tones, f = 1 MHz, reference to 50 Ω | | 49 | | dBm |
| | $V_{OUT}$ = 1 V p-p of composite tones, f = 10 MHz, reference to 50 Ω | | 40 | | dBm |
| | $V_{OUT}$ = 2 V p-p of composite tones, f = 1 MHz, reference to 50 Ω | | 54 | | dBm |
| | $V_{OUT}$ = 2 V p-p of composite tones, f = 10 MHz, reference to 50 Ω | | 39 | | dBm |
| Crosstalk | $V_{OUT}$ = 1 V p-p, f = 1 MHz | | TBD | | dB |
| DC PERFORMANCE | | | | | |
| Input Offset Voltage | | | 1 | | mV |
| Input Offset Voltage Drift | | | 300 | | μV/°C |
| INPUT CHARACTERISTICS | | | | | |
| Input Voltage Range | AC-coupled | | 1.2 | | V p-p |
| Input Resistance | $R_{FB}$ = 150 Ω, f = 100 kHz | | 50 | | Ω |
| | $R_{FB}$ = 226 Ω, f = 100 kHz | | 75 | | Ω |
| | $R_{FB}$ = 301 Ω, f = 100 kHz | | 100 | | Ω |
| | $R_{FB}$ = 619 Ω, f = 100 kHz | | 200 | | Ω |
| | $R_{FB}$ = 3.57 kΩ, f = 100 kHz | | 1 | | kΩ |
| | $R_{FB}$ = ∞, f = 10 kHz | | 6.2 | | kΩ |
| Input Capacitance | | | 6 | | pF |
| Input Common Mode Voltage | | | 3.3 | | V |
| OUTPUT CHARACTERISTCS | | | | | |
| Output Common-Mode Voltage | | | 2.5 | | V |
| Output Offset Voltage | | | 4 | | mV |
| Output Voltage Swing | | | 4.8 | | V p-p |
| Output Resistance | Single-ended, either output | | | 200 | Ω |
| Output Resistance in Shutdown Mode | Single-ended, either output | 1000 | | | Ω |
| Output Short-Circuit Current | $R_L$ = 1 Ω differential | | 60 | | mA |
| POWER SUPPLY | | | | | |
| Supply Voltage | | 4.5 | 5 | 5.5 | V |
| Quiescent Current | | | 24 | | mA |
| Over Temperature | −40°C < $T_A$ < +85°C | 21 | | 27 | mA |
| Supply Current in Shutdown Mode | ENB = GND | | 44 | | μA |
| Power Dissipation | | | 120 | | mW |
| PSRR | f = 10 kHz | | −82 | | dB |

# ABSOLUTE MAXIMUM RATINGS

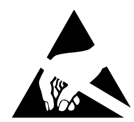
**Table 2.**

| Parameter | Rating |
|---|---|
| Voltage | |
| Supply Voltage | 5.5 V |
| Input Voltage | VPS, COM |
| Power Dissipation | 120 mW |
| Temperature | |
| Operating Temperature | −40°C to +85°C |
| Storage Temperature | −65°C to +150°C |
| Lead Temperature (Soldering, 60 sec) | 300°C |
| Thermal Resistance 24-Lead LFCSP[1] | |
| $\theta_{JA}$ | 57.9°C/W |
| $\theta_{JC}$ | 11.2°C/W |
| $\theta_{JB}$ | 35.9°C/W |
| $\Psi_{JT}$ | 1.1°C/W |

[1] Exposed pad soldered to 4-layer JEDEC Board (2S2P).

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

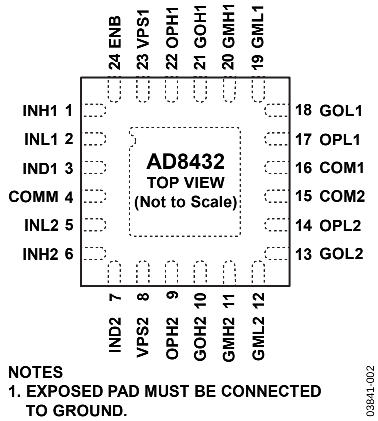



*Figure 2. Pin Configuration*

**Table 3. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | INH1 | Noninverting Input of LNA1 |
| 2 | INL1 | Inverting Input of LNA1 (AC-Coupled to Ground) |
| 3, 7 | IND1, IND2 | Integrated Input Clamping Back-to-Back Diodes |
| 4 | COMM | Input Ground |
| 5 | INL2 | Inverting Input of LNA2 |
| 6 | INH2 | Noninverting Input of LNA2 |
| 8 | VPS2 | 5 V Supply for LNA2 |
| 9 | OPH2 | Noninverting Output of LNA2 |
| 10 | GOH2 | Gain Setting Pin for LNA2 |
| 11 | GMH2 | Gain Setting Pin for LNA2 |
| 12 | GML2 | Gain Setting Pin for LNA2 |
| 13 | GOL2 | Gain Setting Pin for LNA2 |
| 14 | OPL2 | Inverting Output of LNA2 |
| 15 | COM2 | LNA2 Output Ground |
| 16 | COM1 | LNA1 Output Ground |
| 17 | OPL1 | Inverting Output of LNA1 |
| 18 | GOL1 | Gain Setting Pin for LNA1 |
| 19 | GML1 | Gain Setting Pin for LNA1 |
| 20 | GMH1 | Gain Setting Pin for LNA1 |
| 21 | GOH1 | Gain Setting Pin for LNA1 |
| 22 | OPH1 | Noninverting Output of LNA1 |
| 23 | VPS1 | 5 V Supply of LNA1 |
| 24 | ENB | Enable |
| | EPAD | Exposed pad must be connected to ground. |

## TYPICAL PERFORMANCE CHARACTERISTICS

TBD

*Figure 3.*

TBD

*Figure 4.*

TBD

*Figure 5.*

TBD

*Figure 6.*

TBD

*Figure 7.*

TBD

*Figure 8.*

# THEORY OF OPERATION

## LOW NOISE AMPLIFIER (LNA)

A simplified schematic of an LNA is shown in Figure 9. The LNA is driven with a single-ended input and measured differentially at the output. The inverting input INL must be ac-coupled to ground for proper operation. The LNA cannot be driven differentially due to the asymmetry of the internal gain setting resistors. The gain from the inverting input INL to the single-ended output (OPH or OPL) is different from the gain from the noninverting input INH to the single-ended output.

Both inputs are capacitively coupled by the same value capacitor. The dc input bias is 3.3 V, and dc output bias is 2.5 V. The LNA supports a differential output voltage of 4.8 V p-p for the common-mode output voltage of 2.5 V. Therefore, for a differential gain G = 4, the maximum input voltage allowed is 1.2 V p-p.

The clamping technique ensures quick recovery from large input voltages. In addition, the input back-to-back diodes, that are integrated inside the die (IND1 and IND2), should be used for the lowest gain configuration (12.04 dB) to protect the input from overdriving. They should be connected after the source resistance or before INH.

The use of fully differential topology and negative feedback minimizes distortion. A differential signal enables smaller swings at each output that results in reduction of third-order distortion.

The AD8432 is a voltage feedback amplifier. Due to gain bandwidth product (GBW), a decrease in bandwidth should be expected as the gain increases. Table 4 displays the values of −3 dB bandwidth for each gain with unterminated input impedance.

## GAIN SETTING TECHNIQUE

Pin strapping is used to set the gain of the amplifier. Gain setting resistors are integrated in the LNA, with multiple nodes to the resistors available externally. By externally shorting different pins, and thereby shorting or connecting the internal resistors, the AD8432 can be configured for several gains. The single-ended gain from INHx to OPHx (see Figure 9) is defined as

$$G_{OPH-INH} = \frac{R_{G1} + R_{G2} + R_{G3} + R_{G4}}{R_{G1}}$$

By externally shorting the GMHx, GOHx, and OPHx pins, four different gain configurations can be realized.

The single-ended gain from INHx to OPLx is defined as

$$G_{OPL-INH} = -\frac{R_{G5} + R_{G6} + R_{G7}}{R_{G1}}$$

Again, different gain configurations can be realized by externally shorting the GMLx, GOLx, and OPLx pins.

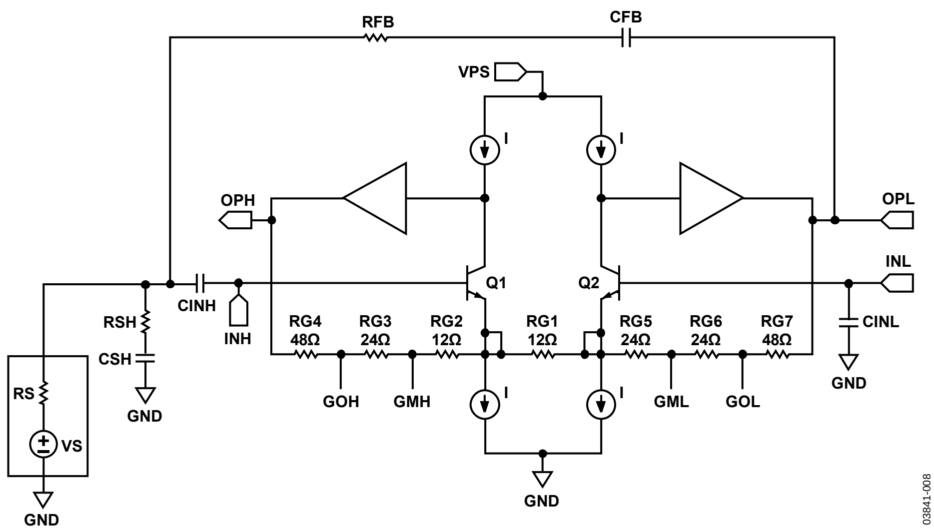



*Figure 9. Simplified Schematic of LNA*

**Table 4. Gain Setting Using Pin-Strapping Technique and −3 dB Bandwidth for Each Gain Configuration**

| Differential Gain (dB) | Single Gain (dB) | RG1 (Ω) | RG2 (Ω) | RG3 (Ω) | RG4 (Ω) | RG5 (Ω) | RG6 (Ω) | RG7 (Ω) | −3 dB BW (Hz) |
|---|---|---|---|---|---|---|---|---|---|
| 12.04 | 6.02 | 12 | 12 | Connect GMH to GOH | Connect GOH to OPH | 24 | Connect GML to GOL | Connect GOL to OPL | 200 M |
| 18.06 | 12.04 | 12 | 12 | 24 | Connect GOH to OPH | 24 | 24 | Connect GOL to OPL | 96 M |
| 21.58 | 15.56 | 12 | 12 | Connect GMH to GOH | 48 | 24 | Connect GML to GOL | 48 | 55 M |
| 24.08 | 18.06 | 12 | 12 | 24 | 48 | 24 | 24 | 48 | 38 M |

The single-ended gain from INHx to OPLx is defined as

$$G_{OPL-INH} = -\frac{R_{G5} + R_{G6} + R_{G7}}{R_{G1}}$$

Again, different gain configurations can be realized by externally shorting the GMLx, GOLx, and OPLx pins.

The values of the seven gain resistors are chosen so that both single-ended gains are equal. For example, to set a gain G = 4 (12.04 dB) differentially, the gain from INHx to each output (OPHx, OPLx) should be ×2 (6.02 dB).

INHx to OPHx: if $R_{G1} = R_G$ and $R_{G2} = R_G$, where $R_G$ = any resistor value, then

$$G_{OPH-INH} = \frac{R_{G1} + R_{G2}}{R_{G1}} = \frac{2 * R_G}{R_G} = 2$$

INHx to OPLx: if $R_{G1} = R_G$ and $R_{G5} = 2 \times R_G$, then

$$G_{OPL-INH} = -\frac{R_{G5}}{R_{G1}} = -\frac{2 * R_G}{R_G} = -2$$

By shorting the different external pins, four gain (4, 8, 12, and 16) configurations can be realized. The gains are set by first selecting a value for $R_{G1}$ and then determining the values of the other resistors in terms of $R_{G1}$, and accordingly shorting the indicated pins.

## ACTIVE INPUT RESISTANCE MATCHING

The AD8432 reduces noise by using active input termination to perform signal source resistance matching. To achieve this, connect a feedback resistor $R_{FB}$ between the INHx and OPLx (see Figure 10). $R_{IN}$ is given in Equation 1, where G/2 is the single-ended gain.

$$R_{IN} = \frac{R_{FB}}{1 + \frac{G}{2}} \quad (1)$$

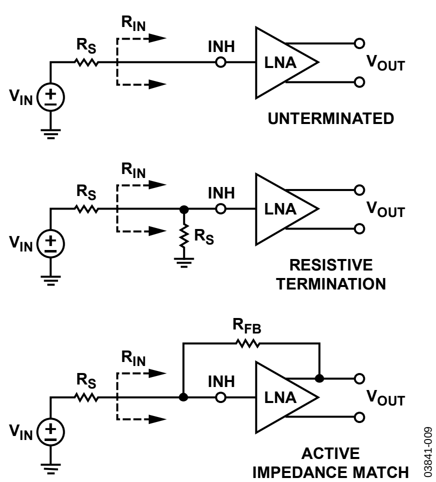



*Figure 10. Input Resistance Matching*

In addition, to further reduce the input resistance, there is an internal resistance of 6.2 kΩ in parallel with the source resistance, such that

$$R_{IN} = \frac{R_{FB}}{1 + \frac{G}{2}} \| R_{INTERNAL} \quad (2)$$

Equation 3 should be used to calculate accurately $R_{FB}$ for a desired input resistance and single-ended gain. Refer to Table 5 for calculated results for $R_{FB}$ for several input resistance and gain combinations.

$$\Rightarrow R_{FB} = \frac{R_{IN}\left(1 + \frac{G}{2}\right)}{1 - \frac{R_{IN}}{R_{INTERNAL}}}, \; R_{INTERNAL} = 6.2\,k\Omega \quad (3)$$

There is a feedback capacitor ($C_{FB}$) in series with $R_{FB}$ because the dc levels of the positive output and the positive input are different. At higher frequencies, the value of the feedback capacitor needs to be considered. The user must determine the level of matching accuracy and adjust $R_{FB}$ accordingly. $C_{SH}$ also enhances the stability at higher frequencies and prevents high peaking especially for the lowest gain, 12.04 dB. (See the Applications Information section for the selection of $C_{SH}$).

The unterminated bandwidth ($R_{FB} = \infty$) is 200 MHz. The LNA has a low input referred voltage noise of 0.8 nV/√Hz at the lowest gain, 12.04 dB (unterminated configuration). To achieve such low noise, the amplifier consumes 21.4 mA, resulting in a power consumption of 107 mW.

The primary purpose of the input impedance matching is to improve the system transient response. With resistive termination, the input noise increases due to the thermal noise of the matching resistor and the increased contribution of the input voltage noise generator of the LNA. With active impedance matching, however, the contributions of both are smaller than they would be for resistive termination by a factor of 1/(1 + LNA Gain).

Table 5. Feedback Resistance for Several $R_{IN}$ and Gain Combinations

| Desired $R_{IN}$ (Ω) | Single-Ended Gain, G/2 (V/V) | Exact $R_{FB}$ (Ω), Equation 2 | $R_{FB}$ (Ω) | Actual $R_{IN}$ (Ω), Equation 2 |
|---|---|---|---|---|
| 50 | 2 | 151.2 | 150 | 49.6 |
| 75 | 2 | 227.8 | 226 | 74.4 |
| 100 | 2 | 304.9 | 301 | 98.7 |
| 200 | 2 | 620 | 619 | 199.7 |
| 1 k | 2 | 3.58 k | 3.57k | 998.4 |
| 50 | 4 | 252 | 250 | 49.6 |
| 100 | 4 | 508.2 | 511 | 100.5 |
| 50 | 6 | 352.9 | 357 | 50.6 |
| 100 | 6 | 711.5 | 715 | 100.5 |
| 50 | 8 | 453.7 | 453 | 49.9 |
| 100 | 8 | 914.8 | 909 | 99.4 |

# APPLICATIONS INFORMATION

The unterminated input impedance of LNA is 6.2 kΩ. Any input resistance between 50 Ω and 6.2 kΩ can be synthesized. When active input termination is used, a decoupling capacitor ($C_{FB}$) is required to isolate the input and output bias voltages of the LNA.

The shunt input capacitor, $C_{SH}$, reduces gain peaking of the lowest gain, 12.04 dB, at higher frequencies. Table 6 shows the required values of $C_{SH}$ and $R_{SH}$ for all four gains for all input impedance combinations. However, the $C_{SH}$ and $R_{SH}$ network can be customized as needed to optimize performance. The $C_{SH}$ is needed only for the lowest gain. In addition, as $R_{IN}$ increases, the value of $C_{SH}$ diminishes, and for higher input impedance values, no capacitor may be required.

The outputs of the AD8432 LNA can be used to drive the differential RFx inputs of the AD8333 I/Q demodulator through 20 Ω resistors.

**Table 6. External Components Selections for Common Input Impedance**

| $R_{IN}$ (Ω) | Gain (dB) | $R_{FB}$ (Ω) | $C_{SH}$ (pF) | $R_{SH}$ (Ω) | −3 dB BW (MHz) |
|---|---|---|---|---|---|
| 50 | 12 | 150 | 47 | 15 | 176 |
| | 18 | 249 | 30 | 15 | 116 |
| | 21 | 357 | None | None | 117 |
| | 24 | 453 | None | None | 87 |
| 75 | 12 | 226 | 36p | 15 | 167 |
| | 18 | 383 | None | None | 144 |
| | 21 | 536 | None | None | 100 |
| | 24 | 681 | None | None | 72 |
| 100 | 12 | 301 | 30p | 15 | 164 |
| | 18 | 511 | None | None | 134 |
| | 21 | 715 | None | None | 90 |
| | 24 | 909 | None | None | 63 |
| 200 | 12 | 619 | 18p | 15 | 164 |
| | 18 | 1.02 k | None | None | 116 |
| | 21 | 1.43 k | None | None | 74 |
| | 24 | 1.87 k | None | None | 51 |
| 1 k | 12 | 3.57 k | 10p | 10 | 160 |
| | 18 | 5.9 k | None | None | 99 |
| | 21 | 8.2 5 k | None | None | 61 |
| | 24 | 10.7 k | None | None | 43 |
| Unterminated, $R_S$ = 50 Ω | 12 | ∞ | None | None | 178 |
| | 18 | ∞ | None | None | 95 |
| | 21 | ∞ | None | None | 59 |
| | 24 | ∞ | None | None | 40 |
| Unterminated, $R_S$ = 0 Ω | 12 | ∞ | None | None | 210 |
| | 18 | ∞ | None | None | 96 |
| | 21 | ∞ | None | None | 55 |
| | 24 | ∞ | None | None | 38 |

# OUTLINE DIMENSIONS

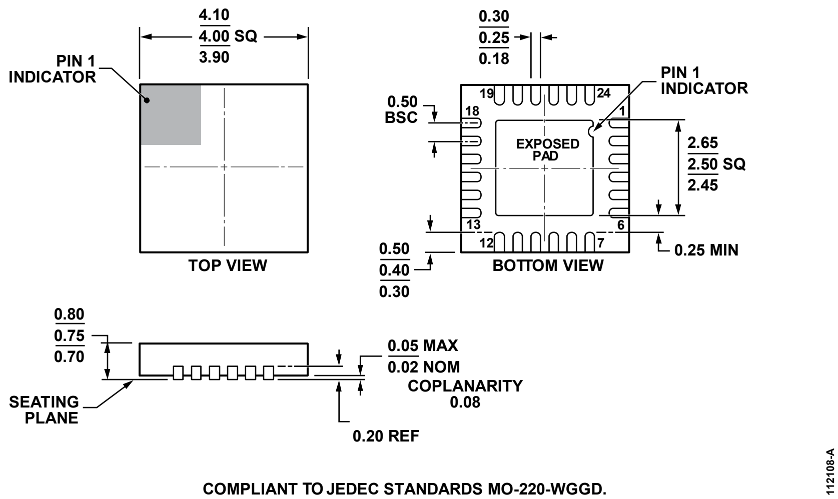



*Figure 11. 24-Lead Lead Frame Chip Scale Package [LFSCP_WQ]*
*4 mm × 4 mm, Very Thin Quad*
*(CP-24-7)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option | Branding |
|---|---|---|---|---|
| AD8432ACPZ[1] | −40°C to +85°C | 24-Lead LFCSP_WQ | CP-24-7 | |
| AD8432ACPZ-R7[1] | -40°C to +85°C | 24-Lead LFCSP_WQ, 7" Tape and Reel | CP-24-7 | |
| AD8432ACPZ-RL[1] | -40°C to +85°C | 24-Lead LFCSP_WQ, 13" Tape and Reel | CP-24-7 | |
| AD8432ACPZ-WP[1] | -40°C to +85°C | 24-Lead LFCSP_WQ, Waffle Pack | CP-24-7 | |
| AD8432-EVALZ[1] | | Evaluation Board | | |

[1] Z = RoHS Compliant Part.