Multiformat HDTV Encoder with Three 11-Bit DACs

ADV7197

FEATURES

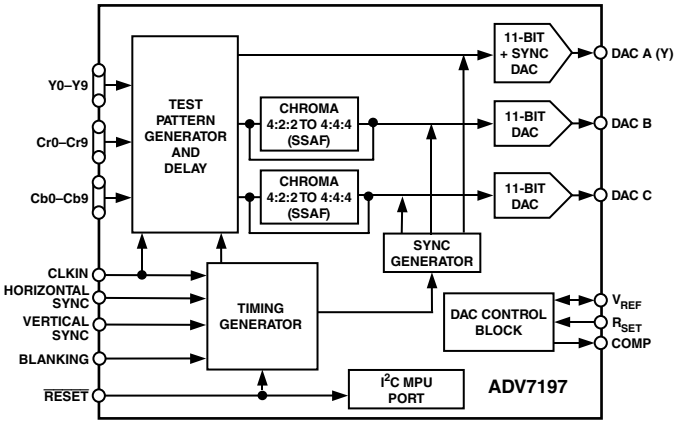
INPUT FORMATS
- YCrCb in 2 × 10-Bit (4:2:2) or 3 × 10-Bit (4:4:4) Format Compliant to SMPTE274M (1080i), SMPTE296M (720p) and Any Other High-Definition Standard Using Async Timing Mode
- RGB in 3 × 10-Bit 4:4:4 Format

OUTPUT FORMATS
- YPrPb HDTV (EIA-770.3)
- RGB Levels Compliant to RS-170 and RS-343A
- 11-Bit + Sync (DAC A)
- 11-Bit DACs (DAC B, C)

PROGRAMMABLE FEATURES
- Internal Test Pattern Generator with Color Control
- Y/C Delay (±)
- Individual DAC On/Off Control
- VBI Open Control
- I^2C Filter
- 2-Wire Serial MPU Interface
- Single Supply 5 V/3.3 V Operation
- 52-Lead MQFP Package

APPLICATIONS
- HDTV Display Devices
- HDTV Projection Systems
- Digital Video Systems
- High Resolution Color Graphics
- Image Processing/Instrumentation
- Digital Radio Modulation/Video Signal Reconstruction

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADV7197 is a triple, high-speed, digital-to-analog encoder on a single monolithic chip. It consists of three high-speed video D/A converters with TTL-compatible inputs.

The ADV7197 has three separate 10-bit-wide input ports that accept data in 4:4:4 10-bit YCrCb or RGB, or 4:2:2 10-bit YCrCb. This data is accepted in HDTV format at 74.25 MHz or 74.1758 MHz. For any other high definition standard but SMPTE274M or SMPTE296M, the Async Timing Mode can be used to input data to the ADV7197. For all standards, external horizontal, vertical, and blanking signals or EAV/SAV codes control the insertion of appropriate synchronization signals into the digital data stream and therefore the output signals.

The ADV7197 outputs analog YPrPb HDTV complying to EIA-770.3, or RGB complying to RS-170/RS-343A.

The ADV7197 requires a single 5 V/3.3 V power supply, an optional external 1.235 V reference, and a 74.25 MHz (or 74.1758 MHz) clock.

The ADV7197 is packaged in a 52-lead MQFP package.

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REV. 0

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ADV7197–SPECIFICATIONS

5 V SPECIFICATIONS[1] (V_{AA} = 4.75 V to 5.25 V, V_{REF} = 1.235 V, R_{SET} = 2470 Ω, R_{LOAD} = 300 Ω. All specifications T_{MIN} to T_{MAX} [0°C to 70°C] unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions
STATIC PERFORMANCE					
Resolution		11		Bits	
Integral Nonlinearity		1.5		LSB	
Differential Nonlinearity		0.9	2.0	LSB	Guaranteed Monotonic
DIGITAL OUTPUTS					
Output High Voltage, V_{OH}	2.4			V	I_{SOURCE} = 400 μA
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 3.2 mA
Three-State Leakage Current			10	μA	V_{IN} = 0.4 V
Three-State Output Capacitance		4		pF	
DIGITAL AND CONTROL INPUTS					
Input High Voltage, V_{IH}	2.0			V	
Input Low Voltage, V_{IL}			0.8	V	
Input Leakage Current		0	1	μA	V_{IN} = 0.4 V or 2.4 V
Input Capacitance, C_{IN}		4		pF	
ANALOG OUTPUTS					
Full-Scale Output Current	3.92	4.25	4.56	mA	DAC A
	2.54	2.83	3.11	mA	DAC B, C
Output Current Range	3.92	4.25	4.56	mA	DAC A
	2.39	2.66	2.93	mA	DAC B, C
DAC-to-DAC Matching		1.4		%	DAC A, B, C
Output Compliance Range, V_{OC}		1.4		V	
Output Impedance, R_{OUT}		100		kΩ	
Output Capacitance, C_{OUT}		7		pF	
VOLTAGE REFERENCE (External and Internal)					
Reference Range, V_{REF}	1.112	1.235	1.359	V	
POWER REQUIREMENTS					
I_{DD}[2]		96	102	mA	With f_{CLK} = 74.25 MHz
I_{AA}[3, 4]		11	15	mA	
Power Supply Rejection Ratio		0.01		%/%	

NOTES

[1]Guaranteed by characterization.

[2]I_{DD} or the circuit current is the continuous current required to drive the digital core.

[3]I_{AA} is the total current required to supply all DACs including V_{REF} circuitry.

[4]All DACs on.

Specifications subject to change without notice.

3.3 V SPECIFICATIONS[1] (V_{AA} = 3.15 V to 3.45 V, V_{REF} = 1.235 V, R_{SET} = 2470 Ω, R_{LOAD} = 300 Ω. All specifications T_{MIN} to T_{MAX} [0°C to 70°C] unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions
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Resolution		11		Bits	
Integral Nonlinearity		1.5		LSB	
Differential Nonlinearity		0.9	2.0	LSB	
DIGITAL OUTPUTS					
Output High Voltage, V_{OH}	2.4			V	I_{SOURCE} = 400 µA
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 3.2 mA
Three-State Leakage Current			10	µA	V_{IN} = 0.4 V
Three-State Output Capacitance		4		pF	
DIGITAL AND CONTROL INPUTS					
Input High Voltage, V_{IH}	2			V	
Input Low Voltage, V_{IL}		0.8	0.65	V	
Input Leakage Current		0	1	µA	V_{IN} = 0.4 V or = 2.4 V
Input Capacitance, C_{IN}		4		pF	
ANALOG OUTPUTS					
Full-Scale Output Current	3.92	4.25	4.56	mA	DAC A
	2.54	2.83	3.11	mA	DAC B, C
Output Current Range	3.92	4.25	4.56	mA	DAC A
	2.39	2.66	2.93	mA	DAC B, C
DAC-to-DAC Matching		1.4		%	DAC A, B, C
Output Compliance Range, V_{OC}	0	1.4		V	
Output Impedance, R_{OUT}		100		kΩ	
Output Capacitance, C_{OUT}		7		pF	
VOLTAGE REFERENCE (External)					
Reference Range, V_{REF}	1.112	1.235	1.359	V	
POWER REQUIREMENTS					
I_{DD}[2]		46		mA	With f_{CLK} = 74.25 MHz
I_{AA}[3, 4]		11	15	mA	
Power Supply Rejection Ratio		0.01		%/%	

NOTES
[1]Guaranteed by characterization.
[2]I_{DD} or the circuit current is the continuous current required to drive the digital core.
[3]I_{AA} is the total current required to supply all DACs including V_{REF} circuitry.
[4]All DACs on.

Specifications subject to change without notice.

ADV7197–SPECIFICATIONS

5 V DYNAMIC–SPECIFICATIONS

(V_{AA} = 4.75 V to 5.25 V, V_{REF} = 1.235 V, R_{SET} = 2470 Ω, R_{LOAD} = 300 Ω. All specifications T_{MIN} to T_{MAX} [0°C to 70°C] unless otherwise noted.)

Parameter	Min	Typ	Max	Unit
Luma Bandwidth		13.5		MHz
Chroma Bandwidth		6.75		MHz
Signal-to-Noise Ratio		64		dB Luma Ramp Unweighted
Chroma/Luma Delay Inequality		0		ns

Specifications subject to change without notice.

3.3 V DYNAMIC–SPECIFICATIONS

(V_{AA} = 3.15 V to 3.45 V, V_{REF} = 1.235 V, R_{SET} = 2470 Ω, R_{LOAD} = 300 Ω. All specifications T_{MIN} to T_{MAX} [0°C to 70°C] unless otherwise noted.)

Parameter	Min	Typ	Max	Unit
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Chroma Bandwidth		6.75		MHz
Signal-to-Noise Ratio		64		dB Luma Ramp Unweighted
Chroma/Luma Delay Inequality		0		ns

Specifications subject to change without notice.

5 V TIMING–SPECIFICATIONS

(V_{AA} = 4.75 V to 5.25 V, V_{REF} = 1.235 V, R_{SET} = 2470 Ω, R_{LOAD} = 300 Ω. All specifications T_{MIN} to T_{MAX} [0°C to 70°C] unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Conditions
MPU PORT[1]					
SCLOCK Frequency	10		400	kHz	
SCLOCK High Pulsewidth, t_1	0.6			µs	
SCLOCK Low Pulsewidth, t_2	1.3			µs	
Hold Time (Start Condition), t_3	0.6			µs	After This Period the 1st Clock Is Generated
Setup Time (Start Condition), t_4	0.6			µs	Relevant for Repeated Start Condition
Data Setup Time, t_5	100			ns	
SDATA, SCLOCK Rise Time, t_6			300	ns	
SDATA, SCLOCK Fall Time, t_7			300	ns	
Setup Time (Stop Condition), t_8	0.6			µs	
$\overline{\text{RESET}}$ Low Time	100			ns	
ANALOG OUTPUTS					
Analog Output Delay[2]		10		ns	
Analog Output Skew		0.5		ns	
CLOCK CONTROL AND PIXEL PORT[3]					
f_{CLK}			74.25	MHz	HDTV Mode
t_{CLK}			81	MHz	Async Timing Mode
Clock High Time, t_9	5	1.5		ns	
Clock Low Time, t_{10}	5	2.0		ns	
Data Setup Time, t_{11}	2.0			ns	
Data Hold Time, t_{12}	4.5			ns	
Control Setup Time, t_{11}	7			ns	
Control Hold Time, t_{12}	4.0			ns	
Pipeline Delay		16		Clock Cycles	For 4:4:4 Pixel Input Format

NOTES
[1]Guaranteed by characterization.
[2]Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of DAC output full-scale transition.
[3]Data: Cb/Cr (9:0), Cr (9:0), Y (9:0); Control: $\overline{\text{HSYNC}}$/$\overline{\text{SYNC}}$, $\overline{\text{VSYNC}}$/TSYNC; DV

Specifications subject to change without notice.

3.3 V TIMING–SPECIFICATIONS

(V_{AA} = 3.15 V to 3.45 V, V_{REF} = 1.235 V, R_{SET} = 2470 Ω, R_{LOAD} = 300 Ω. All specifications T_{MIN} to T_{MAX} [0°C to 70°C] unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Conditions
MPU PORT[1]					
SCLOCK Frequency	10		400	kHz	
SCLOCK High Pulsewidth, t_1	0.6			µs	
SCLOCK Low Pulsewidth, t_2	1.3			µs	
Hold Time (Start Condition), t_3	0.6			µs	After This Period the 1st Clock Is Generated
Setup Time (Start Condition), t_4	0.6			µs	Relevant for Repeated Start Condition
Data Setup Time, t_5	100			ns	
SDATA, SCLOCK Rise Time, t_6			300	ns	
SDATA, SCLOCK Fall Time, t_7			300	ns	
Setup Time (Stop Condition), t_8	0.6			µs	
$\overline{\text{RESET}}$ Low Time	100			ns	
ANALOG OUTPUTS[2]					
Analog Output Delay		10		ns	
Analog Output Skew		0.5		ns	
CLOCK CONTROL AND PIXEL PORT[3]					
f_{CLK}			74.25	MHz	HDTV Mode
t_{CLK}			81	MHz	Async Timing Mode
Clock High Time, t_9	5	1.5		ns	
Clock Low Time, t_{10}	5	2.0		ns	
Data Setup Time, t_{11}	2.0			ns	
Data Hold Time, t_{12}	4.5			ns	
Control Setup Time, t_{11}	7			ns	
Control Hold Time, t_{12}	4.0			ns	
Pipeline Delay		16		Clock Cycles	For 4:4:4 Pixel Input Format

NOTES
[1]Guaranteed by characterization.
[2]Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of DAC output full-scale transition.
[3]Data: Cb/Cr (9:0), Cr (9:0), Y (9:0); Control: $\overline{\text{HSYNC}}$/$\overline{\text{SYNC}}$, $\overline{\text{VSYNC}}$/TSYNC; DV

Specifications subject to change without notice.

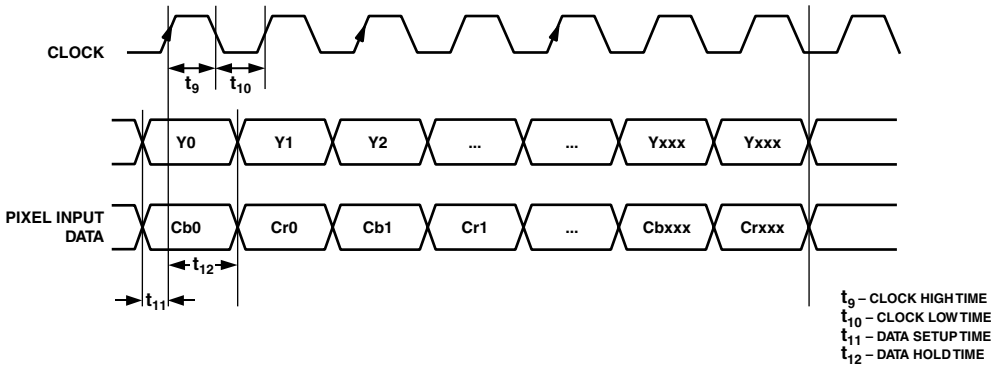


Figure 1. 4:2:2 Input Data Format Timing Diagram

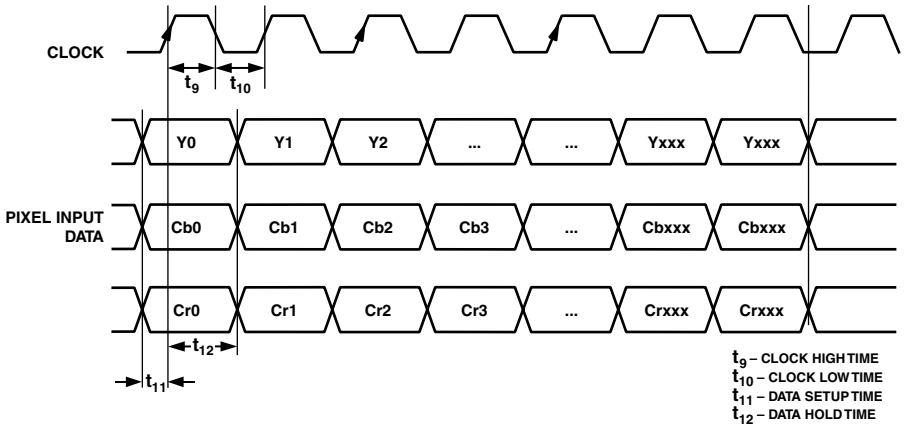


Figure 2. 4:4:4 YCrCb Input Data Format Timing Diagram

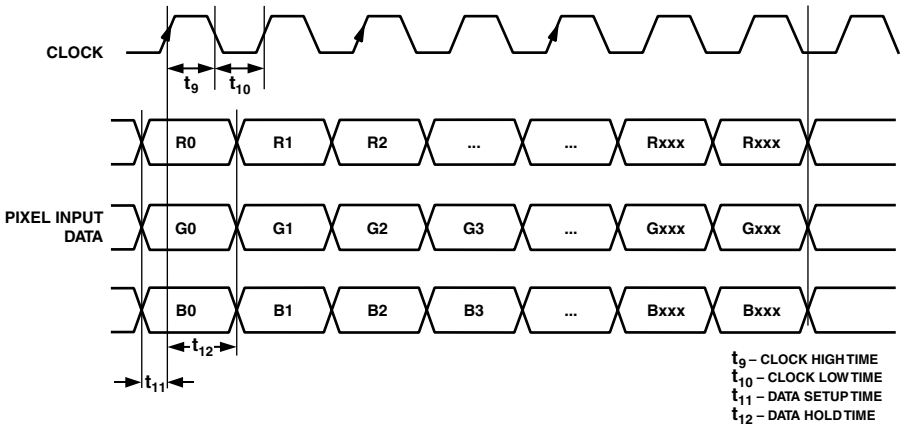


Figure 3. 4:4:4 RGB Input Data Format Timing Diagram

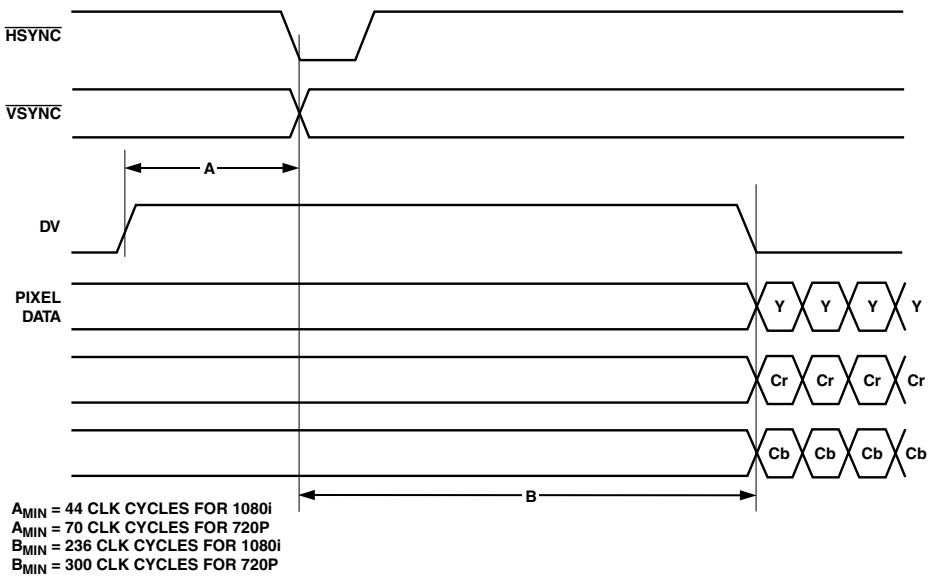


Figure 4. Input Timing Diagram

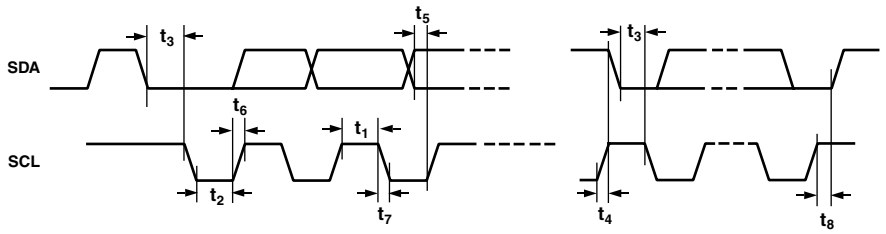


Figure 5. MPU Port Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]

V_{AA} to GND . . . . . 7 V
Voltage on Any Digital Pin . . . . GND – 0.5 V to V_{AA} + 0.5 V
Ambient Operating Temperature (T_A) . . . . . –40°C to +85°C
Storage Temperature (T_S) . . . . . –65°C to +150°C
Junction Temperature (T_J) . . . . . 150°C
Infrared Reflow Soldering (20 secs) . . . . . 225°C
Vapor Phase Soldering (1 minute) . . . . . 220°C
I_{OUT} to GND[2] . . . . . 0 V to V_{AA}

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Analog Output Short Circuit to any Power Supply or Common can be of an indefinite duration.

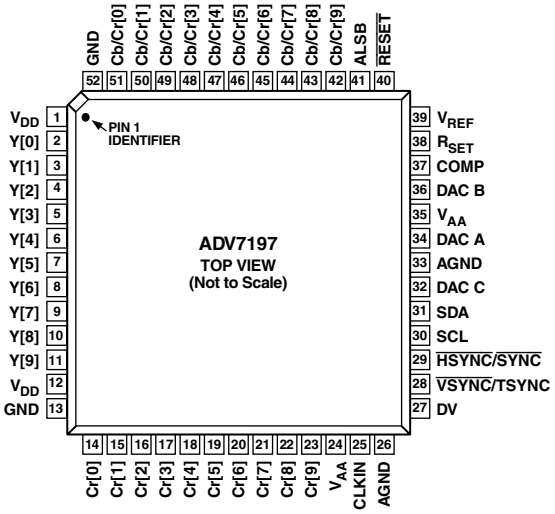
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADV7197KST	0°C to 70°C	Plastic Quad Flatpack (MQFP)	S-52

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV7197 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Input/Output	Function
1, 12	V_{DD}	P	Digital Power Supply.
2–11	Y0–Y9	I	10-Bit HDTV Input Port for Y Data. G data input in RGB mode.
13, 52	GND	G	Digital Ground
14–23	Cr0–Cr9	I	10-Bit HDTV Input Port for Color Data in 4:4:4 Input Mode. In 4:2:2 mode this input port is not used. R data input in RGB mode.
24, 35	V_{AA}	P	Analog Power Supply.
25	CLKIN	I	Pixel Clock Input. Requires a 74.25 MHz (74.1758 MHz) reference clock.
26, 33	AGND	G	Analog Ground
27	DV	I	Video Blanking Control Signal Input.
28	$\overline{\text{VSYNC}}$/ TSYNC	I	$\overline{\text{VSYNC}}$, vertical sync control signal input or TSYNC input control signal in Async Timing Mode.
29	$\overline{\text{HSYNC}}$/ $\overline{\text{SYNC}}$	I	$\overline{\text{HSYNC}}$, horizontal sync control signal input or $\overline{\text{SYNC}}$ input control signal in Async Timing Mode.
30	SCL	I	MPU Port Serial Interface Clock Input.
31	SDA	I/O	MPU Port Serial Data Input/Output.
32	DAC C	O	Color component analog output of input data on Cb/Cr9–0 input pins.
34	DAC A	O	Y Analog Output.
36	DAC B	O	Color component analog output of input data on Cr9–Cr0 input pins.
37	COMP	O	Compensation Pin for DACs. Connect 0.1 μF Capacitor from COMP pin to V_{AA}.
38	R_{SET}	I	A 2470 Ω resistor (for input ranges 64–940 and 64–960, output standards EIA-770.3) must be connected from this pin to ground and is used to control the amplitudes of the DAC outputs. For input ranges 0–1023 (output standards RS-170, RS-343A) the R_{SET} value must be 2820 Ω.
39	V_{REF}	I/O	Optional External Voltage Reference Input for DACs or Voltage Reference Output (1.235 V).
40	$\overline{\text{RESET}}$	I	This input resets the on-chip timing generator and sets the ADV7197 into Default Register setting. Reset is an active low signal.
41	ALSB	I	TTL Address Input. This signal sets up the LSB of the MPU address. When this pin is tied high, the I^2C filter is activated which reduces noise on the I^2C interface. When this pin is tied low, the input bandwidth on the I^2C interface is increased.
42–51	Cb/Cr9–0	I	10-Bit HDTV Input Port for Color Data. In 4:2:2 mode the multiplexed CrCb data must be input on these pins. B data input in RGB mode.

FUNCTIONAL DESCRIPTION

Digital Inputs

The digital inputs of the ADV7197 are TTL-compatible. 30-bit YCrCb or RGB pixel data in 4:4:4 format or 20-bit YCrCb pixel data in 4:2:2 format is latched into the device on the rising edge of each clock cycle at 74.25 MHz or 74.1758 in HDTV mode. It is recommended to input data in 4:2:2 mode to make use of the Chroma SSAFs on the ADV7197. As can be seen in the figures below, these filters have 0 dB passband response and prevent signal components being folded back into the frequency band. In 4:4:4 input mode, the video data is already interpolated by an external input device and the chroma SSAFs of the ADV7197 are bypassed.

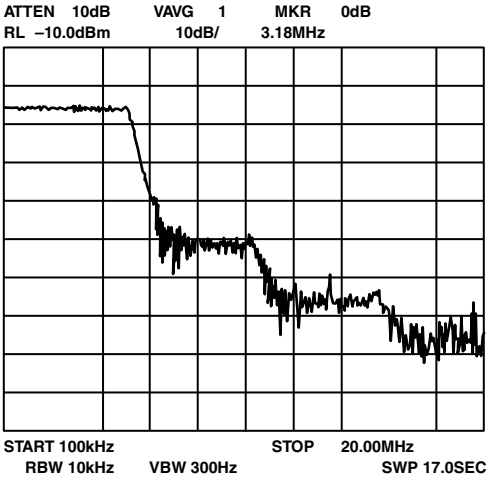


Figure 6. SSAF Response to a 2.5 MHz Chroma Sweep Using 4:2:2 Input Mode

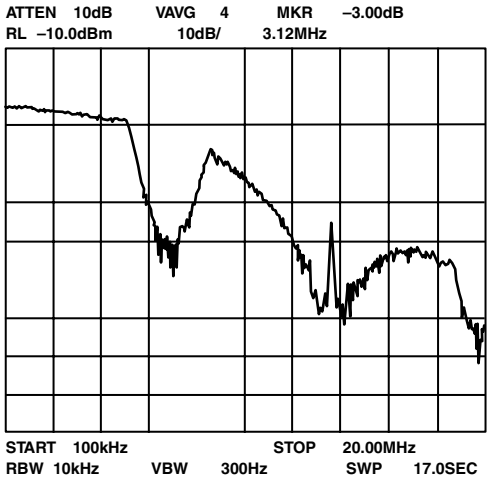


Figure 7. Conventional Filter Response to a 2.5 MHz Chroma Sweep Using 4:4:4 Input Mode

Control Signals

The ADV7197 accepts sync control signals accompanied by valid 4:2:2 or 4:4:4 data. These external horizontal, vertical and blanking pulses (or EAV/SAV codes) control the insertion of appropriate sync information into the output signals.

Analog Outputs

The analog Y signal is output on the 11-bit + Sync DAC A, the color component analog signals on the 11-bit DACs B, C conforming to EIA-770.3 standards R_{SET} has a value of 2470 Ω (EIA-770.3), R_{LOAD} has a value of 300 Ω. For the outputs to conform to RS-170/RS-343A standards R_{SET} must have a value of 2820 Ω.

Internal Test Pattern Generator

The ADV7197 can generate a Cross-Hatch pattern (white lines against a black background). Additionally, the ADV7197 can output a uniform color pattern. The color of the lines or uniform field/frame can be programmed by the user.

Y/CrCb Delay

The Y output and the color component outputs can be delayed wrt the falling edge of the horizontal sync signal by up to four clock cycles.

I^2C Filter

A selectable internal I^2C filter allows significant noise reduction on the I^2C interface. For setting ALSB high, the input bandwidth on the I^2C lines is reduced and pulses of less than 50 ns are not passed to the I^2C controller. Setting ALSB low allows greater input bandwidth on the I^2C lines.

MPU PORT DESCRIPTION

The ADV7197 support a 2-wire serial (I^2C-compatible) microprocessor bus driving multiple peripherals. Two inputs Serial Data (SDA) and Serial Clock (SCL) carry information between any device connected to the bus. Each slave device is recognized by a unique address. The ADV7197 has four possible slave addresses for both read and write operations. These are unique addresses for each device and are illustrated in Figure 8. The LSB sets either a read or write operation. Logic Level "1" corresponds to a read operation while Logic Level "0" corresponds to a write operation. A1 is set by setting the ALSB pin of the ADV7197 to Logic Level "0" or Logic Level "1." When ALSB is set to "0," there is greater input bandwidth on the I^2C lines, which allows high-speed data transfers on this bus. When ALSB is set to "1," there is reduced input bandwidth on the I^2C lines, which means that pulses of less than 50 ns will not pass into the I^2C internal controller. This mode is recommended for noisy systems.

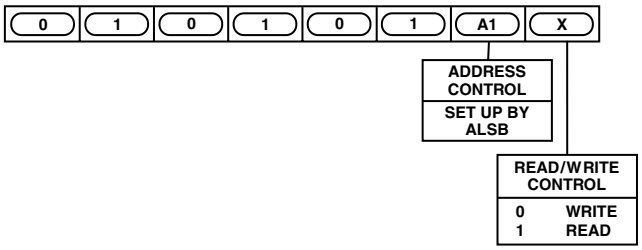


Figure 8. Slave Address

To control the various devices on the bus the following protocol must be followed. First the master initiates a data transfer by establishing a Start condition, defined by a high-to-low transition on SDA while SCL remains high. This indicates that an address/data stream will follow. All peripherals respond to the Start condition and shift the next eight bits (7-bit address + R/$\overline{W}$ bit). The bits are transferred from MSB down to LSB. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an Acknowledge Bit. All other devices withdraw from the bus at this point and maintain an idle condition. The idle condition is where the device monitors the SDA and SCL lines waiting for the Start condition and the correct transmitted address. The R/$\overline{W}$ bit determines the direction of the data.

A Logic "0" on the LSB of the first byte means that the master will write information to the peripheral. A Logic "1" on the LSB of the first byte means that the master will read information from the peripheral.

The ADV7197 acts as a standard slave device on the bus. The data on the SDA pin is 8 bits long supporting the 7-bit addresses plus the R/$\overline{W}$ bit. It interprets the first byte as the device address and the second byte as the starting subaddress. The subaddresses auto-increment, allowing data to be written to or read from the starting subaddress. A data transfer is always terminated by a Stop condition. The user can also access any unique subaddress register on a one-by-one basis without having to update all the registers.

Stop and Start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, they cause an immediate jump to the idle condition. During a given SCL high period the user should issue only one Start condition, one Stop condition or a single Stop condition followed by a single Start condition. If an invalid subaddress is issued by the user, the ADV7197 will not issue an acknowledge and will return to the idle condition. If in auto-increment mode, the user exceeds the highest subaddress, the following action will be taken:

1. In Read Mode, the highest subaddress register contents will continue to be output until the master device issues a no-acknowledge. This indicates the end of a read. A no-acknowledge condition is where the SDA line is not pulled low on the ninth pulse.
2. In Write Mode, the data for the invalid byte will be not be loaded into any subaddress register, a no-acknowledge will be issued by the ADV7197 and the part will return to the idle condition.

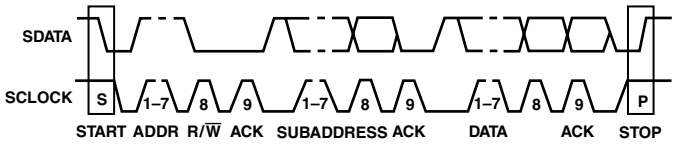


Figure 9. Bus Data Transfer

Figure 9 illustrates an example of data transfer for a read sequence and the Start and Stop conditions.

Figure 10 shows bus write and read sequences.

REGISTER ACCESSES

The MPU can write to or read from all of the registers of the ADV7197 except the Subaddress Registers, which are write-only registers. The Subaddress Register determines which register is accessed by the next read or write operation.

All communications with the part through the bus begin with an access to the Subaddress Register. A read/write operation is performed from/to the target address which then increments to the next address until a Stop command on the bus is performed.

REGISTER PROGRAMMING

The following section describes the functionality of each register. All registers can be read from as well as written to unless otherwise stated.

Subaddress Register (SR7–SR0)

The Communications Register is an eight bit write-only register. After the part has been accessed over the bus and a read/write operation is selected, the subaddress is set up. The Subaddress Register determines to/from which register the operation takes place.

Figure 11 shows the various operations under the control of the Subaddress Register. "0" should always be written to SR7.

Register Select (SR6–SR0)

These bits are set up to point to the required starting address.

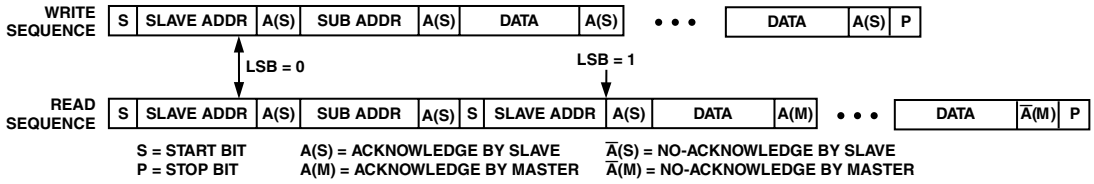


Figure 10. Write and Read Sequence

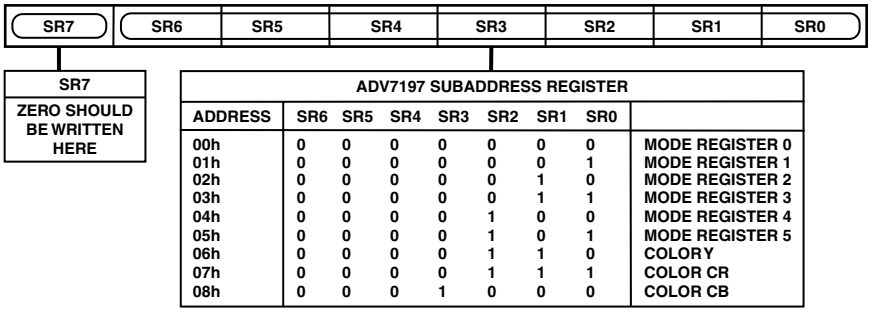


Figure 11. Subaddress Registers

MODE REGISTER 0
MR0 (MR07–MR00)
(Address (SR4–SR0) = 00H)
Figure 14 shows the various operations under the control of Mode Register 0.

MR0 BIT DESCRIPTION
Output Standard Selection (MR00–MR01)
These bits are used to select the output levels from the ADV7197.

If EIA 770.3 (MR01–00 = "00") is selected, the output levels will be: 0 mV for blanking level, 700 mV for peak white (Y channel), ±350 mV for Pr, Pb outputs and –300 mV for tri-level sync.

If Full Input Range (MR01–00 = "10") is selected, the output levels will be 700 mV for peak white for the Y channel, ±350 mV for Pr, Pb outputs, and –300 mV for Sync. This mode is used for RS-170, RS-343A standard output compatibility.

Sync insertion on the Pr, Pb channels is optional. For output levels refer to the Appendix.

Input Control Signals (MR02–MR03)
These control bits are used to select whether data is input with external horizontal, vertical, and blanking sync signals or if the data is input with embedded EAV/SAV codes. An Asynchronous timing mode is also available using TSYNC, $\overline{\text{SYNC}}$ and DV as input control signals.

These timing control signals have to be programmed by the user and are used for any other high definition standard input but SMPTE274M and SMPTE296M.

Figure 12 shows an example of how to program the ADV7197 to accept a different high definition standard but SMPTE274M or SMPTE296M.

Reserved (MR04)
A "0" must be written to this bit.

Input Standard (MR05)
Select between 1080i or 720p input.

DV Polarity (MR06)
This control bit allows to select the polarity of the DV input control signal to be either active high or active low. This is in order to facilitate interfacing from input devices which use an active high blanking signal output.

Reserved (MR07)
A "0" must be written to this bit.

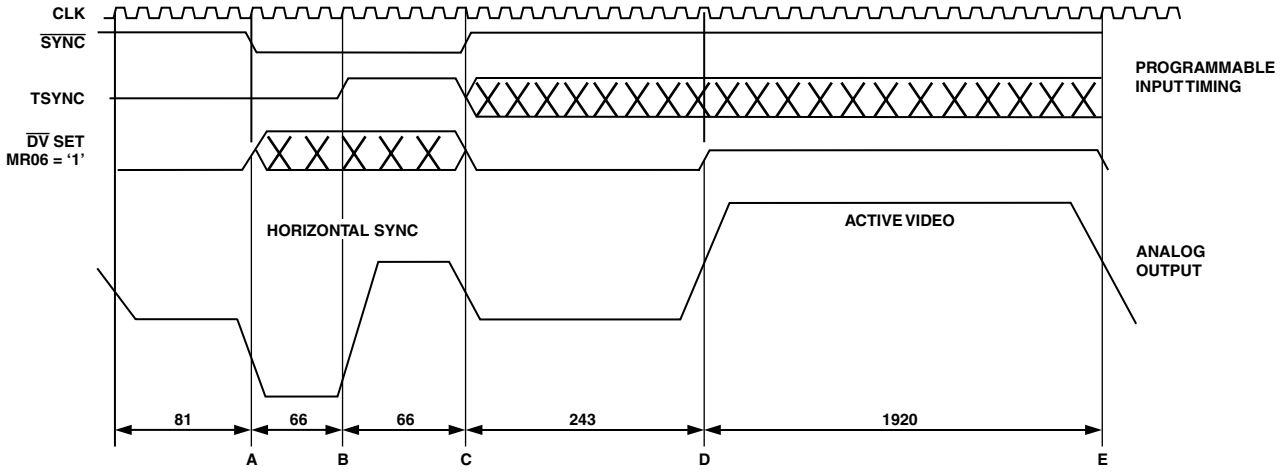


Figure 12. Async Timing Mode—Programming Input Control Signals for SMPTE295M Compatibility

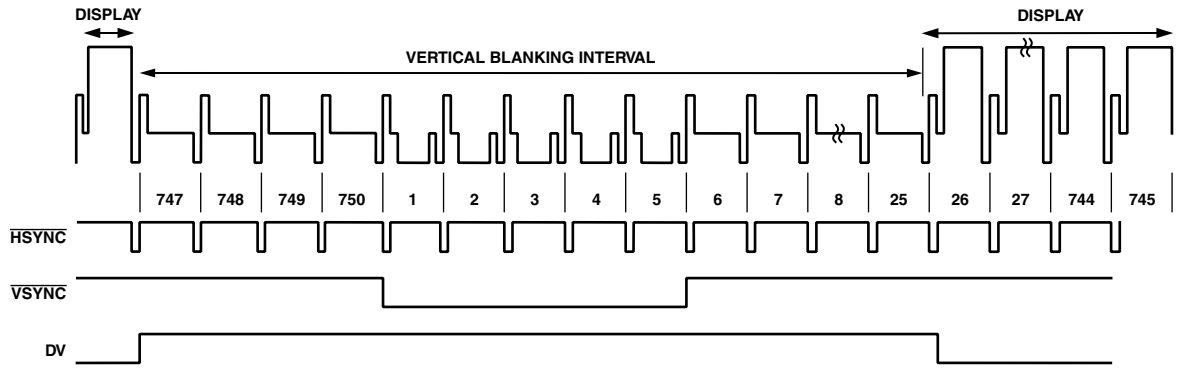


Figure 13. DV Input Control Signal in Relation to Video Output Signal for SMPTE296M (720p)

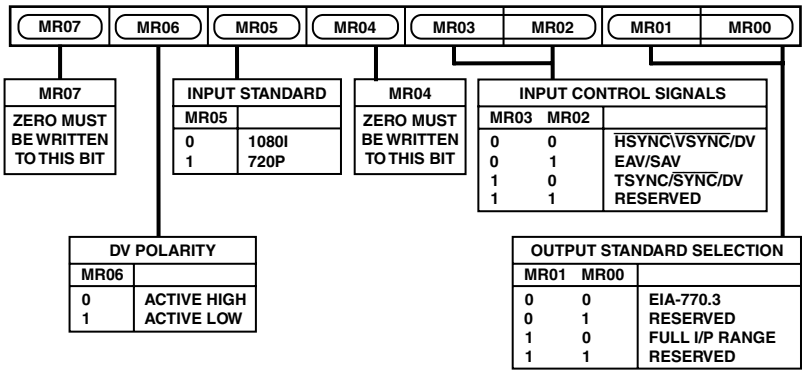


Figure 14. Mode Register 0

Table I must be followed when programming the control signals in Async Timing Mode.

Table I. Truth Table

$\overline{SYNC}$	TSYNC	DV	
1 –> 0	0	0 or 1	50% Point of Falling Edge of Tri-Level Horizontal Sync Signal, a
0	0 –> 1	0 or 1	25% Point of Rising Edge of Tri-Level Horizontal Sync Signal, b
0 –> 1	0 or 1	0	50% Point of Falling Edge of Tri-Level Horizontal Sync Signal, c
1	0 or 1	0 –> 1	50% Start of Active Video, d
1	0 or 1	1 –> 0	50% End of Active Video, e

MODE REGISTER 1
MR1 (MR17–MR10)
(Address (SR4–SR0) = 01H)
Figure 15 shows the various operations under the control of Mode Register 1.

MR1 BIT DESCRIPTION
Pixel Data Enable (MR10)
When this bit is set to "0," the pixel data input to the ADV7197 is blanked such that a black screen is output from the DACs.

When this bit is set to "1," pixel data is accepted at the input pins and the ADV7197 outputs to the standard set in "Output Standard Selection" (MR01–MR00). This bit also must be set to "1" to enable output of the test pattern signals.

Input Format (MR11)
It is possible to input data in 4:2:2 format or in 4:4:4 format.

Test Pattern Enable (MR12)
Enables or disables the internal test pattern generator.

Test Pattern Hatch/Frame (MR13)
If this bit is set to "0," a cross hatch test pattern is output from the ADV7197. The cross hatch test pattern can be used to test monitor convergence.

If this bit is set to "1," a uniform colored frame/field test pattern is output from the ADV7197.

The color of the lines or the frame/field is by default white but can be programmed to be any color using the Color Y, Color Cr, Color Cb Registers.

VBI Open (MR14)
This bit enables or disables the facility of VBI data insertion during the Vertical Blanking Interval.

For this purpose Lines 7–20 in 1080i and Lines 6–25 in 720p can be used for VBI data insertion.

Reserved (MR15–MR17)
A "0" must be written to these bits.

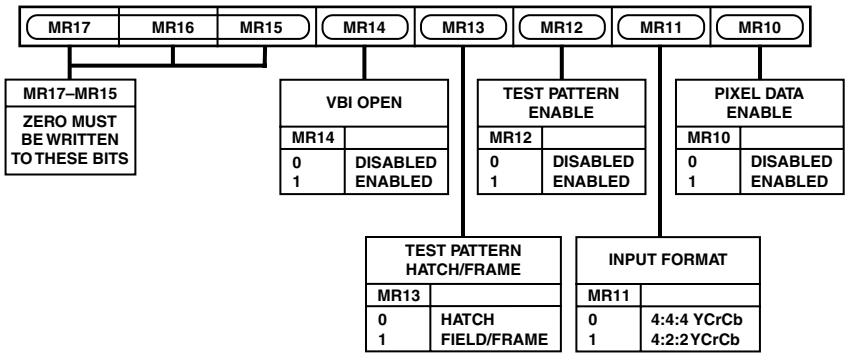


Figure 15. Mode Register 1

MODE REGISTER 2
MR1 (MR27–MR20)
(Address (SR4–SR0) = 02H)
Figure 17 shows the various operations under the control of Mode Register 2.

MR2 BIT DESCRIPTION
Y Delay (MR20–MR22)
With these bits it is possible to delay the Y signal with respect to the falling edge of the horizontal sync signal by up to four pixel clock cycles. Figure 16 demonstrates this facility.

Color Delay (MR23–MR25)
With theses bits it is possible to delay the color signals with respect to the falling edge of the horizontal sync signal by up to four pixel clock cycles. Figure 16 demonstrates this facility.

Reserved (MR26–MR27)
A "0" must be written to these bits.

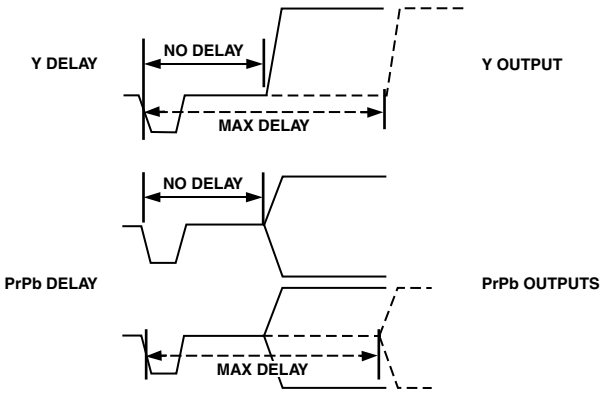


Figure 16. Y and Color Delay

MODE REGISTER 3
MR3 (MR37–MR30)
(Address (SR4–SR0) = 03H)
Figure 18 shows the various operations under the control of Mode Register 3.

MR3 BIT DESCRIPTION
Reserved (MR31–MR32)
A "0" must be written to these bits.

DAC A Control (MR33)
Setting this bit to "1" enables DAC A, otherwise this DAC is powered down.

DAC B Control (MR34)
Setting this bit to "1" enables DAC B, otherwise this DAC is powered down.

DAC C Control (MR35)
Setting this bit to "1" enables DAC C, otherwise this DAC is powered down.

Reserved (MR36–MR37)
A "0" must be written to these bits.

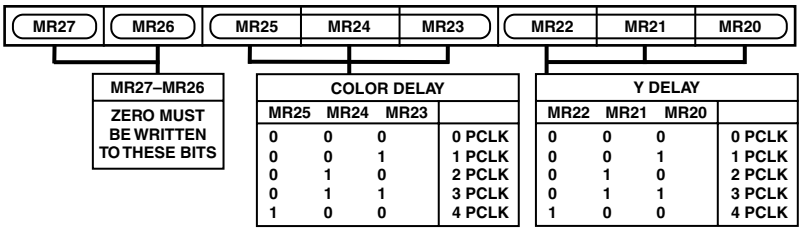


Figure 17. Mode Register 2

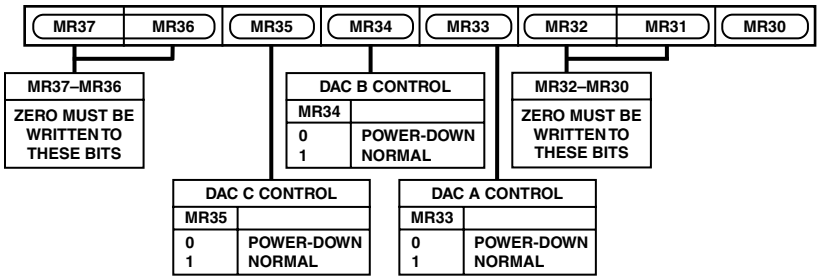


Figure 18. Mode Register 3

MODE REGISTER 4
MR4 (MR47–MR40)
(Address (SR4–SR0) = 04H)
Figure 19 shows the various operations under the control of Mode Register 4.

MR4 BIT DESCRIPTION
Timing Reset (MR40)
Toggling MR40 from low to high and low again resets the internal horizontal and vertical timing counters.

MODE REGISTER 5
MR5 (MR57–MR50)
(Address (SR4-SR0) = 05H)
Figure 20 shows the various operations under the control of Mode Register 5.

MR5 BIT DESCRIPTION
Reserved (MR50)
This bit is reserved for the revision code.

RGB Mode (MR51)
When RGB mode is enabled (MR51 = "1") the ADV7197 accepts unsigned binary RGB data at its input port. This control is also available in Async Timing Mode.

Sync on PrPb (MR52)
By default the color component output signals Pr, Pb do not contain any horizontal sync pulses. They can be inserted when MR52 = "1."

This control is not available in RGB mode.

Color Output Swap (MR53)
By default DAC B is configured as the Pr output and DAC C as the Pb output. In setting this bit to "1" the DAC outputs can be swapped around so that DAC B outputs Pb and DAC C outputs Pr. The table below demonstrates this in more detail. This control is also available in RGB mode.

Reserved (MR54–MR57)
A "0" must be written to these bits.

Table II. Relationship Between Color Input Pixel Port, MR53 and DAC B, DAC C Outputs

In 4:4:4 Input Mode

Color Data Input on Pins	MR53	Analog Output Signal
Cr9–0	0	DAC B
Cb/Cr9–0	0	DAC C
Cr9–0	1	DAC C
Cb/Cr9–0	1	DAC B

In 4:2:2 Input Mode

Color Data Input on Pins	MR53	Analog Output Signal
Cr9–0	0 or 1	Not Operational
Cb/Cr9–0	0	DAC C (Pb)
Cb/Cr9–0	1	DAC C (Pr)

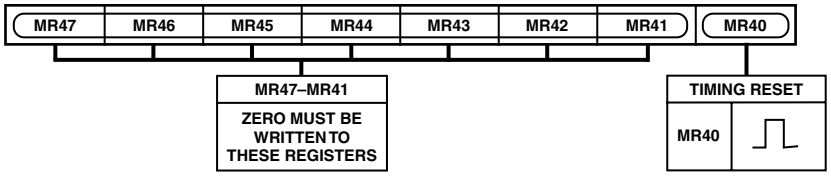


Figure 19. Mode Register 4

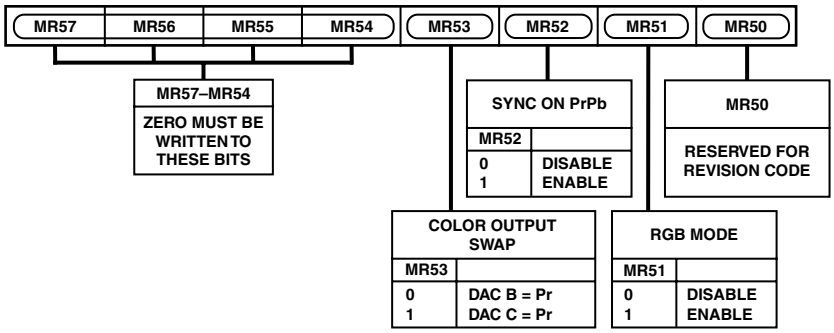


Figure 20. Mode Register 5

COLOR Y
CY (CY7–CY0)
(Address (SR4–SR0) = 06H)

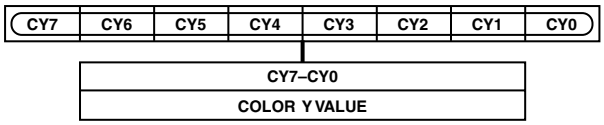


Figure 21. Color Y Register

COLOR CR
CCR (CCR7–CCR0)
(Address (SR4–SR0) = 07H)

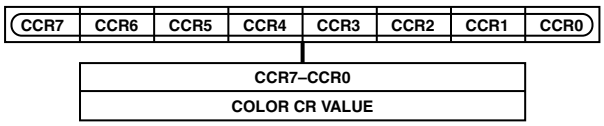


Figure 22. Color Cr Register

COLOR CB
CCB (CCB7–CCB0)
(Address (SR4–SR0) = 08H)

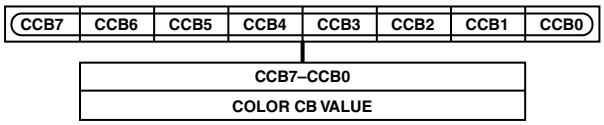


Figure 23. Color Cb Register

These three 8-bit-wide registers are used to program the output color of the internal test pattern generator, be it the lines of the cross hatch pattern or the uniform field test pattern.

The standard used for the values for Y and the color difference signals to obtain white, black and the saturated primary and complementary colors conforms to the ITU-R BT 601-4 standard.

The Table III shows sample color values to be programmed into the color registers.

Table III. Sample Color Values

Sample Color	Color Y Value	Color Cr Value	Color Cb Value
White	235 (EB)	128 (80)	128 (80)
Black	16 (10)	128 (80)	128 (80)
Red	81 (51)	240 (F0)	90 (5A)
Green	145 (91)	34 (22)	54 (36)
Blue	41 (29)	110 (6E)	240 (F0)
Yellow	210 (D2)	146 (92)	16 (10)
Cyan	170 (AA)	16 (10)	166 (A6)
Magenta	106 (6A)	222 (DE)	202 (CA)

DAC TERMINATION AND LAYOUT CONSIDERATIONS

Voltage Reference

The ADV7197 contains an on-board voltage reference. The V_{REF} pin is normally terminated to V_{AA} through a 0.1 µF capacitor when the internal V_{REF} is used. Alternatively, the ADV7197 can be used with an external V_{REF} (AD589).

Resistor R_{SET} is connected between the R_{SET} pin and analog ground and is used to control the full scale output current and therefore the DAC voltage output levels. For full-scale output R_{SET} must have a value of 2470 Ω. R_{LOAD} has a value of 300 Ω. When an input range of 0–1023 is selected the value of R_{SET} must be 2820 Ω.

The ADV7197 has three analog outputs, corresponding to Y, Pr, Pb video signals. The DACs must be used with external buffer circuits in order to provide sufficient current to drive an output device. A suitable op amp would be the AD8057.

PC BOARD LAYOUT CONSIDERATIONS

The ADV7197 is optimally designed for lowest noise performance, both radiated and conducted noise. To complement the excellent noise performance of the ADV7197, it is imperative that great care be given to the PC board layout.

The layout should be optimized for lowest noise on the ADV7197 power and ground lines. This can be achieved by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and AGND and V_{DD} and DGND pins should be kept as short as possible to minimized inductive ringing.

It is recommended that a four-layer printed circuit board is used. With power and ground planes separating the layer of the signal carrying traces of the components and solder side layer. Placement of components should consider to separate noisy circuits, such as crystal clocks, high-speed logic circuitry and analog circuitry.

There should be a separate analog ground plane (AGND) and a separate digital ground plane (GND).

Power planes should encompass a digital power plane (V_{DD}) and a analog power plane (V_{AA}). The analog power plane should contain the DACs and all associated circuitry, and the V_{REF} circuitry.

The digital power plane should contain all logic circuitry. The analog and digital power planes should be individually connected to the common power plane at one single point through a suitable filtering device, such as a ferrite bead.

DAC output traces on a PCB should be treated as transmission lines. It is recommended that the DACs be placed as close as possible to the output connector, with the analog output traces being as short as possible (less than 3 inches. The DAC termination resistors should be placed as close as possible to the DAC outputs and should overlay the PCB's ground plane. As well as minimizing reflections, short analog output traces will reduce noise pickup due to neighboring digital circuitry.

Supply Decoupling

Noise on the analog power plane can be further reduced by the use of decoupling capacitors.

Optimum performance is achieved by the use of 0.1 µF ceramic capacitors. Each of group of V_{AA} or V_{DD} pins should be individually decoupled to ground. This should be done by placing the capacitors as close as possible to the device with the capacitor leads as short as possible, thus minimizing lead inductance.

Digital Signal Interconnect

The digital signal lines should be isolated as much as possible from the analog outputs and other analog circuitry. Digital signal lines should not overlay the analog power plane.

Due to the high clock rates used, long clock lines to the ADV7197 should be avoided to minimize noise pickup. Any active pull-up termination resistors for the digital inputs should be connected to the digital power plane and not the analog power plane.

Analog Signal Interconnect

The ADV7197 should be located as close as possible to the output connectors thus minimizing noise pickup and reflections due to impedance mismatch.

For optimum performance, the analog outputs should each have a source termination resistance to ground of 75 Ω. This termination resistance should be as close as possible to the ADV7197 to minimize reflections.

Any unused inputs should be tied to ground.

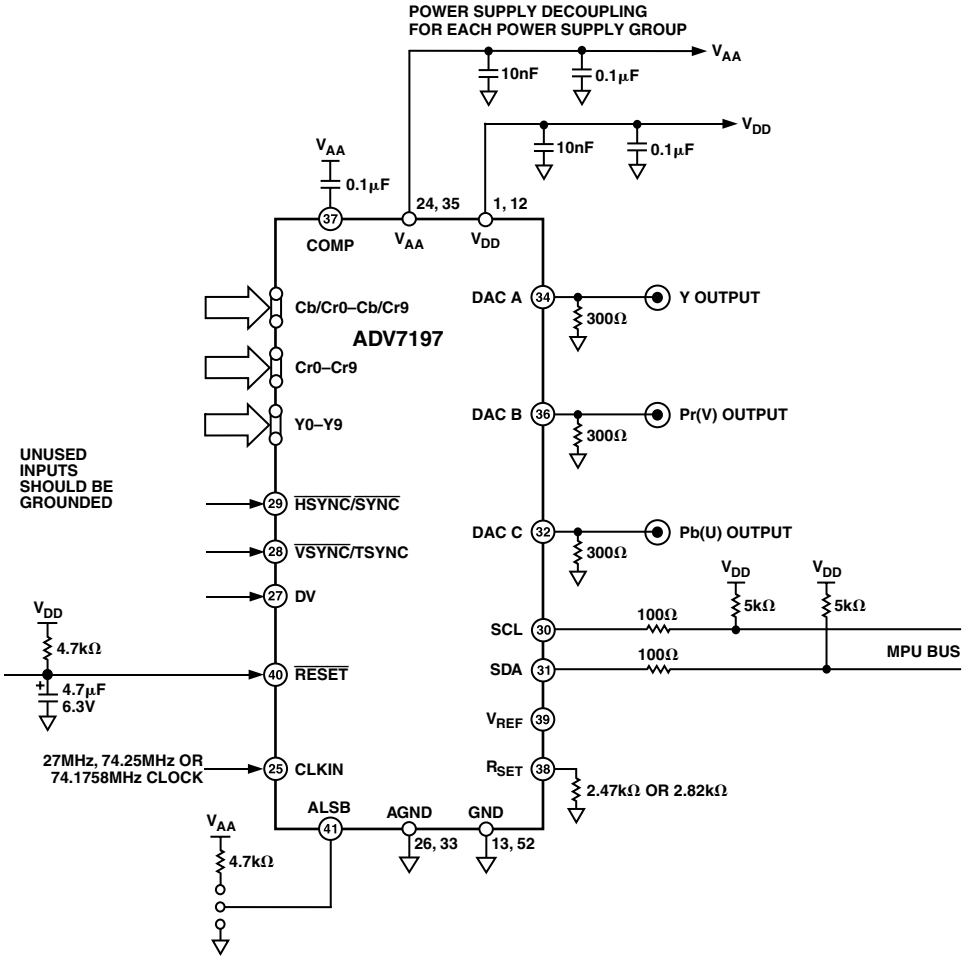


Figure 24. Circuit Layout

Video Output Buffer and Optional Output Filter

Output buffering is necessary in order to drive output devices, such as HDTV monitors.

Analog Devices produces a range of suitable op amps for this application. A suitable op amp would be the AD8057. More information on line driver buffering circuits is given in the relevant op amp data sheets.

An optional analog reconstruction LPF might be required as an antialias filter if the ADV7197 is connected to a device that requires this filtering.

The Eval ADV7196/ADV7197EB evaluation board uses the ML6426 Microlinear IC, which provides buffering and low-pass filtering for HDTV applications.

The Eval ADV7196/ADV7197EB Rev. B and Rev. C evaluation boards use the AD8057 as a buffer and a 6th order LPF.

The Application Note, AN-TBD, describes in detail these two designs and should be consulted when designing external filter and buffers for Analog Devices Video Encoders.

To calculate the output full-scale current and voltage, the following equations should be used:

$$V_{OUT} = I_{OUT} \times R_{LOAD}$$

$$I_{OUT} = (V_{REF} \times K)/R_{SET}$$

where:

K = 5.66 (for input ranges 64–940, 64–960, output standards EIA770.3)

K = 6.46 (for input ranges 0–1023, output standards RS170/343A

V_{REF} = 1.235 V.

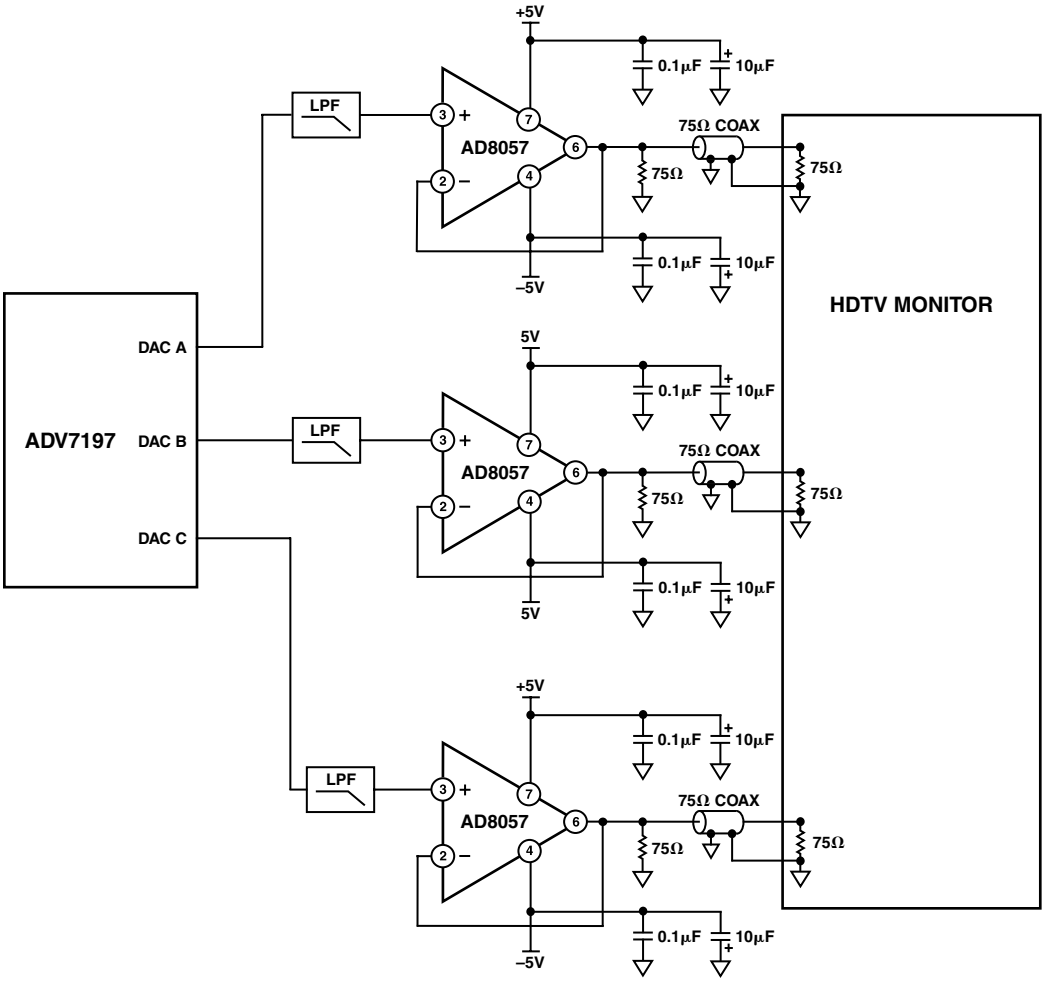


Figure 25. Output Buffer and Optional Filter

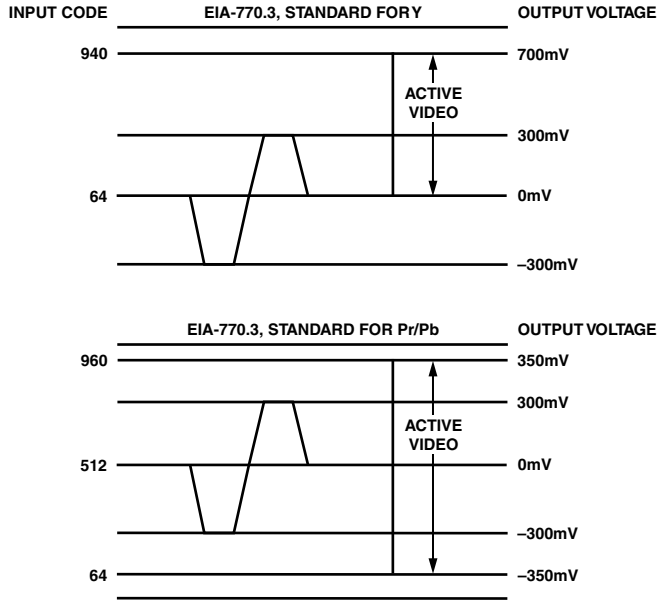


Figure 26. EIA 770.3 Standard Output Signals (1080i, 720p)

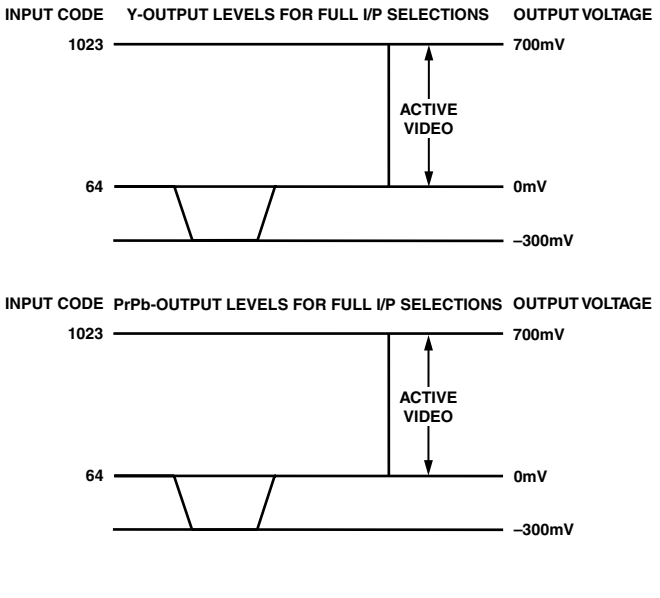


Figure 27. Output Levels for Full I/P Selection

REGISTER SETTINGS
Register Settings on Power-Up

Address		Register Setting
00hex	Mode Register 0	00hex
01hex	Mode Register 1	00hex
02hex	Mode Register 2	00hex
03hex	Mode Register 3	39hex
04hex	Mode Register 4	00hex
05hex	Mode Register 5	00hex
06hex	Color Y	A0hex
07hex	Color Cr	80hex
08hex	Color Cb	80hex

REGISTER SETTINGS
Internal Colorbars (Field), HDTV Mode

Address		Register Setting
00hex	Mode Register 0	00hex
01hex	Mode Register 1	0Dhex
02hex	Mode Register 2	00hex
03hex	Mode Register 3	39hex
04hex	Mode Register 4	00hex
05hex	Mode Register 5	00hex
06hex	Color Y	xxhex
07hex	Color Cr	xxhex
08hex	Color Cb	xxhex

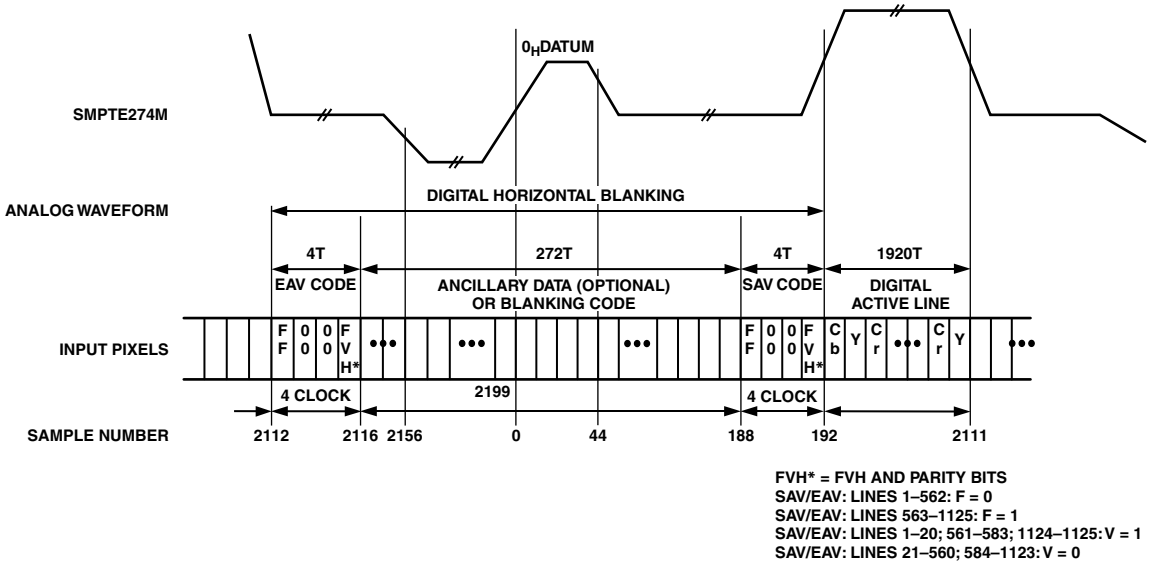


Figure 28. EAV/SAV Input Data Timing Diagram—SMPTE274M (1080i)

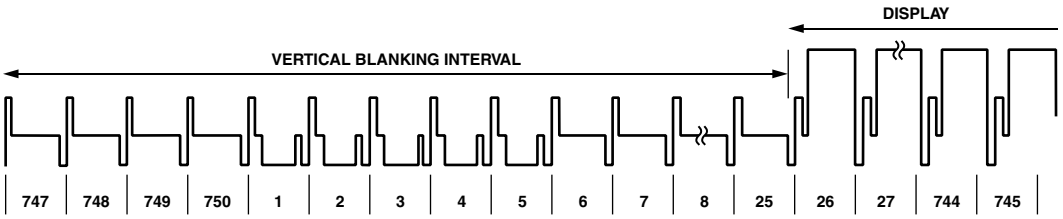


Figure 29. SMPTE296M (720p)

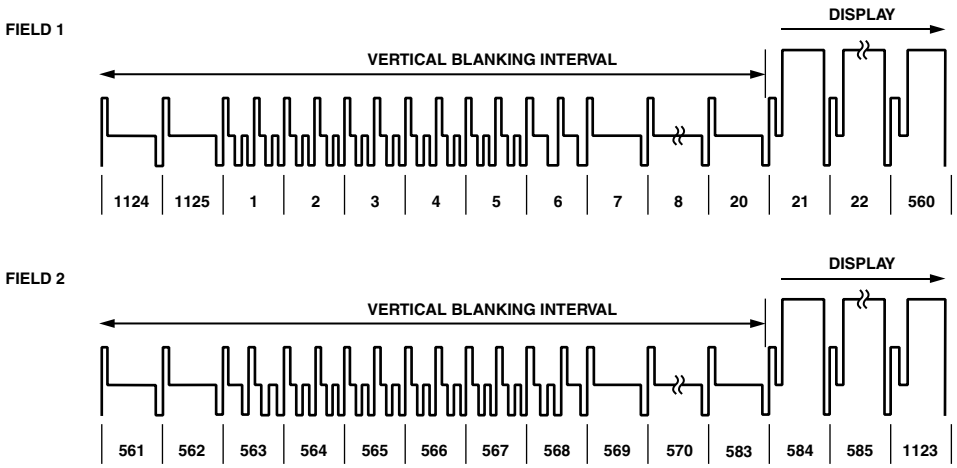
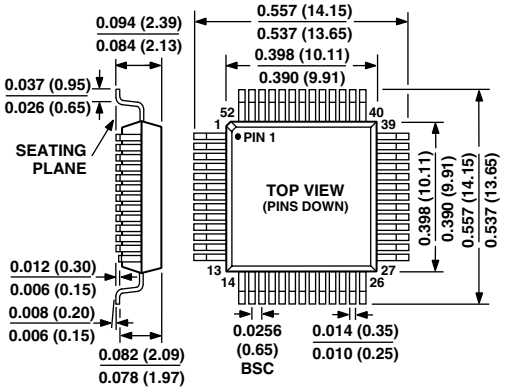


Figure 30. SMPTE274M (1080i)

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

52-Lead Plastic Quad Flatpack (MQFP)
(S-52)



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