CMOS
80 MHz, 10-Bit Video DAC

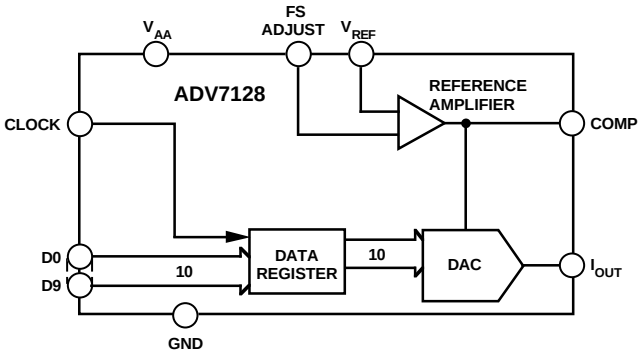
ADV7128

FEATURES
80 MHz Pipelined Operation
10-Bit D/A Converters
RS-343A/RS-170 Compatible Outputs
TTL Compatible Inputs
+5 V CMOS Monolithic Construction
28-Pin SOIC Package

APPLICATIONS
High Definition Television (HDTV)
High Resolution Color Graphics
Digital Radio Modulation
CAE/CAD/CAM Applications
Image Processing
Instrumentation
Video Signal Reconstruction
Direct Digital Synthesis (DDS) & I/O Modulation
Wireless LAN
Wireless Local Loop

SPEED GRADES
80 MHz
50 MHz
30 MHz

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADV7128 (ADV®) is a video speed, digital-to-analog converter on a single monolithic chip. It consists of a high speed, 10-bit, video D/A converters; a standard TTL input interface; and a high impedance, analog output, current source.

The ADV7128 has a 10-bit pixel input port. A single +5 V power supply, an external 1.23 V reference and pixel clock input are and all that are required to make the part operational.

The ADV7128 is capable of generating video output signals which are compatible with RS-343A, RS-170 and most proposed production system HDTV video standards, including SMPTE 240M.

The ADV7128 is fabricated in a +5 V CMOS process. Its monolithic CMOS construction ensures greater functionality with low power dissipation. The ADV7128 is available in a 28-lead small outline IC (SOIC).

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PRODUCT HIGHLIGHTS

1. Fast video refresh rate, 80 MHz.
2. Guaranteed monotonic to 10 bits. Ten bits of resolution allows for implementation of linearization functions such as gamma correction and contrast enhancement.
3. Compatible with a wide variety of high resolution color graphics systems including RS-343A/RS-170 and the proposed SMPTE 240M standard for HDTV.
4. Combined with a numerically controlled oscillator (AD9955), it forms a complete frequency synthesizer (DDS).
5. Using the parts reduced power output DAC modes, it is ideal for power and cost sensitive communications type applications.

REV. 0

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ADV7128–SPECIFICATIONS (V_{AA} = +5 V ± 5%; V_{REF} = +1.235 V; R_L = 37.5 Ω, C_L = 10 pF; R_{SET} = 560 Ω. All specifications T_{MIN} to T_{MAX}[1] unless otherwise noted.)

Parameter	K Version	Units	Test Conditions/Comments
STATIC PERFORMANCE			
Resolution	10	Bits	
Accuracy			
Integral Nonlinearity, INL	±1	LSB max	
Differential Nonlinearity, DNL	±1	LSB max	Guaranteed Monotonic
Gray Scale Error	±5	% Gray Scale max	Max Gray Scale Current = (V_{REF}* 7,969/R_{SET}) mA
Coding		Binary	
DIGITAL INPUTS			
Input High Voltage, V_{INH}	2	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Current, I_{IN}	±1	µA max	V_{IN} = 0.4 V or 2.4 V
Input Capacitance, C_{IN}[2]	10	pF max	
ANALOG OUTPUT			
Gray Scale Current Range	15	mA min	
	22	mA max	
Output Current			
White Level	16.74	mA min	Typically 17.62 mA
	18.50	mA max	
Black Level	0	µA min	Typically 5 µA
	50	µA max	
LSB Size	17.28	µA typ	
Output Compliance, V_{OC}	0	V min	
	+1.4	V max	
Output Impedance, R_{OUT}[2]	100	kΩ typ	
Output Capacitance, C_{OUT}[2]	30	pF max	I_{OUT} = 0 mA
VOLTAGE REFERENCE			
Voltage Reference Range, V_{REF}	1.14/1.26	V min/V max	V_{REF} = 1.235 V for Specified Performance
Input Current, I_{VREF}	–5	mA typ	
POWER REQUIREMENTS			
V_{AA}	5	V nom	
I_{AA}	125	mA max	Typically 80 mA: 80 MHz Parts
	100	mA max	Typically 70 mA: 50 MHz & 35 MHz Parts
Power Supply Rejection Ratio[2]	0.5	%/% max	Typically 0.12%/%: f = 1 kHz, COMP = 0.1 µF
Power Dissipation	625	mW max	Typically 400 mW: 80 MHz Parts
	500	mW max	Typically 350 mW: 50 MHz & 30 MHz Parts
DYNAMIC PERFORMANCE			
Glitch Impulse[2, 3]	50	pV secs typ	
DAC Noise[2, 3, 4]	200	pV secs typ	

NOTES
[1]Temperature range (T_{MIN} to T_{MAX}); 0°C to +70°C.
[2]Sample tested at +25°C to ensure compliance.
[3]TTL input values are 0 to 3 volts, with input rise/fall times ≤3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. See timing notes in Figure 1.
[4]This includes effects due to clock and data feedthrough.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1]

(V_{AA} = +5 V ± 5%; V_{REF} = +1.235 V; R_L = 37.5 Ω, C_L = 10 pF; R_{SET} = 560 Ω. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted.)

Parameter	80 MHz Version	50 MHz Version	30 MHz Version	Units	Conditions/Comments
f_{MAX}	80	50	30	MHz max	Clock Rate
t_1	3	6	8	ns min	Data & Control Setup Time
t_2	2	2	2	ns min	Data & Control Hold Time
t_3	12.5	20	33.3	ns min	Clock Cycle Time
t_4	4	7	9	ns min	Clock Pulse Width High Time
t_5	4	7	9	ns min	Clock Pulse Width Low Time
t_6	30	30	30	ns max	Analog Output Delay
	20	20	20	ns typ	
t_7	3	3	3	ns max	Analog Output Rise/Fall Time
t_8[3]	12	15	15	ns typ	Analog Output Transition Time

NOTES
[1]TTL input values are 0 to 3 volts, with input rise/fall times ≤3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. See timing notes in Figure 1.
[2]Temperature range (T_{MIN} to T_{MAX}): 0°C to +70°C
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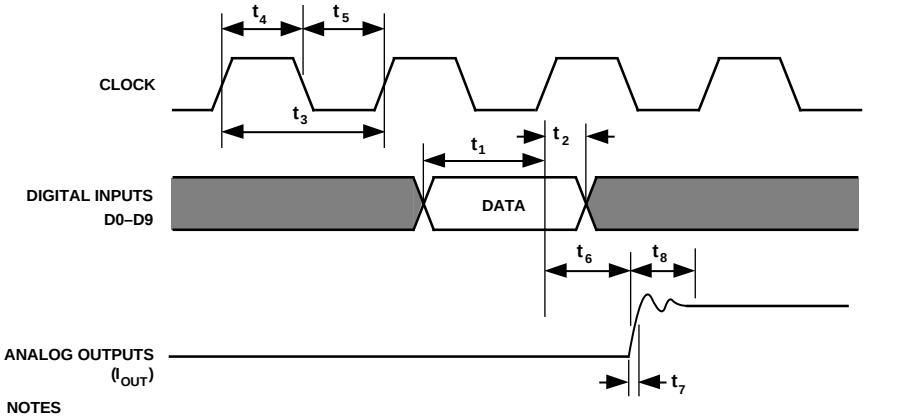


NOTES
1. OUTPUT DELAY (t_6) MEASURED FROM THE 50% POINT OF THE RISING EDGE OF THE CLOCK TO THE 50% POINT OF FULL-SCALE TRANSITION.
2. TRANSITION TIME (t_8) MEASURED FROM THE 50% POINT OF FULL-SCALE TRANSITION TO WITHIN 2% OF THE FINAL OUTPUT VALUE.
3. OUTPUT RISE/FALL TIME (t_7) MEASURED BETWEEN THE 10% AND 90% POINTS OF FULL-SCALE TRANSITION.

Figure 1. Video Input/Output Timing

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	V_{AA}	4.75	5.00	5.25	Volts
Ambient Operating Temperature	T_A	0		+70	°C
Output Load	R_L		37.5		Ω
Reference Voltage	V_{REF}	1.14	1.235	1.26	Volts

ORDERING GUIDE

Model	Speed	Accuracy DNL	Accuracy INL	Temperature Range	Package Option*
ADV7128KR80	80 MHz	±1	±1	0°C to +70°C	R-28
ADV7128KR50	50 MHz	±1	±1	0°C to +70°C	R-28
ADV7128KR30	30 MHz	±1	±1	0°C to +70°C	R-28

*R = SOIC.

ABSOLUTE MAXIMUM RATINGS*

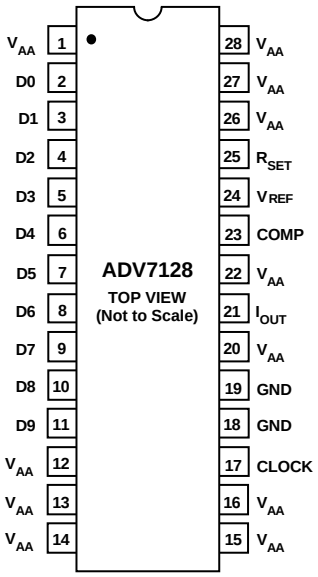
V_{AA} to GND .....+7 V
Voltage on Any Digital Pin ..... GND –0.5 V to V_{AA} +0.5 V
Ambient Operating Temperature (T_A) ..... 0°C to +70°C
Storage Temperature (T_S) .....–65°C to +150°C
Junction Temperature (T_J) ..... +150°C
Lead Temperature (Soldering, 10 secs) ..... +300°C
Vapor Phase Soldering (2 minutes) ..... +220°C
I_{OUT} to GND[1] ..... 0 V to V_{AA}

NOTES

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[1]Analog Output Short Circuit to any Power Supply or Common can be of an indefinite duration.

PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV7128 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTION

Pin Mnemonic	Function
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the R0–R9, G0–G9, B0–B9, $\overline{SYNC}$ and $\overline{BLANK}$ pixel and control inputs. It is typically the pixel clock rate of the video system. CLOCK should be driven by a dedicated TTL buffer.
D0–D9	Data inputs (TTL compatible). Data is latched on the rising edge of CLOCK. D0 is the least significant data bit. Unused data inputs should be connected to either the regular PCB power or ground plane.
I_{OUT}	Current output. This high impedance current source is capable of directly driving a doubly terminated 75 Ω coaxial cable.
R_{SET}	Full-scale adjust control. A resistor (R_{SET}) connected between this pin and GND, controls the magnitude of the full-scale video signal. Note that the IRE relationships are maintained, regardless of the full-scale output current. The relationship between R_{SET} and the full-scale output current on I_{OUT} is given by: I_{OUT} (mA) = 7,969 × V_{REF}(V)/R_{SET}(Ω)
COMP	Compensation pin. This is a compensation pin for the internal reference amplifier. A 0.1 μF ceramic capacitor must be connected between COMP and V_{AA}.
V_{REF}	Voltage reference input. An external 1.23 V voltage reference must be connected to this pin. The use of an external resistor divider network is not recommended. A 0.1 μF decoupling ceramic capacitor should be connected between V_{REF} and V_{AA}.
V_{AA}	Analog power supply (5 V ± 5%). All V_{AA} pins on the ADV7128 must be connected.
GND	Ground. All GND pins must be connected.

TERMINOLOGY

Color Video (RGB)
This usually refers to the technique of combining the three primary colors of red, green and blue to produce color pictures within the usual spectrum. In RGB monitors, three DACs are required, one for each color.

Gray Scale
The discrete levels of video signal between reference black and reference white levels. A 10-bit DAC contains 1024 different levels, while an 8-bit DAC contains 256.

Raster Scan
The most basic method of sweeping a CRT one line at a time to generate and display images.

Reference Black Level
The maximum negative polarity amplitude of the video signal.

Reference White Level
The maximum positive polarity amplitude of the video signal.

Video Signal
That portion of the composite video signal which varies in gray scale levels between reference white and reference black. Also referred to as the picture signal, this is the portion which may be visually observed.

CIRCUIT DESCRIPTION AND OPERATION

The ADV7128 contains one 10-bit D/A converter, with one input channel containing a 10-bit register. Also integrated on board the part is a reference amplifier.

Digital Inputs
Ten bits of data (color information) D0–D9 are latched into the device on the rising edge of each clock cycle. This data is presented to the 10-bit DAC and is then converted to an analog output waveform. See Figure 2.

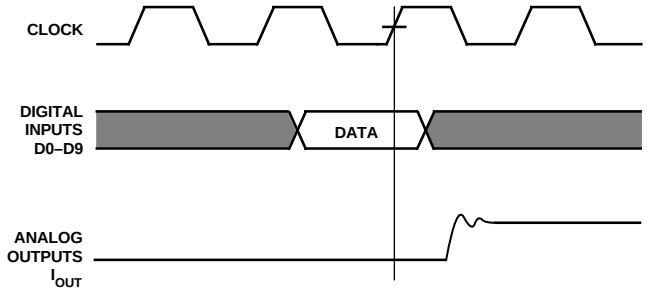


Figure 2. Video Data Input/Output

All these digital inputs are specified to accept TTL logic levels.

Clock Input
The CLOCK input of the ADV7128 is typically the pixel clock rate of the system. It is also known as the dot rate. The dot rate, and hence the required CLOCK frequency, will be determined by the on-screen resolution, according to the following equation:

$$Dot\ Rate = (Horiz\ Res) \times (Vert\ Res) \times (Refresh\ Rate)/(Retrace\ Factor)$$

Horiz Res = Number of Pixels/Line.

Vert Res = Number of Lines/Frame.

Refresh Rate = Horizontal Scan Rate. This is the rate at which the screen must be refreshed, typically 60 Hz for a noninterlaced system or 30 Hz for an interlaced system.

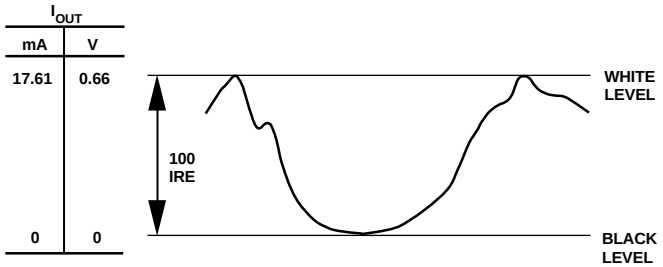
Retrace Factor = Total Blank Time Factor. This takes into account that the display is blanked for a certain fraction of the total duration of each frame (e.g., 0.8).

If we, therefore, have a graphics system with a 1024×1024 resolution, a noninterlaced 60 Hz refresh rate and a retrace factor of 0.8, then:

$$\text{Dot Rate} = 1024 \times 1024 \times 60/0.8$$
$$= 78.6\ \text{MHz}$$

The required CLOCK frequency is thus 78.6 MHz.

All video data and control inputs are latched into the ADV7128 on the rising edge of CLOCK, as previously described in the "Digital Inputs" section. It is recommended that the CLOCK input to the ADV7128 be driven by a TTL buffer (e.g., 74F244).



NOTES
1. OUTPUTS CONNECTED TO A DOUBLY TERMINATED 75Ω LOAD.
2. V_{REF} = 1.235V, R_{SET} = 560Ω.
3. RS–343A LEVELS AND TOLERANCES ASSUMED ON ALL LEVELS.

Figure 3. I_{OUT} Video Output Waveform

Table I. Video Output Truth Table for the ADV7128

Description	I_{OUT}[1]	DAC Input Data
WHITE LEVEL	17.62	3FF
VIDEO	video	data
VIDEO to BLACK	video	data
BLACK LEVEL	0	00H

NOTE
[1]Typical with full scale = 17.62 mA. V_{REF} = 1.235 V, R_{SET} = 560 Ω.

Reference Input

An external 1.23 V voltage reference is required to drive the ADV7128. The AD589 from Analog Devices is an ideal choice of reference. It is a two-terminal, low cost, temperature compensated bandgap voltage reference which provides a fixed 1.23 V output voltage for input currents between 50 µA and 5 mA. Figure 4 shows a typical reference circuit connection diagram. The voltage reference gets its current drive from the ADV7128's V_{AA} through an on-board 1 kΩ resistor to the V_{REF} pin. A 0.1 µF ceramic capacitor is required between the COMP pin and V_{AA}. This is necessary so as to provide compensation for the internal reference amplifier.

A resistance R_{SET} connected between R_{SET} and GND determines the amplitude of the output video level according to the following equation:

$$I_{OUT}\ (mA) = 7{,}969 \times V_{REF}(V)/R_{SET}(\Omega) \qquad (1)$$

Using a variable value of R_{SET}, as shown in Figure 4, allows for accurate adjustment of the analog output video levels. Use of a fixed 560 Ω R_{SET} resistor yields the analog output levels as quoted in the specification page. These values typically correspond to the RS-343A video waveform values as shown in Figure 3.

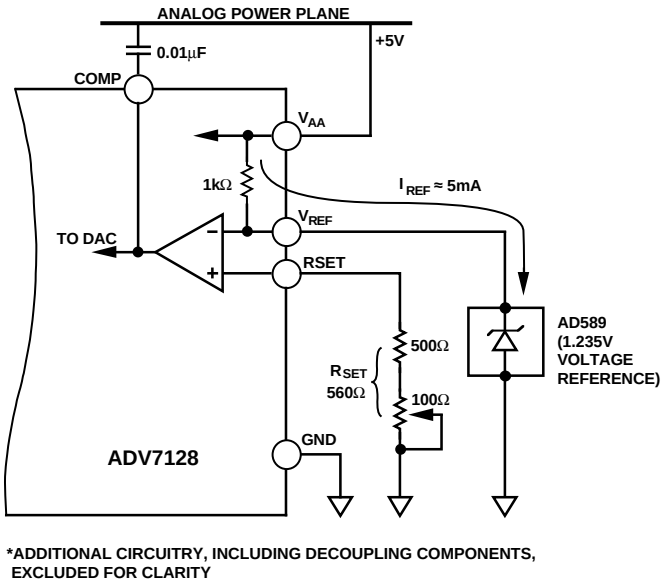


Figure 4. Reference Circuit

D/A Converter

The ADV7128 contains a 10-bit D/A converter. The DAC is designed using an advanced, high speed, segmented architecture. The bit currents corresponding to each digital input are routed to either the analog output (bit = "1") or GND (bit = "0") by a sophisticated decoding scheme. The use of identical current sources in a monolithic design guarantees monotonicity and low glitch. The on-board operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

Analog Output

The analog output of the ADV7128 is a high impedance current source. The current output is capable of directly driving a 37.5 Ω load, such as a doubly terminated 75 Ω coaxial cable. Figure 5a shows the required configuration for the output connected into a doubly terminated 75 Ω load. This arrangement will develop RS-343A video output voltage levels across a 75 Ω monitor.

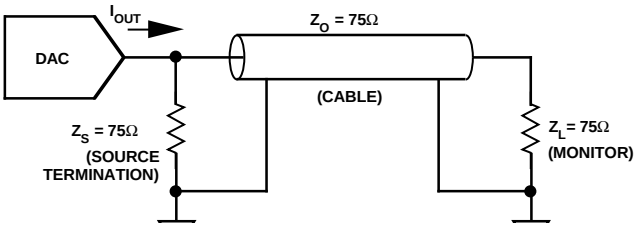


Figure 5a. Analog Output Termination for RS-343A

A suggested method of driving RS-170 video levels into a 75 Ω monitor is shown in Figure 5b. The output current level of the DAC remains unchanged, but the source termination resistance, Z_S, on the DAC is increased from 75 Ω to 150 Ω.

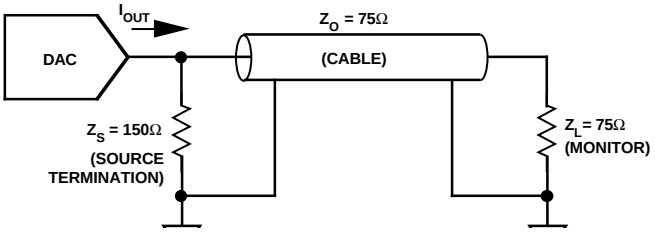


Figure 5b. Analog Output Termination for RS-170

More detailed information regarding load terminations for various output configurations, including RS-343A and RS-170, is available in an Application Note entitled "Video Formats & Required Load Terminations" available from Analog Devices, publication no. E1228-15-1/89.

Figure 3 shows the video waveforms associated with the current output driving the doubly terminated 75 Ω load of Figure 5a.

Gray Scale Operation

The ADV7128 can be used for stand-alone, gray scale (monochrome) or composite video applications (i.e., only one channel used for video information).

Video Output Buffer

The ADV7128 is specified to drive transmission line loads, which is what most monitors are rated as. The analog output configurations to drive such loads are described in the Analog Interface section and illustrated in Figure 5. However, in some applications it may be required to drive long "transmission line" cable lengths. Cable lengths greater than 10 meters can attenuate and distort high frequency analog output pulses. The inclusion of output buffers will compensate for some cable distortion. Buffers with large full power bandwidths and gains between 2 and 4 will be required. These buffers will also need to be able to supply sufficient current over the complete output voltage swing. Analog Devices produces a range of suitable op amps for such applications. These include the AD84x series of monolithic op amps. In very high frequency applications (80 MHz), the AD9617 is recommended. More information on line driver buffering circuits is given in the relevant op amp data sheets.

Use of buffer amplifiers also allows implementation of other video standards besides RS-343A and RS-170. Altering the gain components of the buffer circuit will result in any desired video level.

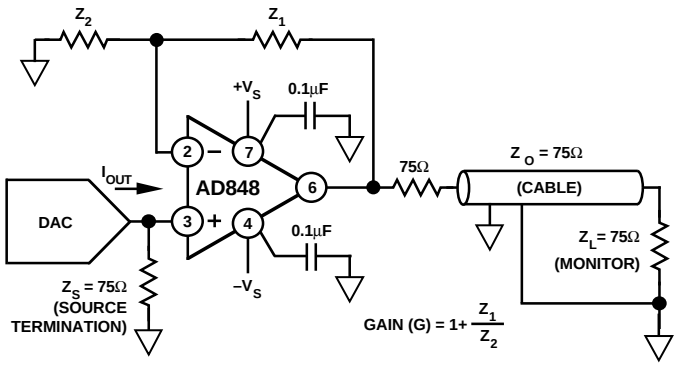


Figure 6. AD848 As an Output Buffer

PC Board Layout Considerations

The ADV7128 is optimally designed for lowest noise performance, both radiated and conducted noise. To complement the excellent noise performance of the ADV7128 it is imperative that great care be given to the PC board layout. Figure 7 shows a recommended connection diagram for the ADV7128.

The layout should be optimized for lowest noise on the ADV7128 power and ground lines. This can be achieved by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and GND pins should be minimized so as to minimize inductive ringing.

Ground Planes

The ADV7128 and associated analog circuitry, should have a separate ground plane referred to as the analog ground plane. This ground plane should connect to the regular PCB ground plane at a single point through a ferrite bead, as illustrated in Figure 7. This bead should be located as close as possible (within 3 inches) to the ADV7128.

The analog ground plane should encompass all ADV7128 ground pins, voltage reference circuitry, power supply bypass circuitry, the analog output traces and any output amplifiers.

The regular PCB ground plane area should encompass all the digital signal traces, excluding the ground pins, leading up to the ADV7128.

Power Planes

The PC board layout should have two distinct power planes, one for analog circuitry and one for digital circuitry. The analog power plane should encompass the ADV7128 (V_{AA}) and all associated analog circuitry. This power plane should be connected to the regular PCB power plane (V_{CC}) at a single point through a ferrite bead, as illustrated in Figure 7. This bead should be located within three inches of the ADV7128.

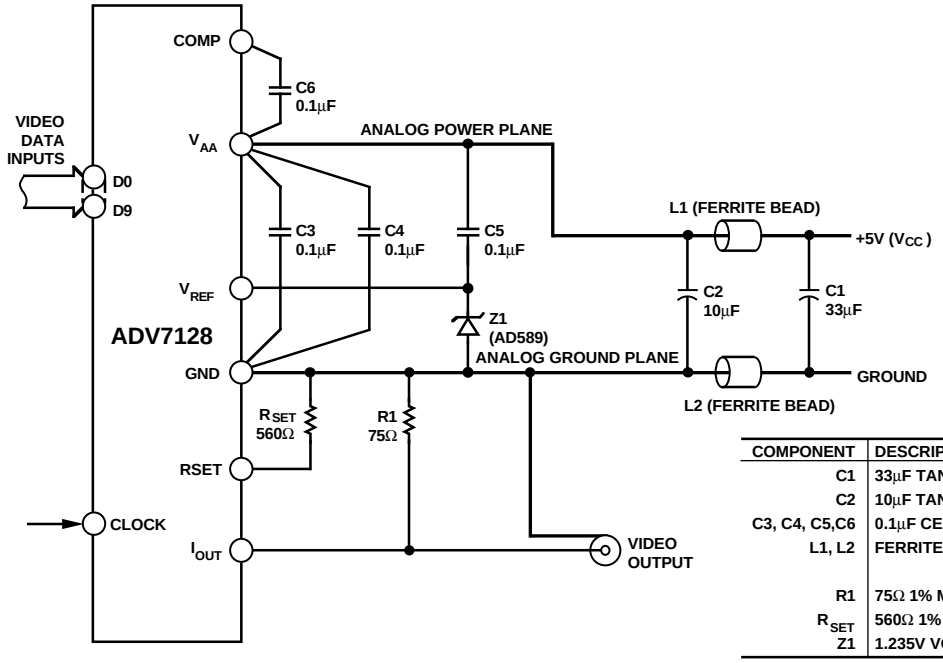
The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all ADV7128 power pins, voltage reference circuitry and any output amplifiers.

The PCB power and ground planes should not overlay portions of the analog power plane. Keeping the PCB power and ground planes from overlaying the analog power plane will contribute to a reduction in plane-to-plane noise coupling.

Supply Decoupling

Noise on the analog power plane can be further reduced by the use of multiple decoupling capacitors. (See Figure 7.)

Optimum performance is achieved by the use of 0.1 µF ceramic capacitors. Each of the two groups of V_{AA} should be individually decoupled to ground. This should be done by placing the capacitors as close as possible to the device with the capacitor leads as short as possible, thus minimizing lead inductance.



COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1	33µF TANTALUM CAPACITOR	
C2	10µF TANTALUM	
C3, C4, C5,C6	0.1µF CERAMIC CAPACITOR	
L1, L2	FERRITE BEAD	FAIR-RITE 274300111 OR MURATA BL01/02/03
R1	75Ω 1% METAL FILM RESISTOR	DALE CMF-55C
R_{SET}	560Ω 1% METAL FILM RESISTOR	DALE CMF-55C
Z1	1.235V VOLTAGE REFERENCE	ANALOG DEVICES AD589JH

Figure 7. ADV7128 Typical Connection Diagram and Component List

It is important to note that while the ADV7128 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise. A dc power supply filter (Murata BNX002) will provide EMI suppression between the switching power supply and the main PCB. Alternatively, consideration could be given to using a three terminal voltage regulator.

Digital Signal Interconnect

The digital signal lines to the ADV7128 should be isolated as much as possible from the analog outputs and other analog circuitry. Digital signal lines should not overlay the analog power plane.

Due to the high clock rates used, long clock lines to the ADV7128 should be avoided so as to minimize noise pickup.

Any active pull-up termination resistors for the digital inputs should be connected to the regular PCB power plane (V_{CC}), and not the analog power plane.

Analog Signal Interconnect

The ADV7128 should be located as close as possible to the output connectors thus minimizing noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, thereby maximizing the high frequency power supply rejection.

For optimum performance, the analog outputs should each have a source termination resistance to ground of 75 Ω (doubly terminated 75 Ω configuration). This termination resistance should be as close as possible to the ADV7128 so as to minimize reflections.

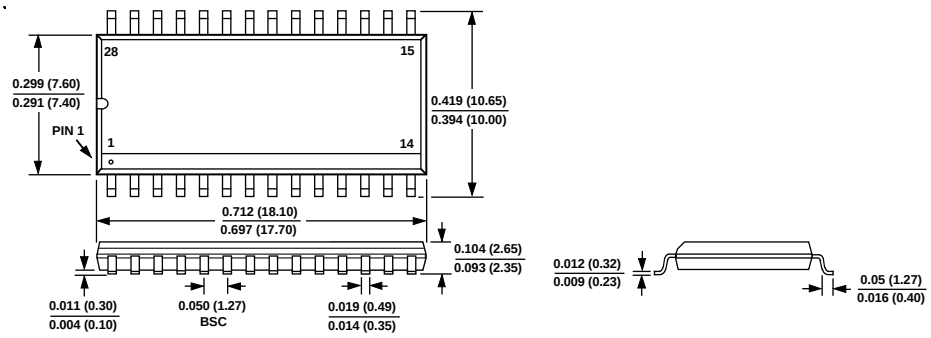
Additional information on PCB design is available in an application note entitled “Design and Layout of a Video Graphics System for Reduced EMI.” This application note is available from Analog Devices, publication number E1309-15-10/89.

C1760–24–1/93

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

SOIC (R-28)



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