TDA9984A

HDMI 1.3 transmitter with 1080p upscaler embedded

Rev. 04 — 15 January 2009 Product data sheet

1. General description

The TDA9984A is a High-Definition Multimedia Interface (HDMI) v. 1.3 transmitter with embedded 1080p upscaling functionality. It is backward compatible DVI 1.0 and can be connected to any DVI 1.0 and HDMI sink. It allows mixing a 3 × 8-bit RGB or YCbCr video stream with a pixel rate up to 150 MHz together with up to 4 × I²S-bus or one S/PDIF audio streams with an audio sampling rate up to 192 kHz. It supports Gamut boundary description (xvYCC), as well as HD audio, both HDMI 1.3 features.

A programmable upscaling block allows creating a 1080p output from a standard definition input. An intrafield deinterlacer is included in the scaler.

In order to be compatible with most applications, and thanks to the integration of a fully programmable input formatter and color space conversion block, the video input formats accepted also include YCbCr 4 : 4 : 4 (up to 3 × 8-bit), YCbCr 4 : 2 : 2 semi-planar (up to 2 × 12-bit) and YCbCr 4 : 2 : 2 compliant with ITU656 (up to 1 × 12-bit). In case of ITU656-like format, the input pixel clock can be made active on both edges.

The TDA9984A includes a HDCP 1.2 compliant cipher block. The HDCP key are stored internally in a non-volatile OTP memory for maximum security.

The TDA9984A includes a true I²C-bus master interface for DDC-bus communication for EDID purpose and HDCP purpose.

The TDA9984A can be controlled by an I²C-bus interface.

2. Features

- 3 × 8-bit video data input buses; CMOS and LV-TTL compatible
- Horizontal synchronization, vertical synchronization and data enable inputs or VREF, HREF and FREF inputs which can be used for synchronization
- Pixel rate clock input can be made active on one or both edges; selectable via I²C-bus
- 4 × I²S-bus audio input channels, one S/PDIF channel; audio data rate up to 192 kHz per input for both standards
- Dolby-True HD and DTS-HD High bit rate audio support through the use of the HBR interface
- 250 MHz to 1.50 GHz TMDS transmitter operation
- Programmable input formatter and upsampler/interpolator allows input of any of the 4 : 4 : 4 or 4 : 2 : 2 semi-planar and 4 : 2 : 2 ITU656-like formats

- Programmable color space converter allows to input RGB video data and to output RGB or YCbCr 4 : 2 : 2 HDMI video data, or to input YCbCr video data and to output RGB or YCbCr 4 : 2 : 2 HDMI video data; converter can be passed
- Upscaler allows creating a 1080p output from a standard definition input by using intelligent edge interpolation
- Repetition of video samples as required by the HDMI standard
- Insertion of HDMI additional information such as InfoFrames
- Color gamut metadata packet transmission (xvYCC)
- Downstream availability using hot plug detection (HPD input) and receiver detection (RxSense circuit)
- Master DDC-bus interface
- Deals with multiple levels of HDCP receivers and repeaters
- Internal SHA-1 calculation
- Controllable via I^2C-bus
- Low power dissipation
- 1.8 V and 3.3 V power supplies
- Power-down mode
- Hard reset
- Pin-to-pin compatible with TDA9983A/B and TDA9981A/B
- Software compatible with TDA9983A/B and TDA9981A/B

3. Applications

- Set-top box
- DVD player
- DVD recorder
- AV receiver
- Home theater
- Digital video camera
- Digital still camera
- Personal video recorder
- Media center PCs, graphic cards
- Switches

4. Quick reference data

Table 1. Quick reference data

$V_{DD(3V3)}$ = 3.3 V; $V_{DD(1V8)}$ = 1.8 V; V_{PP} = 0 V; T_{amb} = −5 °C to +85 °C; unless otherwise specified. Typical values are measured at T_{amb} = 25 °C and f_{clk} = 150 MHz.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{PP}	programming voltage			5.0	5.25	5.5	V
$V_{DDA(FRO)(3V3)}$	free running oscillator analog supply voltage (3.3 V)			3.0	3.3	3.6	V
$V_{DDA(PLL)(3V3)}$	PLL analog supply voltage (3.3 V)			3.0	3.3	3.6	V
$V_{DDD(3V3)}$	digital supply voltage (3.3 V)			3.0	3.3	3.6	V
$V_{DDH(3V3)}$	HDMI supply voltage (3.3 V)			3.0	3.3	3.6	V
$V_{DDC(1V8)}$	core supply voltage (1.8 V)			1.65	1.8	1.95	V
$V_{DDA(PLL)(1V8)}$	PLL analog supply voltage (1.8 V)			1.65	1.8	1.95	V
P_{cons}	power consumption	input 480p, output 1080p	[1][3]	-	500	630	mW
		input 1080i, output 1080p	[1][2]	-	742	940	mW
		input 1080p, output 1080p	[1][4]	-	320	400	mW
P_{tot}	total power dissipation	TMDS output current added					
		input 480p, output 1080p	[1][3]	-	630	770	mW
		input 1080i, output 1080p	[1][2]	-	872	1080	mW
		input 1080p, output 1080p	[1][4]	-	450	540	mW
P_{pd}	power dissipation in power-down mode			-	30	40	mW

[1] The maximum current consumption is in this configuration for this group of pins.

[2] Video format:
a) Input 1080i, YCbCr 4 : 2 : 2 embedded sync, 48 kHz S/PDIF 2 channels.
b) Output 1080p, YCbCr 4 : 2 : 2, 48 kHz S/PDIF.

[3] Video format:
a) Input 480p, ITU656 embedded sync, 48 kHz S/PDIF 2 channels.
b) Output 1080p, YCbCr 4 : 2 : 2, 48 kHz S/PDIF.

[4] Video format:
a) Input 1080p, YCbCr 4 : 2 : 2 embedded sync, 48 kHz S/PDIF 2 channels.
b) Output 1080p, YCbCr 4 : 2 : 2, 48 kHz S/PDIF.

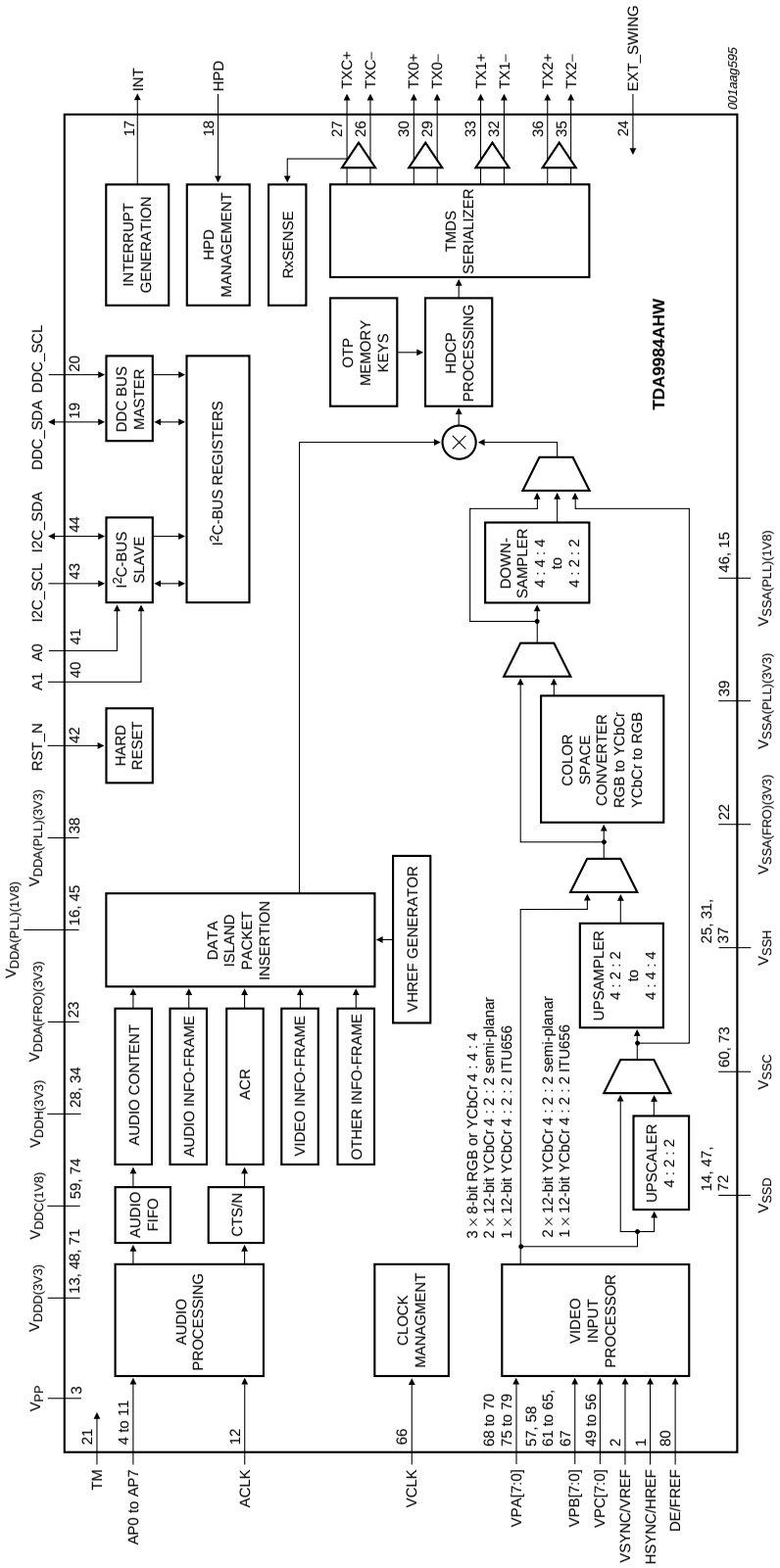
5. Ordering information

Table 2. Ordering information

Type number	Package[1]		
	Name	Description	Version
TDA9984AHW	HTQFP80	plastic thermal enhanced thin quad flat package; 80 leads; body 12 × 12 × 1 mm; exposed die pad	SOT841-4

[1] A lead-free package is required to comply with the new legislation.

6. Block diagram



The device can handle HDCP based on 1.2 features.

Fig 1. Block diagram

7. Pinning information

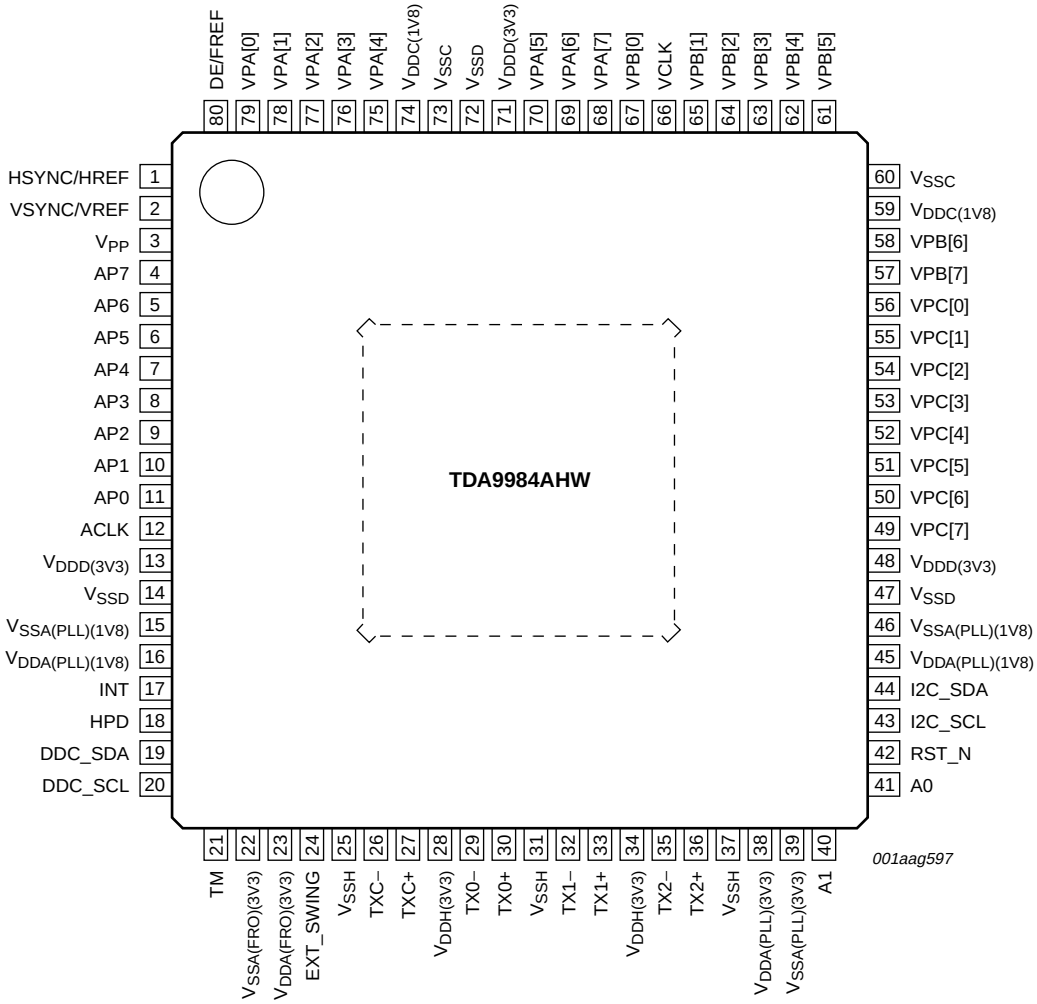


Fig 2. Pin configuration

7.1 Pin description

Table 3. Pin description

Symbol	Pin	Type[1]	Description
HSYNC/HREF	1	I	horizontal synchronization or reference input
VSYNC/VREF	2	I	vertical synchronization or reference input
V_{PP}	3	P	programming voltage for OTP memory; connect to ground for digital core in normal operation
AP7	4	I	audio port 7 input
AP6	5	I	audio port 6 input
AP5	6	I	audio port 5 input
AP4	7	I	audio port 4 input
AP3	8	I	audio port 3 input

Table 3. Pin description *...continued*

Symbol	Pin	Type[1]	Description
AP2	9	I	audio port 2 input
AP1	10	I	audio port 1 input
AP0	11	I	audio port 0 input
ACLK	12	I	audio clock input
$V_{DDD(3V3)}$	13	P	digital supply voltage for I/O ports (3.3 V)
V_{SSD}	14	G	digital ground for I/O ports
$V_{SSA(PLL)(1V8)}$	15	G	analog ground for PLL
$V_{DDA(PLL)(1V8)}$	16	P	PLL analog supply voltage (1.8 V)
INT	17	O	interrupt output; warns the external microprocessor that a special event has occurred
HPD	18	I	hot plug detect input; 5 V tolerant
DDC_SDA	19	I/O	DDC-bus data input/output; 5 V tolerant
DDC_SCL	20	I	DDC-bus clock input; 5 V tolerant
TM	21	I	internal test mode input; connect to ground
$V_{SSA(FRO)(3V3)}$	22	G	analog ground for free running oscillator
$V_{DDA(FRO)(3V3)}$	23	P	analog supply voltage for free running oscillator (3.3 V)
EXT_SWING	24	I	swing adjust input for TMDS output; a fixed resistor must be connected to $V_{DDH(3V3)}$
V_{SSH}	25	G	ground for TMDS (HDMI) transmitter
TXC–	26	O	negative clock channel for TMDS output
TXC+	27	O	positive clock channel for TMDS output
$V_{DDH(3V3)}$	28	P	supply voltage for TMDS (HDMI) transmitter (3.3 V)
TX0–	29	O	negative data channel 0 for TMDS output
TX0+	30	O	positive data channel 0 for TMDS output
V_{SSH}	31	G	ground for TMDS (HDMI) transmitter
TX1–	32	O	negative data channel 1 for TMDS output
TX1+	33	O	positive data channel 1 for TMDS output
$V_{DDH(3V3)}$	34	P	supply voltage for TMDS (HDMI) transmitter (3.3 V)
TX2–	35	O	negative data channel 2 for TMDS output
TX2+	36	O	positive data channel 2 for TMDS output
V_{SSH}	37	G	ground for TMDS (HDMI) transmitter
$V_{DDA(PLL)(3V3)}$	38	P	analog supply voltage for PLL (3.3 V)
$V_{SSA(PLL)(3V3)}$	39	G	analog ground for PLL
A1	40	I	I^2C-bus slave address bit 1 input
A0	41	I	I^2C-bus slave address bit 0 input
RST_N	42	I	hard reset input; active LOW
I2C_SCL	43	I	I^2C-bus clock input
I2C_SDA	44	I/O	I^2C-bus data input/output
$V_{DDA(PLL)(1V8)}$	45	P	PLL analog supply voltage (1.8 V)
$V_{SSA(PLL)(1V8)}$	46	G	analog ground for PLL
V_{SSD}	47	G	digital ground for I/O ports

Table 3. Pin description *...continued*

Symbol	Pin	Type[1]	Description
$V_{DDD(3V3)}$	48	P	digital supply voltage for I/O ports (3.3 V)
VPC[7]	49	I	video port C input bit 7 (MSB)
VPC[6]	50	I	video port C input bit 6
VPC[5]	51	I	video port C input bit 5
VPC[4]	52	I	video port C input bit 4
VPC[3]	53	I	video port C input bit 3
VPC[2]	54	I	video port C input bit 2
VPC[1]	55	I	video port C input bit 1
VPC[0]	56	I	video port C input bit 0 (LSB)
VPB[7]	57	I	video port B input bit 7 (MSB)
VPB[6]	58	I	video port B input bit 6
$V_{DDC(1V8)}$	59	P	supply voltage for digital core (1.8 V)
V_{SSC}	60	G	ground for digital core
VPB[5]	61	I	video port B input bit 5
VPB[4]	62	I	video port B input bit 4
VPB[3]	63	I	video port B input bit 3
VPB[2]	64	I	video port B input bit 2
VPB[1]	65	I	video port B input bit 1
VCLK	66	I	video pixel clock input
VPB[0]	67	I	video port B input bit 0 (LSB)
VPA[7]	68	I	video port A input bit 7 (MSB)
VPA[6]	69	I	video port A input bit 6
VPA[5]	70	I	video port A input bit 5
$V_{DDD(3V3)}$	71	P	digital supply voltage for I/O ports (3.3 V)
V_{SSD}	72	G	digital ground for I/O ports
V_{SSC}	73	G	ground for digital core
$V_{DDC(1V8)}$	74	P	supply voltage for digital core (1.8 V)
VPA[4]	75	I	video port A input bit 4
VPA[3]	76	I	video port A input bit 3
VPA[2]	77	I	video port A input bit 2
VPA[1]	78	I	video port A input bit 1
VPA[0]	79	I	video port A input bit 0
DE/FREF	80	I	video data enable or field reference input

[1] P = Power supply; G = Ground; I = Input; O = Output.

8. Functional description

The TDA9984A is designed to convert digital data (video and audio) provided by a Set-Top Box or DVD into an HDMI output, which could be used in TV with HDMI or DVI input.

The TDA9984A is able to output HDMI with the formats:

- RGB
- YCbCr 4 : 4 : 4
- YCbCr 4 : 2 : 2

The video data input formats are:

- RGB
- YCbCr 4 : 4 : 4
- YCbCr 4 : 2 : 2 semi-planar
- YCbCr 4 : 2 : 2 ITU656-like

It can also handle audio formats:

- 4 × I²S-bus channels
- One S/PDIF channel
- Dolby-True HD and DTS-HD through the use of HBR interface

8.1 Video processing

The TDA9984A has three video input ports VPA[7:0], VPB[7:0] and VPC[7:0] and can handle any of the following video input modes:

- RGB with 8-bit for each component
- YCbCr 4 : 4 : 4 with 8-bit for each component
- YCbCr 4 : 2 : 2 semi-planar with up to 12-bit for each component (Y, Cb and Cr)
- YCbCr 4 : 2 : 2 ITU656 with up to 12-bit data depth

The TDA9984A can be set to latch data at either the rising or the falling edge.

8.1.1 Internal assignment

The aim of the video input processor is to map internally the incoming data to the corresponding mode, which can be handled by the video processing. The device expects to have a big endian digital stream at its input. The internal signal name VP[23:0] is assigned depending on the input mode as defined in Figure 3.

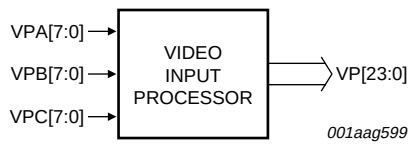


Fig 3. Internal assignment of VP[23:0]

The device can swap and invert (in case of a little endian stream) the incoming video data via the I²C-bus registers VIP_CNTRL_0, VIP_CNTRL_1 and VIP_CNTRL_2 (page 00h) to match the expectation of the video processing block; see Table 4.

When input ports are not used, it is possible to map them to internal ground via the I²C-bus registers ENA_VP_0, ENA_VP_1, ENA_VP_2, GND_VP_0, GND_VP_1 and GND_VP_2 (page 00h).

Table 4. Internal assignment

Internal port	RGB	YCbCr		
		4 : 4 : 4	4 : 2 : 2 semi-planar	4 : 2 : 2 ITU656-like
VP[23]	G[7]	Y[7]	Y[11]	YCbCr[11]
VP[22]	G[6]	Y[6]	Y[10]	YCbCr[10]
VP[21]	G[5]	Y[5]	Y[9]	YCbCr[9]
VP[20]	G[4]	Y[4]	Y[8]	YCbCr[8]
VP[19]	G[3]	Y[3]	Y[7]	YCbCr[7]
VP[18]	G[2]	Y[2]	Y[6]	YCbCr[6]
VP[17]	G[1]	Y[1]	Y[5]	YCbCr[5]
VP[16]	G[0]	Y[0]	Y[4]	YCbCr[4]
VP[15]	B[7]	Cb[7]	Y[3]	YCbCr[3]
VP[14]	B[6]	Cb[6]	Y[2]	YCbCr[2
VP[13]	B[5]	Cb[5]	Y[1]	YCbCr[1]
VP[12]	B[4]	Cb[4]	Y[0]	YCbCr[0]
VP[11]	B[3]	Cb[3]	CbCr[11]	-
VP[10]	B[2]	Cb[2]	CbCr[10]	-
VP[9]	B[1]	Cb[1]	CbCr[9]	-
VP[8]	B[0]	Cb[0]	CbCr[8]	-
VP[7]	R[7]	Cr[7]	CbCr[7]	-
VP[6]	R[6]	Cr[6]	CbCr[6]	-
VP[5]	R[5]	Cr[5]	CbCr[5]	-
VP[4]	R[4]	Cr[4]	CbCr[4]	-
VP[3]	R[3]	Cr[3]	CbCr[3]	-
VP[2]	R[2]	Cr[2]	CbCr[2]	-
VP[1]	R[1]	Cr[7]	CbCr[1]	-
VP[0]	R[0]	Cr[0]	CbCr[0]	-

8.1.2 Input format mappings

See Table 5 for more information concerning input format supported.

Table 5. Inputs of video input formatter

Space color	Format	Channels	Sync	Rising edge	Falling edge	Double edge[1]	Transmission input format	Pixel clock (MHz)	Maximum input format	Reference
RGB	4 : 4 : 4	3 × 8-bit	external	X			-	150 MHz	-	Section 8.1.2.1
					X		-	150 MHz	-	
			embedded	X			-	150 MHz	-	
					X		-	150 MHz	-	
YCbCr	4 : 4 : 4	3 × 8-bit	external	X			-	150 MHz	-	Section 8.1.2.2
					X		-	150 MHz	-	
			embedded	X			-	150 MHz	-	
					X		-	150 MHz	-	
YCbCr	4 : 2 : 2	up to 1 × 12-bit semi-planar	external	X			ITU656-like	54.054 MHz	480p/576p	Section 8.1.2.3
					X		ITU656-like	54.054 MHz	480p/576p	
						X	ITU656-like	27.027 MHz	480p/576p	Section 8.1.2.4
			embedded	X			ITU656-like	54.054 MHz	480p/576p	Section 8.1.2.5
					X		ITU656-like	54.054 MHz	480p/576p	
						X	ITU656-like	27.027 MHz	480p/576p	Section 8.1.2.6
		up to 2 × 12-bit semi-planar	external	X			SMPTE293M	148.5 MHz	1080p	Section 8.1.2.7
					X		SMPTE293M	148.5 MHz	1080p	
			embedded	X			SMPTE293M	148.5 MHz	1080p	Section 8.1.2.8
					X		SMPTE293M	148.5 MHz	1080p	

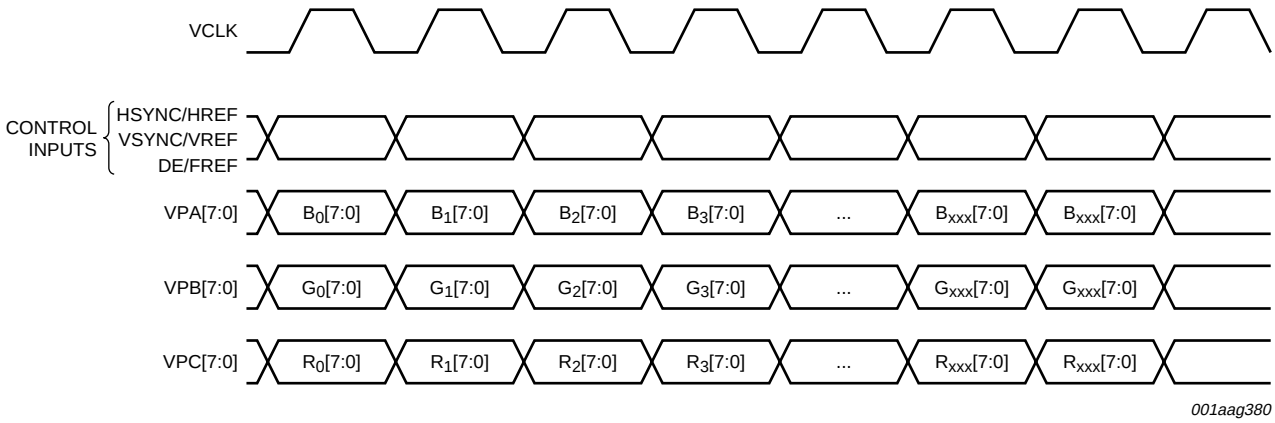
[1] Double edge means both rising and falling edges.

8.1.2.1 RGB 4 : 4 : 4 external sync input (rising edge)

Table 6. RGB 4 : 4 : 4 mapping

Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 45h; VIP_CNTRL_2 = 01h.

Video port A		Video port B		Video port C		Control	
Pin	**RGB 4 : 4 : 4**	**Pin**	**RGB 4 : 4 : 4**	**Pin**	**RGB 4 : 4 : 4**	**Pin**	**RGB 4 : 4 : 4**
VPA[0]	B[0]	VPB[0]	G[0]	VPC[0]	R[0]	HSYNC/HREF	used
VPA[1]	B[1]	VPB[1]	G[1]	VPC[1]	R[1]	VSYNC/VREF	used
VPA[2]	B[2]	VPB[2]	G[2]	VPC[2]	R[2]	DE/FREF	used
VPA[3]	B[3]	VPB[3]	G[3]	VPC[3]	R[3]		
VPA[4]	B[4]	VPB[4]	G[4]	VPC[4]	R[4]		
VPA[5]	B[5]	VPB[5]	G[5]	VPC[5]	R[5]		
VPA[6]	B[6]	VPB[6]	G[6]	VPC[6]	R[6]		
VPA[7]	B[7]	VPB[7]	G[7]	VPC[7]	R[7]		



DE could also be generated from HSYNC/HREF and VSYNC/VREF

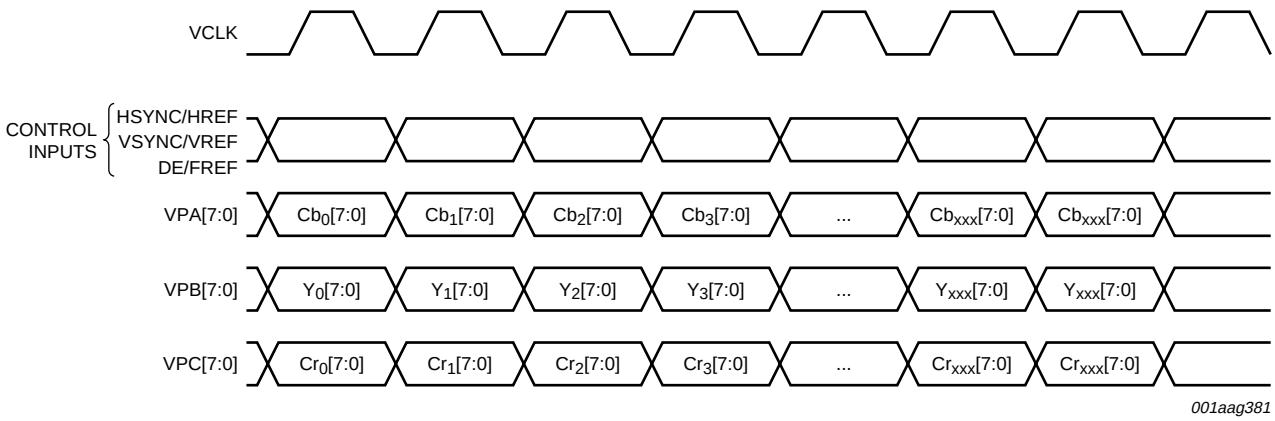
Fig 4. Pixel encoding RGB 4 : 4 : 4 external sync input (rising edge)

8.1.2.2 YCbCr 4 : 4 : 4 external sync input (rising edge)

Table 7. YCbCr 4 : 4 : 4 mapping

Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 45h; VIP_CNTRL_2 = 01h.

Video port A		Video port B		Video port C		Control	
Pin	**YCbCr 4 : 4 : 4**	**Pin**	**YCbCr 4 : 4 : 4**	**Pin**	**YCbCr 4 : 4 : 4**	**Pin**	**YCbCr 4 : 4 : 4**
VPA[0]	Cb[0]	VPB[0]	Y[0]	VPC[0]	Cr[0]	HSYNC/HREF	used
VPA[1]	Cb[1]	VPB[1]	Y[1]	VPC[1]	Cr[1]	VSYNC/VREF	used
VPA[2]	Cb[2]	VPB[2]	Y[2]	VPC[2]	Cr[2]	DE/FREF	used
VPA[3]	Cb[3]	VPB[3]	Y[3]	VPC[3]	Cr[3]		
VPA[4]	Cb[4]	VPB[4]	Y[4]	VPC[4]	Cr[4]		
VPA[5]	Cb[5]	VPB[5]	Y[5]	VPC[5]	Cr[5]		
VPA[6]	Cb[6]	VPB[6]	Y[6]	VPC[6]	Cr[6]		
VPA[7]	Cb[7]	VPB[7]	Y[7]	VPC[7]	Cr[7]		



DE could also be generated from HSYNC/HREF and VSYNC/VREF

Fig 5. Pixel encoding YCbCr 4 : 4 : 4 external sync input (rising edge)

8.1.2.3 YCbCr 4 : 2 : 2 ITU656-like external sync input (rising edge)

Table 8. YCbCr 4 : 2 : 2 ITU656-like rising edge mapping

Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 00h.

Video port A					Video port B					Control	
Pin	YCbCr 4 : 2 : 2 (ITU656-like)				Pin	YCbCr 4 : 2 : 2 (ITU656-like)				Pin	YCbCr 4 : 2 : 2
VPA[0]	Cb[0]	Y_0[0]	Cr[0]	Y_1[0]	VPB[0]	Cb[4]	Y_0[4]	Cr[4]	Y_1[4]	HSYNC/HREF	used
VPA[1]	Cb[1]	Y_0[1]	Cr[1]	Y_1[1]	VPB[1]	Cb[5]	Y_0[5]	Cr[5]	Y_1[5]	VSYNC/VREF	used
VPA[2]	Cb[2]	Y_0[2]	Cr[2]	Y_1[2]	VPB[2]	Cb[6]	Y_0[6]	Cr[6]	Y_1[6]	DE/FREF	used
VPA[3]	Cb[3]	Y_0[3]	Cr[3]	Y_1[3]	VPB[3]	Cb[7]	Y_0[7]	Cr[7]	Y_1[7]		
VPA[4]	-	-	-	-	VPB[4]	Cb[8]	Y_0[8]	Cr[8]	Y_1[8]		
VPA[5]	-	-	-	-	VPB[5]	Cb[9]	Y_0[9]	Cr[9]	Y_1[9]		
VPA[6]	-	-	-	-	VPB[6]	Cb[10]	Y_0[10]	Cr[10]	Y_1[10]		
VPA[7]	-	-	-	-	VPB[7]	Cb[11]	Y_0[11]	Cr[11]	Y_1[11]		

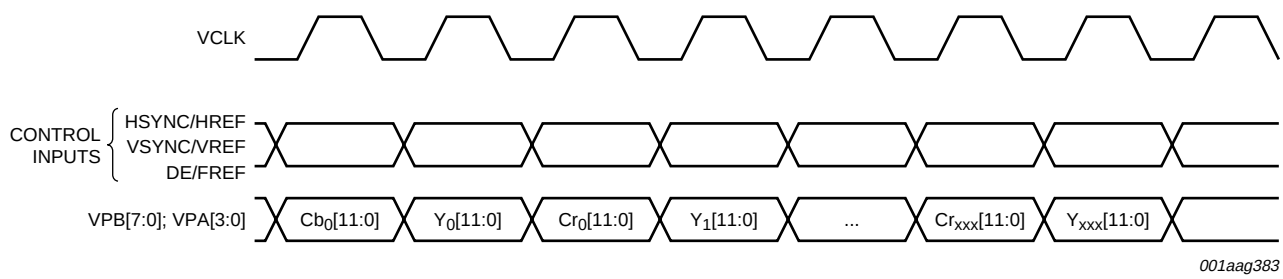


Fig 6. Pixel encoding YCbCr 4 : 2 : 2 ITU656-like external sync input (rising edge)

8.1.2.4 YCbCr 4 : 2 : 2 ITU656-like external sync input (rising and falling)

Table 9. YCbCr 4 : 2 : 2 ITU656-like double edge mapping

Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 00h.

Video port A					Video port B					Control	
Pin	YCbCr 4 : 2 : 2 (ITU656-like)				Pin	YCbCr 4 : 2 : 2 (ITU656-like)				Pin	YCbCr 4 : 2 : 2
VPA[0]	Cb[0]	Y_0[0]	Cr[0]	Y_1[0]	VPB[0]	Cb[4]	Y_0[4]	Cr[4]	Y_1[4]	HSYNC/HREF	used
VPA[1]	Cb[1]	Y_0[1]	Cr[1]	Y_1[1]	VPB[1]	Cb[5]	Y_0[5]	Cr[5]	Y_1[5]	VSYNC/VREF	used
VPA[2]	Cb[2]	Y_0[2]	Cr[2]	Y_1[2]	VPB[2]	Cb[6]	Y_0[6]	Cr[6]	Y_1[6]	DE/FREF	used
VPA[3]	Cb[3]	Y_0[3]	Cr[3]	Y_1[3]	VPB[3]	Cb[7]	Y_0[7]	Cr[7]	Y_1[7]		
VPA[4]	-	-	-	-	VPB[4]	Cb[8]	Y_0[8]	Cr[8]	Y_1[8]		
VPA[5]	-	-	-	-	VPB[5]	Cb[9]	Y_0[9]	Cr[9]	Y_1[9]		
VPA[6]	-	-	-	-	VPB[6]	Cb[10]	Y_0[10]	Cr[10]	Y_1[10]		
VPA[7]	-	-	-	-	VPB[7]	Cb[11]	Y_0[11]	Cr[11]	Y_1[11]		

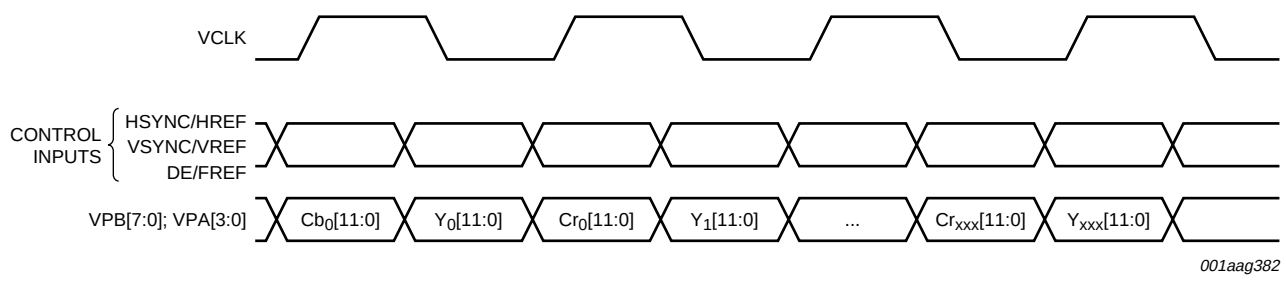


Fig 7. Pixel encoding YCbCr 4 : 2 : 2 ITU656-like external sync input (rising and falling)

8.1.2.5 YCbCr 4 : 2 : 2 ITU656-like embedded sync input (rising edge)

Table 10. YCbCr 4 : 2 : 2 ITU656-like embedded rising edge mapping

Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 00h.

Video port A					Video port B					Control	
Pin	YCbCr 4 : 2 : 2 (ITU656-like)				Pin	YCbCr 4 : 2 : 2 (ITU656-like)				Pin	YCbCr 4 : 2 : 2
VPA[0]	Cb[0]	Y_0[0]	Cr[0]	Y_1[0]	VPB[0]	Cb[4]	Y_0[4]	Cr[4]	Y_1[4]	HSYNC/HREF	not used
VPA[1]	Cb[1]	Y_0[1]	Cr[1]	Y_1[1]	VPB[1]	Cb[5]	Y_0[5]	Cr[5]	Y_1[5]	VSYNC/VREF	not used
VPA[2]	Cb[2]	Y_0[2]	Cr[2]	Y_1[2]	VPB[2]	Cb[6]	Y_0[6]	Cr[6]	Y_1[6]	DE/FREF	not used
VPA[3]	Cb[3]	Y_0[3]	Cr[3]	Y_1[3]	VPB[3]	Cb[7]	Y_0[7]	Cr[7]	Y_1[7]		
VPA[4]	-	-	-	-	VPB[4]	Cb[8]	Y_0[8]	Cr[8]	Y_1[8]		
VPA[5]	-	-	-	-	VPB[5]	Cb[9]	Y_0[9]	Cr[9]	Y_1[9]		
VPA[6]	-	-	-	-	VPB[6]	Cb[10]	Y_0[10]	Cr[10]	Y_1[10]		
VPA[7]	-	-	-	-	VPB[7]	Cb[11]	Y_0[11]	Cr[11]	Y_1[11]		

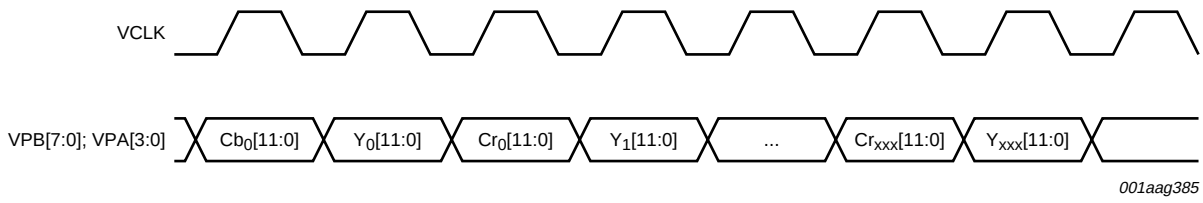


Fig 8. Pixel encoding YCbCr 4 : 2 : 2 ITU656-like embedded sync input (rising edge)

8.1.2.6 YCbCr 4 : 2 : 2 ITU656-like embedded sync input (rising and falling)

Table 11. YCbCr 4 : 2 : 2 ITU656-like embedded double edge mappings

Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 00h.

Video port A					Video port B					Control	
Pin	YCbCr 4 : 2 : 2 (ITU656-like)				Pin	YCbCr 4 : 2 : 2 (ITU656-like)				Pin	YCbCr 4 : 2 : 2
VPA[0]	Cb[0]	Y_0[0]	Cr[0]	Y_1[0]	VPB[0]	Cb[4]	Y_0[4]	Cr[4]	Y_1[4]	HSYNC/HREF	not used
VPA[1]	Cb[1]	Y_0[1]	Cr[1]	Y_1[1]	VPB[1]	Cb[5]	Y_0[5]	Cr[5]	Y_1[5]	VSYNC/VREF	not used
VPA[2]	Cb[2]	Y_0[2]	Cr[2]	Y_1[2]	VPB[2]	Cb[6]	Y_0[6]	Cr[6]	Y_1[6]	DE/FREF	not used
VPA[3]	Cb[3]	Y_0[3]	Cr[3]	Y_1[3]	VPB[3]	Cb[7]	Y_0[7]	Cr[7]	Y_1[7]		
VPA[4]	-	-	-	-	VPB[4]	Cb[8]	Y_0[8]	Cr[8]	Y_1[8]		
VPA[5]	-	-	-	-	VPB[5]	Cb[9]	Y_0[9]	Cr[9]	Y_1[9]		
VPA[6]	-	-	-	-	VPB[6]	Cb[10]	Y_0[10]	Cr[10]	Y_1[10]		
VPA[7]	-	-	-	-	VPB[7]	Cb[11]	Y_0[11]	Cr[11]	Y_1[11]		

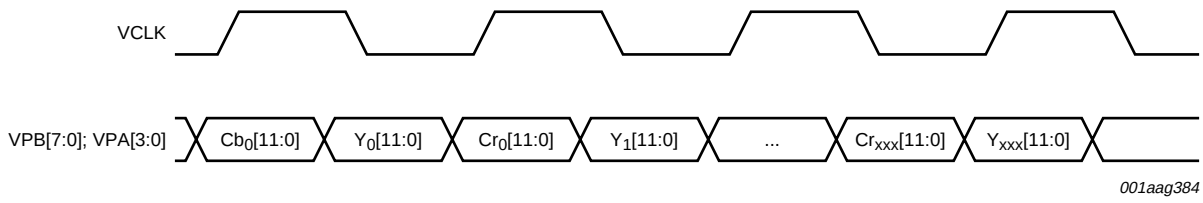


Fig 9. Pixel encoding YCbCr 4 : 2 : 2 ITU656-like embedded sync input (rising and falling)

8.1.2.7 YCbCr 4 : 2 : 2 semi-planar external input (rising edge)

Table 12. YCbCr 4 : 2 : 2 semi-planar rising edge mapping

Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 14h.

Video port A			Video port B			Video port C			Control	
Pin	YCbCr 4 : 2 : 2 semi-planar		Pin	YCbCr 4 : 2 : 2 semi-planar		Pin	YCbCr 4 : 2 : 2 semi-planar		Pin	YCbCr 4 : 2 : 2
VPA[0]	Y_0[0]	Y_1[0]	VPB[0]	Y_0[4]	Y_1[4]	VPC[0]	Cb[4]	Cr[4]	HSYNC/HREF	used
VPA[1]	Y_0[1]	Y_1[1]	VPB[1]	Y_0[5]	Y_1[5]	VPC[1]	Cb[5]	Cr[5]	VSYNC/VREF	used
VPA[2]	Y_0[2]	Y_1[2]	VPB[2]	Y_0[6]	Y_1[6]	VPC[2]	Cb[6]	Cr[6]	DE/FREF	used
VPA[3]	Y_0[3]	Y_1[3]	VPB[3]	Y_0[7]	Y_1[7]	VPC[3]	Cb[7]	Cr[7]		
VPA[4]	Cb[0]	Cr[0]	VPB[4]	Y_0[8]	Y_1[8]	VPC[4]	Cb[8]	Cr[8]		
VPA[5]	Cb[1]	Cr[1]	VPB[5]	Y_0[9]	Y_1[9]	VPC[5]	Cb[9]	Cr[9]		
VPA[6]	Cb[2]	Cr[2]	VPB[6]	Y_0[10]	Y_1[10]	VPC[6]	Cb[10]	Cr[10]		
VPA[7]	Cb[3]	Cr[3]	VPB[7]	Y_0[11]	Y_1[11]	VPC[7]	Cb[11]	Cr[11]		

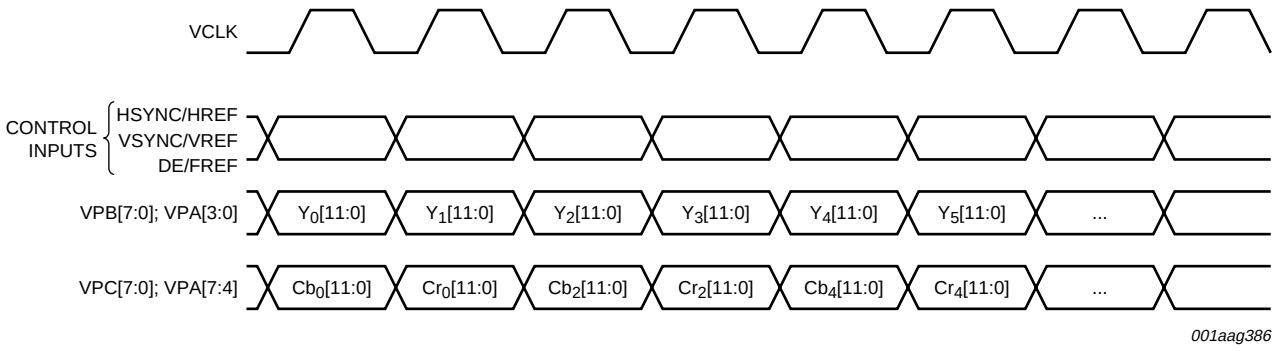


Fig 10. Pixel encoding YCbCr 4 : 2 : 2 semi-planar external input (rising edge)

8.1.2.8 YCbCr 4 : 2 : 2 semi-planar embedded sync input (rising edge)

Table 13. YCbCr 4 : 2 : 2 semi-planar embedded rising edge mapping

Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 14h.

Video port A			Video port B			Video port C			Control	
Pin	YCbCr 4 : 2 : 2 semi-planar		Pin	YCbCr 4 : 2 : 2 semi-planar		Pin	YCbCr 4 : 2 : 2 semi-planar		Pin	YCbCr 4 : 2 : 2
VPA[0]	Y_0[0]	Y_1[0]	VPB[0]	Y_0[4]	Y_1[4]	VPC[0]	Cb[4]	Cr[4]	HSYNC/HREF	not used
VPA[1]	Y_0[1]	Y_1[1]	VPB[1]	Y_0[5]	Y_1[5]	VPC[1]	Cb[5]	Cr[5]	VSYNC/VREF	not used
VPA[2]	Y_0[2]	Y_1[2]	VPB[2]	Y_0[6]	Y_1[6]	VPC[2]	Cb[6]	Cr[6]	DE/FREF	not used
VPA[3]	Y_0[3]	Y_1[3]	VPB[3]	Y_0[7]	Y_1[7]	VPC[3]	Cb[7]	Cr[7]		
VPA[4]	Cb[0]	Cr[0]	VPB[4]	Y_0[8]	Y_1[8]	VPC[4]	Cb[8]	Cr[8]		
VPA[5]	Cb[1]	Cr[1]	VPB[5]	Y_0[9]	Y_1[9]	VPC[5]	Cb[9]	Cr[9]		
VPA[6]	Cb[2]	Cr[2]	VPB[6]	Y_0[10]	Y_1[10]	VPC[6]	Cb[10]	Cr[10]		
VPA[7]	Cb[3]	Cr[3]	VPB[7]	Y_0[11]	Y_1[11]	VPC[7]	Cb[11]	Cr[11]		

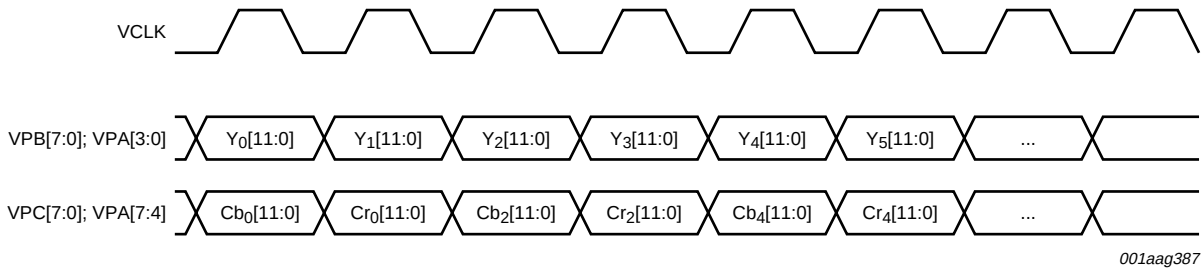


Fig 11. Pixel encoding YCbCr 4 : 2 : 2 semi-planar embedded sync input (rising edge)

8.1.3 Synchronization

The TDA9984A can be synchronized with external input signals HSYNC and VSYNC or with extraction of the sync information from embedded sync codes (SAV/EAV) inside the video.

8.1.3.1 Timing extraction generator

This block can extract the synchronization signals HREF, VREF and FREF from SAV and EAV in case of embedded synchronization in the data stream.

Synchronization signals can be embedded in YCbCr 4 : 2 : 2 ITU656 (up to 1 × 12-bit) and semi-planar (up to 2 × 12-bit).

8.1.3.2 Data enable generator

TDA9984A contains a Data Enable (DE) generator. This circuit generates an internal DE signal for a system which does not provide one. The DE generator is controlled via the I^2C-bus register.

8.1.4 Input and output video format

Due to the flexible video input formatter, the TDA9984A can accept a large range of inputs formats. This flexibility allows the TDA9984A to be compatible with the maximum number of MPEG decoders. Moreover, these input formats may be changed in many ways (space color converter, upsampler and scaler) to be transmitted across the HDMI link.
Table 14 gives the possible inputs and outputs.

Table 14. Inputs and outputs capability

Input			Scaler	Output		
Space color	**Format**	**Channels**		**Space color**	**Format**	**Channels**
RGB	4 : 4 : 4	3 × 8-bit	no scaling	RGB	4 : 4 : 4	3 × 8-bit
				YCbCr	4 : 4 : 4	3 × 8-bit
				YCbCr	4 : 2 : 2	2 × 12-bit
YCbCr	4 : 4 : 4	3 × 8-bit	no scaling	RGB	4 : 4 : 4	3 × 8-bit
				YCbCr	4 : 4 : 4	3 × 8-bit
				YCbCr	4 : 2 : 2	2 × 12-bit
YCbCr	4 : 2 : 2	up to 1 × 12-bit semi-planar	scaling	RGB	4 : 4 : 4	3 × 8-bit
				YCbCr	4 : 4 : 4	3 × 8-bit
				YCbCr	4 : 2 : 2	2 × 12-bit
		up to 2 × 12-bit semi-planar	scaling	RGB	4 : 4 : 4	3 × 8-bit
				YCbCr	4 : 4 : 4	3 × 8-bit
				YCbCr	4 : 2 : 2	2 × 12-bit

8.1.5 Scaler unit

8.1.5.1 Scaler features

The scaler unit has the following features:

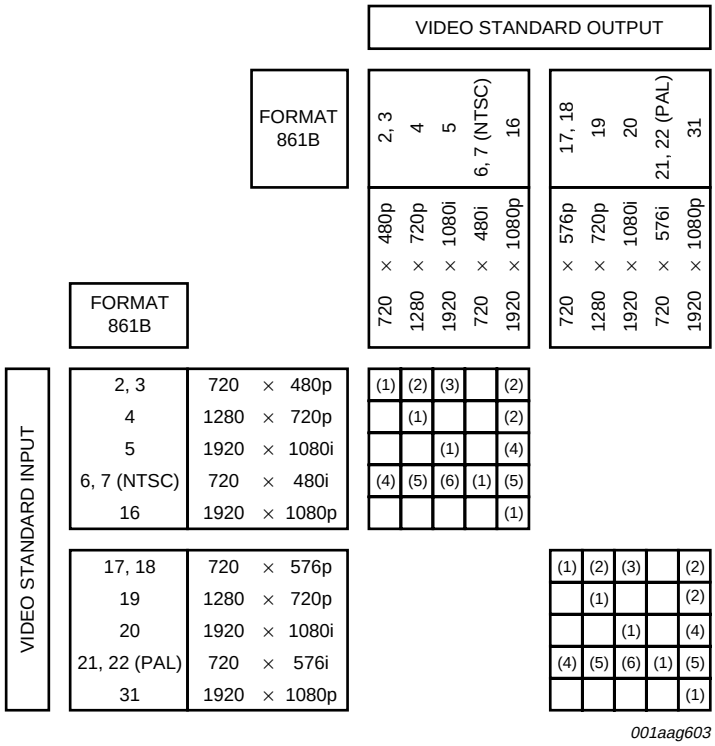
- Up-scaling only: to expand input image horizontally and vertically
- Deinterlacer embedded (no need of output memory)
- Data processing: 12-bit data width

- Maximum output operating frequency is 148.5 MHz; HDTV supported 1080p both PAL and NTSC
- Input video standards YCbCr 4 : 2 : 2 semi-planar and ITU656 (no RGB, nor YCbCr 4 : 4 : 4)

8.1.5.2 Input and output video scaler

The scaler will convert the standard definition (high definition respectively) video signals (480i/576i, 480p/576p and 720p, 1080i respectively) into 1080p as described in Figure 12.

Remark: All 4 : 2 : 2 input video formats can be bypassed, as well as all RGB and YCbCr 4 : 4 : 4 input data, which will be directly fed to the color space converter.



All upscaling modes are available only for YCbCr 4 : 2 : 2 input format.

(1) Pass-through
(2) Upscaling
(3) Upscaling and interlacing
(4) Deinterlacing
(5) Deinterlacing and upscaling
(6) Deinterlacing, upscaling and interlacing

Fig 12. Input and output video scaler

8.1.6 Upsampler

The incoming YCbCr 4 : 2 : 2 (2 × 12-bit) data stream format can be upsampled into an 8-bit YCbCr 4 : 4 : 4 (3 × 8-bit) data stream by repeating or linearly interpolating the chrominance pixels.

8.1.7 Color space converter

The color-space converter is used to convert input video data from one type to another color space (e.g. RGB to YCbCr and YCbCr to RGB). This block can be bypassed and each coefficient is programmable by the I²C-bus registers.

$$\begin{bmatrix} YG \\ CrR \\ CbB \end{bmatrix} = \begin{bmatrix} C_{11} & C_{12} & C_{13} \\ C_{21} & C_{22} & C_{23} \\ C_{31} & C_{32} & C_{33} \end{bmatrix} \times \left(\begin{bmatrix} GY \\ RCr \\ BCb \end{bmatrix} + \begin{bmatrix} Oin_{GY} \\ Oin_{RCr} \\ Oin_{BCb} \end{bmatrix} \right) + \begin{bmatrix} Oout_{YG} \\ Oout_{CrR} \\ Oout_{CbB} \end{bmatrix} \quad (1)$$

8.1.8 Downsampler

This block works only with YCbCr input format. These filters downsample the Cb and Cr signals by a factor of two. A delay is added on the G/Y channel, which corresponds to the pipeline delay of the filters, to put the Y channel in phase with the Cb and Cr channel.

8.2 Audio processing

The TDA9984A is compatible with audio features as per *HDMI specification, Rev. 1.3*:

- S/PDIF
- I²S-bus up to four channels
- Dolby-True HD and DTS-HD through the use of HBR interface

S/PDIF, I²S-bus or HBR can be selected via the I²C-bus. Only one audio format can be used at a same time. Table 15 shows the audio port allocation.

Table 15. Audio port configuration

Audio port	Format		
	S/PDIF	I²S-bus	HBR
AP0	-	WS (word select)	WS (word select)
AP1	-	I²S-bus channel 0	HBR channel 0
AP2	-	I²S-bus channel 1	HBR channel 1
AP3	-	I²S-bus channel 2	HBR channel 2
AP4	-	I²S-bus channel 3	HBR channel 3
AP5	MCLK	-	-
AP6	S/PDIF input	-	-
AP7	AUX (internal test)	AUX (internal test)	AUX (internal test)
ACLK	-	SCK	SCK

All audio ports are LV-TTL compatible.

It is possible to map internally an unused port to internal ground via the I²C-bus registers ENA_APx and GND_APx on page 00h (both audio inputs and clock input as well).

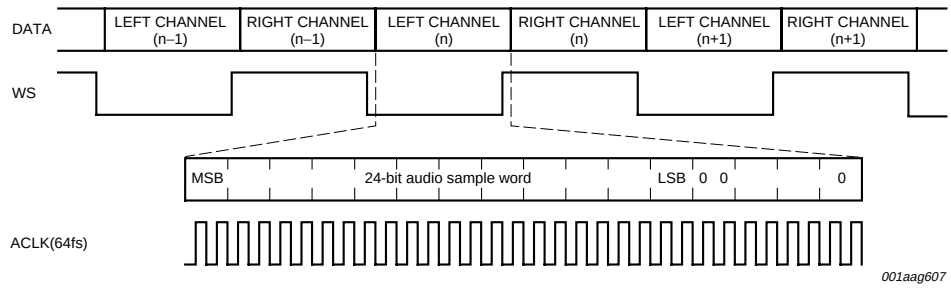
8.2.1 S/PDIF

The audio port AP6 is used for this feature. In this format, the TDA9984A supports 2-channel uncompressed PCM data (IEC 60958) layout 0, or compressed bit stream up to 8 multi-channels (Dolby Digital, DTS, AC3, etc.) layout 1.

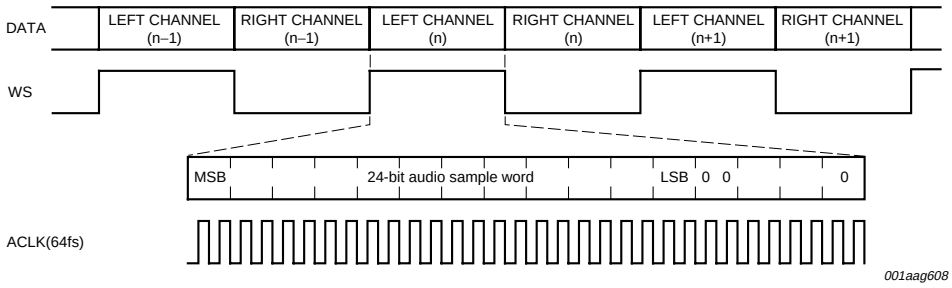
The TDA9984A is able to recover the original clock from the S/PDIF signal (no need of external clock). In addition, it can also use an external clock to decode the S/PDIF signal.

8.2.2 I²S-bus

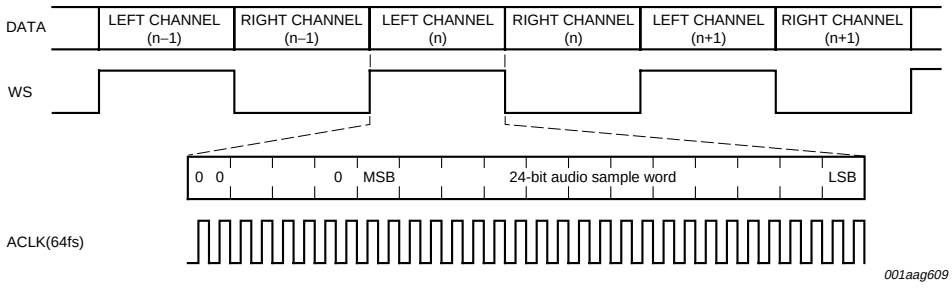
There are 4 × I²S-bus stereo inputs channels (AP1, AP2, AP3 and AP4) which allow carrying eight uncompressed audio channels. The I²S-bus input interface receives an I²S-bus signal including serial data in, word select and serial clock. Various I²S-bus formats are supported and can be selected by setting the appropriate bits of the register. Typical waveforms for the I²S-bus signals at 64f_s are given in Figure 13.



a. Philips format



b. Left justified format



c. Right justified format

Fig 13. I²S-bus formats

The I²S-bus input interface can receive up to 24-bit wide audio samples via the serial data input with a clock frequency of at least 32 times the input sample frequency f_s. Audio samples with a precision better than 24 bits are truncated to 24-bit format.

If the input clock has a frequency of $32f_s$, only 16-bit audio samples can be received. If the input clock has a frequency of $64f_s$ and is left justified or Philips, the audio word is truncated to 24-bit format and padded with zeros. If the input clock has a frequency of $64f_s$ and is right justified, audio sample must be strictly 24-bit length.

The word select signal WS indicates whether left or right channel information is transferred over the serial data.

8.2.3 High bit rate audio

The High Bit Rate audio format is used to support both DTS-HD and Dolby-True HD audio format provided for instance by Blu-Ray DVD. The transmitter is capable to receive a single High Bit Rate IEC 61937 stream at a frame rate of 768 kHz. This is typically stripped across $4 \times I^2S$-bus interface to the HDMI transmitter with a corresponding I^2S-bus clock rate of 192 kHz.

As for I^2S-bus, no additional information is required on the audio infoframe. All relevant information are carried on the stream through the use of the channel status bit via the I^2C-bus table.

8.3 HDCP processing

8.3.1 High-bandwidth digital content protection

The HDMI transmitter contains an HDCP function, which encrypts the transmitted stream content (both video and audio). This function can be enabled and disabled via the I^2C-bus.

The keys can be stored internally in OTP non-volatile memory or can be loaded via the I^2C-bus. As the keys are stored internally, the security is maximized.

8.3.1.1 Repeater function

The TDA9984A can be used in a repeater device according to the *HDCP specification, Rev 1.2*. The TDA9984A is able to store the KSV list of a maximum of 127 devices in a register memory.

8.3.1.2 SHA-1

To deal with repeater, a SHA-1 calculation is performed by the transmitter and by the downstream repeater. For security purposes and in order to relieve the microcontroller, the SHA-1 has been implemented within the TDA9984A.

This calculation is worked out after the transmitter has loaded the KSV list (see *HDCP specification, Rev 1.2*). If SHA-1 calculated by transmitter equals the SHA-1 calculated by repeater, then an interrupt is sent.

8.4 TMDS serializer

8.4.1 RxSense detection

The TDA9984A has the capability to sense the receiver connectivity and working behavior. This feature detects the presence of the 50 Ω pull-up resistor R_T on the downstream side onto the TMDS clock channel.

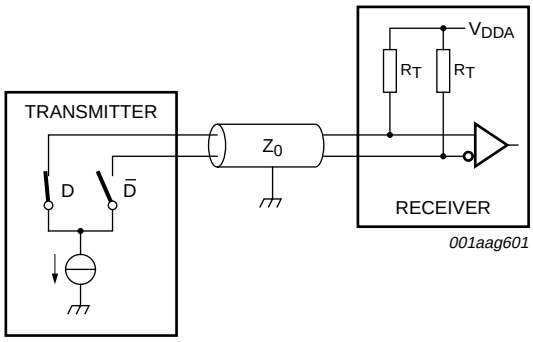


Fig 14. Receiver sensitivity detection

As long as the receiver is connected to the transmitter and powered up, bit RXS_FIL is set to logic 1 (see register INT_FLAGS_3, page 00h, address 12h).

As soon as the cable is unplugged or the receiver side is powered off (assuming in this case that V_{DD} is switched off), the RxSense generates an interrupt inside the TDA9984A, changing the value of bit RXS_FIL to logic 0. This allows the application to stop sending unnecessary video content.

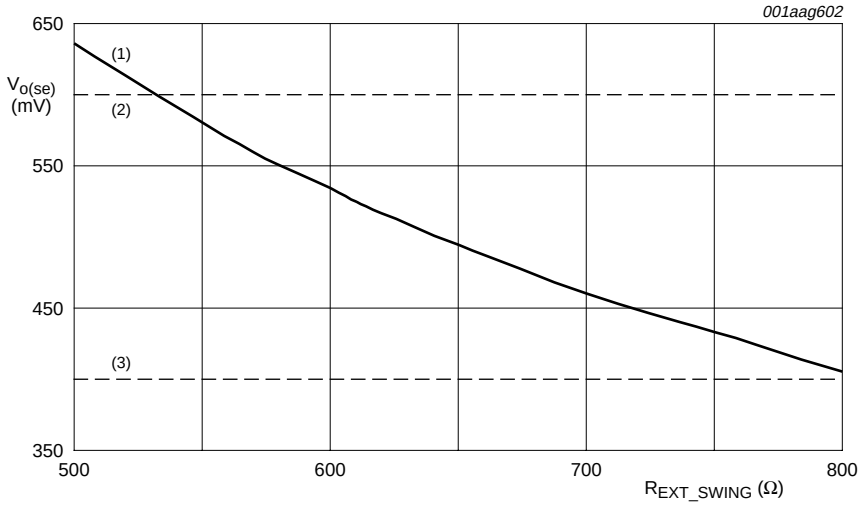
This feature is very useful when the receiver has been recovered from an off-state and does not generate a HPD transition HIGH-to-LOW-to-HIGH. In this particular case, RxSense will generate an interrupt so that the TDA9984A restarts sending video.

Remark: According to the HDMI specification, only the HPD interrupt allows the application to read the EDID. RxSense is not mandatory to initialize the EDID reading procedure.

8.4.2 TMDS output buffers

The TMDS output amplitude can be adjusted via an external resistor connected between pins EXT_SWING and $V_{DDH(3V3)}$; see Figure 15.

It is strongly recommended to use R_{EXT_SWING} = 610 Ω ± 1 % to get a nominal swing of 500 mV. By doing so, the TDA9984A shall meet the minimum low-level output voltage as per *HDMI specification, Rev 1.3a table 4-15.*



(1) Swing character data

(2) Upper limit (600 mV)

(3) Lower limit (400 mV)

Fig 15. TMDS single-ended output swing as a function of external resistor R_{EXT_SWING}

8.4.3 Pixel repetition

To transmit video formats with pixel rates below 25 mega samples per second or to increase the number of audio sample packets in each frame, the TDA9984A uses pixel repetition to increase the number of pixels sent by the frame. The pixel clock is multiplied by the same factor as given in Table 16.

Table 16. Pixel repetition

PR[3:0]	Pixel repetition factor
0000	no repetition: pixel sent once
0001	2 times: pixel repeated once
0010	3 times
0011	4 times
0100	5 times
0101	6 times
0110	7 times
0111	8 times
1000	9 times
1001	10 times
Others	reserved

8.5 Control blocks

8.5.1 Clock management

The system clock is composed of a series of three PLLs, which will generates different clocks in the system taking into account the double edge, the scaling ratio and the serialization.

Here is described briefly the clock system architecture:

- PLL double edge: generates a clock at twice the VCLK input frequency to capture correctly the data at the video formatter input
- PLL scaling: creates a new video processing scaled clock taking into account the scaling ratio programmed in the scaler
- PLL serializer: a system clock generator, which enables the stream produced by the encoder to be transmitted on the TMDS data channel at ten times or above the sampling rate; see Section 8.4.3

Each PLL can be bypassed via the I^2C-bus and then external clock VCLK can be provided independently to each block.

8.5.2 Interrupt controller

Pin INT is used to alert the microcontroller that a critical event concerning the HDMI has occurred. Some of theses interrupts are maskable. See Table 17 for the interrupt types generated by the TDA9984A.

Table 17. Interrupts

Interrupt		Definition	Maskable feature
Domain	**Interrupt name**		
HDCP	r0	r0 = R'0 check done	maskable
	pj	pj = P'j check fails	
	sha-1	V = V' check success	
	bstatus	bstatus available	
	bcaps	bcaps available	
	t0	HDCP goes to initial state	
	security	HDCP encryption is off or blue screen removed	not maskable
HPD	hpd	transition on HPD input	maskable
RxSense	rx_sense	transition on RxSense	
EDID	edid_block_rd	EDID block read finished	
Interrupt	sw_intsoftware	test purpose	

8.5.3 Hot plug detection

Pin HPD is the hot plug detect pin; it is 5 V input tolerant. When asserted, the hot plug detect signal tells the transmitter that the receiver is connected. When changing from LOW to HIGH, the TDA9984A has to read EDID to match the video format to the format the receiver can handle.

8.5.4 Initialization

After power-up, the TDA9984A is activated by a hard reset. Pin RST_N can be used to activate the TDA9984A in a known state.

The device also offers the possibility to perform a soft reset that will affect a certain number of I^2C-bus registers, but not all of them. This soft reset is also mandatory for a proper initialization of the device.

8.5.5 Power management

The TDA9984A can be powered down via the I²C-bus register. In this mode, all PLLs are switched off and the biasing structure of the output stage is disconnected (all activity is reduced). Therefore, the TDA9984A has a very low power consumption which is suitable for portable applications.

8.6 DDC-bus interface

8.6.1 DDC-bus channel

The DDC-bus pins DDC_SDA and DDC_SCL are 5 V tolerant and can work at Standard-mode (100 kHz) and Fast-mode (400 kHz). The DDC-bus is used as a master interface in case of EDID reading, and while proceeding for HDCP. It is recommended not going beyond 100 kHz for EDID as claimed by the HDMI specification. This frequency is linked to the internal free running oscillator whose nominal frequency is 30 MHz as:

$$f_{DDC} = \frac{f_{FRO}}{3 \times 2N_{clk-div}} \quad (2)$$

Where:

f_{FRO} = free running oscillator frequency

$N_{clk\text{-}div}$ = value set by register

Then for convenience, it is recommended to keep the same frequency for HDCP purpose.

8.6.2 E-EDID

8.6.2.1 E-EDID reading

As a master interface for the EDID process, the DDC-bus is compliant to the *I²C-bus specification* and has the possibility of the repeat and start condition to enable quick access to the EDID content, as well as the large EDID reading possibility (with the use of a segment pointer).

The TDA9984A has a full I²C-bus page (page 09h) dedicated to the EDID where one block can be stored. The block can be read by the microprocessor to determine the supported video and audio format of the downstream side.

Remark: When the block is read by the TDA9984A, it generates an interrupt to warn the main processor that the TDA9984A is ready to transmit the content. Once the content is read-out by the microprocessor, it can allow reading other blocks if required.

8.6.2.2 HDMI and DVI receiver discrimination

This information is located in the E-EDID receiver part, more exactly in the ‘Vendor Specific Data block within the first CEA EDID timing extension.

If the 24-bit IEEE Registration Identifier contains the value 00 0C03h, then the receiver will support HDMI; otherwise the device shall be treated as a DVI device.

However, even though the TDA9984A have directly access to that information, this is the task of the microcontroller to ask to switch from DVI to HDMI mode.

8.7 I²C-bus interface

The I²C-bus pins I2C_SDA and I2C_SCL are 5 V tolerant. Pin I2C_SCL is only an input pin. Both Fast-mode (400 kHz) and Standard-mode (100 kHz) are supported. The registers of the TDA9984A can be accessed via the I²C-bus. All registers are R/W except some, which cannot be read for confidentiality.

The TDA9984A is used as a slave I²C-bus device. Bits A0 and A1 of the I²C-bus device address are externally selected by pins A0 and A1 (see Table 18).

Table 18. Device address

Device address							W/R
A6	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**-**
1	1	1	0	0	pin A1	pin A0	0/1

The I²C-bus access format is shown in Figure 16.

Firstly, the master writes the TDA9984A address and the subaddress to access the specific register, and then the data.

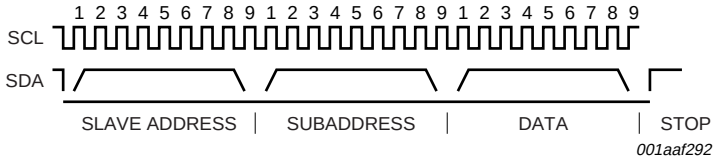


Fig 16. I²C-bus access

9. I²C-bus registers definitions

9.1 Memory page management

The I²C-bus memory is split into several pages and the selection between pages is made with common register CURPAGE_ADR. It is only necessary to write in this register once to change the current page. So multiple read or write operations in the same page need a write register CURPAGE_ADR once at the beginning.

Table 19. Memory pages

Page address	Memory page description
00h	general control
01h	scaler and PLL scaling
02h	PLL settings
09h	EDID control page
10h	InfoFrames and packets
11h	audio settings and content info packets
12h	HDCP and OTP

9.2 ID version

The ID-version readable via I²C-bus is defined as follows:

- TDA9984AHW will have the value 1000 XXXX

The four LSBs are used for indicating the die version.

10. Limiting values

Table 20. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD(3V3)}$	supply voltage (3.3 V)		–0.5	+4.6	V
$V_{DD(1V8)}$	supply voltage (1.8 V)		–0.5	+2.5	V
ΔV_{DD}	supply voltage difference		–0.5	+0.5	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–5	+85	°C
T_j	junction temperature		-	+125	°C
V_{esd}	electrostatic discharge voltage	human body model	-	±2000	V

11. Thermal characteristics

Table 21. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	26.5	K/W

12. Static characteristics

Table 22. Supplies

$V_{DD(3V3)}$ = 3.3 V; $V_{DD(1V8)}$ = 1.8 V; V_{PP} = 0 V; T_{amb} = –5 °C to +85 °C; unless otherwise specified.
Typical values are measured at T_{amb} = 25 °C and f_{clk} = 150 MHz.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{PP}	programming voltage			5.0	5.25	5.5	V
$V_{DDA(FRO)(3V3)}$	free running oscillator analog supply voltage (3.3 V)			3.0	3.3	3.6	V
$V_{DDA(PLL)(3V3)}$	PLL analog supply voltage (3.3 V)			3.0	3.3	3.6	V
$V_{DDD(3V3)}$	digital supply voltage (3.3 V)			3.0	3.3	3.6	V
$V_{DDH(3V3)}$	HDMI supply voltage (3.3 V)			3.0	3.3	3.6	V
$V_{DDC(1V8)}$	core supply voltage (1.8 V)			1.65	1.8	1.95	V
$V_{DDA(PLL)(1V8)}$	PLL analog supply voltage (1.8 V)			1.65	1.8	1.95	V
$I_{DDA(FRO)(3V3)}$	free running oscillator analog supply current (3.3 V)			-	0.1	1	mA
$I_{DDA(PLL)(3V3)}$	PLL analog supply current (3.3 V)	input 1080i, output 1080p	[1][2]	-	6	6.4	mA
$I_{DDD(3V3)}$	digital supply current (3.3 V)	input 1080p, output 1080p	[1][4]	-	-	5	mA
$I_{DDH(3V3)}$	HDMI supply current (3.3 V)			-	14	15	mA
$I_{DDA(PLL)(1V8)}$	PLL analog supply current (1.8 V)	input 1080i, output 1080p	[1][2]	-	75	92	mA
$I_{DDC(1V8)}$	core supply current (1.8 V)	input 1080i, output 1080p	[1][2]	-	283	345	mA

Table 22. Supplies *...continued*

$V_{DD(3V3)}$ = 3.3 V; $V_{DD(1V8)}$ = 1.8 V; V_{PP} = 0 V; T_{amb} = −5 °C to +85 °C; unless otherwise specified. Typical values are measured at T_{amb} = 25 °C and f_{clk} = 150 MHz.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
P_{cons}	power consumption	input 480p, output 1080p	[1][3]	-	500	630	mW
		input 1080i, output 1080p	[1][2]	-	742	940	mW
		input 1080p, output 1080p	[1][4]	-	320	400	mW
P_{tot}	total power dissipation	TMDS output current added					
		input 480p, output 1080p	[1][3]	-	630	770	mW
		input 1080i, output 1080p	[1][2]	-	872	1080	mW
		input 1080p, output 1080p	[1][4]	-	450	540	mW
P_{pd}	power dissipation in power-down mode			-	30	40	mW

[1] The maximum current consumption is in this configuration for this group of pins.

[2] Video format:
a) Input 1080i, YCbCr 4 : 2 : 2 embedded sync, 48 kHz S/PDIF 2 channels.
b) Output 1080p, YCbCr 4 : 2 : 2, 48 kHz S/PDIF.

[3] Video format:
a) Input 480p, ITU656 embedded sync, 48 kHz S/PDIF 2 channels.
b) Output 1080p, YCbCr 4 : 2 : 2, 48 kHz S/PDIF.

[4] Video format:
a) Input 1080p, YCbCr 4 : 2 : 2 embedded sync, 48 kHz S/PDIF 2 channels.
b) Output 1080p, YCbCr 4 : 2 : 2, 48 kHz S/PDIF.

Table 23. LV-TTL digital inputs

$V_{DD(3V3)}$ = 3.3 V; $V_{DD(1V8)}$ = 1.8 V; V_{PP} = 0 V; T_{amb} = −5 °C to +85 °C; typical values are measured at T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Not 5 V tolerant inputs: pins HSYNC, VSYNC, AP[7:0], ACLK, TM, A0, A1, VPA[7:0], VPB[7:0], VPC[7:0], VCLK, DE and RST_N						
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
5 V tolerant input: pin HPD						
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
Output: pin INT						
V_{OL}	LOW-level output voltage	C_L = 10 pF; I_{OL} = 2 mA	-	-	0.4	V
V_{OH}	HIGH-level output voltage	C_L = 10 pF; I_{OH} = −2 mA	2.4	-	-	V

Table 24. TMDS outputs

$V_{DD(3V3)}$ = 3.3 V; $V_{DD(1V8)}$ = 1.8 V; V_{PP} = 0 V; T_{amb} = −5 °C to +85 °C; typical values are measured at T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TMDS output pins: TX0−, TX0+, TX1−, TX1+, TX2−, TX2+, TXC− and TXC+						
$V_{O(dif)}$	differential output voltage	R_{EXT_SWING} = 610 Ω (1 % tolerance); R_L = 50 Ω	480	525	560	mV

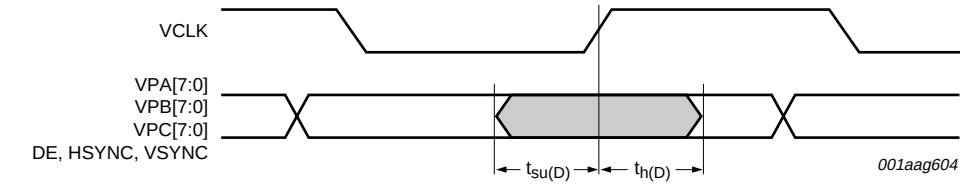
13. Dynamic characteristics

Table 25. Timing characteristics

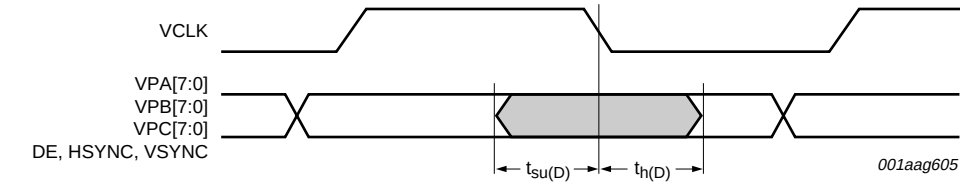
$V_{DD(3V3)}$ = 3.3 V; $V_{DD(1V8)}$ = 1.8 V; V_{PP} = 0 V; T_{amb} = −5 °C to +85 °C; typical values are measured at T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Video inputs; see Figure 17							
$f_{clk(max)}$	maximum clock frequency	pin VCLK		150	-	-	MHz
δ_{clk}	clock duty cycle	pin VCLK		40	50	60	%
$t_{su(D)}$	data input set-up time			1.0	-	-	ns
$t_{h(D)}$	data input hold time			0.8	-	-	ns
Audio input							
S/PDIF mode							
f_s	sampling frequency	2 channels		32	-	192	kHz
f_{clk}	clock frequency	pin AP5 (MCLK)	[1]	-	-	75	MHz
T_{clk}	clock period	pin AP5 (MCLK)	[1]	13.3	-	-	ns
δ_{clk}	clock duty cycle			40	-	60	%
HBR mode							
f_s	sampling frequency			-	192	192	kHz
I^2S-bus mode							
f_s	sampling frequency			32	-	192	kHz
TMDS output pins: TX0−, TX0+, TX1−, TX1+, TX2−, TX2+, TXC− and TXC+							
$f_{clk(max)}$	maximum clock frequency			150	-	-	MHz
DDC-bus; 5 V tolerant; master bus: pins DDC_SDA and DDC_SCL							
f_{SCL}	SCL clock frequency	Standard-mode		-	-	100	kHz
		Fast-mode		-	-	400	kHz
I^2C-bus; 5 V tolerant; slave bus: pins I2C_SDA and I2C_SCL							
f_{SCL}	SCL clock frequency	Standard-mode		-	-	100	kHz
		Fast-mode		-	-	400	kHz

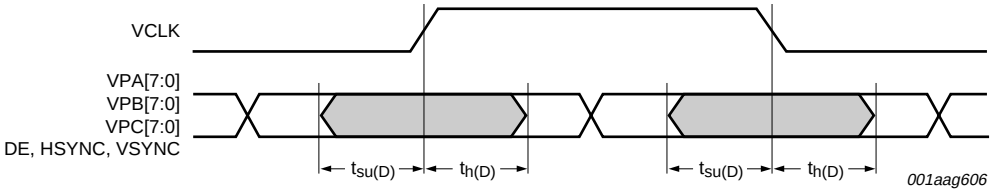
[1] In case of MCLK is required, this frequency has to be coherent with S/PDIF input.



a. Sync on rising edge



b. Sync on falling edge



c. Sync on rising and falling (double) edge

Data is not allowed to change in the shaded area.

Fig 17. Set-up and hold time for various clock modes

13.1 Input format

Mapping of the video ports:

- Port VPA has been mapped to Cb for YCbCr space and B for RGB color space
- Port VPB has been mapped to Y for YCbCr space and G for RGB color space
- Port VPC has been mapped to Cr for YCbCr space and R for RGB color space

Table 26. Input format

Input pins	Signal	RGB	YCbCr						
		4 : 4 : 4	4 : 4 : 4	4 : 2 : 2 (semi-planar)		4 : 2 : 2 (ITU656-like)[1]			
Video port A									
VPA[0]	Cb[0]/B[0]	B[0]	Cb[0]	Y_0[0]	Y_1[0]	Cb[0]	Y_0[0]	Cr[0]	Y_1[0]
VPA[1]	Cb[1]/B[1]	B[1]	Cb[1]	Y_0[1]	Y_1[1]	Cb[1]	Y_0[1]	Cr[1]	Y_1[1]
VPA[2]	Cb[2]/B[2]	B[2]	Cb[2]	Y_0[2]	Y_1[2]	Cb[2]	Y_0[2]	Cr[2]	Y_1[2]
VPA[3]	Cb[3]/B[3]	B[3]	Cb[3]	Y_0[3]	Y_1[3]	Cb[3]	Y_0[3]	Cr[3]	Y_1[3]
VPA[4]	Cb[4]/B[4]	B[4]	Cb[4]	Cb[0]	Cr[0]	L	L	L	L
VPA[5]	Cb[5]/B[5]	B[5]	Cb[5]	Cb[1]	Cr[1]	L	L	L	L
VPA[6]	Cb[6]/B[6]	B[6]	Cb[6]	Cb[2]	Cr[2]	L	L	L	L
VPA[7]	Cb[7]/B[7]	B[7]	Cb[7]	Cb[3]	Cr[3]	L	L	L	L

Table 26. Input format *…continued*

Input pins	Signal	RGB	YCbCr						
		4 : 4 : 4	4 : 4 : 4	4 : 2 : 2 (semi-planar)		4 : 2 : 2 (ITU656-like)[1]			
Video port B									
VPB[0]	Y[0]/G[0]	G[0]	Y[0]	Y_0[4]	Y_1[4]	Cb[4]	Y_0[4]	Cr[4]	Y_1[4]
VPB[1]	Y[1]/G[1]	G[1]	Y[1]	Y_0[5]	Y_1[5]	Cb[5]	Y_0[5]	Cr[5]	Y_1[5]
VPB[2]	Y[2]/G[2]	G[2]	Y[2]	Y_0[6]	Y_1[6]	Cb[6]	Y_0[6]	Cr[6]	Y_1[6]
VPB[3]	Y[3]/G[3]	G[3]	Y[3]	Y_0[7]	Y_1[7]	Cb[7]	Y_0[7]	Cr[7]	Y_1[7]
VPB[4]	Y[4]/G[4]	G[4]	Y[4]	Y_0[8]	Y_1[8]	Cb[8]	Y_0[8]	Cr[8]	Y_1[8]
VPB[5]	Y[5]/G[5]	G[5]	Y[5]	Y_0[9]	Y_1[9]	Cb[9]	Y_0[9]	Cr[9]	Y_1[9]
VPB[6]	Y[6]/G[6]	G[6]	Y[6]	Y_0[10]	Y_1[10]	Cb[10]	Y_0[10]	Cr[10]	Y_1[10]
VPB[7]	Y[7]/G[7]	G[7]	Y[7]	Y_0[11]	Y_1[11]	Cb[11]	Y_0[11]	Cr[11]	Y_1[11]
Video port C									
VPC[0]	Cr[0]/R[0]	R[0]	Cr[0]	Cb[4]	Cr[4]	L	L	L	L
VPC[1]	Cr[1]/R[1]	R[1]	Cr[1]	Cb[5]	Cr[5]	L	L	L	L
VPC[2]	Cr[2]/R[2]	R[2]	Cr[2]	Cb[6]	Cr[6]	L	L	L	L
VPC[3]	Cr[3]/R[3]	R[3]	Cr[3]	Cb[7]	Cr[7]	L	L	L	L
VPC[4]	Cr[4]/R[4]	R[4]	Cr[4]	Cb[8]	Cr[8]	L	L	L	L
VPC[5]	Cr[5]/R[5]	R[5]	Cr[5]	Cb[9]	Cr[9]	L	L	L	L
VPC[6]	Cr[6]/R[6]	R[6]	Cr[6]	Cb[10]	Cr[10]	L	L	L	L
VPC[7]	Cr[7]/R[7]	R[7]	Cr[7]	Cb[11]	Cr[11]	L	L	L	L

[1] L stands for tying to LOW voltage recommendation, e.g. ground.

13.2 Timing parameters for supported video

The TDA9984A supports all EIA/CEA-861B standards and ATSC video input formats.

Table 27. Timing parameters for EIA/CEA-861B

Format	Format	V frequency (Hz)	H total	V total	H frequency (kHz)	Pixel frequency (MHz)	Pixel repetition	Scaler
59.94 Hz systems								
1 (VGA)	640 × 480p	59.9401	800	525	31.469	25.175	1	-
2, 3	720 × 480p	59.9401	858	525	31.469	27.000	1	X
4	1280 × 720p	59.9401	1650	750	44.955	74.175	1	X
5	1920 × 1080i	59.9401	2200	1125	33.716	74.175	1	X
6, 7 (NTSC)	1440 × 480i	59.9401	1716	525	15.734	27.000	2	X
8, 9	1440 × 240p	59.9401	1716	262	15.734	27.000	2	-
8, 9	1440 × 240p	59.9401	1716	263	15.734	27.000	2	-
10, 11	2880 × 480i	59.9401	3452	525	15.734	54.000	4[1]	-
12, 13	2880 × 240p	59.9401	3452	262	15.734	54.000	4[1]	-
12, 13	2880 × 240p	59.9401	3452	263	15.734	54.000	4[1]	-
14, 15	1440 × 480p	59.9401	1716	525	31.469	54.000	2	-
16	1920 × 1080p	59.9401	2200	1125	67.432	148.350	1	-
60 Hz systems								
1 (VGA)	640 × 480p	60.000	800	525	31.500	25.200	1	-
2, 3	720 × 480p	60.000	858	525	31.500	27.027	1	X
4	1280 × 720p	60.000	1650	750	45.000	74.250	1	X
5	1920 × 1080i	60.000	2200	1125	33.750	74.250	1	X
6, 7 (NTSC)	1440 × 480i	60.000	1716	525	15.750	27.027	2	X
8, 9	1440 × 240p	60.000	1716	262	15.750	27.027	2	-
8, 9	1440 × 240p	60.000	1716	263	15.750	27.027	2	-
10, 11	2880 × 480i	60.000	3452	525	15.750	54.054	4[1]	-
12, 13	2880 × 240p	60.000	3452	262	15.750	54.054	4[1]	-
12, 13	2880 × 240p	60.000	3452	263	15.750	54.054	4[1]	-
14, 15	1440 × 480p	60.000	1716	525	31.500	54.054	2	-
16	1920 × 1080p	60.000	2200	1125	67.500	148.50	1	-
50 Hz systems								
17, 18	720 × 576p	50.000	864	625	31.250	27.000	1	X
19	1280 × 720p	50.000	1980	750	37.500	74.250	1	X
20	1920 × 1080i	50.000	2640	1125	28.125	74.250	1	X
21, 22 (PAL)	1440 × 576i	50.000	1728	625	15.625	27.000	1	X
23, 24	1440 × 288p	50.000	1728	312	15.625	27.000	2	-
23, 24	1440 × 288p	50.000	1728	313	15.625	27.000	2	-
23, 24	1440 × 288p	50.000	1728	314	15.625	27.000	2	-
25, 26	2880 × 576i	50.000	3456	625	15.625	54.000	4[1]	-
27, 28	2880 × 288p	50.000	3456	312	15.625	54.000	4[1]	-
27, 28	2880 × 288p	50.000	3456	313	15.625	54.000	4[1]	-

Table 27. Timing parameters for EIA/CEA-861B *…continued*

Format	Format	V frequency (Hz)	H total	V total	H frequency (kHz)	Pixel frequency (MHz)	Pixel repetition	Scaler
27, 28	720 × 288p	50.000	3456	314	15.625	54.000	4	-
29, 30	1440 × 576p	50.000	1728	625	31.250	54.000	2	-
31	1920 × 1080p	50.000	2640	1125	56.250	148.50	1	-

[1] The format can also be defined with a repetition factor of up to 10.

Table 28. Timing parameters for ATSC DTV standards, which are not defined in EIA/CEA-861B

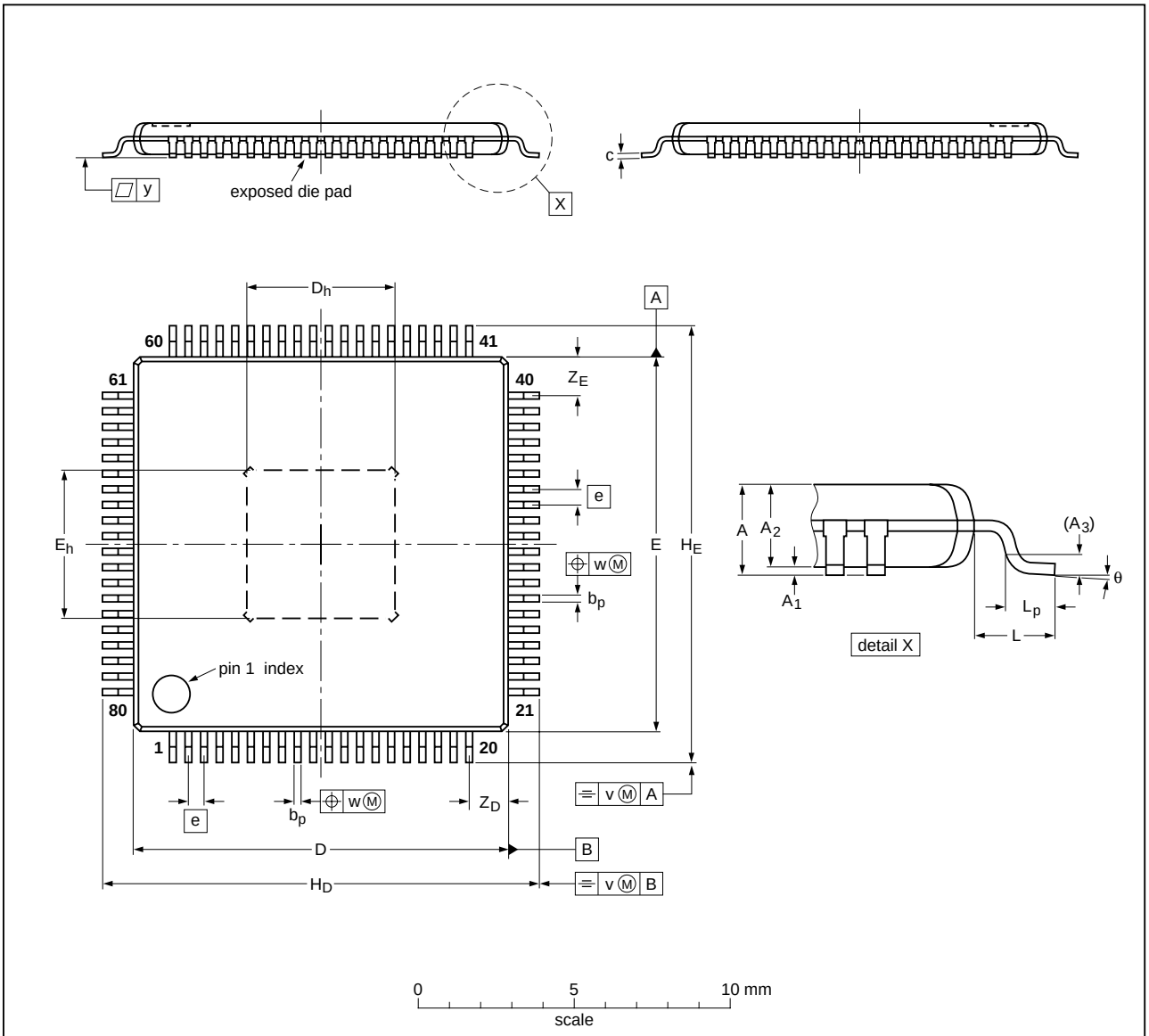
Standard	Format	V frequency (Hz)	H total	V total	H frequency (kHz)	Pixel frequency (MHz)	Pixel repetition	Scaler
SMPTE-296M	1280 × 720p	30.000	3300	750	22.500	74.250	1	-
		29.970	3300	750	22.478	74.175	1	-
		25.000	3960	750	18.750	74.250	1	-
		23.976	4125	750	17.982	74.175	1	-

Table 29. Timing parameters for PC standards below 165 MHz

Standard	Format	V frequency (Hz)	H total	V total	H frequency (kHz)	Pixel frequency (MHz)	Pixel repetition	Scaler
	640 × 350p	85.080	832	445	37.861	31.500	1	-
	640 × 400p	85.080	832	445	37.861	31.500	1	-
	720 × 400p	85.039	936	446	37.937	35.500	1	-
VGA	640 × 480p	59.9401	800	525	31.469	25.175	1	-
		72.809	832	525	37.861	31.500	1	-
		75.000	840	500	37.500	31.500	1	-
		85.008	832	520	43.269	36.000	1	-
SVGA	800 × 600p	56.250	1024	625	35.156	36.000	1	-
		60.317	1056	628	37.879	40.000	1	-
		72.188	1040	666	48.077	50.000	1	-
		75.000	1056	625	46.875	49.500	1	-
		85.061	1048	631	53.673	56.250	1	-
XGA	1024 × 768p	60.004	1344	806	48.362	65.000	1	-
		70.069	1328	806	56.476	75.000	1	-
		75.029	1312	800	60.023	78.750	1	-
		84.997	1376	808	68.677	94.500	1	-
	1024 × 768i	86.957	1264	817	35.522	44.900	1	-
	1152 × 864p	75.000	1600	900	67.500	108.000	1	-
		85.000	1576	907	77.094	121.500	1	-
	1280 × 960p	60.000	1800	1000	60.000	108.000	1	-
		85.002	1728	1011	85.937	148.450	1	-
SXGA	1280 × 1024p	60.002	1688	1066	63.981	108.000	1	-
		75.025	1688	1066	79.977	135.000	1	-

14. Package outline

HTQFP80: plastic thermal enhanced thin quad flat package; 80 leads; body 12 x 12 x 1 mm; exposed die pad **SOT841-4**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	A_3	b_p	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.2	0.15 0.05	1.05 0.95	0.25	0.27 0.17	0.20 0.09	12.1 11.9	4.79 4.69	12.1 11.9	4.79 4.69	0.5	14.15 13.85	14.15 13.85	1	0.75 0.45	0.2	0.08	0.1	1.45 1.05	1.45 1.05	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT841-4		MS-026				~~06-04-25~~ 06-06-20

Fig 18. Package outline SOT841-4 (HTQFP80)

15. Abbreviations

Table 30. Abbreviations

Acronym	Description
ACR	Audio Clock Recovery
AV	Audio Video
CMOS	Complementary Metal-Oxide Semiconductor
CTS	Clock Time Stamp
CTS/N	Clock Time Stamp integer divider
DDC	Display Data Channel
DE	Data Enable
DTS	Digital Transmission System
DTV	Desk Top Video
DVD	Digital Versatile Disc
DVI	Digital Visual Interface
EAV	End Active Video
EDID	Extended Display Identification Data
E-EDID	Enhanced Extended Display Identification Data
FREF	Field REFerence
HBR	High Bit Rate
HD	High Definition
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface
HDTV	High-Definition Television
HREF	Horizontal REFerence
HSYNC	Horizontal SYNChronization
KSV	Key Selection Vector
LSB	Least Significant Bit
LV-TTL	Low Voltage Transistor-Transistor Logic
MSB	Most Significant Bit
NTSC	National Television System Committee
OTP	One Time Programming
PAL	Phase Alternated Line
PCM	Pulse Code Modulation
PLL	Phase-Locked Loop
SAV	Start Active Video
SHA-1	Secure Hash Algorithm 1
S/PDIF	Sony/Philips Digital Interface
TMDS	Transition Minimized Differential Signalling
VHREF	Vertical Horizontal REFerence
VREF	Vertical REFerence
VSYNC	Vertical SYNChronization
YCbCr	Y = luminance, Cb = Chroma component blue, Cr = Chroma component red

16. Revision history

Table 31. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA9984A_4	20090115	Product data sheet		TDA9984A_3
Modifications:	• All document: changed Y-C_B-C_R in YCbCr, C_B in Cb and C_R in Cr for consistency • Section 1: rewritten the first sentence • Section 2: added "Dolby-True HD and DTS-HD" • Figure 1, Figure 2 and Table 3: updated the pins 15, 16 and 45: name and description • Table 1: added the row $V_{DDA(PLL)(1V8)}$ • Section 8.2: changed the reference HDMI 1.2a in 1.3 and in the table 15, added the column HBR • Section 8.2.2: updated the input clock with a frequency at 64fs • Section 8.2.3: added this paragraph High bit rate audio • Table 22: updated • Table 25: added the part HBR mode • Table 1, Table 20, Table 22, Table 23, Table 24 and Table 25: changed the temperature min 0 °C to –5 °C and temperature max 70 °C to +85 °C			
TDA9984A_3	20080410	Product data sheet	-	TDA9984A_2
TDA9984A_2	20080115	Preliminary data sheet	-	TDA9984_1
TDA9984_1	20070723	Objective data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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19. Contents

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