DATA SHEET

TDA9870A
Digital TV Sound Processor (DTVSP)

Product specification
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Philips Semiconductors

PHILIPS

CONTENTS

1 FEATURES

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- Sound IF (SIF) input switch e.g. to select between terrestrial TV SIF and SAT SIF sources
- SIF AGC with 24 dB control range
- SIF 8-bit Analog-to-Digital Converter (ADC)
- Two-carrier multistandard FM demodulation (B/G, D/K and M standard)
- Decoding for three analog multi-channel systems (A2, A2+ and A2*) and satellite sound
- Programmable identification (B/G, D/K and M standard) and different identification times.

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- Digital crossbar switch for all digital signal sources and destinations
- Control of volume, balance, contour, bass, treble, pseudo stereo, spatial, bass boost and soft mute
- Plop-free volume control
- Automatic Volume Level (AVL) control
- Adaptive de-emphasis for satellite
- Programmable beeper
- Monitor selection for FM/AM DC values and signals, with peak detection option
- I^2S-bus interface for a feature extension (e.g. Dolby surround) with matrix, level adjust and mute.

1.3 Analog audio section

- Analog crossbar switch with inputs for mono and stereo (also applicable as SCART 3 input), SCART 1 input/output, SCART 2 input/output and line output
- User defined full-level/–3 dB scaling for SCART outputs
- Output selection of mono, stereo, dual A/B, dual A or dual B
- 20 kHz bandwidth for SCART-to-SCART copies
- Standby mode with functionality for SCART copies
- Dual audio Digital-to-Analog Converter (DAC) from DSP to analog crossbar switch, bandwidth of 15 kHz
- Dual audio ADC from analog inputs to DSP
- Two dual audio DACs for loudspeaker (Main) and headphone (Auxiliary) outputs; also applicable for L, R, C and S in the Dolby Pro Logic mode with feature extension.

2 GENERAL DESCRIPTION

The TDA9870A is a single-chip Digital TV Sound Processor (DTVSP) for analog multi-channel sound systems in TV sets and satellite receivers.

2.1 Supported standards

The multistandard/multi-stereo capability of the TDA9870A is mainly of interest in Europe, but also in Hong Kong/Peoples Republic of China and South East Asia. This includes B/G, D/K, I, M and L standard. In other application areas there exists only subsets of those standard combinations otherwise only single standards are transmitted.

M standard is transmitted in Europe by the American Forces Network (AFN) with European channel spacing (7 MHz VHF, 8 MHz UHF) and monaural sound.

Korea has a stereo sound system similar to Europe and is supported by the TDA9870A. Differences include deviation, modulation contents and identification. It is based on M standard.

An overview of the supported standards and sound systems and their key parameters is given in Table 1.

The analog multi-channel sound systems (A2, A2+ and A2*) are 2-Carrier Systems (2CS).

2.1.1 ANALOG 2-CARRIER SYSTEMS

Table 1 Frequency modulation

STANDARD	SOUND SYSTEM	CARRIER FREQUENCY (MHz)	FM DEVIATION (kHz)			MODULATION		BANDWIDTH/ DE-EMPHASIS (kHz/μs)
			NOM.	MAX.	OVER	SC1	SC2	
M	mono	4.5	15	25	50	mono	–	15/75
M	A2+	4.5/4.724	15	25	50	½(L + R)	½(L – R)	15/75 (Korea)
B/G	A2	5.5/5.742	27	50	80	½(L + R)	R	15/50
I	mono	6.0	27	50	80	mono	–	15/50
D/K	A2	6.5/6.742	27	50	80	½(L + R)	R	15/50
D/K	A2*	6.5/6.258	27	50	80	½(L + R)	R	15/50

Table 2 Identification for A2 systems

PARAMETER	A2/A2*	A2+ (KOREA)
Pilot frequency	54.6875 kHz = 3.5 × line frequency	55.0699 kHz = 3.5 × line frequency
Stereo identification frequency	$117.5\ \text{Hz} = \frac{\text{line frequency}}{133}$	$149.9\ \text{Hz} = \frac{\text{line frequency}}{105}$
Dual identification frequency	$274.1\ \text{Hz} = \frac{\text{line frequency}}{57}$	$276.0\ \text{Hz} = \frac{\text{line frequency}}{57}$
AM modulation depth	50%	50%

2.1.2 SATELLITE SYSTEMS

An important specification for satellite TV reception is the *"Astra specification"*. The TDA9870A is suited for the reception of Astra and other satellite signals.

Table 3 FM satellite sound

CARRIER TYPE	CARRIER FREQUENCY (MHz)	MODULATION INDEX	MAXIMUM FM DEVIATION (kHz)	MODULATION	BANDWIDTH/ DE-EMPHASIS (kHz/μs)
Main	6.50[1]	0.26	85	mono	15/50[2]
Sub	7.02/7.20	0.15	50	m/st/d[3]	15/adaptive[4]
Sub	7.38/7.56				
Sub	7.74/7.92				
Sub	8.10/8.28				

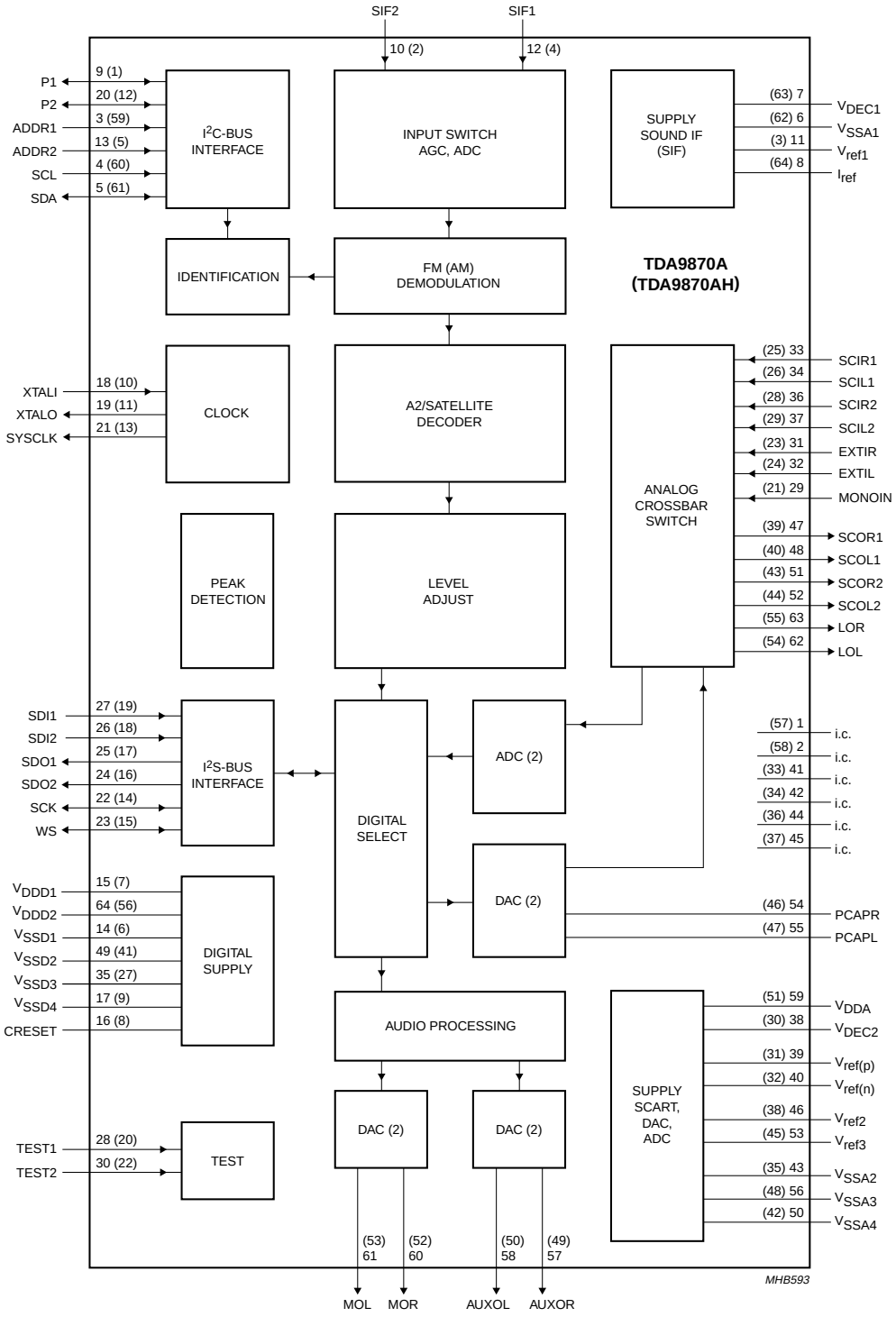
Notes

1. For other satellite systems, frequencies of, for example, 5.80, 6.60 or 6.65 MHz can also be received.
2. A de-emphasis of 60 μs, or in accordance with J17, is available.
3. m/st/d = mono, stereo or dual language sound.
4. Adaptive de-emphasis is compatible to transmitter specification.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9870A	SDIP64	plastic shrink dual in-line package; 64 leads (750 mil)	SOT274-1
TDA9870AH	QFP64	plastic quad flat package; 64 leads (lead length 1.6 mm); body $14 \times 14 \times 2.7$ mm	SOT393-1

4 BLOCK DIAGRAM



The pin numbers given in parenthesis refer to the TDA9870AH version.

Fig.1 Block diagram.

5 PINNING

SYMBOL	PIN		PIN TYPE(1)	DESCRIPTION
	TDA9870A	TDA9870AH		
i.c.	1	57	–	internally connected; note 2
i.c.	2	58	–	internally connected; note 2
ADDR1	3	59	I	I^2C-bus slave address input 1
SCL	4	60	I	I^2C-bus clock input
SDA	5	61	I/O	I^2C-bus data input/output
V_{SSA1}	6	62	S	supply ground 1; analog front-end circuitry
V_{DEC1}	7	63	–	supply voltage decoupling 1; analog front-end circuitry
I_{ref}	8	64	–	resistor for reference current generator; analog front-end circuitry
P1	9	1	I/O	general purpose input/output pin 1
SIF2	10	2	I	sound IF input 2
V_{ref1}	11	3	–	reference voltage 1; analog front-end circuitry
SIF1	12	4	I	sound IF input 1
ADDR2	13	5	I	I^2C-bus slave address input 2
V_{SSD1}	14	6	S	supply ground 1; digital circuitry
V_{DDD1}	15	7	S	digital supply voltage 1; digital circuitry
CRESET	16	8	–	capacitor for Power-on reset
V_{SSD4}	17	9	S	supply ground 4; digital circuitry
XTALI	18	10	I	crystal oscillator input
XTALO	19	11	O	crystal oscillator output
P2	20	12	I/O	general purpose input/output pin 2
SYSCLK	21	13	O	system clock output
SCK	22	14	I/O	I^2S-bus clock input/output
WS	23	15	I/O	I^2S-bus word select input/output
SDO2	24	16	O	I^2S-bus data output 2 (I^2S2 output)
SDO1	25	17	O	I^2S-bus data output 1 (I^2S1 output)
SDI2	26	18	I	I^2S-bus data input 2 (I^2S2 input)
SDI1	27	19	I	I^2S-bus data input 1 (I^2S1 input)
TEST1	28	20	I	test pin 1; connected to V_{SSD1} for normal operation
MONOIN	29	21	I	audio mono input
TEST2	30	22	I	test pin 2; connected to V_{SSD1} for normal operation
EXTIR	31	23	I	external audio input right channel
EXTIL	32	24	I	external audio input left channel
SCIR1	33	25	I	SCART 1 input right channel
SCIL1	34	26	I	SCART 1 input left channel
V_{SSD3}	35	27	S	supply ground 3; digital circuitry
SCIR2	36	28	I	SCART 2 input right channel
SCIL2	37	29	I	SCART 2 input left channel
V_{DEC2}	38	30	–	supply voltage decoupling 2; audio analog-to-digital converter circuitry

SYMBOL	PIN		PIN TYPE(1)	DESCRIPTION
	TDA9870A	TDA9870AH		
$V_{ref(p)}$	39	31	–	positive reference voltage; audio analog-to-digital converter circuitry
$V_{ref(n)}$	40	32	–	reference voltage ground; audio analog-to-digital converter circuitry
i.c.	41	33	–	internally connected; note 3
i.c.	42	34	–	internally connected; note 4
V_{SSA2}	43	35	S	supply ground 2; audio analog-to-digital converter circuitry
i.c.	44	36	–	internally connected; note 4
i.c.	45	37	–	internally connected; note 3
V_{ref2}	46	38	–	reference voltage 2; audio analog-to-digital converter circuitry
SCOR1	47	39	O	SCART 1 right channel output
SCOL1	48	40	O	SCART 1 left channel output
V_{SSD2}	49	41	S	supply ground 2; digital circuitry
V_{SSA4}	50	42	S	supply ground 4; audio operational amplifier circuitry
SCOR2	51	43	O	SCART 2 right channel output
SCOL2	52	44	O	SCART 2 left channel output
V_{ref3}	53	45	–	reference voltage 3; audio digital-to-analog converter and operational amplifier circuitry
PCAPR	54	46	–	post-filter capacitor pin right channel, audio digital-to-analog converter
PCAPL	55	47	–	post-filter capacitor pin left channel, audio digital-to-analog converter
V_{SSA3}	56	48	S	supply ground 3; audio digital-to-analog converter circuitry
AUXOR	57	49	O	headphone (Auxiliary) right channel output
AUXOL	58	50	O	headphone (Auxiliary) left channel output
V_{DDA}	59	51	S	analog power supply voltage; analog circuitry
MOR	60	52	O	loudspeaker (Main) right channel output
MOL	61	53	O	loudspeaker (Main) left channel output
LOL	62	54	O	line output left channel
LOR	63	55	O	line output right channel
V_{DDD2}	64	56	S	digital supply voltage 2; digital circuitry

Notes

1. Pin type: I = Input; O = Output; S = Supply.
2. Test pin: CMOS 3-state stage, pull-up resistor, can be connected to V_{SS}.
3. Test pin: CMOS level input, pull-up resistor, can be connected to V_{SS}.
4. Test pin: CMOS 3-state stage, can be connected to V_{SS}.

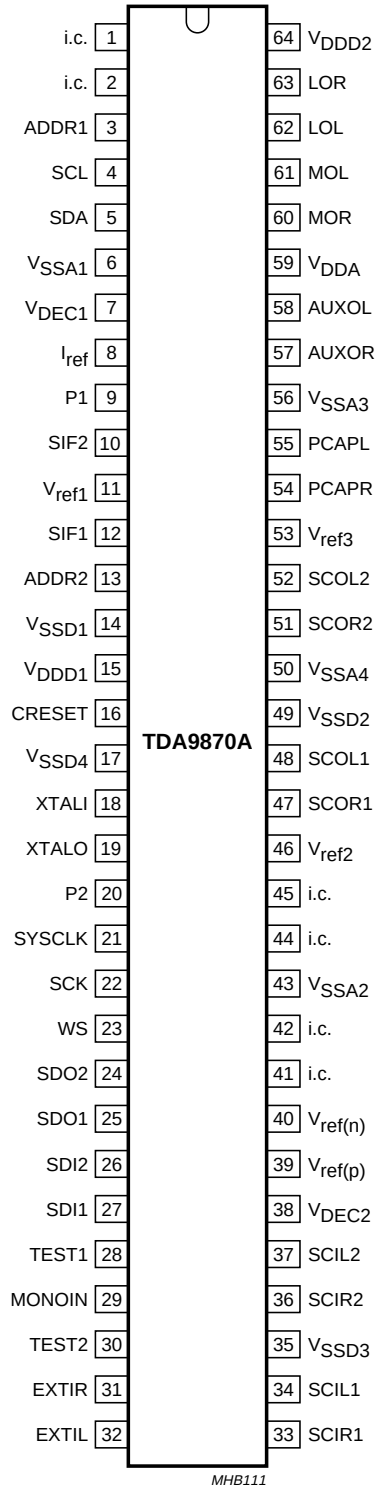


Fig.2 Pin configuration (TDA9870A).

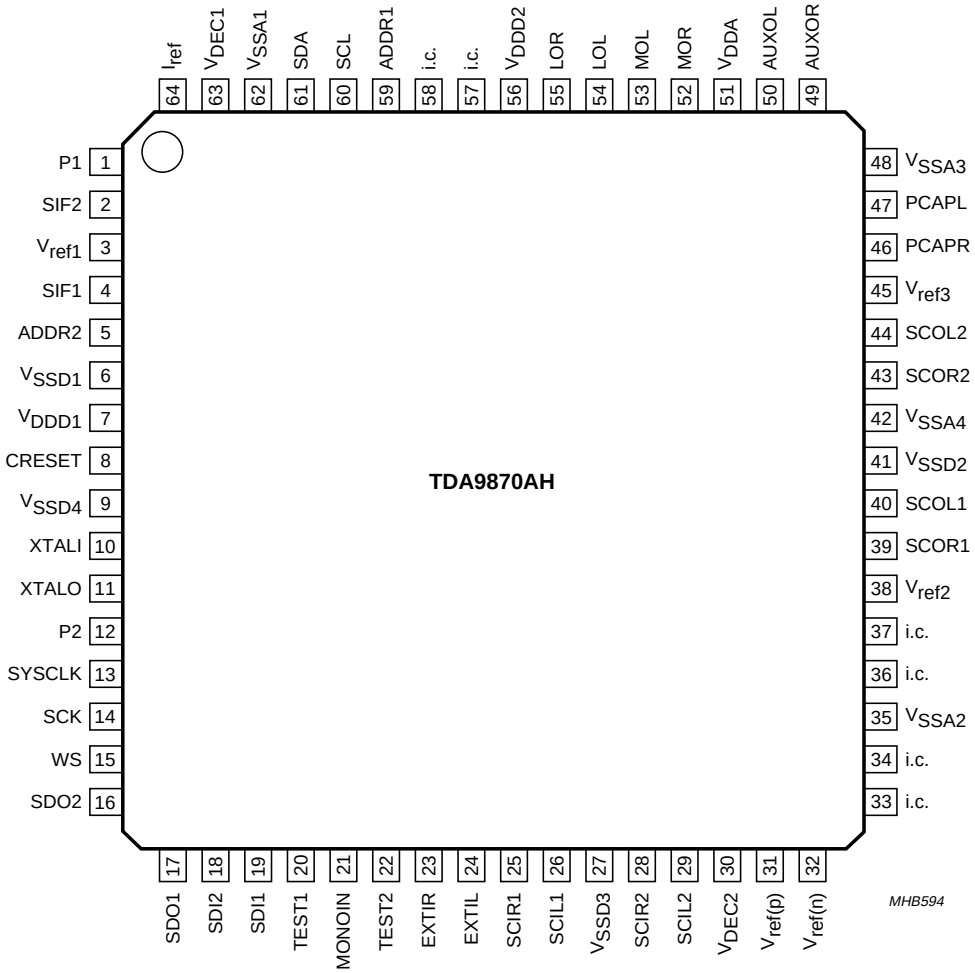


Fig.3 Pin configuration (TDA9870AH).

6 FUNCTIONAL DESCRIPTION

6.1 Demodulator and decoder section

6.1.1 SIF INPUT

Two input pins are provided: SIF1 e.g. for terrestrial TV and SIF2 e.g. for a satellite tuner. For higher SIF signal levels the SIF input can be attenuated with an internally switchable −10 dB resistor divider. As no specific filters are integrated, both inputs have the same specification giving flexibility in application. The selected signal is passed through an AGC circuit and then digitized by an 8-bit ADC operating at 24.576 MHz.

6.1.2 AGC

The gain of the AGC amplifier is controlled from the ADC output by means of a digital control loop employing hysteresis. The AGC has a fast attack behaviour to prevent ADC overloads and a slow decay behaviour to prevent AGC oscillations. For AM demodulation the AGC must be switched off. When switched off, the control loop is reset and fixed gain settings can be chosen (see Table 14; subaddress 0).

The AGC can be controlled via the I^2C-bus. Details can be found in the I^2C-bus register definitions (see Chapter 10).

6.1.3 MIXER

The digitized input signal is fed to the mixers, which mix one or both input sound carriers down to zero IF. A 24-bit control word for each carrier sets the required frequency. Access to the mixer control word registers is via the I^2C-bus.

6.1.4 FM AND AM DEMODULATION

An FM or AM input signal is fed via a band-limiting filter to a demodulator that can be used for either FM or AM demodulation. Apart from the standard (fixed) de-emphasis characteristic, an adaptive de-emphasis is available for encoded satellite programs. A stereo decoder recovers the left and right signal channels from the demodulated sound carriers. Both the European and Korean stereo systems are supported.

6.1.5 FM IDENTIFICATION

The identification of the FM sound mode is performed by AM synchronous demodulation of the pilot signal and narrow-band detection of the identification frequencies. The result is available via the I^2C-bus interface. A selection can be made via the I^2C-bus for B/G, D/K and M standard and for three different modes that represent different trade-offs between speed and reliability of identification.

6.1.6 CRYSTAL OSCILLATOR

The circuitry of the crystal oscillator is fully integrated, only the external 24.576 MHz crystal is needed (see Fig.10).

6.1.7 TEST PINS

Test pins TEST1 and TEST2 are active HIGH and in normal operating mode of the device they are connected to V_{SSD1}. Test functions are for manufacturing tests only and are not available to customers. Without external circuitry these pins are pulled down to LOW level with internal resistors.

6.1.8 POWER FAIL DETECTOR

The power fail detector monitors the internal power supply for the digital part of the device. If the supply has temporarily been lower than the specified lower limit, the Power-on reset bit POR (see Section 10.4.1), will be set to logic 1. Bit CLRPOR (see Section 10.3.2) resets the Power-on reset flip-flop to LOW. If this is detected, an initialization of the TDA9870A has to be carried out to ensure reliable operation.

6.1.9 POWER-ON RESET

The reset is active LOW. In order to perform a reset at power-up, a simple RC circuit may be used which consists of the integrated passive pull-up resistor and an external capacitor connected to ground. The pull-up resistor has a nominal value of 50 kΩ, which can easily be measured between pins CRESET and V_{DDD2}. Before the supply voltage has reached a certain minimum, the state of the circuit is completely undefined, and it remains in this undefined state unless a reset is applied.

The reset is guaranteed to be active when:

- The power supply is within the specified limits (4.75 and 5.5 V)
- The crystal oscillator is functioning
- The voltage at pin CRESET is below $0.3V_{DDD}$ (1.5 V if V_{DDD} = 5.0 V, typically below 1.8 V).

The required capacitor value depends on the gradient of the rising power supply voltage. The time constant of the RC circuit should be clearly larger than the rise time of the power supply, to make sure that the reset condition is always satisfied (see Fig.4), even considering the tolerance spread. To avoid problems with a too slow discharging of the capacitor at power-down, it may be helpful to add a diode from pin CRESET to V_{DDD}. It should be noted that the internal ESD protection diode does not help here as it only conducts at higher voltages. Under difficult power supply conditions (e.g. very slow or non-monotonic ramp-up), it is recommended to drive the reset line from a microcontroller port or the like.

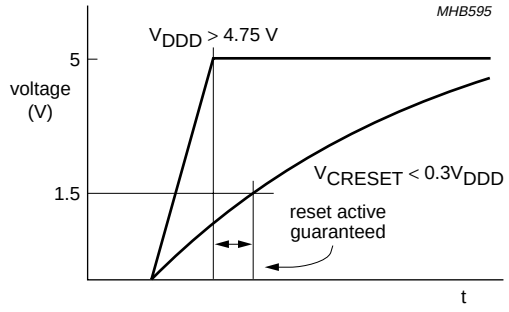


Fig.4 Reset at power-on.

6.2 Digital signal processing

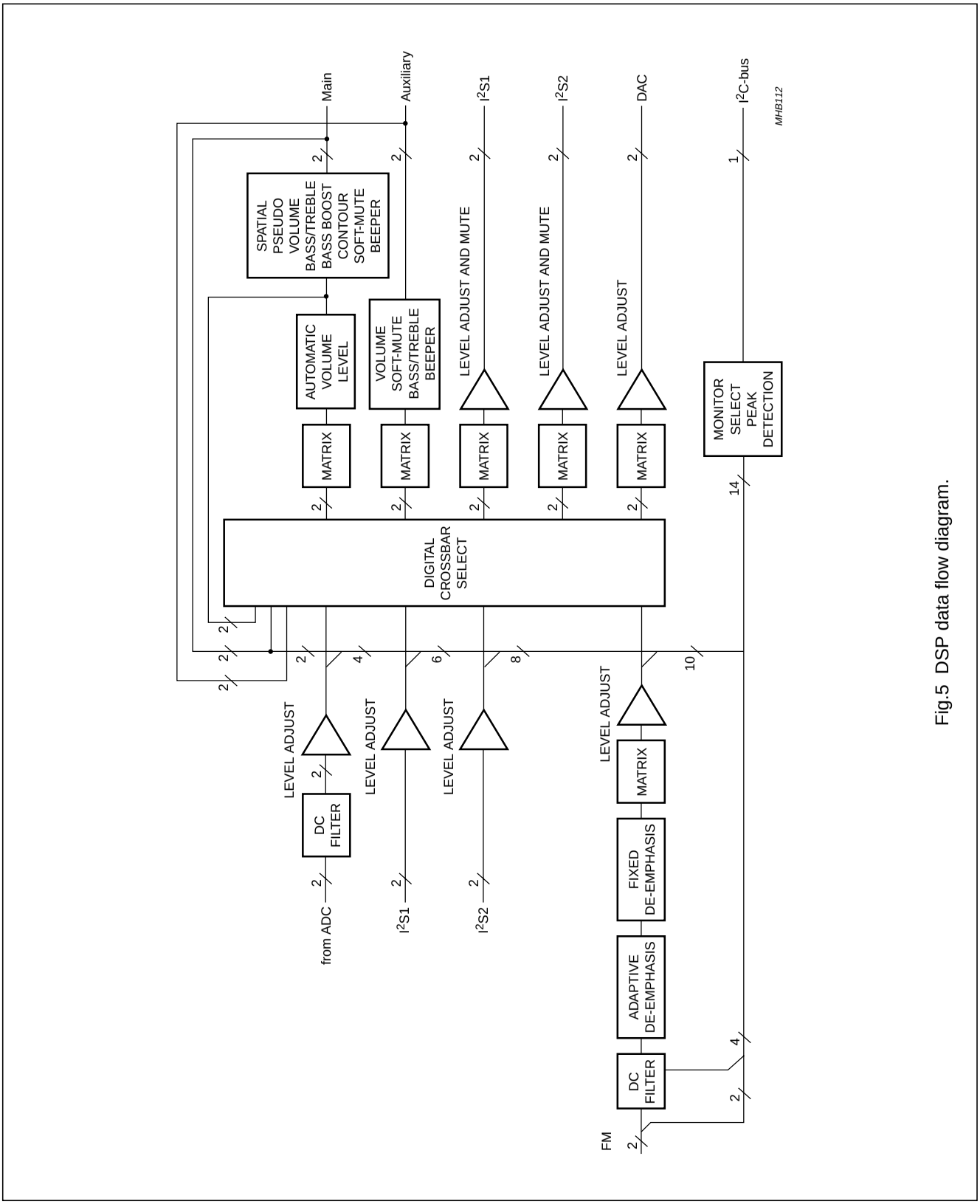


Fig.5 DSP data flow diagram.

6.2.1 LEVEL SCALING

All input channels to the digital crossbar switch (except for the loudspeaker feedback path) are equipped with a level adjust facility to change the signal level in a range from +15 to −15 dB (see Fig.5). It is recommended to scale all input channels to be 15 dB below full-scale (−15 dB full-scale) under nominal conditions.

6.2.2 FM (AM) PATH

A high-pass filter suppresses DC offsets from the FM demodulator, due to carrier frequency offsets, and supplies the monitor/peak function with DC values and an unfiltered signal, e.g. for the purpose of carrier detection.

The de-emphasis function offers fixed settings for the supported standards (50, 60 and 75 μs).

An adaptive de-emphasis is available for Wegener-Panda 1 encoded programs.

A matrix performs the dematrixing of the A2 stereo, dual and mono signals.

6.2.3 MONITOR

This function provides data words from a number of locations of the signal processing paths to the I²C-bus interface (2 data bytes). Signal sources include the FM demodulator outputs, most inputs to the digital crossbar switch and the outputs of the ADC. Source selection and data read-out is performed via the I²C-bus.

Optionally, the peak value can be measured instead of simply taking samples. The internally stored peak value is reset to zero when the data is read via the I²C-bus. The monitor function may be used, for example, for signal level measurements or carrier detection.

6.2.4 LOUDSPEAKER (MAIN) CHANNEL

The matrix provides the following functions: forced mono, stereo, channel swap, channel 1, channel 2 and spatial effects.

There are fixed coefficient sets for spatial settings of 30%, 40% and 52%.

The Automatic Volume Level (AVL) function provides a constant output level of −23 dB full-scale for input levels between 0 and −29 dB full-scale. There are some fixed decay time constants to choose from, i.e. 2, 4 and 8 s.

Pseudo stereo is based on a phase shift in one channel via a second-order all-pass filter. There are fixed coefficient sets to provide 90 degrees phase shift at frequencies of 150, 200 and 300 Hz.

Volume is controlled individually for each channel ranging from +24 to −83 dB with 1 dB resolution. There is also a mute position. For the purpose of a simple control software in the microcontroller, the decimal number that is sent as an I²C-bus data byte for volume control is identical to the volume setting in dBs (e.g. the I²C-bus data byte +10 sets the new volume value to +10 dB).

Balance can be realized by independent control of the left and right channel volume settings.

Contour is adjustable between 0 and +18 dB with 1 dB resolution. This function is linked to the volume setting by means of microcontroller software.

Bass is adjustable between +15 and −12 dB with 1 dB resolution and treble is adjustable between +12 and −12 dB with 1 dB resolution.

For the purpose of a simple control software in the microcontroller, the decimal number that is sent as an I²C-bus data byte for contour, bass or treble is identical to the new contour, bass or treble setting in dBs (e.g. the I²C-bus data byte +8 sets the new value to +8 dB).

Extra bass boost is provided up to 20 dB with 2 dB resolution. The implemented coefficient set serves merely as an example on how to use this filter.

The beeper provides tones in a range from approximately 400 Hz to 30 kHz. The frequency can be selected via the I²C-bus. The beeper output signal is added to the loudspeaker and headphone channel signals. The beeper volume is adjustable with respect to full-scale between 0 and −93 dB with 3 dB resolution. The beeper is not effected by mute.

Soft mute provides a mute ability in addition to volume control with a well defined time (32 ms) after which the soft mute is completed. A smooth fading is achieved by a cosine masking.

6.2.5 HEADPHONE (AUXILIARY) CHANNEL

The matrix provides the following functions: forced mono, stereo, channel swap, channel 1 and channel 2 (or C and S in Dolby Surround Pro Logic mode).

Volume is controlled individually for each channel in a range from +24 to −83 dB with 1 dB resolution. There is also a mute position.

For the purpose of a simple control software in the microcontroller, the decimal number that is sent as an I²C-bus data byte for volume control is identical to the volume setting in dB (e.g. the I²C-bus data byte +10 sets the new volume value to +10 dB).

Balance can be realized by independent control of the left and right channel volume settings.

Bass is adjustable between +15 and −12 dB with 1 dB resolution and treble is adjustable between +12 and −12 dB with 1 dB resolution.

For the purpose of a simple control software in the microcontroller, the decimal number that is sent as an I²C-bus data byte for bass or treble is identical to the new bass or treble setting in dB (e.g. the I²C-bus data byte +8 sets the new value to +8 dB).

The beeper provides tones in a range from approximately 400 Hz to 30 kHz. The frequency can be selected via the I²C-bus. The beeper output signal is added to the loudspeaker and headphone channel signals. The beeper volume is adjustable with respect to full-scale between 0 and −93 dB with 3 dB resolution. The beeper is not effected by mute.

Soft mute provides a mute ability in addition to volume control with a well defined time (32 ms) after which the soft mute is completed. A smooth fading is achieved by a cosine masking.

6.2.6 Feature interface

The feature interface comprises two I²S-bus input/output ports and a system clock output. Each I²S-bus port is equipped with level adjust facilities that can change the signal level in a range from +15 to −15 dB with 1 dB resolution. Outputs can be disabled to improve EMC performance.

The I²S-bus output matrix provides the following functions: forced mono, stereo, channel swap, channel 1 and channel 2.

One example of how the feature interface can be used in a TV set is to connect an external Dolby Surround Pro Logic DSP, such as the SAA7710, to the I²S-bus ports. Outputs must be enabled and a suitable master clock signal for the DSP can be taken from pin SYSCLK.
A stereo signal from any source will be output on one of the I²S-bus serial data outputs and the four processed signal channels will be entered at both I²S-bus serial data inputs. Left and right could then be output to the power amplifiers via the Main channel, centre and surround via the Auxiliary channel.

6.2.7 Channel from the audio ADC

The signal level at the output of the ADC can be adjusted in a range from +15 to −15 dB with 1 dB resolution.
The audio ADC itself is scaled to a gain of −6 dB.

6.2.8 Channel to the analog crossbar path

Level adjust with control positions 0, +3, +6 and +9 dB.

6.2.9 Digital crossbar switch

Input channels to the crossbar switch are from the audio ADC, I²S1, I²S2, FM path and from the loudspeaker channel path after matrix and AVL (see Fig.6).

Output channels comprise loudspeaker, headphone, I²S1, I²S2 and the audio DACs for line output and SCART.

The I²S1 and I²S2 outputs also provide digital outputs from the loudspeaker and headphone channels, but without the beeper signals.

6.2.10 Signal gain

There are a number of functions that can provide signal gain, e.g. volume, bass and treble control. Great care has to be taken when using gain with large input signals in order not to exceed the maximum possible signal swing, which would cause severe signal distortion. The nominal signal level of the various signal sources to the digital crossbar switch should be 15 dB below digital full-scale (−15 dB full-scale). This means that a volume setting of, say, +15 dB would just produce a full-scale output signal and not cause clipping, if the signal level is nominal.

Sending illegal data patterns via the I²C-bus will not cause any changes of the current setting for the volume, bass, treble, bass boost and level adjust functions.

6.2.11 Expert mode

The TDA9870A provides a special expert mode that gives direct write access to the internal Coefficient RAM (CRAM) of the DSP. It can be used to create user-defined characteristics, such as a tone control with different corner frequencies or special boost/cut characteristics to correct the low-frequency loudspeaker and/or cabinet frequency responses by means of the bass boost filter. However, this mode must be used with great care.

More information on the functions of this device, such as the number of coefficients per function, their default values, memory addresses etc., can be made available on request.

6.2.12 DSP FUNCTIONS

Table 4 Overview of DSP functions

FUNCTION	EXPERT MODE	PARAMETER	VALUE	UNIT
Bass control for loudspeaker and headphone output	yes	control range	–12 to +15	dB
		resolution	1	dB
		resolution at frequency	40	Hz
Treble control for loudspeaker and headphone output	yes	control range	–12 to +12	dB
		resolution	1	dB
		resolution at frequency	14	kHz
Contour for loudspeaker output	yes	control range	0 to +18	dB
		resolution	1	dB
		resolution at frequency	40	Hz
Bass boost for loudspeaker output	yes	control range	0 to +20	dB
		resolution	2	dB
		resolution at frequency	20	Hz
		corner frequency	350	Hz
Volume control for each separate channel in loudspeaker and headphone output	no	control range	–83 to +24	dB
		resolution	1	dB
		mute position at step	10101100	
Soft mute for loudspeaker and headphone output	no	processing time	32	ms
Spatial effects	yes	anti-phase crosstalk positions	30, 40 and 52	%
Pseudo stereo	yes	90 degrees phase shift at frequency	150, 200 and 300	Hz
Beeper additional to the signal in the loudspeaker and headphone channel	yes	beep frequencies	see Section 10.3.38	
		control range	0 to –93	dB
		resolution	3	dB
		mute position at step	00100000	
Automatic Volume Level (AVL)	yes	step width	quasi continuously	
		AVL output level for an input level between 0 and –29 dB full-scale	–23	dB
		attack time	10	ms
		decay time constant	2, 4 and 8	s
General	no	–3 dB lower corner frequency of DSP	10	Hz
		–1 dB bandwidth of DSP	14.5	kHz
Level adjust I^2S1 and I^2S2 inputs	yes	control range	–15 to +15	dB
		resolution	1	dB
Level adjust I^2S1 and I^2S2 outputs	yes	control range	–15 to +15	dB
		resolution	1	dB
		mute position at step	00010000	
Level adjust analog crossbar path	no	control positions	0, 3, 6 and 9	dB

FUNCTION	EXPERT MODE	PARAMETER	VALUE	UNIT
Level adjust audio ADC outputs	yes	control range	+15 to –15	dB
		resolution	1	dB
Level adjust FM path	yes	control range	+15 to –15	dB
		resolution	1	dB

6.3 Analog audio section

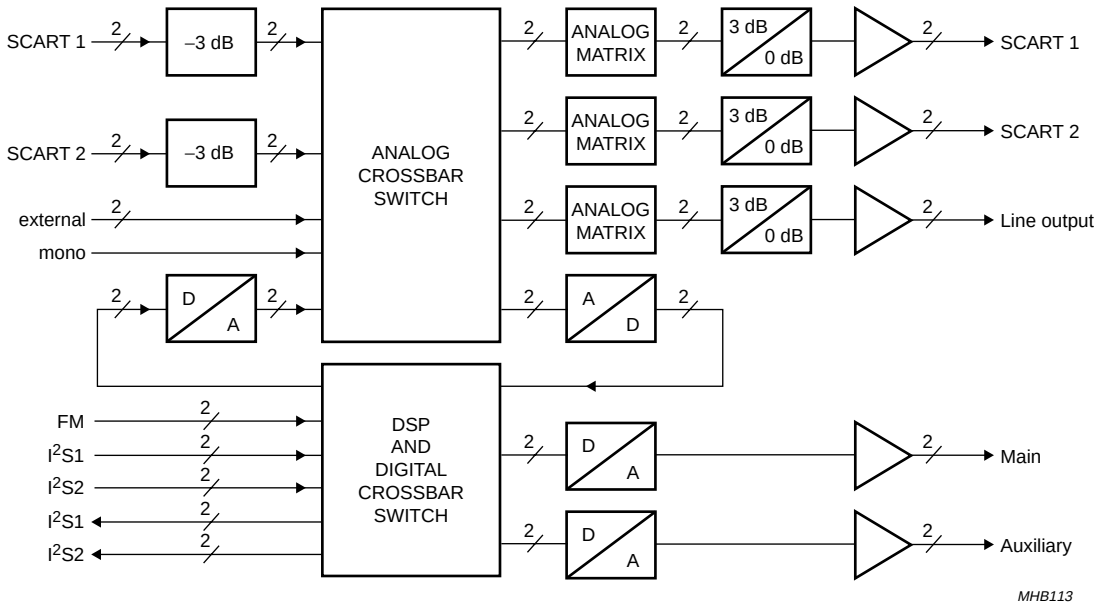


Fig.6 Block diagram for the audio section.

6.3.1 Analog crossbar switch and analog matrix

There are a number of analog input and output ports with the TDA9870A (see Figs 6 and 8). Analog source selector switches are employed to provide the desired analog signal routing capability. The analog signal routing is performed by the analog crossbar switch section. A dual audio ADC provides the connection to the DSP section and a dual audio DAC provides the connection from the DSP section to the analog crossbar switch. The digital signal routing is performed by a digital crossbar switch.

The basic signal routing philosophy of the TDA9870A is that each switch handles two signal channels at the same time, e.g. left and right, language A and B, directly at the source.

Each source selector switch is followed by an analog matrix to perform further selection tasks, such as putting a signal from one input channel, say language A, to both output channels or for swapping left and right channels (see Fig.7).

Fig.7 Analog matrix.

The analog matrix provides the functions given in Table 5.

Table 5 Analog matrix functions

MODE	MATRIX OUTPUT	
	LEFT OUTPUT	RIGHT OUTPUT
1	left input	right input
2	right input	left input
3	left input	left input
4	right input	right input

All switches and matrices are controlled via the I^2C-bus.

6.3.2 SCART inputs

The SCART specification allows for a signal level of up to 2 V (RMS). Because of signal handling limitations, due to the 5 V supply voltage of the TDA9870A, it is necessary to have fixed 3 dB attenuators at the SCART inputs to obtain a 2 V input. This results in a −3 dB SCART-to-SCART copy gain. If 0 dB copy gain is preferred (with maximum 1.4 V input), there are 3 and 0 dB amplifiers at the outputs of SCART 1 and SCART 2 and at the line output.

The input attenuator is realized by an external series resistor in combination with the input impedance, both of which form a voltage divider. With this voltage divider the maximum SCART signal level of 2 V (RMS) is scaled down to 1.4 V (RMS) at the input pin.

6.3.3 External and mono inputs

The 3 dB input attenuators are not required for the external and mono inputs, because those signal levels are under control of the TV designer. The maximum allowed input level is 1.4 V (RMS). By adding external series resistors, the external inputs can be used as an additional SCART input.

6.3.4 SCART outputs

The SCART outputs employ amplifiers with two gain settings. The gain can be set to 3 or 0 dB via the I^2C-bus. The 3 dB position is needed to compensate for the 3 dB attenuation at the SCART inputs should SCART-to-SCART copies with 0 dB gain be preferred [under the condition of 1.4 V (RMS) maximum input level]. The 0 dB position is needed, for example, for an external-to-SCART copy with 0 dB gain.

6.3.5 Line output

The line output can provide an unprocessed copy of the audio signal in the loudspeaker channels. This can be either an external signal that comes from the dual audio ADC, or a signal from an internal digital audio source that comes from the dual audio DAC. The line output employs amplifiers with two gain settings. The 3 dB position is needed to compensate for the attenuation at the SCART inputs, while the 0 dB position is needed, for example, for non-attenuated external or internal digital signals (see Section 6.3.4).

6.3.6 Loudspeaker (Main) and headphone (Auxiliary) outputs

Signals from any audio source can be applied to the loudspeaker and to the headphone output channels via the digital crossbar switch and the DSP.

6.3.7 Dual audio DAC

The TDA9870A contains three dual audio DACs, one for the connection from the DSP to the analog crossbar switch section and two for the loudspeaker and headphone outputs. Each of the three dual low-noise high-dynamic range DACs consists of two 15-bit DACs with current outputs, followed by a buffer operational amplifier. The audio DACs operate with four-fold oversampling and noise shaping.

6.3.8 Dual audio ADC

There is one dual audio ADC in the TDA9870A for the connection of the analog crossbar switch section to the DSP. The dual audio ADC consists of two bitstream 3rd-order sigma-delta audio ADCs and a high-order decimation filter.

6.3.9 Standby mode

The standby mode, selected by setting bit STDBY to logic 1 (see Section 10.3.2) disables most functions and reduces power dissipation. The analog crossbar switch and the SCART section remain operational and can be controlled by the I^2C-bus to support copying of analog signals from SCART-to-SCART.

Unused internal registers may lose their information in the standby mode. Therefore, the device needs to be initialized on returning to the normal operating mode. This can be accomplished in the same way as after a Power-on reset.

6.3.10 Supply ground

The different supply grounds V_{SS} are internally connected via the substrate. It is recommended to connect all ground pins by a copper plane close to the pins.

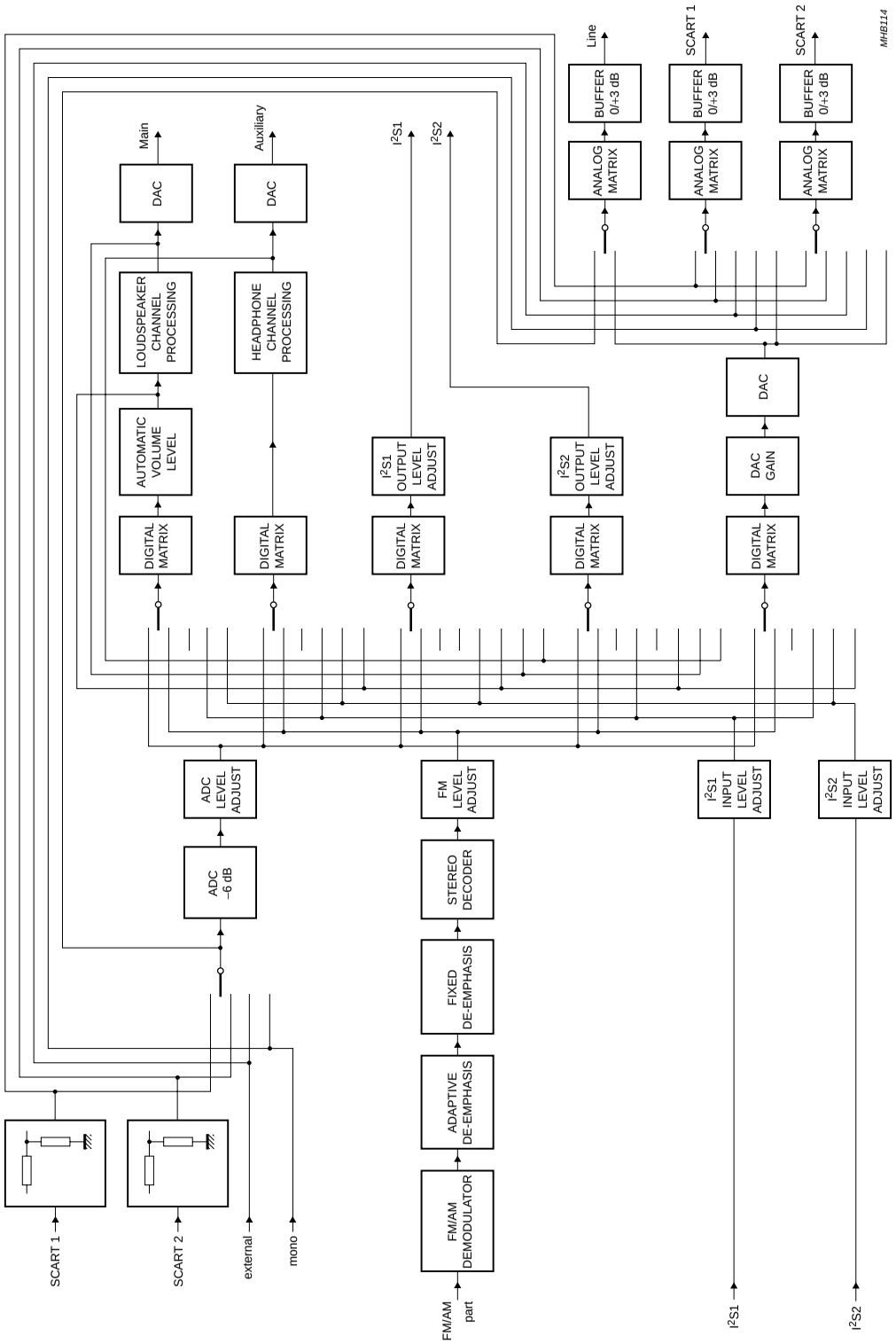


Fig.8 Audio signal flow diagram.

7 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	DC supply voltage		–0.5	+6.0	V
ΔV_{DD}	voltage differences between two V_{DD} pins		–	550	mV
V_n	voltage on any other pin		–0.5	V_{DD} + 0.5	V
I_{DDD},I_{SSD}	DC current per digital supply pin		–	±180	mA
$I_{lu(prot)}$	latch-up protection current		100	–	mA
P_{tot}	total power dissipation		–	1.0	W
T_{stg}	storage temperature		–55	+125	°C
T_{amb}	ambient temperature		–20	+70	°C
V_{es}	electrostatic handling voltage	note 1	–2000	+2000	V
		note 2	–200	+200	V

Notes

1. Human body model: C = 100 pF; R = 1.5 kΩ.
2. Machine model: C = 200 pF; L = 0.75 μH; R = 0 Ω.

8 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
	TDA9870A (SDIP64)		40	K/W
	TDA9870AH (QFP64)		50	K/W

9 CHARACTERISTICS

$V_{SIF(p-p)}$ = 300 mV; AGCOFF = 0; AGCSLOW = 0; AGCLEV = 0; level and gain settings in accordance with note 1; V_{DD} = 5 V; T_{amb} = 25 °C; settings in accordance with B/G standard; FM deviation ±50 kHz; f_{mod} = 1 kHz; FM sound parameters in accordance with system A2; 1 kΩ measurement source resistance for AF inputs; with external components of Fig.10; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDD1}	digital supply voltage 1		4.75	5.0	5.5	V
V_{SSD1}	digital supply ground 1	note 2	–	0.0	–	V
I_{DDD1}	digital supply current 1	V_{DDD1} = 5.0 V	53	68	83	mA
V_{DDD2}	digital supply voltage 2		4.75	5.0	5.5	V
V_{SSD2}	digital supply ground 2	note 2	–	0.0	–	V
I_{DDD2}	digital supply current 2	V_{DDD2} = 5.0 V; system clock output disabled	0.1	0.4	2	mA
V_{SSD3}	digital supply ground 3	note 2	–	0.0	–	V
V_{SSD4}	digital supply ground 4	note 2	–	0.0	–	V
V_{DDA}	analog supply voltage		4.75	5.0	5.5	V
I_{DDA}	analog supply current for DAC part	V_{DDA} = 5.0 V; digital silence	44	56	68	mA
V_{SSA1}	analog ground for analog front-end	note 2	–	0.0	–	V
V_{SSA2}	analog ground for audio ADC part	note 2	–	0.0	–	V
V_{SSA3}	analog ground for audio DAC part	note 2	–	0.0	–	V
V_{SSA4}	analog ground for SCART		–	0.0	–	V
Demodulator supply decoupling and references						
V_{DEC1}	analog supply decoupling voltage for demodulator part		3.0	3.3	3.6	V
V_{ref1}	analog reference voltage for demodulator part		–	2	–	V
$I_{ref1(sink)}$	sink current at pin V_{ref1}		–	200	–	μA
Audio supply decoupling and references						
V_{DEC2}	analog supply decoupling voltage for audio ADC part		3.0	3.3	3.6	V
V_{ref2}	reference voltage ratio for audio ADCs	referenced to V_{DEC2} and V_{SSA2}	–	50	–	%
$Z_{Vref2-VDEC2}$	impedance pins V_{ref2} to V_{DEC2}		–	20	–	kΩ
$Z_{Vref2-VSSA2}$	impedance pins V_{ref2} to V_{SSA2}		–	20	–	kΩ
V_{ref3}	reference voltage ratio for audio DAC and operational amplifier	referenced to V_{DDA} and V_{SSA3}	–	50	–	%
$Z_{Vref3-VDDA}$	impedance pins V_{ref3} to V_{DDA}		–	20	–	kΩ
$Z_{Vref3-VSSA3}$	impedance pins V_{ref3} to V_{SSA3}		–	20	–	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power fail detector						
$V_{th(pf)}$	power fail threshold voltage		–	3.9	–	V
Digital inputs and outputs						
INPUTS						
CMOS level input, pull-down (pins TEST1 and TEST2)						
V_{IL}	LOW-level input voltage		–	–	$0.3V_{DDD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDD}$	–	–	V
C_i	input capacitance		–	–	10	pF
Z_i	input impedance		–	50	–	kΩ
CMOS level input, hysteresis, pull-up (pin CRESET)						
V_{IL}	LOW-level input voltage		–	–	$0.3V_{DDD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDD}$	–	–	V
V_{hys}	hysteresis voltage		–	1.3	–	V
C_i	input capacitance		–	–	10	pF
Z_i	input impedance		30	50	–	kΩ
INPUTS/OUTPUTS						
I^2C-bus level input with Schmitt trigger, open-drain output stage, 400 kHz I^2C-bus operation (pins SCL and SDA)						
V_{IL}	LOW-level input voltage		–	–	$0.3V_{DDD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDD}$	–	–	V
V_{hys}	hysteresis voltage		–	$0.05V_{DDD}$	–	V
I_{LI}	input leakage current		–	–	±10	µA
C_i	input capacitance		–	–	10	pF
V_{OL}	LOW-level output voltage		–	–	0.6	V
C_L	load capacitance		–	–	400	pF
TTL/CMOS level, 4 mA 3-state output stage, pull-up (pins ADDR1, ADDR2, P1, P2, SCK, WS, SDO1, SDO2, SDI1 and SDI2)						
V_{IL}	LOW-level input voltage		–	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	–	V
C_i	input capacitance		–	–	10	pF
V_{OL}	LOW-level output voltage		–	–	0.4	V
V_{OH}	HIGH-level output voltage		2.4	–	–	V
C_L	load capacitance		–	–	100	pF
Z_i	input impedance		–	50	–	kΩ
OUTPUTS						
CMOS level output, 4 mA 3-state output stage, slew rate controlled (pin SYSCLK)						
V_{OL}	LOW-level output voltage		–	–	$0.3V_{DDD}$	V
V_{OH}	HIGH-level output voltage		$0.7V_{DDD}$	–	–	V
C_L	load capacitance		–	–	100	pF
I_{LIZ}	3-state leakage current	V_i = 0 to V_{DDD}	–	–	±10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SIF1 and SIF2 analog inputs						
$V_{SIF(max)(p-p)}$	maximum composite SIF input voltage for clipping (peak-to-peak value)	SIF input level adjust 0 dB	–	941	–	mV
		SIF input level adjust −10 dB	–	2976	–	mV
$V_{SIF(min)(p-p)}$	minimum composite SIF input voltage for lower limit of AGC (peak-to-peak value)	SIF input level adjust 0 dB	–	59	–	mV
		SIF input level adjust −10 dB	–	188	–	mV
AGC	AGC range		–	24	–	dB
f_i	input frequency		4	–	9.2	MHz
R_i	input resistance	AGCLEV = 0	10	–	–	kΩ
C_i	input capacitance		–	7.5	11	pF
Δf_{FM}	FM deviation	B/G standard; THD < 1%	±100	–	–	kHz
$\Delta f_{FM(FS)}$	FM deviation full-scale level	terrestrial FM; level adjust 0 dB	±150	–	–	kHz
C/N_{FM}	FM carrier-to-noise ratio	N_{FM} bandwidth = 6 MHz; white noise for S/N = 40 dB; *"CCIR468"*; quasi peak	–	77	–	$\frac{dB}{Hz}$
α_{ct}	crosstalk attenuation SIF1 to SIF2	f_i = 4 to 9.2 MHz; note 3	50	–	–	dB
Demodulator performance						
THD + N	total harmonic distortion plus noise	from FM source to any output; V_o = 1 V (RMS) with low-pass filter	–	0.3	0.5	%
S/N	signal-to-noise ratio	SC1 from FM source to any output; V_o = 1 V (RMS); *"CCIR468"*; quasi peak	64	70	–	dB
		SC2 from FM source to any output; V_o = 1 V (RMS); *"CCIR468"*; quasi peak	60	66	–	dB
B_{-3dB}	−3 dB bandwidth	from FM source to any output	14.5	15	–	kHz
f_{res}	frequency response 20 Hz to 14 kHz	from FM to any output; f_{ref} = 1 kHz; inclusive pre-emphasis and de-emphasis	–	±2	–	dB
$\alpha_{cs(dual)}$	dual signal channel separation	note 4	65	70	–	dB
$\alpha_{cs(stereo)}$	stereo channel separation	note 5	40	45	–	dB
α_{AM}	AM suppression for FM	AM: 1 kHz, 30% modulation; reference: 1 kHz, 50 kHz deviation	50	–	–	dB
S/N_{AM}	AM demodulation	SIF level 100 mV (RMS); 54% AM; 1 kHz AF; *"CCIR468"*; quasi peak	36	45	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IDENTIFICATION FOR FM SYSTEMS						
mod_p	pilot modulation for identification		25	50	75	%
C/N_p	pilot sideband carrier-to-noise ratio for identification start		–	27	–	$\frac{dB}{Hz}$
f_{ident}	identification window	B/G stereo				
		slow mode	116.85	–	118.12	Hz
		medium mode	116.11	–	118.89	Hz
		fast mode	114.65	–	120.46	Hz
		B/G dual				
		slow mode	273.44	–	274.81	Hz
		medium mode	272.07	–	276.20	Hz
		fast mode	270.73	–	277.60	Hz
$t_{ident(on)}$	total identification time ON	slow mode	–	–	2	s
		medium mode	–	–	1	s
		fast mode	–	–	0.5	s
$t_{ident(off)}$	total identification time OFF	slow mode	–	–	2	s
		medium mode	–	–	1	s
		fast mode	–	–	0.5	s
Analog audio inputs						
MONO INPUT AND EXTERNAL INPUT						
$V_{i(nom)(rms)}$	nominal level input voltage (RMS value)		–	500	–	mV
$V_{i(clip)(rms)}$	clipping level input voltage (RMS value)	THD < 3%; note 6	1250	1400	–	mV
R_i	input resistance	note 6	28	35	42	kΩ
SCART INPUTS						
$V_{i(nom)(rms)}$	nominal level input voltage at input pin (RMS value)	−3 dB divider with external 15 kΩ resistor; note 7	–	350	–	mV
$V_{i(clip)(rms)}$	clipping level input voltage at input pin (RMS value)	−3 dB divider with external 15 kΩ resistor; THD < 3%; notes 6 and 7	1250	1400	–	mV
R_i	input resistance	note 6	28	35	42	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog audio outputs						
LOUDSPEAKER (MAIN) AND HEADPHONE (AUXILIARY) OUTPUTS						
$V_{o(clip)(rms)}$	clipping level output voltage (RMS value)	THD < 3%	1250	1400	–	mV
R_o	output resistance		150	250	375	Ω
$R_{L(AC)}$	AC load resistance		10	–	–	kΩ
$R_{L(DC)}$	DC load resistance		10	–	–	kΩ
C_L	load capacitance		–	10	12	nF
$V_{offset(DC)}$	static DC offset voltage		–	30	70	mV
α_{mute}	mute suppression	nominal input signal from any source; f_i = 1 kHz	80	–	–	dB
$G_{ro(main,aux)}$	roll-off gain at 14.5 kHz for Main and Auxiliary channels	from any source	–3	–2	–	dB
$PSRR_{main,aux}$	power supply ripple rejection for Main and Auxiliary channels	f_{ripple} = 70 Hz; V_{ripple} = 100 mV (peak); C_{Vref} = 47 µF; signal from I²S-bus	40	45	–	dB
SCART OUTPUTS AND LINE OUTPUT						
$V_{o(nom)(rms)}$	nominal level output voltage (RMS value)	3 dB amplification	–	500	–	mV
$V_{o(clip)(rms)}$	clipping level output voltage (RMS value)	THD < 3%	1250	1400	–	mV
R_o	output resistance		150	250	375	Ω
$R_{L(AC)}$	AC load resistance		10	–	–	kΩ
$R_{L(DC)}$	DC load resistance		10	–	–	kΩ
C_L	load capacitance		–	–	2.5	nF
$V_{offset(DC)}$	static DC offset voltage	output amplifiers at 3 dB position	–	30	50	mV
α_{mute}	mute suppression	nominal input signal from any source; f_i = 1 kHz	80	–	–	dB
B	bandwidth	from SCART, external and mono sources; –3 dB bandwidth	20	–	–	kHz
		from DSP sources; –3 dB bandwidth	14.5	–	–	kHz
PSRR	power supply ripple rejection	f_{ripple} = 70 Hz; V_{ripple} = 100 mV (peak); C_{Vref} = 47 µF; signal from I²S-bus	40	45	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Audio performance						
THD + N	total harmonic distortion plus noise	$V_i = V_o$ = 1 V (RMS); f_i = 1 kHz; bandwidth 20 Hz to 15 kHz; note 8				
		from any analog audio input to I²S-bus	–	0.1	0.3	%
		from I²S-bus to any analog audio output	–	0.1	0.3	%
		SCART-to-SCART copy	–	0.1	0.3	%
		SCART-to-Main copy	–	0.2	0.5	%
S/N	signal-to-noise ratio	reference voltage V_o = 1.4 V (RMS); f_i = 1 kHz; *"CCIR468"*; quasi peak; note 8				
		from any analog audio input to I²S-bus	73	77	–	dB
		from I²S-bus to any analog audio output	78	85	–	dB
		SCART-to-SCART copy	78	85	–	dB
		SCART-to-Main copy	73	77	–	dB
α_{ct}	crosstalk attenuation	between any analog input pairs; f_i = 1 kHz	70	–	–	dB
		between any analog output pairs; f_i = 10 kHz	65	–	–	dB
α_{cs}	channel separation	between left and right of any input pair	65	–	–	dB
		between left and right of any output pair	60	–	–	dB
G_A	gain from SCART-to-SCART with –3 dB input voltage divider	output amplifier in 3 dB position; R_{ext} = 15 kΩ ±10%	–1.5	0	+1.1	dB
		output amplifier in 0 dB position; R_{ext} = 15 kΩ ±10%	–4.5	–3.0	–1.9	dB
Crystal specification (fundamental mode)						
f_{xtal}	crystal frequency		–	24.576	–	MHz
C_L	load capacitance		–	20	–	pF
C_1	series capacitance		–	20	–	fF
C_0	parallel capacitance		–	–	7	pF
Φ_{pull}	pulling sensitivity	C_L changed from 18 to 16 pF	–	25	–	$\frac{10^{-6}}{pF}$
R_R	equivalent series resistance	at nominal frequency	–	–	30	Ω
R_N	equivalent series resistance of unwanted mode		$2R_R$	–	–	Ω
ΔT	temperature range		–20	+25	+70	°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
X_J	adjustment tolerance		–	–	±30	10^{-6}
X_D	drift	across temperature range	–	–	±30	10^{-6}
X_A	ageing		–	–	±5	$\frac{10^{-6}}{year}$

Notes

1. Definitions of levels and level setting:
   a) The full-scale level for analog audio signals is 1.4 V (RMS).
   b) The nominal level at the digital crossbar switch is defined at –15 dB (full-scale).
   c) Nominal audio input levels for external and mono: 500 mV (RMS) at –9 dB (full-scale).
   d) See also Tables 6 and 7.
2. All analog and digital supply ground pins are connected internally.
3. Set demodulator to AM mode. Apply an AM carrier (with 1 kHz and 100%) to one channel. Check AGC step. Switch AGC off and set AGC to the gain step found. Measure the 1 kHz signal level of this channel and take it as a reference. Switch to the other SIF input to which no signal is connected and which is terminated with 50 Ω. Now measure the 1 kHz crosstalk signal level. The SIF source resistance should be low (50 Ω).
4. FM source; in dual mode only A (respectively B) signal modulated; measured at B (respectively A) channel output; V_o = 1 V (RMS) of modulated channel.
5. FM source; in stereo mode only L (respectively R) signal modulated; measured at R (respectively L) channel output; V_o = 1 V (RMS) of modulated channel. The stereo channel separation may be limited by adjustment tolerances of the transmitter.
6. If the supply voltage for the TDA9870A is switched off, because of the ESD protection circuitry, all audio input pins are short-circuited. To avoid a short-circuit at the SCART inputs a 15 kΩ resistor (–3 dB divider) has to be used.
7. The SCART specification allows a signal level of up to 2 V (RMS). Because of signal handling limitations due to the 5 V supply voltage for the TDA9870A, there is a need for fixed 3 dB attenuators at the SCART inputs. To achieve SCART-to-SCART copies with 0 dB gain, there are 3 and 0 dB amplifiers at the outputs of SCART 1 and SCART 2 and at the line output. The attenuator is realized by an internal resistor that works together with an external series resistor as a voltage divider. With this voltage divider the maximum SCART input signal level of 2 V (RMS) is scaled down to 1.4 V (RMS) at the input pin. To avoid clipping, the 3 dB gain must not be used if the SCART input signal is larger than 1.4 V (RMS).
8. ADC level adjust is 6 dB, all other level adjusts are 0 dB. If an external –3 dB divider is used set output buffer gain to 3 dB, tone control to 0 dB, AVL off and volume control to 0 dB.

Table 6 Level setting FM at 0 dB (full-scale) = 1.4 V (RMS); note 1

2 CHANNEL FM STANDARD	TRANSMITTER NOMINAL MODULATION DEPTH	NOMINAL LEVEL AT DEMODULATOR OUTPUT	CARRIER 1 FREQUENCY	CARRIER 2		DE-EMPHASIS OF CARRIER 1 AND CARRIER 2	FM LEVEL ADJUST SETTING OF CARRIER 1 AND CARRIER 2
				FREQUENCY	IDENT		
M	15 kHz deviation	–24 dB (full-scale); note 2	4.5 MHz	4.724 MHz	on	75 µs	+9 dB
B/G	27 kHz deviation	–19 dB (full-scale)	5.5 MHz	5.742 MHz	on	50 µs	+4 dB
D/K	27 kHz deviation	–19 dB (full-scale)	6.5 MHz	6.742 MHz	on	50 µs	+4 dB
	27 kHz deviation	–19 dB (full-scale)	6.5 MHz	6.25 MHz	on	50 µs	+4 dB
	27 kHz deviation	–19 dB (full-scale)	6.5 MHz	5.742 MHz	on	50 µs	+4 dB

Notes

1. Nominal level at digital crossbar is defined at –15 dB (full-scale). DAC gain setting 6 dB. Output buffer setting 0 dB. Nominal SCART output level 500 mV (RMS).
2. For stereo signals the output level is 6 dB lower. The level adjust has to be increased by 6 dB.

Table 7 Level setting SAT FM at 0 dB (full-scale) = 1.4 V (RMS)

SOURCE	TRANSMITTER MAXIMUM MODULATION DEPTH	NOMINAL LEVEL AT DEMODULATOR OUTPUT	FM LEVEL ADJUST SETTING	MAXIMUM LEVEL AT CROSSBAR	DAC GAIN SETTING	OUTPUT BUFFER	NOMINAL SCART OUTPUT VOLTAGE
SAT FM, stereo	50 kHz deviation	–13 dB (full-scale)	+4 dB	–9 dB (full-scale)	+6 dB	0 dB	1 V (RMS)
SAT FM, mono	85 kHz deviation	–9 dB (full-scale)	0 dB				

10 I²C-BUS CONTROL

10.1 Introduction

The TDA9870A is fully controlled via the I²C-bus. Control is exercised by writing data to one or more internal registers. Status information can be read from an array of registers to enable the controlling microcontroller to determine whether any action is required.

The device has an I²C-bus slave transceiver, in accordance with the fast-mode specification, with a maximum speed of 400 kbits/s. Information concerning the I²C-bus can be found in brochure *"I²C-bus and how to use it"* (order number 9398 393 40011). To avoid conflicts in a real application with other ICs providing similar or complementary functions, there are four possible slave addresses available which can be selected by pins ADDR1 and ADDR2 (see Table 8).

Table 8 Possible slave addresses

ADDR2	ADDR1	SLAVE ADDRESS						
		A6	A5	A4	A3	A2	A1	A0
LOW	LOW	1	0	1	1	0	0	0
LOW	HIGH	1	0	1	1	0	0	1
HIGH	LOW	1	0	1	1	0	1	0
HIGH	HIGH	1	0	1	1	0	1	1

The I²C-bus interface remains operational in the standby mode of the TDA9870A to allow control of the analog source selectors with regard to SCART-to-SCART copying.

The device will not respond to a 'general call' on the I²C-bus, i.e. when a slave address of 0000000 is sent by a master.

The data transmission between the microcontroller and the other I²C-bus controlled ICs is not disturbed when the supply voltage of the TDA9870A is not connected.

10.2 Power-up state

At power-up the device is in the following state:

- All outputs muted
- No sound carrier frequency loaded
- General purpose I/O pins ready for input (HIGH)
- Input SIF1 selected with:
  - AGC on
  - Small hysteresis
  - SIF input level shift 0 dB.
- Demodulators for both sound carriers set to FM with:
  - Identification for B/G, D/K, response time 1 s
  - Level adjust set to 0 dB
  - De-emphasis 50 μs
  - Matrix set to mono.
- Main channel set to FM input with:
  - Spatial off
  - Pseudo off
  - AVL off
  - Volume mute
  - Bass flat
  - Treble flat
  - Contour off
  - Bass boost flat.
- Auxiliary channel set to FM input with:
  - Volume mute
  - Bass flat
  - Treble flat.
- Feature interface all outputs off
- Beeper off
- Monitoring of carrier 1 FM demodulator DC output.

After power-up a device initialization has to be performed via the I²C-bus to put the TDA9870A into the proper mode of operation, in accordance with the desired TV standard, audio control settings, etc.

10.3 Slave receiver mode

As a slave receiver, the TDA9870A provides 46 registers for storing commands and data. These registers are accessed via so-called subaddresses. A subaddress can be thought of as a pointer to an internal memory location.

Table 9 I^2C-bus; slave address, subaddress and data format

S	SLAVE ADDRESS	0	ACK	SUBADDRESS	ACK	DATA	ACK	P

Table 10 Explanation of Table 9

BIT	FUNCTION
S	START condition
SLAVE ADDRESS	7-bit device address
0	data direction bit (write to device)
ACK	acknowledge by slave
SUBADDRESS	address of register to write to
DATA	data byte to be written into register
P	STOP condition

It is allowed to send more than one data byte per transmission to the TDA9870A. In this event, the subaddress is automatically incremented after each data byte, resulting in storing the sequence of data bytes at successive register locations, starting at SUBADDRESS. A transmission can start at any valid subaddress. Each byte is acknowledged with ACK (acknowledge).

There is no ‘wrap-around’ of subaddresses.

Commands and data are processed as soon as they have been completely received. Functions requiring more than one byte will, thus, be executed only after all bytes for that function have been received. If the transmission is terminated (STOP condition) before all bytes have been received, the incomplete data for that function are ignored.

Table 11 Format for a transmission employing auto-increment of subaddresses

S	SLAVE ADDRESS	0	ACK	SUBADDRESS	ACK	DATA BYTE A(1)	DATA	ACK	P

Note

1. n data bytes with auto-increment of subaddresses.

Data patterns sent to the various subaddresses are not checked for being illegal or not at that address, except for the functions of volume, bass and treble control, bass boost and level adjust.

Detection of a STOP condition without a preceding acknowledge bit is regarded as a bus error. The last operation will then not be executed.

Table 12 Overview of the slave receiver registers

SUBADDRESS (DECIMAL)	DATA								FUNCTION
	MSB							LSB	
0	0	0	s	g	g	g	g	g	AGC level shift, AGC gain selection
1	c	c	c	c	c	c	c	c	general configuration
2	p	0	0	m	m	s	s	s	monitor select, peak detector on/off
3	f	f	f	f	f	f	f	f	carrier 1 frequency; most significant part
4	f	f	f	f	f	f	f	f	carrier 1 frequency
5	f	f	f	f	f	f	f	f	carrier 1 frequency; least significant part
6	f	f	f	f	f	f	f	f	carrier 2 frequency; most significant part
7	f	f	f	f	f	f	f	f	carrier 2 frequency
8	f	f	f	f	f	f	f	f	carrier 2 frequency; least significant part
9	c	c	c	c	c	c	c	c	demodulator configuration
10	d	d	d	d	d	d	d	d	FM de-emphasis
11	0	0	0	0	0	m	m	m	FM matrix
12	0	0	0	l	l	l	l	l	channel 1 output level adjust
13	0	0	0	l	l	l	l	l	channel 2 output level adjust
14	0	0	0	0	0	0	0	0	set to logic 0; note 1
15	0	0	0	0	0	0	0	0	set to logic 0; note 1
16	0	0	0	0	0	0	0	0	set to logic 0; note 1
17	0	0	0	0	0	0	0	0	set to logic 0; note 1
18	m	m	m	m	m	m	m	m	audio mute control
19	g	m	m	m	g	s	s	s	DAC output select
20	0	g	m	m	0	s	s	s	SCART 1 output select
21	0	g	m	m	0	s	s	s	SCART 2 output select
22	0	g	m	m	0	0	0	s	line output select
23	s	s	s	l	l	l	l	l	ADC output select
24	0	m	m	m	0	s	s	s	Main channel select
25	0	0	s	s	p	p	a	a	audio effects (AVL, pseudo and spatial)
26	v	v	v	v	v	v	v	v	volume control, Main left
27	v	v	v	v	v	v	v	v	volume control, Main right
28	0	0	0	c	c	c	c	c	contour control, Main
29	0	0	0	b	b	b	b	b	bass control, Main
30	0	0	0	t	t	t	t	t	treble control, Main
31	0	m	m	m	0	s	s	s	Auxiliary channel select
32	v	v	v	v	v	v	v	v	volume control, Auxiliary left
33	v	v	v	v	v	v	v	v	volume control, Auxiliary right
34	0	0	0	b	b	b	b	b	bass control, Auxiliary
35	0	0	0	t	t	t	t	t	treble control, Auxiliary
36	0	0	0	c	c	c	c	c	feature interface configuration
37	0	m	m	m	0	s	s	s	I^2S1 output select

SUBADDRESS (DECIMAL)	DATA								FUNCTION
	MSB							LSB	
38	0	0	0	i	i	i	i	i	I^2S1 input level adjust
39	0	0	0	o	o	o	o	o	I^2S1 output level adjust
40	0	m	m	m	0	s	s	s	I^2S2 output select
41	0	0	0	i	i	i	i	i	I^2S2 input level adjust
42	0	0	0	o	o	o	o	o	I^2S2 output level adjust
43	0	0	0	0	0	f	f	f	beeper frequency
44	0	0	v	v	v	v	v	v	beeper volume, Main and Auxiliary
45	b	b	b	b	b	b	b	b	bass boost, Main left and right

Note

1. These bits have not been assigned to a function.

The following sub-sections provide a detailed description of the slave receiver registers.

10.3.1 AGC GAIN REGISTER

If the automatic gain control function is switched off in the general configuration register, the contents of this register will define a fixed gain of the AGC stage. The input voltages given are meant to generate a full-scale output from the SIF ADC. If automatic gain control is on, the AGCGAIN setting is ignored. After switching off the automatic gain control function, the latest gain control setting is copied to the AGC gain register.

If the AGC input level shift bit AGCLEV is set to logic 1 the input signal is scaled with −10 dB. The AGCLEV bit is also active if the automatic gain function is enabled.

It should be noted that the input voltages should be considered as approximate target values.

Table 13 Subaddress 0 (note 1)

BIT	NAME	VALUE	DESCRIPTION
7 (MSB)	B7	0	set to logic 0
6	B6	0	set to logic 0
5	AGCLEV	1	input signal scaled with −10 dB
		0	input signal not scaled
4	AGCGAIN	−	gain control bits (see Table 14).
3			
2			
1			
0 (LSB)			

Note

1. The default setting at power-up is 00000000.

Table 14 Gain control bits

MSB							LSB	AGC GAIN (dB)	SIF INPUT VOLTAGE [mV (p-p)]
B7	B6	B5	B4	B3	B2	B1	B0		
0	0	0/1	1	1	1	1	1	0.0	941/2976
0	0	0/1	1	1	1	1	0	0.8	861/2723
0	0	0/1	1	1	1	0	1	1.5	788/2490
0	0	0/1	1	1	1	0	0	2.3	720/2278
0	0	0/1	1	1	0	1	1	3.1	659/2084
0	0	0/1	1	1	0	1	0	3.9	603/1906
0	0	0/1	1	1	0	0	1	4.6	551/1744
0	0	0/1	1	1	0	0	0	5.4	504/1595
0	0	0/1	1	0	1	1	1	6.2	461/1459
0	0	0/1	1	0	1	1	0	7.0	422/1334
0	0	0/1	1	0	1	0	1	7.7	386/1221
0	0	0/1	1	0	1	0	0	8.5	353/1117
0	0	0/1	1	0	0	1	1	9.3	323/1021
0	0	0/1	1	0	0	1	0	10.1	295/934
0	0	0/1	1	0	0	0	1	10.8	270/855
0	0	0/1	1	0	0	0	0	11.6	247/782
0	0	0/1	0	1	1	1	1	12.4	226/715
0	0	0/1	0	1	1	1	0	13.2	207/654
0	0	0/1	0	1	1	0	1	13.9	189/598
0	0	0/1	0	1	1	0	0	14.7	173/547
0	0	0/1	0	1	0	1	1	15.5	158/501
0	0	0/1	0	1	0	1	0	16.3	145/458
0	0	0/1	0	1	0	0	1	17.0	132/419
0	0	0/1	0	1	0	0	0	17.8	121/383
0	0	0/1	0	0	1	1	1	18.6	111/350
0	0	0/1	0	0	1	1	0	19.4	101/321
0	0	0/1	0	0	1	0	1	20.1	93/293
0	0	0/1	0	0	1	0	0	20.9	85/268
0	0	0/1	0	0	0	1	1	21.7	78/245
0	0	0/1	0	0	0	1	0	22.5	71/224
0	0	0/1	0	0	0	0	1	23.2	65/205
0	0	0/1	0	0	0	0	0	24.0	59/188 (note 1)

Note

1. The default setting at power-up is 00000000.

10.3.2 General configuration register

Table 15 Subaddress 1 (note 1)

BIT	NAME	VALUE	DESCRIPTION
7 (MSB)	P2OUT	–	This bit controls the general purpose input/output pin P2. The contents of this bit is written directly to the corresponding pin. If input is desired, the bit must be set to logic 1 to allow the pin to be pulled LOW externally. Input from the pin is reflected in the device status register (see Section 10.4.1, subaddress 0).
6	P1OUT	–	This bit controls the general purpose input/output pin P1. The contents of this bit is written directly to the corresponding pin. If input is desired, the bit must be set to logic 1 to allow the pin to be pulled LOW externally. Input from the pin is reflected in the device status register (see Section 10.4.1, subaddress 0). P1OUT is recommended to be used for switching an SIF trap for the adjacent picture carrier in designs that employ such a trap.
5	STDBY	1	The TDA9870A is in the standby mode. Most functions are disabled and power dissipation is somewhat reduced, but the analog selectors/matrices remain operational to support analog copying from SCART-to-SCART.
		0	The TDA9870A is in normal operating mode. On return from standby mode, the device is in its Power-on reset mode and needs to be re-initialized.
4	INIT	1	Causes initialization of the TDA9870A to its default settings. This has the same effect as a Power-on reset. If there is a conflict between the default settings and any bit set to logic 1 in this register, the bits of this register have priority over the corresponding default setting.
		0	Automatically reset to logic 0 after initialization. When set to logic 0, the TDA9870A is in normal operating mode.
3	CLRPOR	1	Resets the power fail detector to LOW.
		0	This bit is automatically reset to logic 0 after bit POR in the device status register has been reset.
2	AGCSLOW	1	A longer decay time is selected for input signals with strong video modulation (intercarrier). This bit only has an effect when bit AGCOFF = 0.
		0	Selects normal attack and decay times for the AGC.
1	AGCOFF	1	Forces the AGC block to a fixed gain as defined in the AGC gain register.
		0	The automatic gain control function is enabled and the contents of the AGC gain register is ignored.
0 (LSB)	SIFSEL	1	Selects pin SIF2 for input (recommended for satellite tuner).
		0	Selects pin SIF1 for input (terrestrial TV).

Note

1. The default setting at power-up is 11000000.

10.3.3 MONITOR SELECT REGISTER

This register is used to define the signal source, the level of which is to be monitored, and if the peak level is to be monitored. Peak level refers to the magnitude of the maximum excursion of a signal.

Audio magnitude/phase is related to the FM demodulator output. Phase information is provided, when it operates in FM mode, while magnitude is supplied in AM mode.

Data can be read-out in the I^2C-bus slave transmitter mode. By reading out level read-out registers (subaddresses 5 and 6, see Section 10.4), the current peak level will be reset.

Table 16 Subaddress 2 (note 1)

BIT	NAME	VALUE	DESCRIPTION
7 (MSB)	PEAKMON	1	selects the peak level of a source to be monitored
		0	the last sample will be supplied
6	B6	0	default value
5	B5	0	default value
4	B4	–	monitor output (see Table 17)
3	B3		
2	B2	–	signal source (see Table 18)
1	B1		
0 (LSB)	B0		

Note

1. The default setting at power-up is 00000000.

Table 17 Monitor output

B4	B3	MONITOR OUTPUT
0	0	$\frac{\text{L input} + \text{R input}}{2}$
0	1	L input (channel 1, respectively)
1	0	R input (channel 2, respectively)

Table 18 Signal source (note 1)

B2	B1	B0	SIGNAL SOURCE
0	0	0	DC output of FM demodulator
0	0	1	audio magnitude/phase, FM demodulator output
0	1	0	crossbar input from FM/AM channel
0	1	1	don’t care
1	0	0	crossbar input from I^2S1 channel
1	0	1	crossbar input from I^2S2 channel
1	1	0	crossbar input from audio ADC channel
1	1	1	input to Main channel DAC (without beeper)

Note

1. The term ‘crossbar’ refers to the digital selector, where level-adjusted signals from various sources are available.

10.3.4 CARRIER 1 FREQUENCY REGISTER

The three bytes together constitute a 24-bit frequency control word to represent the sound carrier (i.e. mixer) frequency in accordance with the following formula:

$$data = \frac{f_{mix}}{f_{clk}} \times 2^{24}$$

Where:

data = 24-bit frequency control word

f_{mix} = desired sound carrier frequency

f_{clk} = 12.288 MHz (clock frequency of mixer)

2^{24} = 16777216 (number of steps in a 24-bit word size).

Example: A 5.5 MHz sound carrier frequency will be generated by sending the following sequence of data bytes to the TDA9870A (data = 7509333 in decimal notation or 729555 in hexadecimal):
01110010 10010101 01010101.

As three bytes are required to define a carrier frequency, execution of this command starts only after all bytes have been received. If an error occurs, e.g. a premature STOP condition, partial data for this function is ignored.

The default setting at power-up is 00000000 for all three bytes.

Most significant part at subaddress 3 and least significant part at subaddress 5 (see Table 19).

Table 19 Subaddresses 3 to 5

SUB-ADDRESS	BIT	DESCRIPTION
3	7 (MSB)	carrier 1 frequency; most significant part
	6	
	5	
	4	
	3	
	2	
	1	
	0	
4	7	carrier 1 frequency
	6	
	5	
	4	
	3	
	2	
	1	
	0	
5	7	carrier 1 frequency; least significant part
	6	
	5	
	4	
	3	
	2	
	1	
	0 (LSB)	

10.3.5 Carrier 2 frequency register

Same as for sound carrier 1, except for subaddresses (subaddresses 6 to 8). If the carrier 2 frequency register is used, it will be for the second FM sound carrier of a terrestrial or satellite FM program.

10.3.6 Demodulator configuration register

It is recommended to switch the FM sound mode identification off whenever the received program is not a terrestrial 2-carrier sound. Switching the identification off will reset the associated hardware to a defined state.

Table 20 Subaddress 9 (note 1)

BIT	NAME	VALUE	DESCRIPTION
7 (MSB)	IDMOD1	–	these bits define the response time after which a FM sound mode identification result may be expected; the longer the time, the more reliable the identification (see Table 21)
6	IDMOD0		
5	IDAREA	1	selects FM identification frequencies in accordance with the specification for Korea
		0	selects frequencies for Europe (B/G and D/K standard)
4	FILTBW1	–	selects filter bandwidth (see Table 22)
3	CH2MOD1	–	channel 2 receive mode: these bits control the hardware for the second sound carrier (see Table 23)
2	CH2MOD0		
1	FILTBW0	–	selects filter bandwidth (see Table 22)
0 (LSB)	CH1MODE	1	selects the hardware for the first sound carrier to operate in AM mode
		0	FM mode is assumed; this applies to both terrestrial and satellite FM reception

Note

1. The default setting at power-up is 00000000.

Table 21 Identification mode

B7	B6	IDENT MODE
0	0	slow
0	1	medium
1	0	fast
1	1	off/reset

Table 22 Filter bandwidth channel 1 and channel 2

B4	B1	FILTER BANDWIDTH		FILTER MODES
		CH1	CH2	
0	0	narrow	narrow	recommended for nominal terrestrial broadcast conditions and SAT with 2 carriers
0	1	extra wide	narrow	recommended only for high-deviation SAT mono carriers (e.g. obsolete Main channel on Astra)
1	0	medium	medium	recommended for moderately overmodulated broadcast conditions
1	1	wide	wide	recommended for strongly overmodulated broadcast conditions

Table 23 Channel 2 receive mode

B3	B2	CHANNEL 2
0	0	FM
0	1	AM
1	0	don't care

10.3.7 FM DE-EMPHASIS REGISTER

This register is used to select the proper de-emphasis characteristics as appropriate for the standard of the received carrier. Bits B3 to B0 apply to sound carrier 1, bits B7 to B4 apply to sound carrier 2.

In the event of A2 reception, both groups must be set to the same characteristics.

Table 24 Subaddress 10 (note 1)

BIT	NAME	VALUE	DESCRIPTION
7 (MSB)	ADEEM2	1	Activates the adaptive de-emphasis function, which is required for certain satellite FM channels. The standard FM de-emphasis must then be set to 75 μs (note 2).
		0	The adaptive de-emphasis is off.
6	B6	–	Time constant selection for FM de-emphasis (see Table 25).
5	B5		
4	B4		
3	ADEEM1	1	Activates the adaptive de-emphasis function, which is required for certain satellite FM channels. The standard FM de-emphasis must then be set to 75 μs (note 2).
		0	The adaptive de-emphasis is off.
2	B2	–	Time constant selection for FM de-emphasis (see Table 26).
1	B1		
0 (LSB)	B0		

Notes

1. The default setting at power-up is 00000000.
2. The FM de-emphasis gain is 0 dB at 40 Hz.

Table 25 De-emphasis sound carrier 2

B6	B5	B4	DE-EMPHASIS
0	0	0	50 μs (Europe)
0	0	1	60 μs
0	1	0	75 μs (M standard)
0	1	1	J17
1	0	0	off

Table 26 De-emphasis sound carrier 1

B2	B1	B0	DE-EMPHASIS
0	0	0	50 μs (Europe)
0	0	1	60 μs
0	1	0	75 μs (M standard)
0	1	1	J17
1	0	0	off

10.3.8 FM MATRIX REGISTER

This register is used to select the proper dematrixing characteristics as appropriate for the standard of the received carrier and the related sound mode identification.

Table 27 Subaddress 11 (note 1)

BIT	NAME	VALUE	DESCRIPTION
7 (MSB)	B7	0	default value
6	B6	0	default value
5	B5	0	default value
4	B4	0	default value
3	B3	0	default value
2	B2	–	dematrixing characteristics (see Table 28)
1	B1		
0 (LSB)	B0		

Note

1. The default setting at power-up is 00000000.

Table 28 Dematrixing characteristics

B2	B1	B0	L OUTPUT	R OUTPUT	MODE
0	0	0	CH1 input; note 1	CH1 input; note 1	mono 1
0	0	1	CH2 input; note 2	CH2 input; note 2	mono 2
0	1	0	CH1 input; note 1	CH2 input; note 2	dual
0	1	1	CH2 input; note 2	CH1 input; note 1	dual swapped
1	0	0	2CH1 input – CH2 input	CH2 input; note 2	stereo Europe
1	0	1	$\frac{\text{CH1 input} + \text{CH2 input}}{2}$	$\frac{\text{CH1 input} - \text{CH2 input}}{2}$	stereo Korea; note 3

Notes

1. CH1 input: audio signal from FM channel 1.
2. CH2 input: audio signal from FM channel 2.
3. For stereo Korea the dematrix applies 6 dB attenuation (see Table 6).

10.3.9 FM CHANNEL 1 LEVEL ADJUST REGISTER

This register is used to correct for standard and station-dependent differences of signal levels.

Table 29 applies to sound carrier 1.

Table 29 Subaddress 12

MSB							LSB	GAIN SETTING (dB)
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
0	0	0	0	1	1	1	1	+15
0	0	0	0	1	1	1	0	+14
0	0	0	0	1	1	0	1	+13
0	0	0	0	1	1	0	0	+12
0	0	0	0	1	0	1	1	+11
0	0	0	0	1	0	1	0	+10
0	0	0	0	1	0	0	1	+9
0	0	0	0	1	0	0	0	+8
0	0	0	0	0	1	1	1	+7
0	0	0	0	0	1	1	0	+6
0	0	0	0	0	1	0	1	+5
0	0	0	0	0	1	0	0	+4
0	0	0	0	0	0	1	1	+3
0	0	0	0	0	0	1	0	+2
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0 (note 1)
0	0	0	1	1	1	1	1	−1
0	0	0	1	1	1	1	0	−2
0	0	0	1	1	1	0	1	−3
0	0	0	1	1	1	0	0	−4
0	0	0	1	1	0	1	1	−5
0	0	0	1	1	0	1	0	−6
0	0	0	1	1	0	0	1	−7
0	0	0	1	1	0	0	0	−8
0	0	0	1	0	1	1	1	−9
0	0	0	1	0	1	1	0	−10
0	0	0	1	0	1	0	1	−11
0	0	0	1	0	1	0	0	−12
0	0	0	1	0	0	1	1	−13
0	0	0	1	0	0	1	0	−14
0	0	0	1	0	0	0	1	−15
0	0	0	1	0	0	0	0	mute

Note

1. The default setting at power-up is 00000000.

10.3.10 FM CHANNEL 2 LEVEL ADJUST REGISTER

This register is used to correct for standard and station-dependent differences of signal levels. Table 30 applies to sound carrier 2 in its FM and AM modes. In the event of A2, channels 1 and 2 should be adjusted to the same level.

Table 30 Subaddress 13

MSB							LSB	GAIN SETTING (dB)
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
0	0	0	0	1	1	1	1	+15
0	0	0	0	1	1	1	0	+14
0	0	0	0	1	1	0	1	+13
0	0	0	0	1	1	0	0	+12
0	0	0	0	1	0	1	1	+11
0	0	0	0	1	0	1	0	+10
0	0	0	0	1	0	0	1	+9
0	0	0	0	1	0	0	0	+8
0	0	0	0	0	1	1	1	+7
0	0	0	0	0	1	1	0	+6
0	0	0	0	0	1	0	1	+5
0	0	0	0	0	1	0	0	+4
0	0	0	0	0	0	1	1	+3
0	0	0	0	0	0	1	0	+2
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0 (note 1)
0	0	0	1	1	1	1	1	–1
0	0	0	1	1	1	1	0	–2
0	0	0	1	1	1	0	1	–3
0	0	0	1	1	1	0	0	–4
0	0	0	1	1	0	1	1	–5
0	0	0	1	1	0	1	0	–6
0	0	0	1	1	0	0	1	–7
0	0	0	1	1	0	0	0	–8
0	0	0	1	0	1	1	1	–9
0	0	0	1	0	1	1	0	–10
0	0	0	1	0	1	0	1	–11
0	0	0	1	0	1	0	0	–12
0	0	0	1	0	0	1	1	–13
0	0	0	1	0	0	1	0	–14
0	0	0	1	0	0	0	1	–15
0	0	0	1	0	0	0	0	mute

Note

1. The default setting at power-up is 00000000.

10.3.11 Register 14

Set to logic 0. These bits have not been assigned to a function.

10.3.12 Register 15

Set to logic 0. These bits have not been assigned to a function.

10.3.13 Register 16

Set to logic 0. These bits have not been assigned to a function.

10.3.14 Register 17

Set to logic 0. These bits have not been assigned to a function.

10.3.15 Audio mute control register

When any of these bits are set to logic 1, the corresponding pair of output channels will be muted. A bit set to logic 0 allows normal signal output.

There is a soft-mute facility for the Main and Auxiliary output channels to provide click-free muting independent of the volume control. This is switched on/off by bits MUTMAIN and MUTAUX.

Table 31 Subaddress 18 (note 1)

BIT	NAME	VALUE	DESCRIPTION
7 (MSB)	MUTI^{2}S2	1	mute I^{2}S2 outputs
		0	normal I^{2}S2 outputs
6	MUTI^{2}S1	1	mute I^{2}S1 outputs
		0	normal I^{2}S1 outputs
5	MUTDAC	1	mute internal DAC
		0	normal internal DAC
4	MUTLINE	1	mute line outputs
		0	normal line outputs
3	MUTSC2	1	mute SCART 2 outputs
		0	normal SCART 2 outputs
2	MUTSC1	1	mute SCART 1 outputs
		0	normal SCART 1 outputs
1	MUTAUX	1	mute Auxiliary outputs
		0	normal Auxiliary outputs
0 (LSB)	MUTMAIN	1	mute Main outputs
		0	normal Main outputs

Note

1. The default setting at power-up is 11111111.

10.3.16 DAC OUTPUT SELECT REGISTER

This register is used to define both the signal source to be entered into the DAC and the mode of the digital matrix for signal selection. The DAC is used for signal output from digital sources at analog outputs.

The bits DACGAIN1 and DACGAIN2 can introduce some extra gain at the input to the DAC. DACGAIN1 adds 3 dB and DACGAIN2 adds 6 dB of gain, respectively.

Table 32 Subaddress 19 (note 1)

BIT	NAME	VALUE	DESCRIPTION
7 (MSB)	DACGAIN2	–	extra gain setting (see Table 33)
6	B6	–	DAC output selection (see Table 34)
5	B5		
4	B4		
3	DACGAIN1	–	extra gain setting (see Table 33)
2	B2	–	signal source selection (see Table 35)
1	B1		
0 (LSB)	B0		

Note

1. The default setting at power-up is 00000000.

Table 33 Extra gain setting

B7	B3	GAIN (dB)
0	0	0
0	1	3
1	0	6
1	1	9

Table 34 DAC output selection

B6	B5	B4	L OUTPUT	R OUTPUT
0	0	0	L input	R input
0	0	1	L input	L input
0	1	0	R input	R input
0	1	1	R input	L input
1	0	0	$\frac{L + R}{2}$	$\frac{L + R}{2}$

Table 35 Signal source selection

B2	B1	B0	SIGNAL SOURCE	
			LEFT	RIGHT
0	0	0	FM left	FM right
0	0	1	don’t care	
0	1	0	I^2S1 left	I^2S1 right
0	1	1	I^2S2 left	I^2S2 right
1	0	0	ADC left	ADC right
1	0	1	AVL left	AVL right
1	1	0	don’t care	
1	1	1	don’t care	

10.3.17 SCART 1 OUTPUT SELECT REGISTER

This register is used to define both the signal source to be output at SCART 1 and the output channel selector mode.

Table 36 Subaddress 20 (note 1)

BIT	NAME	VALUE	DESCRIPTION
7 (MSB)	B7	0	default value
6	SC1GAIN	1	Activates the 3 dB gain stage at the SCART 1 output buffers. As any SCART input passes a 3 dB attenuator, this gain stage can be used to compensate that attenuation, resulting in a 0 dB insertion loss when copying from SCART 2 input to SCART 1 output. However, that gain must be used with great care, as it will cause signal clipping at high input levels.
		0	the audio signal output will be unchanged (0 dB gain)
5	B5	–	output channel selection (see Table 37)
4	B4		
3	B3	0	default value
2	B2	–	signal source selection (see Table 38)
1	B1		
0 (LSB)	B0		

Note

1. The default setting at power-up is 00000001.

Table 37 Output channel selection

B5	B4	L OUTPUT	R OUTPUT
0	0	L input	R input
0	1	L input	L input
1	0	R input	R input
1	1	R input	L input

Table 38 Signal source selection

B2	B1	B0	SIGNAL SOURCE
0	0	0	SCART 1 input
0	0	1	SCART 2 input
0	1	0	external input
0	1	1	mono input
1	0	0	DAC input

10.3.18 SCART 2 OUTPUT SELECT REGISTER

This register is used to define both the signal source to be output at SCART 2 and the output channel selector mode.

Table 39 Subaddress 21 (note 1)

BIT	NAME	VALUE	DESCRIPTION
7 (MSB)	B7	0	default value
6	SC2GAIN	1	Activates the 3 dB gain stage at the SCART 2 output buffers. As any SCART input passes a 3 dB attenuator, this gain stage can be used to compensate that attenuation, resulting in a 0 dB insertion loss when copying from SCART 1 input to SCART 2 output. However, that gain must be used with great care, as it will cause signal clipping at high input levels.
		0	the audio signal output will be unchanged (0 dB gain)
5	B5	–	output channel selection (see Table 40)
4	B4		
3	B3	0	default value
2	B2	–	signal source selection (see Table 41)
1	B1		
0 (LSB)	B0		

Note

1. The default setting at power-up is 00000000.

Table 40 Output channel selection

B5	B4	L OUTPUT	R OUTPUT
0	0	L input	R input
0	1	L input	L input
1	0	R input	R input
1	1	R input	L input

Table 41 Signal source selection

B2	B1	B0	SIGNAL SOURCE
0	0	0	SCART 1 input
0	0	1	SCART 2 input
0	1	0	external input
0	1	1	mono input
1	0	0	DAC input

10.3.19 LINE OUTPUT SELECT REGISTER

By definition, the line output conveys the same signal as the Main (loudspeaker) channel, but in a non-processed form. This register is used to characterize the signal to be output at the line output and define the output channel selector mode.

Table 42 Subaddress 22 (note 1)

BIT	NAME	VALUE	DESCRIPTION
7 (MSB)	B7	0	set to logic 0
6	LINGAIN	1	activates the 3 dB gain stage at the line output buffers
		0	the audio signal output will be unchanged (0 dB gain)
5	B5	–	output channel selection (see Table 43)
4	B4		
3	B3	0	set to logic 0
2	B2	0	set to logic 0
1	B1	0	set to logic 0
0 (LSB)	LINSEL	1	A signal from an analog source is being processed in the Main channel for line output. Analog signal sources comprise SCART 1 input, SCART 2 input, external input and mono input, i.e. any input to the ADC.
		0	A signal from a digital source is being processed in the Main channel for line output. Digital signal sources comprise FM, I^2S1 input and I^2S2 input.

Note

1. The default setting at power-up is 00000000.

Table 43 Output channel selection

B5	B4	L OUTPUT	R OUTPUT
0	0	L input	R input
0	1	L input	L input
1	0	R input	R input
1	1	R input	L input

10.3.20 ADC OUTPUT SELECT REGISTER

This register is used to define the signal source for the ADC. There is no output channel selector, because all digital signal sinks of the ADC have their own matrix. Instead, a level adjustment facility for the ADC output is provided.

Table 44 Subaddress 23 (note 1)

BIT	NAME	VALUE	DESCRIPTION
7 (MSB)	B7	–	signal source selection (see Table 45)
6	B6		
5	B5		
4	B4	–	ADC level adjust (see Table 46)
3	B3		
2	B2		
1	B1		
0 (LSB)	B0		

Note

1. The default setting at power-up is 00000000.

Table 45 Signal source selection

B7	B6	B5	SIGNAL SOURCE
0	0	0	SCART 1 input
0	0	1	SCART 2 input
0	1	0	external input
0	1	1	mono input

Table 46 ADC level adjust (note 1)

B4	B3	B2	B1	B0	GAIN SETTING (dB)
0	1	1	1	1	+15
0	1	1	1	0	+14
0	1	1	0	1	+13
0	1	1	0	0	+12
0	1	0	1	1	+11
0	1	0	1	0	+10
0	1	0	0	1	+9
0	1	0	0	0	+8
0	0	1	1	1	+7
0	0	1	1	0	+6
0	0	1	0	1	+5
0	0	1	0	0	+4
0	0	0	1	1	+3
0	0	0	1	0	+2
0	0	0	0	1	+1
0	0	0	0	0	0
1	1	1	1	1	−1
1	1	1	1	0	−2
1	1	1	0	1	−3
1	1	1	0	0	−4
1	1	0	1	1	−5
1	1	0	1	0	−6
1	1	0	0	1	−7
1	1	0	0	0	−8
1	0	1	1	1	−9
1	0	1	1	0	−10
1	0	1	0	1	−11
1	0	1	0	0	−12
1	0	0	1	1	−13
1	0	0	1	0	−14
1	0	0	0	1	−15
1	0	0	0	0	mute

Note

1. If the ADC level adjust is set to 0 dB a full-scale input signal to the ADC results into a level of −6 dB full-scale at the digital crossbar.

10.3.21 MAIN CHANNEL SELECT REGISTER

This register is used to define both the signal source to be processed in the Main (loudspeaker) channel and the mode of the digital matrix for signal selection.

Table 47 Subaddress 24 (note 1)

BIT	NAME	VALUE	DESCRIPTION
7 (MSB)	B7	0	default value
6	B6	–	output channel selection (see Table 48)
5	B5		
4	B4		
3	B3	0	default value
2	B2	–	signal source selection (see Table 49)
1	B1		
0 (LSB)	B0		

Note

1. The default setting at power-up is 00000000.

Table 48 Output channel selection

B6	B5	B4	L OUTPUT	R OUTPUT
0	0	0	L input	R input
0	0	1	L input	L input
0	1	0	R input	R input
0	1	1	R input	L input
1	0	0	$\frac{L+R}{2}$	$\frac{L+R}{2}$

Table 49 Signal source selection

B2	B1	B0	SIGNAL SOURCE
0	0	0	FM input
0	0	1	don’t care
0	1	0	I^2S1 input
0	1	1	I^2S2 input
1	0	0	ADC input

10.3.22 AUDIO EFFECTS REGISTER

Switching the AVL off will reset the associated hardware to a defined state.

When the signal source for the Main channel is changed while the AVL is on, the AVL needs to be reset in order to avoid excessive settling times. This can be achieved by switching the AVL off and on again.

The pseudo stereo function is based on an all-pass filter. A 90 degrees phase shift occurs at the frequencies stated in Table 52. There is a gain of 3 dB in the left audio channel.

Table 50 Subaddress 25 (note 1)

BIT	NAME	VALUE	DESCRIPTION
7 (MSB)	B7	0	Default value.
6	B6	0	Default value.
5	SPATIAL1	–	These bits set the amount of the effect function (stereo base width expansion) for stereo signals in the Main channel (see Table 51). This function should be activated only in accordance with the result of the sound mode identification.
4	SPATIAL0		
3	PSEUDO1	–	These bits set the amount of the effect function (pseudo stereo) for mono signals in the Main channel (see Table 52). This function should be activated only in accordance with the result of the sound mode identification.
2	PSEUDO0		
1	AVL1	–	These bits set the mode of operation of the automatic volume level control function at the entrance to the Main (loudspeaker) channel (see Table 53).
0 (LSB)	AVL0		

Note

1. The default setting at power-up is 00000000.

Table 51 Spatial control setting

B5	B4	SPATIAL SETTING (%)
0	0	off
0	1	30
1	0	40
1	1	52

Table 52 Pseudo control setting

B3	B2	PSEUDO SETTING (Hz)
0	0	off
0	1	300
1	0	200
1	1	150

Table 53 AVL control mode

B1	B0	AVL MODE
0	0	off/reset
0	1	short decay
1	0	medium decay
1	1	long decay

10.3.23 VOLUME CONTROL REGISTERS (MAIN)

These two registers control the volume setting of the Main (loudspeaker) channel. The register at subaddress 26 applies to the left channel signal, while the register at subaddress 27 applies to the right channel signal.

Balance control is exercised by offsetting the left and right channel volume settings.

Table 54 Subaddresses 26 and 27

MSB							LSB	VOLUME SETTING (dB)
B7	B6	B5	B4	B3	B2	B1	B0	
0	0	0	1	1	0	0	0	+24
0	0	0	1	0	1	1	1	+23
0	0	0	1	0	1	1	0	+22
0	0	0	1	0	1	0	1	+21
0	0	0	1	0	1	0	0	+20
0	0	0	1	0	0	1	1	+19
0	0	0	1	0	0	1	0	+18
0	0	0	1	0	0	0	1	+17
0	0	0	1	0	0	0	0	+16
0	0	0	0	1	1	1	1	+15
0	0	0	0	1	1	1	0	+14
0	0	0	0	1	1	0	1	+13
0	0	0	0	1	1	0	0	+12
0	0	0	0	1	0	1	1	+11
0	0	0	0	1	0	1	0	+10
0	0	0	0	1	0	0	1	+9
0	0	0	0	1	0	0	0	+8
0	0	0	0	0	1	1	1	+7
0	0	0	0	0	1	1	0	+6
0	0	0	0	0	1	0	1	+5
0	0	0	0	0	1	0	0	+4
0	0	0	0	0	0	1	1	+3
0	0	0	0	0	0	1	0	+2
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1	–1
1	1	1	1	1	1	1	0	–2
1	1	1	1	1	1	0	1	–3
1	1	1	1	1	1	0	0	–4
1	1	1	1	1	0	1	1	–5
1	1	1	1	1	0	1	0	–6
1	1	1	1	1	0	0	1	–7
1	1	1	1	1	0	0	0	–8
1	1	1	1	0	1	1	1	–9

MSB							LSB	VOLUME SETTING (dB)
B7	B6	B5	B4	B3	B2	B1	B0	
1	1	1	1	0	1	1	0	–10
1	1	1	1	0	1	0	1	–11
1	1	1	1	0	1	0	0	–12
1	1	1	1	0	0	1	1	–13
1	1	1	1	0	0	1	0	–14
1	1	1	1	0	0	0	1	–15
1	1	1	1	0	0	0	0	–16
1	1	1	0	1	1	1	1	–17
1	1	1	0	1	1	1	0	–18
1	1	1	0	1	1	0	1	–19
1	1	1	0	1	1	0	0	–20
1	1	1	0	1	0	1	1	–21
1	1	1	0	1	0	1	0	–22
1	1	1	0	1	0	0	1	–23
1	1	1	0	1	0	0	0	–24
1	1	1	0	0	1	1	1	–25
1	1	1	0	0	1	1	0	–26
1	1	1	0	0	1	0	1	–27
1	1	1	0	0	1	0	0	–28
1	1	1	0	0	0	1	1	–29
1	1	1	0	0	0	1	0	–30
1	1	1	0	0	0	0	1	–31
1	1	1	0	0	0	0	0	–32
1	1	0	1	1	1	1	1	–33
1	1	0	1	1	1	1	0	–34
1	1	0	1	1	1	0	1	–35
1	1	0	1	1	1	0	0	–36
1	1	0	1	1	0	1	1	–37
1	1	0	1	1	0	1	0	–38
1	1	0	1	1	0	0	1	–39
1	1	0	1	1	0	0	0	–40
1	1	0	1	0	1	1	1	–41
1	1	0	1	0	1	1	0	–42
1	1	0	1	0	1	0	1	–43
1	1	0	1	0	1	0	0	–44
1	1	0	1	0	0	1	1	–45
1	1	0	1	0	0	1	0	–46
1	1	0	1	0	0	0	1	–47
1	1	0	1	0	0	0	0	–48

MSB							LSB	VOLUME SETTING (dB)
B7	B6	B5	B4	B3	B2	B1	B0	
1	1	0	0	1	1	1	1	–49
1	1	0	0	1	1	1	0	–50
1	1	0	0	1	1	0	1	–51
1	1	0	0	1	1	0	0	–52
1	1	0	0	1	0	1	1	–53
1	1	0	0	1	0	1	0	–54
1	1	0	0	1	0	0	1	–55
1	1	0	0	1	0	0	0	–56
1	1	0	0	0	1	1	1	–57
1	1	0	0	0	1	1	0	–58
1	1	0	0	0	1	0	1	–59
1	1	0	0	0	1	0	0	–60
1	1	0	0	0	0	1	1	–61
1	1	0	0	0	0	1	0	–62
1	1	0	0	0	0	0	1	–63
1	1	0	0	0	0	0	0	–64
1	0	1	1	1	1	1	1	–65
1	0	1	1	1	1	1	0	–66
1	0	1	1	1	1	0	1	–67
1	0	1	1	1	1	0	0	–68
1	0	1	1	1	0	1	1	–69
1	0	1	1	1	0	1	0	–70
1	0	1	1	1	0	0	1	–71
1	0	1	1	1	0	0	0	–72
1	0	1	1	0	1	1	1	–73
1	0	1	1	0	1	1	0	–74
1	0	1	1	0	1	0	1	–75
1	0	1	1	0	1	0	0	–76
1	0	1	1	0	0	1	1	–77
1	0	1	1	0	0	1	0	–78
1	0	1	1	0	0	0	1	–79
1	0	1	1	0	0	0	0	–80
1	0	1	0	1	1	1	1	–81
1	0	1	0	1	1	1	0	–82
1	0	1	0	1	1	0	1	–83
1	0	1	0	1	1	0	0	mute (note 1)

Note

1. The default setting at power-up is 10101100.

10.3.24 CONTOUR CONTROL REGISTER

This register is used to apply the contour or loudness function (physiological volume control) to the left and right signal channels of the Main channel by means of an extra bass boost. The gain setting must be chosen in accordance with the volume control setting for the Main channel. For example, the contour gain could be incremented for every 5 dB, or so, of decrease of the volume setting. This needs to be done by the microcontroller. The 0 dB contour setting is equal to contour off.

Table 55 Subaddress 28

MSB							LSB	CONTOUR GAIN (dB)
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
0	0	0	1	0	0	1	0	18
0	0	0	1	0	0	0	1	17
0	0	0	1	0	0	0	0	16
0	0	0	0	1	1	1	1	15
0	0	0	0	1	1	1	0	14
0	0	0	0	1	1	0	1	13
0	0	0	0	1	1	0	0	12
0	0	0	0	1	0	1	1	11
0	0	0	0	1	0	1	0	10
0	0	0	0	1	0	0	1	9
0	0	0	0	1	0	0	0	8
0	0	0	0	0	1	1	1	7
0	0	0	0	0	1	1	0	6
0	0	0	0	0	1	0	1	5
0	0	0	0	0	1	0	0	4
0	0	0	0	0	0	1	1	3
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	0 (note 1)

Note

1. The default setting at power-up is 00000000.

10.3.25 BASS CONTROL REGISTER (MAIN)

This register is used to apply bass control to the left and right signal channels of the Main channel.

Table 56 Subaddress 29

MSB							LSB	BASS SETTING (dB)
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
0	0	0	0	1	1	1	1	+15
0	0	0	0	1	1	1	0	+14
0	0	0	0	1	1	0	1	+13
0	0	0	0	1	1	0	0	+12
0	0	0	0	1	0	1	1	+11
0	0	0	0	1	0	1	0	+10
0	0	0	0	1	0	0	1	+9
0	0	0	0	1	0	0	0	+8
0	0	0	0	0	1	1	1	+7
0	0	0	0	0	1	1	0	+6
0	0	0	0	0	1	0	1	+5
0	0	0	0	0	1	0	0	+4
0	0	0	0	0	0	1	1	+3
0	0	0	0	0	0	1	0	+2
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0 (note 1)
0	0	0	1	1	1	1	1	–1
0	0	0	1	1	1	1	0	–2
0	0	0	1	1	1	0	1	–3
0	0	0	1	1	1	0	0	–4
0	0	0	1	1	0	1	1	–5
0	0	0	1	1	0	1	0	–6
0	0	0	1	1	0	0	1	–7
0	0	0	1	1	0	0	0	–8
0	0	0	1	0	1	1	1	–9
0	0	0	1	0	1	1	0	–10
0	0	0	1	0	1	0	1	–11
0	0	0	1	0	1	0	0	–12

Note

1. The default setting at power-up is 00000000.

10.3.26 TREBLE CONTROL REGISTER (MAIN)

This register is used to apply treble control to the left and right signal channels of the Main channel.

Table 57 Subaddress 30

MSB							LSB	TREBLE SETTING (dB)
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
0	0	0	0	1	1	0	0	+12
0	0	0	0	1	0	1	1	+11
0	0	0	0	1	0	1	0	+10
0	0	0	0	1	0	0	1	+9
0	0	0	0	1	0	0	0	+8
0	0	0	0	0	1	1	1	+7
0	0	0	0	0	1	1	0	+6
0	0	0	0	0	1	0	1	+5
0	0	0	0	0	1	0	0	+4
0	0	0	0	0	0	1	1	+3
0	0	0	0	0	0	1	0	+2
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0 (note 1)
0	0	0	1	1	1	1	1	–1
0	0	0	1	1	1	1	0	–2
0	0	0	1	1	1	0	1	–3
0	0	0	1	1	1	0	0	–4
0	0	0	1	1	0	1	1	–5
0	0	0	1	1	0	1	0	–6
0	0	0	1	1	0	0	1	–7
0	0	0	1	1	0	0	0	–8
0	0	0	1	0	1	1	1	–9
0	0	0	1	0	1	1	0	–10
0	0	0	1	0	1	0	1	–11
0	0	0	1	0	1	0	0	–12

Note

1. The default setting at power-up is 00000000.

10.3.27 AUXILIARY CHANNEL SELECT REGISTER

This register is used to define both the signal source to be processed in the Auxiliary (headphone) channel and the mode of the digital matrix for signal selection.

Table 58 Subaddress 31 (note 1)

BIT	NAME	VALUE	DESCRIPTION
7 (MSB)	B7	0	default value
6	B6	–	output channel selection (see Table 59)
5	B5		
4	B4		
3	B3	0	default value
2	B2	–	signal source selection (see Table 60)
1	B1		
0 (LSB)	B0		

Note

1. The default setting at power-up is 00000000.

Table 59 Output channel selection

B6	B5	B4	L OUTPUT	R OUTPUT
0	0	0	L input	R input
0	0	1	L input	L input
0	1	0	R input	R input
0	1	1	R input	L input
1	0	0	$\frac{L+R}{2}$	$\frac{L+R}{2}$

Table 60 Signal source selection

B2	B1	B0	SIGNAL SOURCE
0	0	0	FM input
0	0	1	don’t care
0	1	0	I^2S1 input
0	1	1	I^2S2 input
1	0	0	ADC input
1	0	1	AVL input

10.3.28 VOLUME CONTROL REGISTERS (AUXILIARY)

These two registers control the volume setting of the Auxiliary (headphone) channel. The register at subaddress 32 applies to the left channel signal, while the register at subaddress 33 applies to the right channel signal.

Balance control is exercised by offsetting the left and right channel volume settings.

Table 61 Subaddresses 32 and 33

MSB							LSB	VOLUME SETTING (dB)
B7	B6	B5	B4	B3	B2	B1	B0	
0	0	0	1	1	0	0	0	+24
0	0	0	1	0	1	1	1	+23
0	0	0	1	0	1	1	0	+22
0	0	0	1	0	1	0	1	+21
0	0	0	1	0	1	0	0	+20
0	0	0	1	0	0	1	1	+19
0	0	0	1	0	0	1	0	+18
0	0	0	1	0	0	0	1	+17
0	0	0	1	0	0	0	0	+16
0	0	0	0	1	1	1	1	+15
0	0	0	0	1	1	1	0	+14
0	0	0	0	1	1	0	1	+13
0	0	0	0	1	1	0	0	+12
0	0	0	0	1	0	1	1	+11
0	0	0	0	1	0	1	0	+10
0	0	0	0	1	0	0	1	+9
0	0	0	0	1	0	0	0	+8
0	0	0	0	0	1	1	1	+7
0	0	0	0	0	1	1	0	+6
0	0	0	0	0	1	0	1	+5
0	0	0	0	0	1	0	0	+4
0	0	0	0	0	0	1	1	+3
0	0	0	0	0	0	1	0	+2
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1	−1
1	1	1	1	1	1	1	0	−2
1	1	1	1	1	1	0	1	−3
1	1	1	1	1	1	0	0	−4
1	1	1	1	1	0	1	1	−5
1	1	1	1	1	0	1	0	−6
1	1	1	1	1	0	0	1	−7
1	1	1	1	1	0	0	0	−8
1	1	1	1	0	1	1	1	−9
1	1	1	1	0	1	1	0	−10

MSB							LSB	VOLUME SETTING (dB)
B7	B6	B5	B4	B3	B2	B1	B0	
1	1	1	1	0	1	0	1	–11
1	1	1	1	0	1	0	0	–12
1	1	1	1	0	0	1	1	–13
1	1	1	1	0	0	1	0	–14
1	1	1	1	0	0	0	1	–15
1	1	1	1	0	0	0	0	–16
1	1	1	0	1	1	1	1	–17
1	1	1	0	1	1	1	0	–18
1	1	1	0	1	1	0	1	–19
1	1	1	0	1	1	0	0	–20
1	1	1	0	1	0	1	1	–21
1	1	1	0	1	0	1	0	–22
1	1	1	0	1	0	0	1	–23
1	1	1	0	1	0	0	0	–24
1	1	1	0	0	1	1	1	–25
1	1	1	0	0	1	1	0	–26
1	1	1	0	0	1	0	1	–27
1	1	1	0	0	1	0	0	–28
1	1	1	0	0	0	1	1	–29
1	1	1	0	0	0	1	0	–30
1	1	1	0	0	0	0	1	–31
1	1	1	0	0	0	0	0	–32
1	1	0	1	1	1	1	1	–33
1	1	0	1	1	1	1	0	–34
1	1	0	1	1	1	0	1	–35
1	1	0	1	1	1	0	0	–36
1	1	0	1	1	0	1	1	–37
1	1	0	1	1	0	1	0	–38
1	1	0	1	1	0	0	1	–39
1	1	0	1	1	0	0	0	–40
1	1	0	1	0	1	1	1	–41
1	1	0	1	0	1	1	0	–42
1	1	0	1	0	1	0	1	–43
1	1	0	1	0	1	0	0	–44
1	1	0	1	0	0	1	1	–45
1	1	0	1	0	0	1	0	–46
1	1	0	1	0	0	0	1	–47
1	1	0	1	0	0	0	0	–48
1	1	0	0	1	1	1	1	–49
1	1	0	0	1	1	1	0	–50
1	1	0	0	1	1	0	1	–51

MSB							LSB	VOLUME SETTING (dB)
B7	B6	B5	B4	B3	B2	B1	B0	
1	1	0	0	1	1	0	0	–52
1	1	0	0	1	0	1	1	–53
1	1	0	0	1	0	1	0	–54
1	1	0	0	1	0	0	1	–55
1	1	0	0	1	0	0	0	–56
1	1	0	0	0	1	1	1	–57
1	1	0	0	0	1	1	0	–58
1	1	0	0	0	1	0	1	–59
1	1	0	0	0	1	0	0	–60
1	1	0	0	0	0	1	1	–61
1	1	0	0	0	0	1	0	–62
1	1	0	0	0	0	0	1	–63
1	1	0	0	0	0	0	0	–64
1	0	1	1	1	1	1	1	–65
1	0	1	1	1	1	1	0	–66
1	0	1	1	1	1	0	1	–67
1	0	1	1	1	1	0	0	–68
1	0	1	1	1	0	1	1	–69
1	0	1	1	1	0	1	0	–70
1	0	1	1	1	0	0	1	–71
1	0	1	1	1	0	0	0	–72
1	0	1	1	0	1	1	1	–73
1	0	1	1	0	1	1	0	–74
1	0	1	1	0	1	0	1	–75
1	0	1	1	0	1	0	0	–76
1	0	1	1	0	0	1	1	–77
1	0	1	1	0	0	1	0	–78
1	0	1	1	0	0	0	1	–79
1	0	1	1	0	0	0	0	–80
1	0	1	0	1	1	1	1	–81
1	0	1	0	1	1	1	0	–82
1	0	1	0	1	1	0	1	–83
1	0	1	0	1	1	0	0	mute (note 1)

Note

1. The default setting at power-up is 10101100.

10.3.29 BASS CONTROL REGISTER (AUXILIARY)

This register is used to apply bass control to the left and right signal channels of the Auxiliary channel.

Table 62 Subaddress 34

MSB							LSB	BASS SETTING (dB)
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
0	0	0	0	1	1	1	1	+15
0	0	0	0	1	1	1	0	+14
0	0	0	0	1	1	0	1	+13
0	0	0	0	1	1	0	0	+12
0	0	0	0	1	0	1	1	+11
0	0	0	0	1	0	1	0	+10
0	0	0	0	1	0	0	1	+9
0	0	0	0	1	0	0	0	+8
0	0	0	0	0	1	1	1	+7
0	0	0	0	0	1	1	0	+6
0	0	0	0	0	1	0	1	+5
0	0	0	0	0	1	0	0	+4
0	0	0	0	0	0	1	1	+3
0	0	0	0	0	0	1	0	+2
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0 (note 1)
0	0	0	1	1	1	1	1	–1
0	0	0	1	1	1	1	0	–2
0	0	0	1	1	1	0	1	–3
0	0	0	1	1	1	0	0	–4
0	0	0	1	1	0	1	1	–5
0	0	0	1	1	0	1	0	–6
0	0	0	1	1	0	0	1	–7
0	0	0	1	1	0	0	0	–8
0	0	0	1	0	1	1	1	–9
0	0	0	1	0	1	1	0	–10
0	0	0	1	0	1	0	1	–11
0	0	0	1	0	1	0	0	–12

Note

1. The default setting at power-up is 00000000.

10.3.30 TREBLE CONTROL REGISTER (AUXILIARY)

This register is used to apply treble control to the left and right signal channels of the Auxiliary channel.

Table 63 Subaddress 35

MSB							LSB	TREBLE SETTING (dB)
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
X	X	X	0	1	1	0	0	+12
X	X	X	0	1	0	1	1	+11
X	X	X	0	1	0	1	0	+10
X	X	X	0	1	0	0	1	+9
X	X	X	0	1	0	0	0	+8
X	X	X	0	0	1	1	1	+7
X	X	X	0	0	1	1	0	+6
X	X	X	0	0	1	0	1	+5
X	X	X	0	0	1	0	0	+4
X	X	X	0	0	0	1	1	+3
X	X	X	0	0	0	1	0	+2
X	X	X	0	0	0	0	1	+1
X	X	X	0	0	0	0	0	0 (note 1)
X	X	X	1	1	1	1	1	–1
X	X	X	1	1	1	1	0	–2
X	X	X	1	1	1	0	1	–3
X	X	X	1	1	1	0	0	–4
X	X	X	1	1	0	1	1	–5
X	X	X	1	1	0	1	0	–6
X	X	X	1	1	0	0	1	–7
X	X	X	1	1	0	0	0	–8
X	X	X	1	0	1	1	1	–9
X	X	X	1	0	1	1	0	–10
X	X	X	1	0	1	0	1	–11
X	X	X	1	0	1	0	0	–12

Note

1. The default setting at power-up is 00000000.

10.3.31 Feature interface configuration register

Table 64 Subaddress 36 (note 1)

BIT	NAME	VALUE	DESCRIPTION
7 (MSB)	B7	0	default value
6	B6	0	default value
5	B5	0	default value
4	SYSCL1	–	system clock frequency selection (see Table 65)
3	SYSCL0		
2	SYSOUT	1	enables the output of a system (or master) clock signal at pin SYSCLK
		0	the output will be off, thereby improving the EMC performance
1	I^2SFORM	1	an MSB-aligned (MSB-first) serial output format is selected, i.e. a level change at pin WS indicates the beginning of a new audio sample
		0	the standard I^2S-bus output format is selected
0 (LSB)	I^2SOUT	1	enables the I^2S-bus outputs (both serial data outputs plus serial bit clock and word select) in a format determined by bit I^2SFORM; the TDA9870A is then an I^2S-bus master
		0	the outputs mentioned will be 3-stated, thereby improving the EMC performance

Note

1. The default setting at power-up is 00000000.

Table 65 System clock frequency selection

B4	B3	SYSCLK OUTPUT	FREQUENCY (MHz)
0	0	$256f_s$	8.192
0	1	$384f_s$	12.288
1	0	$512f_s$	16.384[1]
1	1	$768f_s$	24.576

Note

1. With 16.384 MHz the duty cycle is 33%.

10.3.32 I^2S1 OUTPUT SELECT REGISTER

This register is used to define both the signal source to be output at I^2S1 and the mode of the digital matrix for signal selection.

Table 66 Subaddress 37 (note 1)

BIT	NAME	VALUE	DESCRIPTION
7 (MSB)	B7	0	default value
6	B6	–	output selection (see Table 67)
5	B5		
4	B4		
3	B3	0	default value
2	B2	–	signal source selection (see Table 68)
1	B1		
0 (LSB)	B0		

Note

1. The default setting at power-up is 00000000.

Table 67 Output selection

B6	B5	B4	L OUTPUT	R OUTPUT
0	0	0	L input	R input
0	0	1	L input	L input
0	1	0	R input	R input
0	1	1	R input	L input
1	0	0	$\frac{L+R}{2}$	$\frac{L+R}{2}$

Table 68 Signal source selection (note 1)

B2	B1	B0	SIGNAL SOURCE
0	0	0	FM output
0	0	1	don’t care
0	1	0	I^2S1 input
0	1	1	I^2S2 input
1	0	0	ADC output
1	0	1	AVL output
1	1	0	Auxiliary output
1	1	1	Main output

Note

1. The Main and Auxiliary channel outputs will not contain the beeper signal.

10.3.33 I²S1 INPUT LEVEL ADJUST REGISTER

This register is used to adjust the input level at the I²S1 interface. Left and right signal channel are treated identically.

Table 69 Subaddress 38

MSB							LSB	GAIN SETTING (dB)
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
0	0	0	0	1	1	1	1	+15
0	0	0	0	1	1	1	0	+14
0	0	0	0	1	1	0	1	+13
0	0	0	0	1	1	0	0	+12
0	0	0	0	1	0	1	1	+11
0	0	0	0	1	0	1	0	+10
0	0	0	0	1	0	0	1	+9
0	0	0	0	1	0	0	0	+8
0	0	0	0	0	1	1	1	+7
0	0	0	0	0	1	1	0	+6
0	0	0	0	0	1	0	1	+5
0	0	0	0	0	1	0	0	+4
0	0	0	0	0	0	1	1	+3
0	0	0	0	0	0	1	0	+2
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0 (note 1)
0	0	0	1	1	1	1	1	–1
0	0	0	1	1	1	1	0	–2
0	0	0	1	1	1	0	1	–3
0	0	0	1	1	1	0	0	–4
0	0	0	1	1	0	1	1	–5
0	0	0	1	1	0	1	0	–6
0	0	0	1	1	0	0	1	–7
0	0	0	1	1	0	0	0	–8
0	0	0	1	0	1	1	1	–9
0	0	0	1	0	1	1	0	–10
0	0	0	1	0	1	0	1	–11
0	0	0	1	0	1	0	0	–12
0	0	0	1	0	0	1	1	–13
0	0	0	1	0	0	1	0	–14
0	0	0	1	0	0	0	1	–15
0	0	0	1	0	0	0	0	mute

Note

1. The default setting at power-up is 00000000.

10.3.34 I^2S1 OUTPUT LEVEL ADJUST REGISTER

This register is used to adjust the output level at the I^2S1 interface. Left and right signal channel are treated identically.

Table 70 Subaddress 39

MSB							LSB	GAIN SETTING (dB)
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
0	0	0	0	1	1	1	1	+15
0	0	0	0	1	1	1	0	+14
0	0	0	0	1	1	0	1	+13
0	0	0	0	1	1	0	0	+12
0	0	0	0	1	0	1	1	+11
0	0	0	0	1	0	1	0	+10
0	0	0	0	1	0	0	1	+9
0	0	0	0	1	0	0	0	+8
0	0	0	0	0	1	1	1	+7
0	0	0	0	0	1	1	0	+6
0	0	0	0	0	1	0	1	+5
0	0	0	0	0	1	0	0	+4
0	0	0	0	0	0	1	1	+3
0	0	0	0	0	0	1	0	+2
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0 (note 1)
0	0	0	1	1	1	1	1	–1
0	0	0	1	1	1	1	0	–2
0	0	0	1	1	1	0	1	–3
0	0	0	1	1	1	0	0	–4
0	0	0	1	1	0	1	1	–5
0	0	0	1	1	0	1	0	–6
0	0	0	1	1	0	0	1	–7
0	0	0	1	1	0	0	0	–8
0	0	0	1	0	1	1	1	–9
0	0	0	1	0	1	1	0	–10
0	0	0	1	0	1	0	1	–11
0	0	0	1	0	1	0	0	–12
0	0	0	1	0	0	1	1	–13
0	0	0	1	0	0	1	0	–14
0	0	0	1	0	0	0	1	–15
0	0	0	1	0	0	0	0	mute

Note

1. The default setting at power-up is 00000000.

10.3.35 I^2S2 OUTPUT SELECT REGISTER

This register is used to define both the signal source to be output at I^2S2 and the mode of the digital matrix for signal selection.

Table 71 Subaddress 40 (note 1)

BIT	NAME	VALUE	DESCRIPTION
7 (MSB)	B7	0	default value
6	B6	–	output selection (see Table 72)
5	B5		
4	B4		
3	B3	0	default value
2	B2	–	signal source selection (see Table 73)
1	B1		
0 (LSB)	B0		

Note

1. The default setting at power-up is 00000000.

Table 72 Output selection

B6	B5	B4	L OUTPUT	R OUTPUT
0	0	0	L input	R input
0	0	1	L input	L input
0	1	0	R input	R input
0	1	1	R input	L input
1	0	0	$\frac{L+R}{2}$	$\frac{L+R}{2}$

Table 73 Signal source selection (note 1)

B2	B1	B0	SIGNAL SOURCE
0	0	0	FM output
0	0	1	don’t care
0	1	0	I^2S1 input
0	1	1	I^2S2 input
1	0	0	ADC output
1	0	1	AVL output
1	1	0	Auxiliary output
1	1	1	Main output

Note

1. The Main and Auxiliary channel outputs will not contain the beeper signal.

10.3.36 I²S2 INPUT LEVEL ADJUST REGISTER

This register is used to adjust the input level at the I²S2 interface. Left and right signal channel are treated identically.

Table 74 Subaddress 41

MSB							LSB	GAIN SETTING (dB)
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
0	0	0	0	1	1	1	1	+15
0	0	0	0	1	1	1	0	+14
0	0	0	0	1	1	0	1	+13
0	0	0	0	1	1	0	0	+12
0	0	0	0	1	0	1	1	+11
0	0	0	0	1	0	1	0	+10
0	0	0	0	1	0	0	1	+9
0	0	0	0	1	0	0	0	+8
0	0	0	0	0	1	1	1	+7
0	0	0	0	0	1	1	0	+6
0	0	0	0	0	1	0	1	+5
0	0	0	0	0	1	0	0	+4
0	0	0	0	0	0	1	1	+3
0	0	0	0	0	0	1	0	+2
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0 (note 1)
0	0	0	1	1	1	1	1	−1
0	0	0	1	1	1	1	0	−2
0	0	0	1	1	1	0	1	−3
0	0	0	1	1	1	0	0	−4
0	0	0	1	1	0	1	1	−5
0	0	0	1	1	0	1	0	−6
0	0	0	1	1	0	0	1	−7
0	0	0	1	1	0	0	0	−8
0	0	0	1	0	1	1	1	−9
0	0	0	1	0	1	1	0	−10
0	0	0	1	0	1	0	1	−11
0	0	0	1	0	1	0	0	−12
0	0	0	1	0	0	1	1	−13
0	0	0	1	0	0	1	0	−14
0	0	0	1	0	0	0	1	−15
0	0	0	1	0	0	0	0	mute

Note

1. The default setting at power-up is 00000000.

10.3.37 I²S2 OUTPUT LEVEL ADJUST REGISTER

This register is used to adjust the output level at the I²S2 interface. Left and right signal channel are treated identically.

Table 75 Subaddress 42

MSB							LSB	GAIN SETTING (dB)
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
0	0	0	0	1	1	1	1	+15
0	0	0	0	1	1	1	0	+14
0	0	0	0	1	1	0	1	+13
0	0	0	0	1	1	0	0	+12
0	0	0	0	1	0	1	1	+11
0	0	0	0	1	0	1	0	+10
0	0	0	0	1	0	0	1	+9
0	0	0	0	1	0	0	0	+8
0	0	0	0	0	1	1	1	+7
0	0	0	0	0	1	1	0	+6
0	0	0	0	0	1	0	1	+5
0	0	0	0	0	1	0	0	+4
0	0	0	0	0	0	1	1	+3
0	0	0	0	0	0	1	0	+2
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0 (note 1)
0	0	0	1	1	1	1	1	–1
0	0	0	1	1	1	1	0	–2
0	0	0	1	1	1	0	1	–3
0	0	0	1	1	1	0	0	–4
0	0	0	1	1	0	1	1	–5
0	0	0	1	1	0	1	0	–6
0	0	0	1	1	0	0	1	–7
0	0	0	1	1	0	0	0	–8
0	0	0	1	0	1	1	1	–9
0	0	0	1	0	1	1	0	–10
0	0	0	1	0	1	0	1	–11
0	0	0	1	0	1	0	0	–12
0	0	0	1	0	0	1	1	–13
0	0	0	1	0	0	1	0	–14
0	0	0	1	0	0	0	1	–15
0	0	0	1	0	0	0	0	mute

Note

1. The default setting at power-up is 00000000.

10.3.38 BEEPER FREQUENCY CONTROL REGISTER

This register is used to select from sample beeper oscillator frequencies. The beeper output signal is added to the Main and Auxiliary channel output DAC.

Due to the frequency response of the audio DACs upsampling filters, the 25 kHz beep is approximately 5 dB louder than the 390 Hz beep.

Table 76 Subaddress 43 (note 1)

MSB							LSB	GENERATED FREQUENCY (Hz)
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
0	0	0	0	0	1	1	1	25000
0	0	0	0	0	1	1	0	7040
0	0	0	0	0	1	0	1	3580
0	0	0	0	0	1	0	0	1770
0	0	0	0	0	0	1	1	1270
0	0	0	0	0	0	1	0	900
0	0	0	0	0	0	0	1	640
0	0	0	0	0	0	0	0	390

Note

1. The default setting at power-up is 00000000.

10.3.39 BEEPER VOLUME CONTROL REGISTER

This register is used to set the beeper volume. The gain setting is relative to digital full-scale at the input to the Main and Auxiliary channel output DACs. The beeper volume is independent of any other volume setting.

The beeper signal is added to the Main and Auxiliary channel output signals in the $2 \times f_s$ domain. The beeper volume should be set with great care, when the audio signals in the Main and Auxiliary channels are close to digital full-scale, to avoid output signal distortion due to overload.

Table 77 Subaddress 44

MSB							LSB	GAIN SETTING (dB)
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
0	0	0	0	0	0	0	0	0
0	0	1	1	1	1	1	1	–3
0	0	1	1	1	1	1	0	–6
0	0	1	1	1	1	0	1	–9
0	0	1	1	1	1	0	0	–12
0	0	1	1	1	0	1	1	–15
0	0	1	1	1	0	1	0	–18
0	0	1	1	1	0	0	1	–21
0	0	1	1	1	0	0	0	–24
0	0	1	1	0	1	1	1	–27
0	0	1	1	0	1	1	0	–30
0	0	1	1	0	1	0	1	–33
0	0	1	1	0	1	0	0	–36
0	0	1	1	0	0	1	1	–39
0	0	1	1	0	0	1	0	–42
0	0	1	1	0	0	0	1	–45
0	0	1	1	0	0	0	0	–48
0	0	1	0	1	1	1	1	–51
0	0	1	0	1	1	1	0	–54
0	0	1	0	1	1	0	1	–57
0	0	1	0	1	1	0	0	–60
0	0	1	0	1	0	1	1	–63
0	0	1	0	1	0	1	0	–66
0	0	1	0	1	0	0	1	–69
0	0	1	0	1	0	0	0	–72
0	0	1	0	0	1	1	1	–75
0	0	1	0	0	1	1	0	–78
0	0	1	0	0	1	0	1	–81
0	0	1	0	0	1	0	0	–84
0	0	1	0	0	0	1	1	–87
0	0	1	0	0	0	1	0	–90
0	0	1	0	0	0	0	1	–93
0	0	1	0	0	0	0	0	mute (note 1)

Note

1. The default setting at power-up is 00100000.

10.3.40 BASS BOOST CONTROL REGISTER

This register is used to select from a few sample bass boost settings to modify the frequency characteristics of the Main channel (shelving filter). Bits B3 to B0 apply to the left channel, bits B7 to B4 apply to the right channel. This function must be used with care in order to avoid clipping distortion at high volume settings.

More sophisticated control of the bass boost filter can be exercised in the expert mode (see Section 10.5). The user then has full control over this second-order filter and can, within limits, realize bass equalizers with arbitrary centre frequencies, Q factors and boost/cut settings.

Table 78 Subaddress 45 (note 1)

BIT	NAME	VALUE	DESCRIPTION
7 (MSB)	B7	–	gain setting of right channel (see Table 79)
6	B6		
5	B5		
4	B4		
3	B3	–	gain setting of left channel (see Table 80)
2	B2		
1	B1		
0 (LSB)	B0		

Note

1. The default setting at power-up is 00000000.

Table 79 Gain setting of right channel

B7	B6	B5	B4	GAIN SETTING (dB)	CORNER FREQUENCY (Hz)
1	0	1	0	20	350
1	0	0	1	18	350
1	0	0	0	16	350
0	1	1	1	14	350
0	1	1	0	12	350
0	1	0	1	10	350
0	1	0	0	8	350
0	0	1	1	6	350
0	0	1	0	4	350
0	0	0	1	2	350
0	0	0	0	0	350

Table 80 Gain setting of left channel

B3	B2	B1	B0	GAIN SETTING (dB)	CORNER FREQUENCY (Hz)
1	0	1	0	20	350
1	0	0	1	18	350
1	0	0	0	16	350
0	1	1	1	14	350
0	1	1	0	12	350
0	1	0	1	10	350
0	1	0	0	8	350
0	0	1	1	6	350
0	0	1	0	4	350
0	0	0	1	2	350
0	0	0	0	0	350

10.4 Slave transmitter mode

As a slave transmitter, the TDA9870A provides 13 registers with status information and data, a part of which is for Philips internal purposes only. These registers can be accessed by means of subaddresses.

Table 81 General format for reading data from the TDA9870A

S	SLAVE ADDRESS	0	ACK	SUBADDRESS	ACK	Sr	SLAVE ADDRESS	1	ACK	DATA	NAm	P

Table 82 Explanation of Tables 81 and 83

BIT	FUNCTION
S	START condition
SLAVE ADDRESS	7-bit device address
0	data direction bit (write to device)
ACK	acknowledge (by the slave)
SUBADDRESS	address of register to read from
Sr	repeated START condition
1	data direction bit (read from device)
DATA	data byte read from register
NAm	not acknowledge (by the master)
Am	acknowledge (by the master)
P	STOP condition

Reading of data can start at any valid subaddress. It is allowed to read more than 1 data byte per transmission from the TDA9870A. In this situation, the subaddress is automatically incremented after each data byte, which results in reading the sequence of data bytes from successive register locations, starting at SUBADDRESS.

Table 83 Format of a transmission using automatic incrementing of subaddresses

S	SLAVE ADDRESS	0	ACK	SUBADDRESS	ACK	Sr	SLAVE ADDRESS	1	ACK	DATA BYTE Am[1]	DATA	NAm	P

Note

1. n data bytes with auto-increment of subaddresses.

Each data byte in a read sequence, except for the last one, is acknowledged with Am (acknowledge by the master). The subaddresses ‘wrap around’ from decimal 255 to 0. If an attempt is made to read from a non-existing subaddress, the device will send a data pattern of all ones, i.e. FF in hexadecimal notation.

Table 84 Overview of the slave transmitter registers; note 1

SUBADDRESS (DECIMAL)	DATA								FUNCTION
	MSB							LSB	
0	s	s	X	X	X	s	s	s	device status (power-on, identification, etc.)
1	X	X	X	X	X	X	X	X	don't care; note 1
2	X	X	X	X	X	X	X	X	don't care; note 1
3	X	X	X	X	X	X	X	X	don't care; note 1
4	X	X	X	X	X	X	X	X	don't care; note 1
5	l	l	l	l	l	l	l	l	level read-out (MSB)
6	l	l	l	l	l	l	l	l	level read-out (LSB)
7	X	X	X	c	c	c	c	c	SIF level
251	a	a	a	a	a	a	a	a	test register 3; note 2
252	a	a	a	a	a	a	a	a	test register 2; note 2
253	a	a	a	a	a	a	a	a	test register 1; note 2
254	d	d	d	d	d	d	d	d	device identification code
255	s	s	s	s	s	s	s	s	software identification code

Notes

1. X indicates a bit that has not been assigned to a function. This bit is reserved for future extensions.
2. Registers from subaddress 251 to 255 are for Philips internal purposes only. They are considered as a set of registers for the identification of individual members and some key parameters in a family of devices.

The following sub-sections provide a detailed description of the slave transmitter registers.

10.4.1 DEVICE STATUS REGISTER

Table 85 Subaddress 0

BIT	NAME	VALUE	DESCRIPTION
7 (MSB)	P2IN	–	This bit reflects the status of the corresponding general purpose port of pin P2 (see Section 10.3.2).
6	P1IN	–	This bit reflects the status of the corresponding general purpose port of pin P1 (see Section 10.3.2).
5	B5	–	don't care
4	B4	–	don't care
3	B3	–	don't care
2	IDDUA	–	This bit is logic 1 if an FM dual-language signal has been identified. When neither IDSTE nor IDDUA are set, the received signal has to be assumed to be FM mono.
1	IDSTE	–	This bit is logic 1 if an FM stereo signal has been identified.
0 (LSB)	POR	–	Power fail bit: the power supply for the digital part of the device, V_{DDD2}, has temporarily been lower than the specified lower limit. If this is detected an initialization of the TDA9870A has to be carried out to ensure a reliable operation.

10.4.2 REGISTER 1

Subaddress 1: These bits have not been assigned to a function. These bits are reserved for future extensions.

10.4.3 REGISTER 2

Subaddress 2: These bits have not been assigned to a function. These bits are reserved for future extensions.

10.4.4 REGISTER 3

Subaddress 3: These bits have not been assigned to a function. These bits are reserved for future extensions.

10.4.5 REGISTER 4

Subaddress 4: These bits have not been assigned to a function. These bits are reserved for future extensions.

10.4.6 LEVEL READ-OUT REGISTERS

These two bytes constitute a word that provides data from a location that has been specified with the monitor select register. The most significant byte of the data is stored at subaddress 5.

If peak-level monitoring has been selected, the peak-level monitoring register is cleared and monitoring resumes after its contents has been transferred to these two bytes.

Table 86 Subaddresses 5 and 6

SUB-ADDRESS	BIT	DESCRIPTION
5	7 (MSB)	most significant bit or sign bit
	6	
	5	
	4	
	3	
	2	
	1	
	0 (LSB)	
6	7 (MSB)	
	6	
	5	
	4	
	3	
	2	
	1	
	0 (LSB)	least significant bit

10.4.7 SIF LEVEL REGISTER

When the SIF AGC is on, bits B4 to B0 of this register contain a number that gives an indication of the SIF input level. That number corresponds to the AGC gain register setting (see Section 10.3.1).

When the SIF AGC is off, this register returns the contents of the AGC gain register.

Table 87 Subaddress 7

BIT	NAME	VALUE	DESCRIPTION
7 (MSB)	B7	X	bit not assigned
6	B6	X	bit not assigned
5	B5	X	bit not assigned
4	B4	–	indication of SIF input level
3	B3		
2	B2		
1	B1		
0 (LSB)	B0		

10.4.8 TEST REGISTER 3

This register contains, as a binary number, the highest memory address used for the Coefficient RAM (CRAM, expert mode).

Table 88 Subaddress 251

MSB							LSB
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
0	1	1	1	1	1	1	1

10.4.9 TEST REGISTER 2

This register contains, as a binary number, the highest subaddress used for slave receiver registers.

Table 89 Subaddress 252

MSB							LSB
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
0	0	1	0	1	1	0	1

10.4.10 TEST REGISTER 1

This register contains, as a binary number, the highest subaddress used for slave transmitter (status) registers.

Table 90 Subaddress 253

MSB							LSB
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
0	0	0	0	0	1	1	1

10.4.11 DEVICE IDENTIFICATION CODE

There will be several devices in the digital TV sound processor family. This byte is used to identify the individual family members.

Table 91 Subaddress 254

MSB							LSB
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
0	0	1	0	0	0	1	0

10.4.12 SOFTWARE IDENTIFICATION CODE

It is likely that during the life time of this family of devices several versions of the DSP software will be made, e.g., to accommodate new application concepts, respond to customer wishes, etc. This byte is used to identify the different releases.

Table 92 Subaddress 255

MSB							LSB
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
0	0	0	0	0	0	1	0

10.5 Expert mode

In addition to the slave receiver and slave transmitter modes previously described, there is a special ‘expert’ mode that gives direct write access to the internal CRAM of the DSP.

In this mode, transferred data contains 12-bit coefficients. As these coefficients bypass on-chip coefficient look-up tables for many functions, they directly influence the processing of signals within the DSP.

This mode must be used with great care. It can be used to create user-defined characteristics, such as a tone control with different corner frequencies or special boost/cut characteristics to correct the low-frequency loudspeaker and/or cabinet frequency responses.

As the coefficients do not fit into one data byte, they have to be split and arranged (see Table 95). The most significant bit is transferred first.

The general format described in Table 95 shows the minimum number of data bytes required, i.e. two bytes for the transfer of a single coefficient.

Should more than one coefficient be sent, then the CRAM address will be automatically incremented after each coefficient, resulting in writing the sequence of coefficients into successive memory locations, starting at CRAM ADDRESS. A transmission can start with any valid CRAM address. If two coefficients are to be transferred, they are arranged as shown in Table 96.

With any odd number of coefficients to be transferred, the least significant nibble of the last byte is regarded as containing don’t care data.

As the transfer of coefficients cannot be accomplished within one audio sample period, it is necessary that received coefficients be buffered and made active all at the same time to avoid audio signal transients. The receive buffer is designed to store up to 8 coefficients in addition to the CRAM address. Each byte that fits into the buffer is acknowledged with ACK (acknowledge). If an attempt is made to write more coefficients than the buffer can store, the device acknowledges with NACK (not acknowledge) and any further coefficients are ignored. Coefficients that are already in the receive buffer remain intact.

An expert mode transfer ends when the I^2C-bus STOP condition or a repeated START condition has been detected. Only those coefficients that have been received during the last transmission will then be copied from the buffer to the CRAM.

To make efficient and correct use of the expert mode, it is recommended to transfer all coefficients for any one function in a single transmission.

There is no checking of memory addresses and the automatic incrementing of addresses does not stop at the highest used CRAM address. The user of this expert mode must be fully acquainted with the relevant procedures.

More information concerning the functions of this device, such as the number of coefficients per function, their default values, memory addresses, etc., can be supplied on request at a later date.

Table 93 General format for entering the expert mode and writing coefficients into the TDA9870A

S	SLAVE ADDRESS	0	ACK	10000000	ACK	CRAM ADDRESS	ACK	DATA	ACK	DATA	ACK	P

Table 94 Explanation of Table 93

BIT	FUNCTION
S	START condition
SLAVE ADDRESS	7-bit device address
0	data direction bit (write to device)
ACK	acknowledge
10000000	pattern to enter the expert mode
CRAM ADDRESS	start address of coefficient RAM to write to
DATA	data byte containing part of a coefficient
P	STOP condition

Table 95 General format (notes 1, 2 and 3)

BYTE	DATA								DESCRIPTION
1 data byte	a	a	a	a	a	a	a	a	2 MST of 1st coefficient
2 data byte	a	a	a	a	X	X	X	X	1 LST of 1st coefficient

Notes

1. X = don’t care.
2. MST = most significant third.
3. LST = least significant third.

Table 96 Transfer of two coefficients

BYTE	DATA								DESCRIPTION
1 data byte	a	a	a	a	a	a	a	a	2 MST of 1st coefficient
2 data byte	a	a	a	a	b	b	b	b	1 LST of 1st coefficient + 1 MST of 2nd coefficient
3 data byte	b	b	b	b	b	b	b	b	2 LST of 2nd coefficient

11 I²S-BUS DESCRIPTION

The feature interface of the TDA9870A contains two serial audio inputs and outputs and associated clock signals. It can be used to supply, for example, audio signals from received TV programs to a digital audio output device (AES/EBU format), or import serial audio signals from other sources for reproduction through the TV set's loudspeaker and/or headphone channels. Apart from such simple data input or output, it is also possible to run audio signals through an external DSP, which performs some additional functions, such as room simulation, Dolby Surround Pro Logic etc. and feed those signals back into the loudspeaker and/or headphone channels of the TDA9870A.

Two serial audio formats are supported at the feature interface, i.e. the I²S-bus format and a very similar MSB-aligned format. The difference is illustrated in Fig.9.

In both formats the left audio channel of a stereo sample pair is output first and is placed on the serial data line (SDI for input, SDO for output) when the Word Select line (WS) is LOW. Data is written at the trailing edge of SCK and read at the leading edge of SCK. The most significant bit is sent first.

At power-up, the outputs of the feature interface are 3-stated to reduce EMC and allow for combinations with other ICs. If output is desired, it has to be activated by means of an I²C-bus command.

When the output is enabled, the serial audio data can be taken from pins SDO1 and SDO2. Depending on the signal source, switch and matrix positions, the output can be either mono, stereo or dual language sound on either output.

The word select output is clocked with the audio sample frequency at 32 kHz. The serial clock output (SCK) is clocked at a frequency of 2.048 MHz. This means, that there are 64 clock pulses per pair of stereo output samples, or 32 clock pulses per sample. Depending again on the signal source, the number of significant bits on the serial data outputs, SDO1 and SDO2, is between 14 and 18.

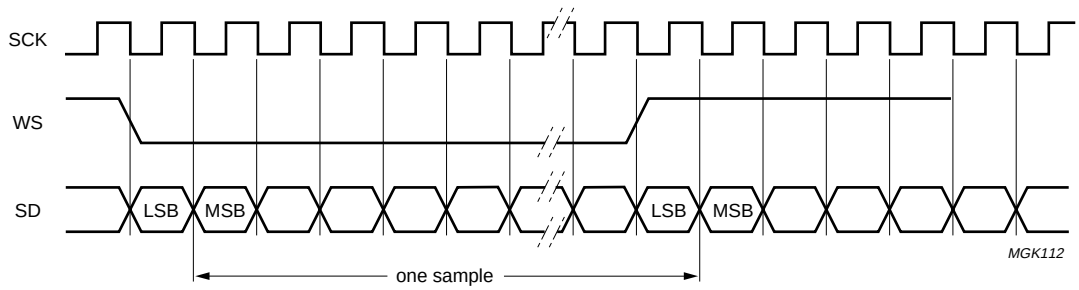
Apart from just feeding a digital audio device, such as a DAC or an AES/EBU transmitter, the serial data outputs can be connected directly to the serial inputs (loop-back connection) or first to an external device, e.g. a feature DSP such as the SAA7710 and then back to the serial inputs. In all of these configurations, the SCK and WS clocks will be generated by the TDA9870A, which then is the I²S-bus master.

The serial data inputs, SDI1 and SDI2, are active at all times, independent of the serial data outputs being on or off. When the serial data outputs are off (either after power-up or via the appropriate I²C-bus command) serial data and clocks WS and SCK from a separate digital audio source can be fed into the TDA9870A, be processed and output in accordance with internal selector positions, provided that the following criteria are met:

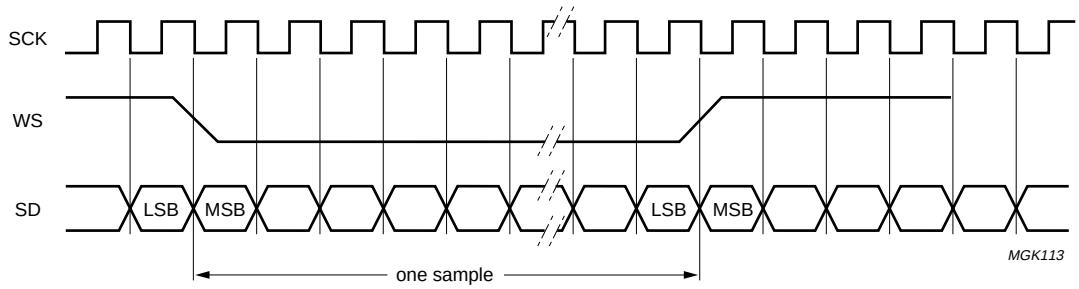
- 32 kHz audio sample frequency
- 32 clock bits per sample
- External timing and data synchronized to TDA9870A.

In such cases, the external source is the I²S-bus master and the TDA9870A is the I²S-bus slave.

To support synchronization of external devices or as a master clock for them, a system clock output, SYSCLK, is available from the TDA9870A. At power-up it is off. It can be enabled and the output frequency set via an I²C-bus command. Available output frequencies are 8.192, 12.288, 16.384 and 24.576 MHz.



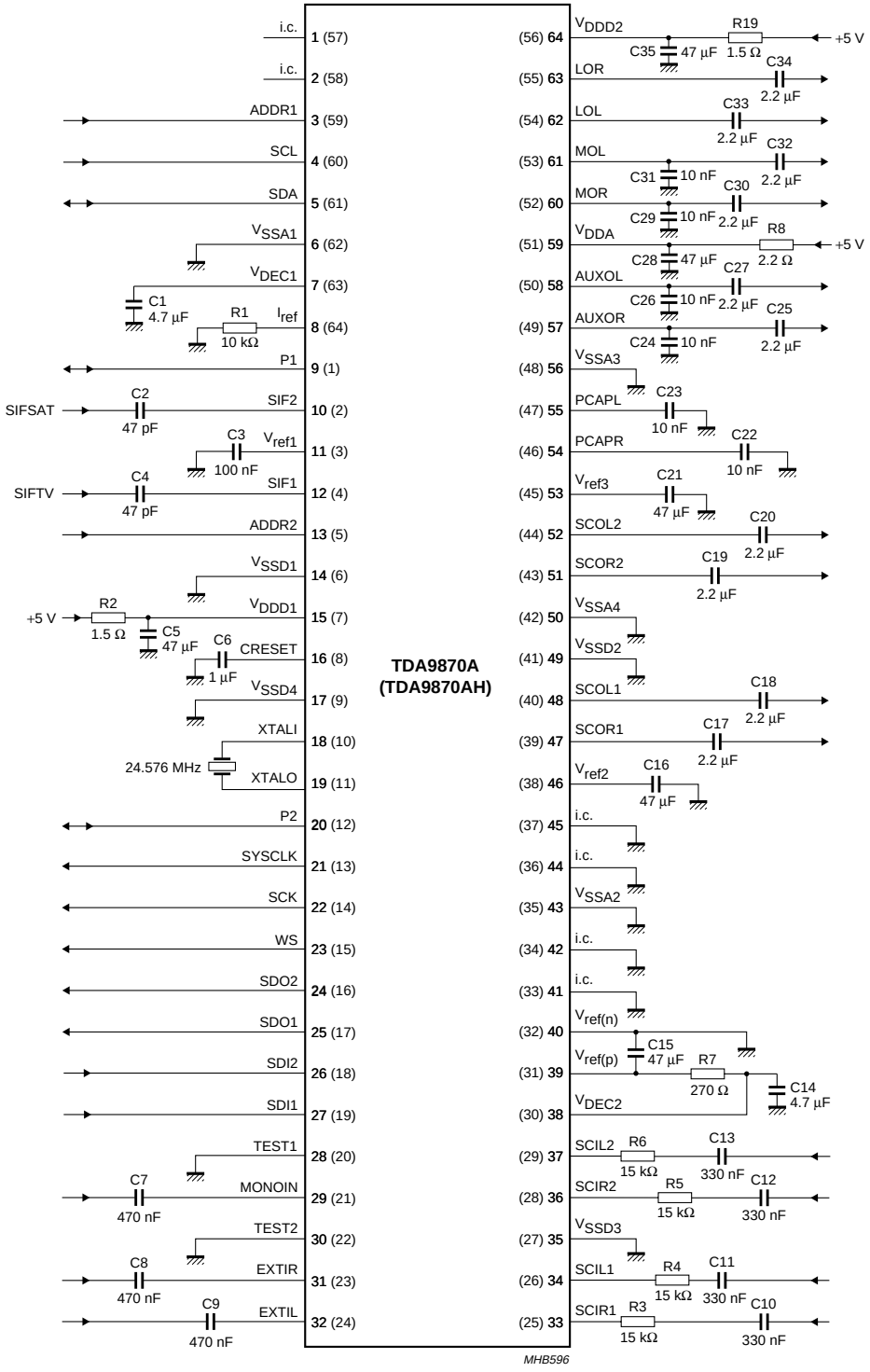
a. I^2S-bus format.



b. MSB-aligned format.

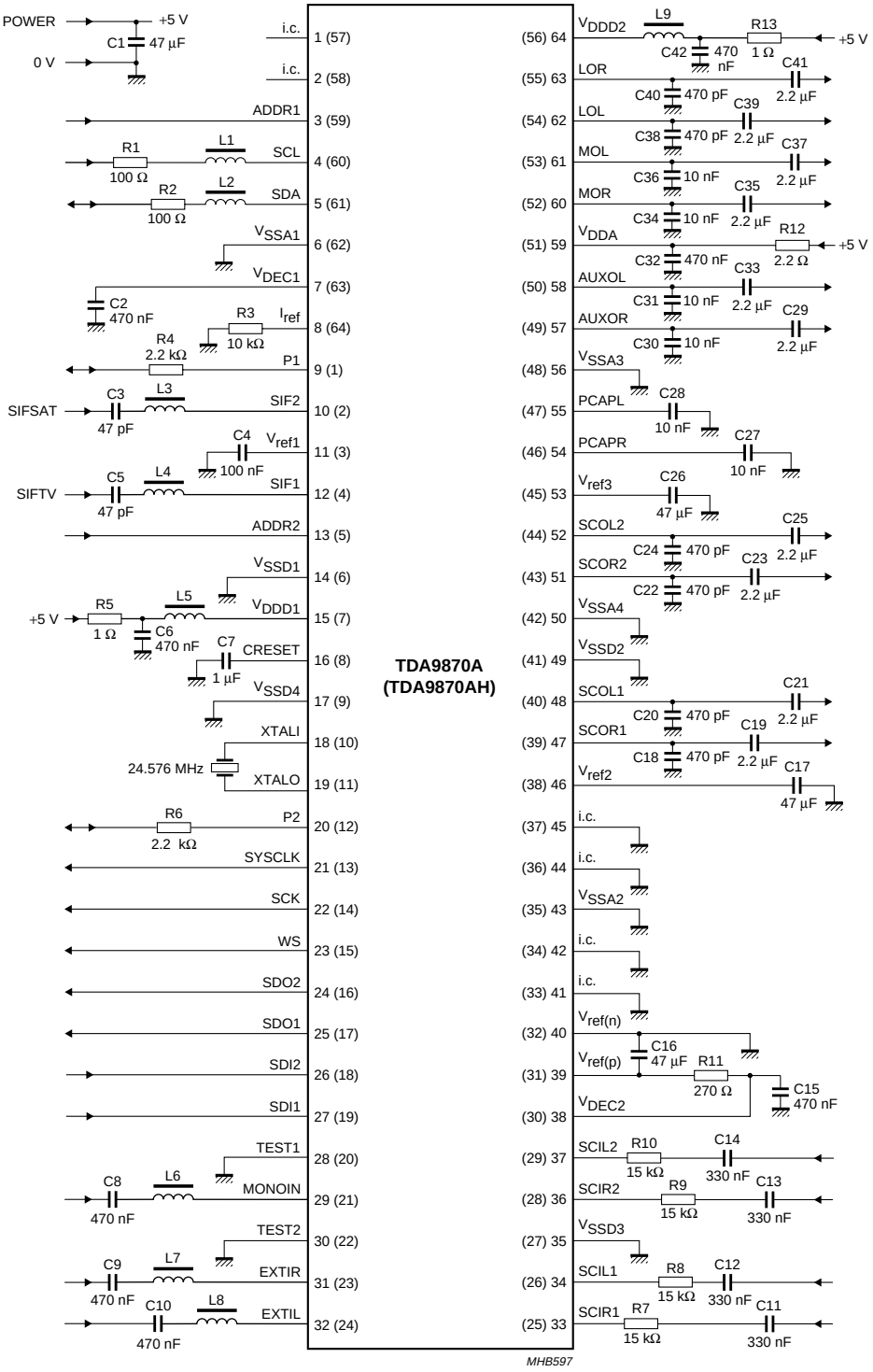
Fig.9 Serial audio interface formats.

12 APPLICATION INFORMATION



The pin numbers given in parenthesis refer to the TDA9870AH version.

Fig.10 Schematic for measurements.



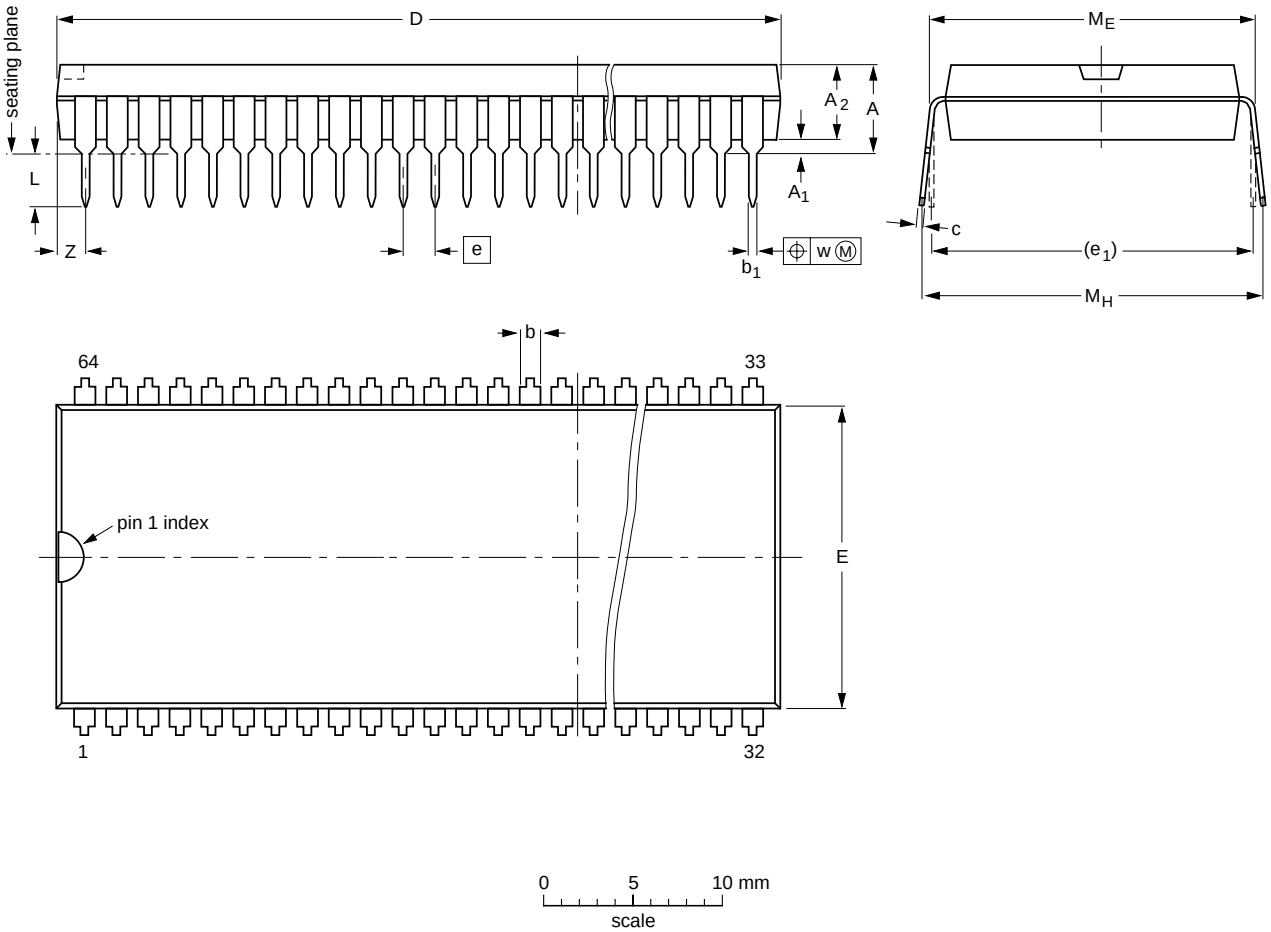
L1 to L9 are ferrite beads.

The pin numbers given in parenthesis refer to the TDA9870AH version.

Fig.11 Schematic for application.

13 PACKAGE OUTLINES

SDIP64: plastic shrink dual in-line package; 64 leads (750 mil) **SOT274-1**



DIMENSIONS (mm are the original dimensions)

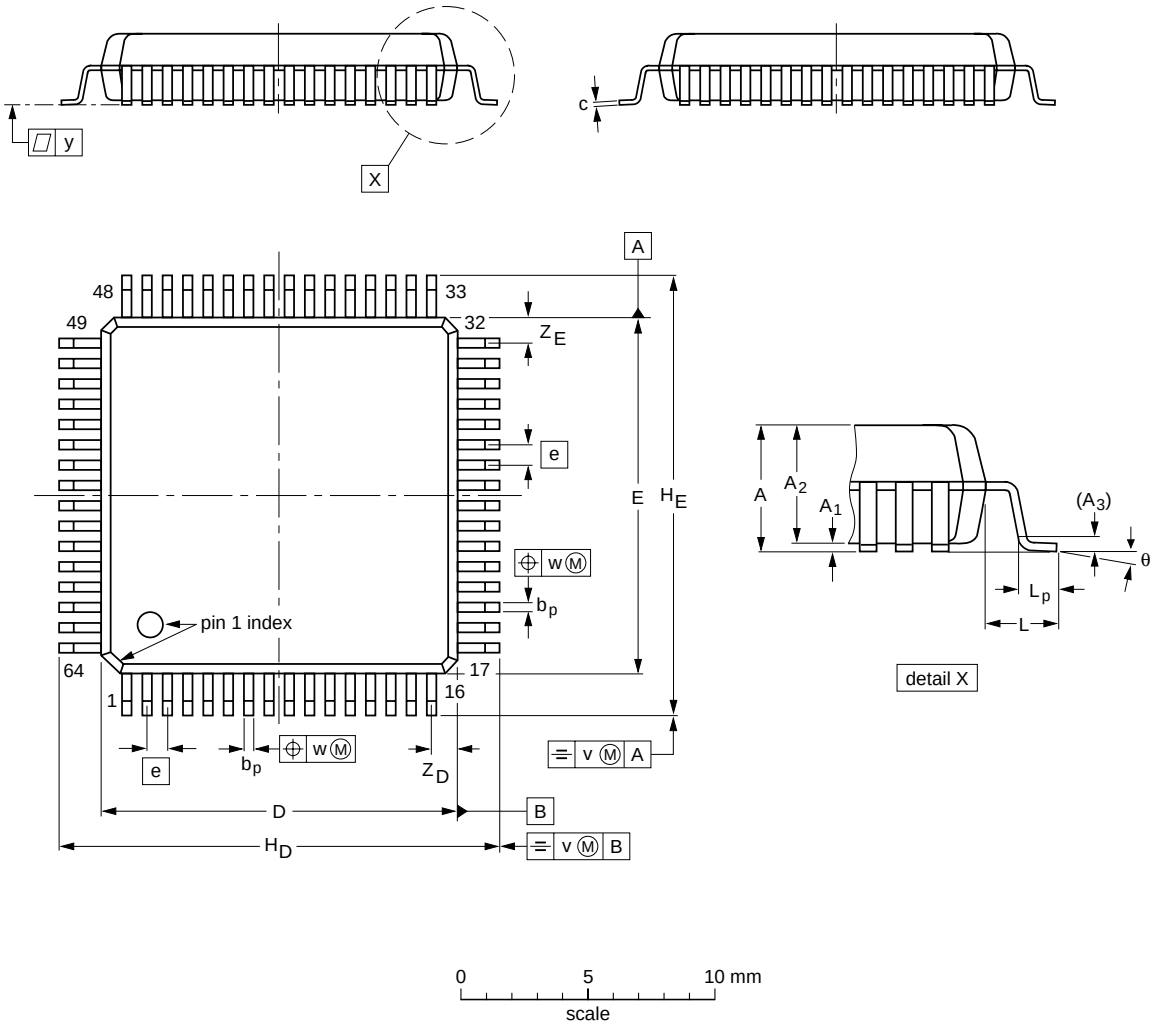
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.84	0.51	4.57	1.3 0.8	0.53 0.40	0.32 0.23	58.67 57.70	17.2 16.9	1.778	19.05	3.2 2.8	19.61 19.05	20.96 19.71	0.18	1.73

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT274-1		MS-021				~~95-02-04~~ 99-12-27

QFP64: plastic quad flat package; 64 leads (lead length 1.6 mm); body 14 x 14 x 2.7 mm **SOT393-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.00	0.25 0.10	2.75 2.55	0.25	0.45 0.30	0.23 0.13	14.1 13.9	14.1 13.9	0.8	17.45 16.95	17.45 16.95	1.60	1.03 0.73	0.16	0.16	0.10	1.2 0.8	1.2 0.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT393-1		MS-022				~~97-08-04~~ 99-12-27

14 SOLDERING

14.1 Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

14.2 Through-hole mount packages

14.2.1 SOLDERING BY DIPPING OR BY SOLDER WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

14.2.2 MANUAL SOLDERING

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

14.3 Surface mount packages

14.3.1 REFLOW SOLDERING

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

14.3.2 WAVE SOLDERING

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.3.3 MANUAL SOLDERING

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

14.4 Suitability of IC packages for wave, reflow and dipping soldering methods

MOUNTING	PACKAGE	SOLDERING METHOD		
		WAVE	REFLOW(1)	DIPPING
Through-hole mount	DBS, DIP, HDIP, SDIP, SIL	suitable(2)	–	suitable
Surface mount	BGA, SQFP	not suitable	suitable	–
	HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(3)	suitable	–
	PLCC(4), SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended(4)(5)	suitable	–
	SSOP, TSSOP, VSO	not recommended(6)	suitable	–

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
3. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

15 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

16 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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