DATA SHEET

TDA9874H
Digital TV sound demodulator/decoder

Product specification
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Philips
Semiconductors

PHILIPS

CONTENTS

1 FEATURES

- Sound IF (SIF) input switch e.g. to select between terrestrial TV SIF and SAT SIF sources
- SIF Automatic Gain Control (AGC) with 21 dB control range
- SIF 8-bit Analog-to-Digital Converter (ADC)
- Differential Quadrature Phase Shift Keying (DQPSK) demodulation for different standards, simultaneously with 1-channel FM demodulation
- Near Instantaneous Companded Audio Multiplexing (NICAM) decoding (B/G, D/K, I and L standard)
- 2-carrier multi-standard FM demodulation (B/G, D/K, I and M standard)
- Decoding for three analog multi-channel systems (A2, A2+ and A2*) and satellite sound
- Adaptive de-emphasis for satellite
- Programmable identification (B/G, D/K and M standard) and different identification times
- Optional AM demodulation for L standard, simultaneously with NICAM
- Monitor selection for FM/AM demodulator outputs and FM and NICAM signals
- Digital crossbar switch
- I^2S-bus serial audio output with matrix, level adjust and mute
- Dual audio Digital-to-Analog Converter (DAC) from digital crossbar switch to analog crossbar switch, bandwidth 15 kHz
- Analog crossbar switch with inputs for mono and stereo
- Output selection of mono, stereo, dual, dual A or dual B
- 20 kHz bandwidth for analog path
- Standby mode.

2 GENERAL DESCRIPTION

The TDA9874H is a single-chip Digital TV Sound Demodulator/Decoder (DTVSD) for analog and digital multi-channel sound systems in TV/VCR sets and satellite receivers.

2.1 Supported standards

The multi-standard/multi-stereo capability of the TDA9874H is mainly of interest in Europe, but also in Hong Kong/PR China and South East Asia. This includes B/G, D/K, I, M and L standards. In other application areas there exist subsets of those standard combinations or only single standards are transmitted.

Standard M is transmitted in Europe by the American Forces Network with European channel spacing (7 MHz VHF, 8 MHz UHF) and monaural sound.

The AM sound of L/L' standard is normally demodulated in the 1st sound IF. The resulting AF signal has to be entered into the mono audio input of the TDA9874H. A second possibility is to use the internal AM demodulator stage, which gives limited performance.

Korea has a stereo sound system similar to Europe which is supported by the TDA9874H. Differences include deviation, modulation contents and identification. It is based on M standard.

An overview of the supported standards, sound systems and their key parameters is given in Tables 1 to 3.

The analog multi-channel systems are sometimes also referred to as 2-carrier systems (2CS).

2.1.1 Analog 2-carrier systems

Table 1 Frequency modulation

STANDARD	SOUND SYSTEM	CARRIER FREQUENCY (MHz)	FM DEVIATION (kHz)			MODULATION		BANDWIDTH/ DE-EMPHASIS (kHz/μs)
			NOM.	MAX.	OVER.	SC1	SC2	
M	mono	4.5	15	25	50	mono	–	15/75
M	A2+	4.5/4.724	15	25	50	½(L + R)	½(L – R)	15/75 (Korea)
B/G	A2	5.5/5.742	27	50	80	½(L + R)	R	15/50
I	mono	6.0	27	50	80	mono	–	15/50
D/K	A2	6.5/6.742	27	50	80	½(L + R)	R	15/50
D/K	A2*	6.5/6.258	27	50	80	½(L + R)	R	15/50

Table 2 Identification for A2 systems

PARAMETER	A2; A2*	A2+ (KOREA)
Pilot frequency	54.6875 kHz = 3.5 × line frequency	55.0699 kHz = 3.5 × line frequency
Stereo identification frequency	$117.5\ \text{Hz} = \frac{\text{line frequency}}{133}$	$149.9\ \text{Hz} = \frac{\text{line frequency}}{105}$
Dual identification frequency	$274.1\ \text{Hz} = \frac{\text{line frequency}}{57}$	$276.0\ \text{Hz} = \frac{\text{line frequency}}{57}$
AM modulation depth	50%	50%

2.1.2 2-carrier systems with NICAM

Table 3 NICAM

STANDARD	SC1						SC2 (MHz) NICAM	DE-EMPHASIS	ROLL-OFF (%)	NICAM CODING
	FREQUENCY (MHz)	TYPE	MODULATION							
			INDEX (%)		DEVIATION (kHz)					
			NOM.	MAX.	NOM.	MAX.				
B/G	5.5	FM	–	–	27	50	5.85	J17	40	note 1
I	6.0	FM	–	–	27	50	6.552	J17	100	note 1
D/K	6.5	FM	–	–	27	50	5.85	J17	40	note 2
L	6.5	AM	54	100	–	–	5.85	J17	40	note 1

Notes

1. See *"EBU specification"* or equivalent specification.
2. Not yet officially defined.

2.1.3 SATELLITE SYSTEMS

An important specification for satellite TV reception is the Astra specification. The TDA9874H is suited for the reception of Astra and other satellite signals, with sound carrier frequencies from 4 to 9.2 MHz.

Table 4 FM satellite sound

CARRIER TYPE	CARRIER FREQUENCY (MHz)	MODULATION INDEX	MAXIMUM FM DEVIATION (kHz)	MODULATION	BANDWIDTH/ DE-EMPHASIS (kHz/μs)
Main	6.50[1]	0.26	85	mono	15/50[2]
Sub	7.02/7.20	0.15	50	m/st/d[3]	15/adaptive[4]
Sub	7.38/7.56	0.15	50	m/st/d[3]	15/adaptive[4]
Sub	7.74/7.92	0.15	50	m/st/d[3]	15/adaptive[4]
Sub	8.10/8.28	0.15	50	m/st/d[3]	15/adaptive[4]

Notes

1. For other satellite systems, frequencies of e.g. 5.80, 6.60 or 6.65 MHz can also be received.
2. A de-emphasis of 60 μs or in accordance with J17 is available.
3. m/st/d = mono or stereo or dual language sound.
4. Adaptive de-emphasis = compatible to transmitter specification.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9874H	QFP44	plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 × 14 × 2.2 mm	SOT205-1

4 BLOCK DIAGRAM

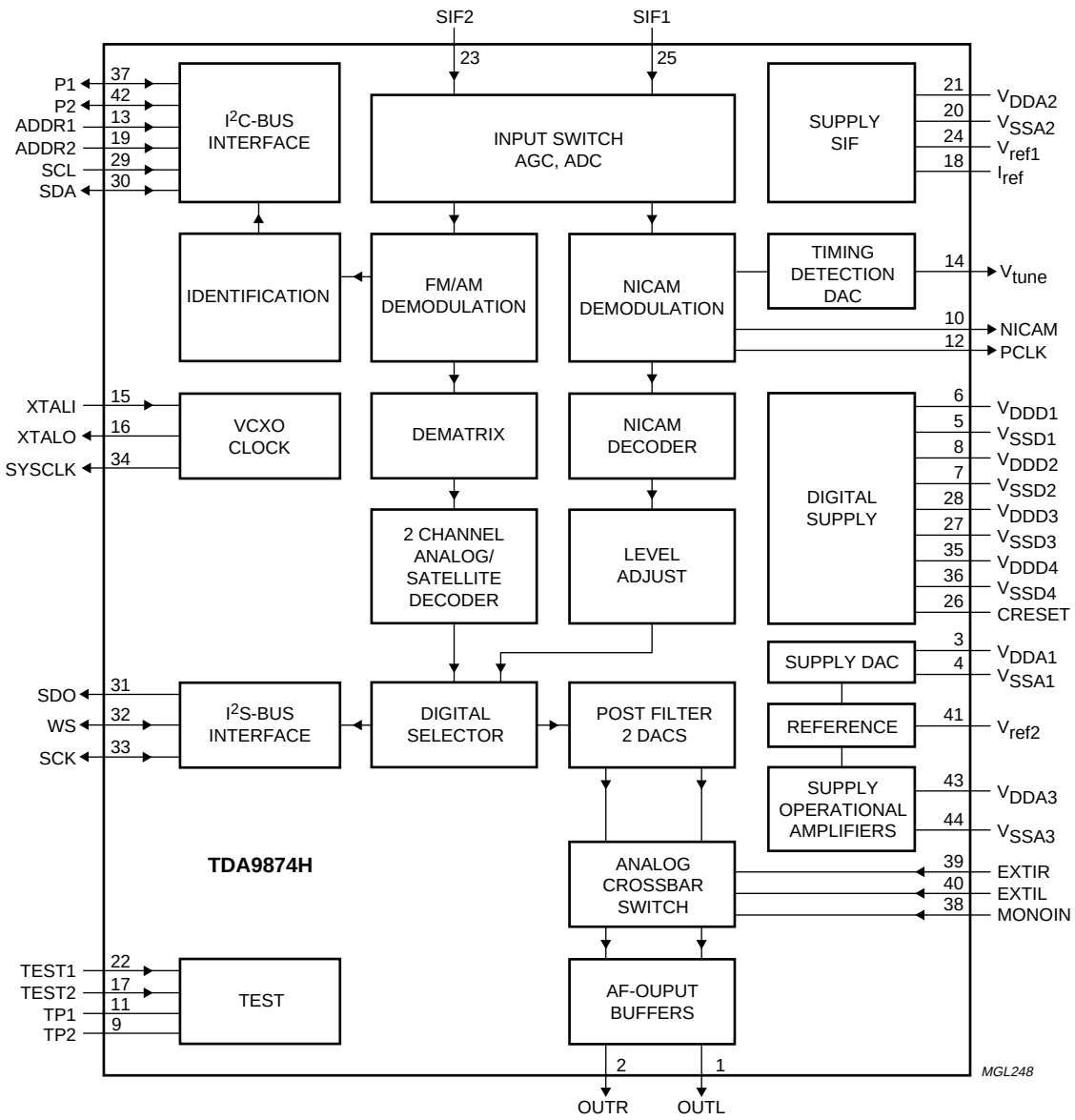


Fig.1 Block diagram.

5 PINNING

SYMBOL	PIN	DESCRIPTION
OUTL	1	analog output left
OUTR	2	analog output right
V_{DDA1}	3	analog supply voltage 1; DAC circuitry
V_{SSA1}	4	analog ground supply 1; DAC circuitry
V_{SSD1}	5	digital ground supply 1; DAC circuitry
V_{DDD1}	6	digital supply voltage 1; DAC circuitry
V_{SSD2}	7	digital ground supply 2; Digital Signal Processing (DSP) part
V_{DDD2}	8	digital supply voltage 2; DSP part
TP2	9	additional test pin 2; connected to V_{SSD} for normal operation
NICAM	10	serial NICAM data output at 728 kHz
TP1	11	additional test pin 1; connected to V_{SSD} for normal operation
PCLK	12	NICAM clock output at 728 kHz
ADDR1	13	first I^2C-bus slave address modifier input
V_{tune}	14	tuning voltage output for crystal oscillator
XTALI	15	crystal oscillator input
XTALO	16	crystal oscillator output
TEST2	17	test pin 2; connected to V_{SSD} for normal operation
I_{ref}	18	resistor for reference current generation; front-end circuitry
ADDR2	19	second I^2C-bus slave address modifier input
V_{SSA2}	20	analog ground supply 2; analog front-end circuitry
V_{DDA2}	21	analog supply voltage 2; analog front-end circuitry
TEST1	22	test pin 1; connected to V_{SSD} for normal operation
SIF2	23	sound IF input 2
V_{ref1}	24	reference voltage; analog front-end circuitry
SIF1	25	sound IF input 1
CRESET	26	capacitor for Power-on reset
V_{SSD3}	27	digital ground supply 3; front-end circuitry
V_{DDD3}	28	digital supply voltage 3; front-end circuitry
SCL	29	I^2C-bus clock input
SDA	30	I^2C-bus data input/output
SDO	31	I^2S-bus serial data output
WS	32	I^2S-bus word select input/output
SCK	33	I^2S-bus clock input/output
SYSCLK	34	system clock output
V_{DDD4}	35	digital supply voltage 4; demodulator circuitry
V_{SSD4}	36	digital ground supply 4; demodulator circuitry
P1	37	first general purpose I/O pin
MONOIN	38	analog mono input
EXTIR	39	external audio input right channel
EXTIL	40	external audio input left channel

SYMBOL	PIN	DESCRIPTION
V_{ref2}	41	analog reference voltage DAC and operational amplifiers
P2	42	second general purpose I/O pin
V_{DDA3}	43	analog supply voltage 3; operational amplifiers
V_{SSA3}	44	analog ground supply 3; operational amplifiers

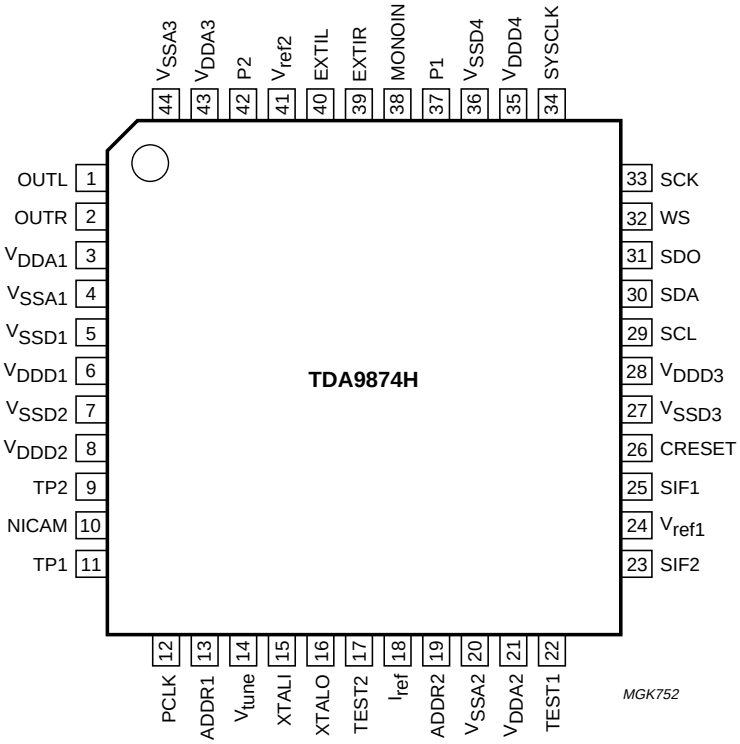


Fig.2 Pin configuration.

6 FUNCTIONAL DESCRIPTION

6.1 Description of the demodulator and decoder section

6.1.1 SIF INPUTS

Two input pins are provided. SIF1 e.g. for terrestrial TV and SIF2 e.g. for a satellite tuner. As no specific filters are integrated, both inputs have the same specification giving flexibility in application. The selected signal is passed through an AGC and then digitized by an 8-bit ADC running at 24.576 MHz.

6.1.2 AGC

The gain of the AGC amplifier is controlled from the ADC output by means of a digital control loop employing hysteresis. The AGC has a fast attack behaviour to prevent ADC overloads, and a slow decay behaviour to prevent AGC oscillations. For AM demodulation the AGC must be switched off. When switched off, the control loop is reset and fixed gain settings can be chosen (see Table 11).

The AGC can be controlled via the I^2C-bus. Details can be found in Sections 7.3.1, 7.3.2 and 7.4.6.

6.1.3 MIXER

The digitized input signal is passed on to the mixers, which mix one or both input sound carriers down to zero IF. A 24-bit control word for each carrier sets the required frequency. Access to the mixer control word registers is via the I^2C-bus (see Sections 7.3.4 and 7.3.5). When receiving NICAM programs, a feedback signal is added to the control word of the second carrier mixer to establish a carrier-frequency loop.

6.1.4 FM AND AM DEMODULATION

An FM or AM input signal is passed through a band-limiting filter onto a demodulator that can be used for either FM or AM demodulation. Apart from the standard (fixed) de-emphasis characteristic, an adaptive de-emphasis is available for Wegener-Panda 1 encoded satellite programs.

6.1.5 FM DECODING

A 2-carrier stereo decoder recovers the left and right signal channels from the demodulated sound carriers. Both the European and Korean stereo systems are supported.

6.1.6 FM IDENTIFICATION

The identification of the FM sound mode is performed by AM synchronous demodulation of the pilot and narrow-band detection of the identification frequencies. The result is available via the I^2C-bus interface. A selection can be made via the I^2C-bus for B/G, D/K and M standards, and for three different time constants that represent different trade-offs between speed and reliability of identification.

6.1.7 NICAM DEMODULATION

The NICAM signal is transmitted in a DQPSK code at a bit rate of 728 kbits/s. The NICAM demodulator performs DQPSK demodulation and passes the resulting bitstream and clock signal to the NICAM decoder and, for evaluation purposes, to pins.

A timing loop controls the frequency of the crystal oscillator to lock the sampling instants to the symbol timing of the NICAM data. The polarity of the control signal is selectable to support applications, in which external circuitry is used to boost the tuning voltage of the oscillator.

6.1.8 NICAM DECODING

The device performs all decoding functions in accordance with the *"EBU NICAM 728 specification"*. After locking to the frame alignment word, the data are de-scrambled by application of the defined pseudo-random binary sequence, and the device synchronizes to the periodic frame flag bit C0.

The status of the NICAM decoder can be read out from the NICAM Status Register by the user (see Section 7.4.2). Bit OSB indicates that the decoder has locked to the NICAM data. Bit VDSP indicates that the decoder has locked to the NICAM data and that the data is valid sound data. Bit C4 indicates that the sound conveyed by the FM mono channel is identical to the sound conveyed by the NICAM channel. The error byte contains the number of sound sample errors, resulting from parity checking, that occurred in the past 128 ms period. The Bit Error Rate (BER) can be calculated using the following equation:

$$\mathrm{BER} = \frac{\text{bit errors}}{\text{total bits}} \approx \text{error byte} \times 1.74 \times 10^{-5}$$

6.1.9 NICAM AUTO-MUTE

This function is enabled by setting bit AMUTE to logic 0 (see Section 7.3.11). Lower and upper error limits may be defined by writing appropriate values to two registers in the I^2C-bus section (see Sections 7.3.13 and 7.3.14). When the number of errors in a 128 ms period exceeds the upper error limit, the auto-mute function will switch the output sound from NICAM to whatever sound is on the first sound carrier (FM or AM) or to the analog mono input. When the error count is smaller than the lower error limit, the NICAM sound is restored.

The auto-mute function can be disabled by setting bit AMUTE = 1. In this case clicks become audible, when the error count increases. The user will hear a signal of degrading quality.

A decision to enable/disable the auto-muting is taken by the microprocessor based on an interpretation of the application control bits C1, C2, C3 and C4, and possibly any additional strategy implemented by the set maker in the microcontroller software.

When the AM sound in NICAM L systems is demodulated in the 1st sound IF and the audio signal connected to the mono input of the TDA9874H, the controlling microprocessor has to take care of switching from NICAM reception to mono input, if auto-muting is desired. This could be achieved by setting bit AMSEL = 1 and bit AMUTE = 0.

6.1.10 CRYSTAL OSCILLATOR

A circuit diagram of the external components of the voltage-controlled crystal oscillator is shown in Fig.7 in Chapter 12.

6.1.11 TEST PINS

All test pins are active HIGH. In normal operation of the device they can be left open-circuit, as they have internal pull-down resistors. Test functions are for manufacturing tests only and are not available to customers.

6.2 Description of the DSP

6.2.1 LEVEL SCALING

All input channels to the digital crossbar switch are equipped with a level adjust facility to change the signal level in a range of ±15 dB. Adjusting the signal level is intended to compensate for the different modulation parameters of the various TV standards. It is recommended to scale all input channels to be 15 dB below full-scale (–15 dB full-scale) under nominal conditions. This will create sufficient headroom to cope with overmodulation and avoids changes of the volume impression when switching from FM to NICAM or vice versa.

6.2.2 NICAM PATH

The NICAM path has a switchable J17 de-emphasis.

6.2.3 NICAM AUTO-MUTE

If NICAM is received, the auto-mute is enabled and the signal quality becomes poor, the digital crossbar switches automatically to FM, channel 1 or the analog mono input, as selected by bit AMSEL. This automatic switching depends on the NICAM bit error rate. The auto-mute function can be disabled via the I²C-bus.

6.2.4 FM (AM) PATH

A high-pass filter suppresses DC offsets from the FM demodulator that may occur due to carrier frequency offsets and supplies the FM monitor function with DC values, e.g. for the purpose of microprocessor controlled carrier search or fine tuning functions.

An adaptive de-emphasis is available for Wegener-Panda 1 encoded satellite programs.

The de-emphasis stage offers a choice of settings for the supported TV standards.

The 2 channel decoder performs the dematrixing of $\frac{1}{2}$(L + R) and R to L and R signals, of $\frac{1}{2}$(L + R) and $\frac{1}{2}$(L – R) to L and R signals or of channel 1 and channel 2 to L and R signals, as demanded by the different TV standards or user preferences.

6.2.5 FM MONITOR

This function provides data words from the FM demodulator outputs and FM and NICAM signals for external use, such as carrier search or fine tuning. Source selection and data read out are performed via the I²C-bus.

6.2.6 DIGITAL CROSSBAR SWITCH

Input channels come from the FM and NICAM paths, while output channels comprise I²S and the audio DACs to the analog crossbar switch. Note that there is no connection from the external analog audio inputs to the digital crossbar switch.

6.2.7 DIGITAL AUDIO OUTPUT

The digital audio output interface comprises an I²S output port and a system clock output. The I²S port is equipped with a level adjust facility that can change the signal level in a ±15 dB range in 1 dB steps. Muting is possible, too, and outputs can be disabled to improve EMC performance.

The I²S-bus output matrix provides the functions of forced mono, stereo, channel swap, channel 1 or channel 2.

6.2.8 CHANNEL TO THE ANALOG CROSSBAR PATH

A level adjust function is provided with control positions 0 dB, +3 dB, +6 dB and +9 dB in combination with the audio DACs.

6.2.9 GENERAL

The level adjust functions can provide signal gain at multiple locations. Great care has to be taken when using gain with large input signals, e.g., due to overmodulation, in order not to exceed the maximum possible signal swing, which would cause severe signal distortion. The nominal signal level of the various signal sources to the digital crossbar switch should be 15 dB below digital full-scale (–15 dB full-scale).

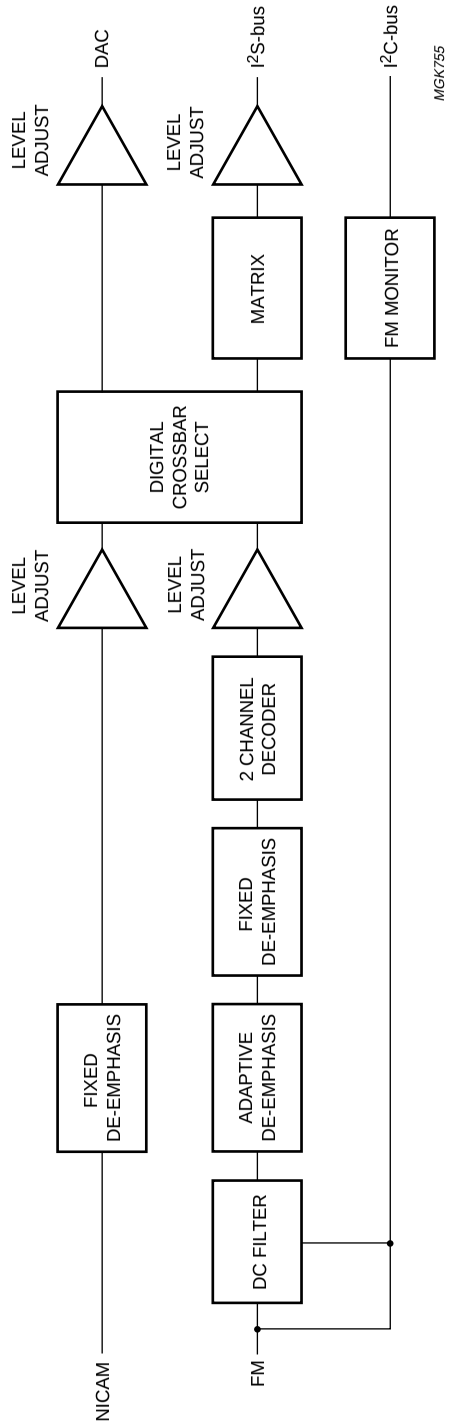


Fig.3 DSP data flow diagram.

6.3 Description of the analog audio section

6.3.1 Analog crossbar switch and analog matrix

The TDA9874H has one external analog stereo input, one mono input and one two-channel output port. Analog source selector switches are employed to provide the desired analog signal routing capability, which is done by the analog crossbar switch section.

The basic signal routing philosophy of the TDA9874H is that each switch handles two signal channels at the same time, e.g. Left and Right, language A and B, directly at the source. For an overview of the signal flow see Fig.5.

Each source selector switch is followed by an analog matrix to perform further selection tasks, like putting a signal from one input channel, say, language A, to both output channels or for swapping left and right channel. The analog matrix provides the functions given in Table 5.

All switches and matrices are controlled via the I^2C-bus.

Table 5 Analog matrix functions

MODE	MATRIX OUTPUT	
	L OUTPUT	R OUTPUT
1	L input	R input
2	R input	L input
3	L input	L input
4	R input	R input

6.3.2 External and mono inputs

The external and mono inputs accept signal levels of up to 1.4 V (RMS). By adding external series resistors to provide a suitable attenuation, the external input could be used as a SCART input. Whenever the external or mono input is selected, the output of the DAC is muted to improve the crosstalk performance.

6.3.3 Dual audio DAC

The TDA9874H comprises a two-channel audio DAC for feeding signals from the DSP section to the analog crossbar switch. These DACs have a resolution of 15 bits and employ four-fold oversampling and noise shaping.

6.3.4 Audio output buffers

The output buffers provide 0 dB of gain and offer a muting possibility. The post filter capacitors of the audio DACs are connected to the buffer outputs.

6.3.5 Standby mode

The standby mode (see Section 7.3.2) disables most functions and reduces power dissipation of the TDA9874H, but provides no other functionality.

Internal registers may lose their information in standby mode. Therefore, the device needs to be initialized on returning to normal operation. This can be accomplished in the same way as after a Power-on reset.

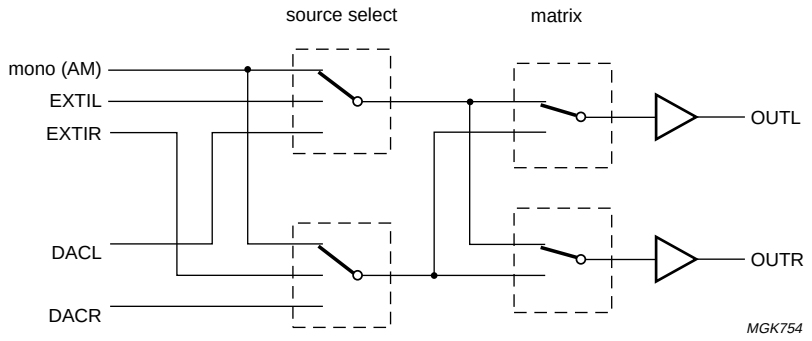


Fig.4 Switch diagram for the audio section.

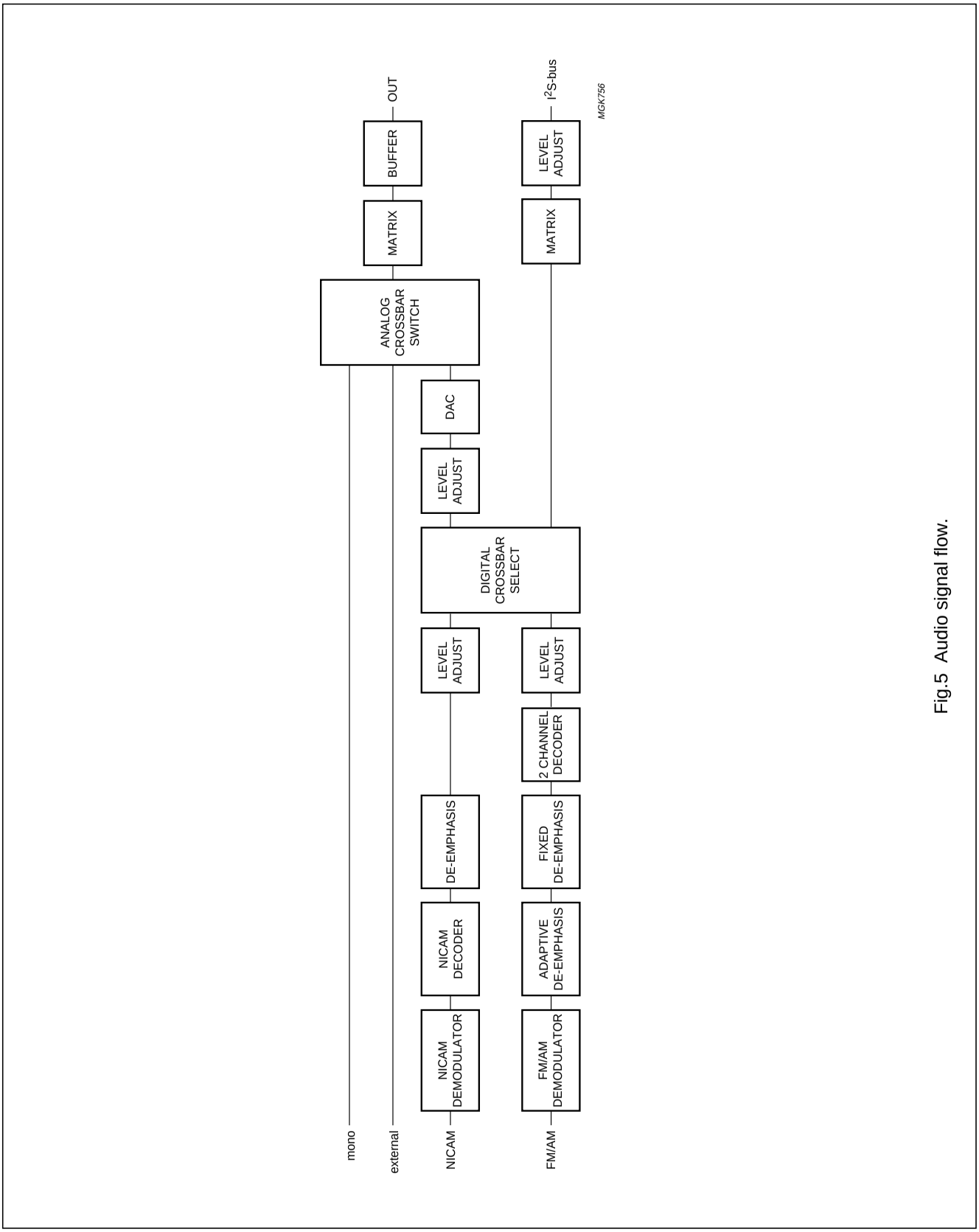


Fig.5 Audio signal flow.

7 I²C-BUS CONTROL

7.1 Introduction

The TDA9874H is controlled only via the I²C-bus. Control is exercised by writing data to one or more internal registers. Status information can be read from an array of registers to let the controlling microprocessor determine whether any action is required.

The device has an I²C-bus slave transceiver in accordance with the fast-mode specification with a maximum speed of 400 kbits/s. Information about the I²C-bus can be found in brochure *"I²C-bus and how to use it"* (order number 9398 393 40011). To avoid conflicts in a real application with other ICs providing similar or complementing functions, there are four possible slave addresses available, which can be selected by pins ADDR1 and ADDR2 (see Table 6).

Table 6 Possible slave addresses

ADDR2	ADDR1	SLAVE ADDRESS						
		A6	A5	A4	A3	A2	A1	A0
0	0	1	0	1	1	0	0	0
0	1	1	0	1	1	0	0	1
1	0	1	0	1	1	0	1	0
1	1	1	0	1	1	0	1	1

The I²C-bus interface remains operational in the standby mode of the TDA9874H to allow the device to be reactivated via the I²C-bus.

The device will not respond to a 'general call' on the I²C-bus, i.e. when a slave address of 000 0000 is sent by a master.

7.2 Power-up state

At power-up the device is in the following state:

- All outputs muted
- No sound carrier frequency loaded
- General purpose I/O pins ready for input (HIGH)
- Input SIF1 selected with:
  - AGC on
  - Small hysteresis.
- Demodulators for both sound carriers set to FM with:
  - Identification for B/G, D/K, identification mode 'slow'
  - Level adjust set to 0 dB
  - De-emphasis 50 μs
  - Dematrix set to mono
  - Adaptive de-emphasis on.
- Outputs OUTL and OUTR set to mono and connected to DAC
- Digital audio interface all outputs off
- Monitor set to carrier 1 DC output.

After power-up a device initialization has to be performed via the I²C-bus to put the TDA9874H into the proper mode of operation, in accordance with the desired TV standard, etc. This can be done by writing to all registers with a single I²C-bus transmission (like a refresh operation) or by writing selectively only to those registers, the contents of which need to be changed with regard to the power-up state.

7.3 Slave receiver mode

As a slave receiver, the TDA9874H provides 24 registers for storing commands and data. Each register is accessed via a so-called subaddress. A subaddress can be thought of as a pointer to an internal memory location.

Detailed descriptions of the slave receiver registers are given in Sections 7.3.1 to 7.3.20.

It is allowed to send more than one data byte per transmission to the TDA9874H. In that case, the subaddress is automatically incremented after each data byte, resulting in storing the sequence of data bytes at successive register locations, starting at SUBADDRESS. A transmission can start at any valid subaddress. Each byte that is properly stored, is acknowledged with A (acknowledge). If an attempt is made to write data to a non-existing subaddress, the device acknowledges with $\overline{A}$ (not acknowledge), therefore telling the I^2C-bus master to abort the transmission. There is no 'wrap-around' of subaddresses.

Commands and data will be processed as soon as they have been received completely. Functions requiring more than one byte will, thus, be executed only after all bytes for that function have been received. If the transmission is terminated (STOP condition) before all bytes have been received, the incomplete data for that function are ignored.

Data patterns sent to the various subaddresses are not checked for being illegal or not at that address, except for the level adjust functions.

Detection of a STOP condition without a preceding acknowledge bit is regarded as a bus error. In this case, the last operation will not be executed.

Table 7 I^2C-bus; slave address, subaddress and data format

S	SLAVE ADDRESS	0	A	SUBADDRESS	A	DATA	A	P

Table 8 Explanation of Table 7

BIT	FUNCTION
S	START condition
SLAVE ADDRESS	7-bit device address
0	data direction bit (write to device)
A	acknowledge
SUBADDRESS	address of register to write to
DATA	data byte to be written into register
P	STOP condition

Table 9 Format for a transmission employing auto-increment of subaddresses

S	SLAVE ADDRESS	0	A	SUBADDRESS	A	DATA BYTE(1)	DATA	A	P

Note

1. n data bytes with auto-increment of subaddresses.

Table 10 Overview of the slave receiver registers

SUBADDRESS (DECIMAL)	DATA								FUNCTION
	7	6	5	4	3	2	1	0	
0	B7	B6	B5	B4	B3	B2	B1	B0	AGC gain selection (ignored, if AGC on)
1	P2OUT	P1OUT	STDBY	INIT	0	AGCSLOW	AGCOFF	SIFSEL	general configuration
2	–	–	–	MCSM1	MCSM0	–	MSS1	MSS0	monitor select
3	B7	B6	B5	B4	B3	B2	B1	B0	carrier 1 frequency; MS part
4	B7	B6	B5	B4	B3	B2	B1	B0	carrier 1 frequency
5	B7	B6	B5	B4	B3	B2	B1	B0	carrier 1 frequency; LS part
6	B7	B6	B5	B4	B3	B2	B1	B0	carrier 2 frequency; MS part
7	B7	B6	B5	B4	B3	B2	B1	B0	carrier 2 frequency
8	B7	B5	B5	B4	B3	B2	B1	B0	carrier 2 frequency; LS part
9	IDMOD1	IDMOD0	IDAREA	–	CH2MOD1	CH2MOD0	CH1WIDE	CH1MODE	demodulator configuration
10	ADEEM2	FMDSC23	FMDSC22	FMDSC21	ADEEM1	FMDSC13	FMDSC12	FMDSC11	FM de-emphasis
11	–	–	–	–	–	FDMS2	FDMS1	FDMS0	FM dematrix
12	B7	B6	B5	B4	B3	B2	B1	B0	channel 1 output level adjust
13	B7	B6	B5	B4	B3	B2	B1	B0	channel 2 output level adjust
14	–	–	TIMPOL	DOUTEN	–	AMSEL	NDEEM	AMUTE	NICAM configuration
15	B7	B6	B5	B4	B3	B2	B1	B0	NICAM output level adjust
16	B7	B6	B5	B4	B3	B2	B1	B0	NICAM lower error limit
17	B7	B6	B5	B4	B3	B2	B1	B0	NICAM upper error limit
18	1	MUTI2S	1	1	1	MUTOUT	1	1	audio mute control
19	DGS1	–	–	–	DGS0	–	DOS1	DOS0	DAC output select
20	–	CSM2	CSM1	CSM0	–	–	SS1	SS0	analog output select
21	–	–	–	SYSCL1	SYSCL0	SYSOUT	I2SFORM	IS2OUT	digital audio interface configuration
22	–	ICSM2	ICSM1	ICSM0	–	–	ISS1	ISS0	I^2S-bus output select
23	B7	B6	B5	B4	B3	B2	B1	B0	I^2S-bus output level adjust

7.3.1 AGC GAIN REGISTER

If the AGC function is switched off in the general configuration register (see Section 7.3.2), the contents of this register defines a fixed gain of the SIF input stage. The input voltages given are meant to generate a nearly full-scale output from the SIF ADC. If the AGC is on, the content of this register is ignored. The default setting at power-up is 0000 0000.
In Table 11 the stated step number corresponds with the SIF level read from subaddress 7 (see Section 7.4.6); the input voltages should be considered as approximate target values.

Table 11 AGC gain register (subaddress 0)

7	6	5	4	3	2	1	0	STEP	SIF INPUT VOLTAGE [mV (RMS)]
B7	B6	B5	B4	B3	B2	B1	B0		
0	0	0	1	1	1	1	1	31	240
0	0	0	1	1	1	1	0	30	214
0	0	0	1	1	1	0	1	29	195
0	0	0	1	1	1	0	0	28	176
0	0	0	1	1	0	1	1	27	159
0	0	0	1	1	0	1	0	26	145
0	0	0	1	1	0	0	1	25	131
0	0	0	1	1	0	0	0	24	119
0	0	0	1	0	1	1	1	23	107
0	0	0	1	0	1	1	0	22	99
0	0	0	1	0	1	0	1	21	90
0	0	0	1	0	1	0	0	20	82
0	0	0	1	0	0	1	1	19	76
0	0	0	1	0	0	1	0	18	70
0	0	0	1	0	0	0	1	17	65
0	0	0	1	0	0	0	0	16	60
0	0	0	0	1	1	1	1	15	55
0	0	0	0	1	1	1	0	14	51
0	0	0	0	1	1	0	1	13	48
0	0	0	0	1	1	0	0	12	45
0	0	0	0	1	0	1	1	11	42
0	0	0	0	1	0	1	0	10	39
0	0	0	0	1	0	0	1	9	36
0	0	0	0	1	0	0	0	8	34
0	0	0	0	0	1	1	1	7	32
0	0	0	0	0	1	1	0	6	30
0	0	0	0	0	1	0	1	5	29
0	0	0	0	0	1	0	0	4	27
0	0	0	0	0	0	1	1	3	25
0	0	0	0	0	0	1	0	2	24
0	0	0	0	0	0	0	1	1	23
0	0	0	0	0	0	0	0	0	22

7.3.2 General configuration register

The default setting at power-up is 1100 0000.

Table 12 General configuration register (subaddress 1)

7	6	5	4	3	2	1	0
P2OUT	P1OUT	STDBY	INIT	–	AGCSLOW	AGCOFF	SIFSEL

Table 13 Description of the general configuration register bits

BIT	SYMBOL	DESCRIPTION
7	P2OUT	General purpose I/O pins 1 and 2: these bits control general-purpose input/output pins. The contents of these bits is written directly to the corresponding pins. If an input is desired, the bits must be set to logic 1 to allow the pins to be pulled to logic 0 externally. Input from the pins is reflected in the device status register (see Section 7.4.1). Bit P1OUT is recommended to be used for switching an SIF trap for the adjacent picture carrier in designs that employ such a trap.
6	P1OUT	
5	STDBY	Standby mode on/off: bit STDBY = 1 puts the TDA9874H into the standby mode. Most functions are disabled and power dissipation is somewhat reduced. If bit STDBY = 0 the TDA9874H is in its normal mode of operation. On return from standby mode, the device is in its Power-on reset mode and needs to be re-initialized with data defined by the set maker.
4	INIT	Initialize to default settings: bit INIT = 1 causes initialization of the TDA9874H to its default settings. This has the same effect as a Power-on reset. In case there is a conflict between the default settings and any bit set to logic 1 in this register, the bits of this register have priority over the corresponding default setting. This bit is automatically reset to logic 0 after initialization has completed. If set to logic 0, the TDA9874H is in its normal mode of operation.
3	–	this bit is not used and should be set to a logic 0
2	AGCSLOW	AGC decay time: if bit AGCSLOW = 1 a longer decay time and larger hysteresis are selected for input signals with strong video modulation (intercarrier). This bit only has an effect if bit AGCOFF = 0. If bit AGCSLOW = 0 the normal attack and decay times for the AGC and a small hysteresis are selected.
1	AGCOFF	AGC on/off: bit AGCOFF = 1 forces the AGC block to a fixed gain as defined in the AGC gain register (see Section 7.3.1). If bit AGCOFF = 0 the automatic gain control function is enabled and the contents of the AGC gain register is ignored.
0	SIFSEL	SIF input select: bit SIFSEL = 1 selects pin SIF2 for input (recommended for satellite tuner). If bit SIFSEL = 0 pin SIF1 (recommended for terrestrial TV) is selected.

Note

1. Bit AGCSLOW should be set to logic 1 for best possible audio performance.

7.3.3 MONITOR SELECT REGISTER

This register is used to define the signal source, the level of which is to be monitored, and the signal channel. Data can be monitored before or behind the DC filter at the FM/AM demodulator outputs. The last available data sample can be read out in the I^2C-bus slave transmitter mode (see Section 7.4.5).

Phase means the differentiated phase output of the FM demodulator and is provided, when the demodulator operates in FM mode, while magnitude is supplied in AM mode.

The default setting at power-up is 0000 0000.

Table 14 Monitor select register (subaddress 2)

7	6	5	4	3	2	1	0
–	–	–	MCSM1	MCSM0	–	MSS1	MSS0

Table 15 Description of the monitor select register bits

BIT	SYMBOL	DESCRIPTION
7	–	these bits are not used and should be set to logic 0
6	–	
5	–	
4	MCSM1	Signal channel select: the state of these bits determine which signal channel is selected (see Table 16).
3	MCSM0	
2	–	this bit is not used and should be set to logic 0
1	MSS1	Signal source select: the state of these bits determine which signal source is selected (see Table 17).
0	MSS0	

Table 16 Signal channel selection

MCSM1	MCSM0	SIGNAL CHANNEL
0	0	$\frac{\text{channel 1} + \text{channel 2}}{2}$
0	1	channel 1
1	0	channel 2

Table 17 Signal source selection

MSS1	MSS0	SIGNAL SOURCE
0	0	DC output of FM/AM demodulator
0	1	magnitude/phase output of FM/AM demodulator
1	0	FM/AM path output
1	1	NICAM path output

7.3.4 CARRIER 1 FREQUENCY REGISTER

Three bytes are required to define a 24-bit frequency control word to represent the sound carrier (i.e. mixer) frequency. These three bytes are stored at subaddresses 3 to 5; subaddress 3 being the high byte. Execution of the command starts only after all bytes have been received. If an error occurs, e.g. a premature STOP condition, partial data for this function are ignored. The relation of the sound carrier frequency and the control word is given in the following formula:

$$data = \frac{f_{mix}}{f_{clk}} \times 2^{24}$$

where:

data = 24-bit frequency control word

f_{mix} = desired sound carrier frequency

f_{clk} = 12.288 MHz (clock frequency of mixer)

2^{24} = 16777216 (number of steps in a 24-bit word size).

Example: A 5.5 MHz sound carrier frequency will be generated by sending the following sequence of data bytes to the TDA9874H (data is 7509333 in decimal notation or 729555 in hexadecimal notation):
0111 0010 1001 0101 0101 0101.

The default setting at power-up is 0000 0000 for all three bytes.

Table 18 Carrier 1 frequency register high byte (subaddress 3)

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

Table 19 Carrier 1 frequency register middle byte (subaddress 4)

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

Table 20 Carrier 1 frequency register low byte (subaddress 5)

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

7.3.5 CARRIER 2 FREQUENCY REGISTER

The format is the same as for sound carrier 1, except subaddresses 6 to 8 are used. Subaddress 6 holds the high byte.

If the carrier 2 frequency register is used, it will be for either the second FM sound carrier of a terrestrial or satellite FM program or the NICAM sound carrier.

7.3.5.1 Note

While NICAM mode is used, the sound carrier 2 frequency should be set ±2 kHz of the NICAM carrier frequency to improve carrier loop settling. For a deviation of +2 kHz this results in the following settings:

Standard B/G, D/K and L:
5.850 MHz + 2 kHz = 5.852 MHz = (79EAAAH).

Standard I:
6.552 MHz + 2 kHz = 6.554 MHz = (888AAAH).

7.3.6 DEMODULATOR CONFIGURATION REGISTER

The default setting at power-up is 0000 0000.

Table 21 Demodulator configuration register (subaddress 9)

7	6	5	4	3	2	1	0
IDMOD1	IDMOD0	IDAREA	–	CH2MOD1	CH2MOD0	CH1WIDE	CH1MODE

Table 22 Description of the demodulation configuration register bits

BIT	SYMBOL	DESCRIPTION
7	IDMOD1	Identification mode for FM sound: these bits define the integrator time of the FM identification. A valid result may be expected after twice this time has expired, at the latest. The longer the time, the more reliable the identification (see Table 23).
6	IDMOD0	
5	IDAREA	Application area for FM identification: bit IDAREA = 1 selects FM identification frequencies in accordance with the specification for Korea. If bit IDAREA = 0 the frequencies for Europe are selected (B/G and D/K standard).
4	–	this bit is not used and should be set to logic 0
3	CH2MOD1	Channel 2 receive mode: these bits control the hardware for the second sound carrier in accordance with Table 24. NICAM mode employs a wider bandwidth of the decimation filters than FM mode.
2	CH2MOD0	
1	CH1WIDE	Channel 1 bandwidth: bit CH1WIDE = 1 switches the decimation filters for the first sound carrier to a wide bandwidth, so that the main sound carrier of a satellite channel with its larger deviation can be handled without additional distortion. If bit CH1WIDE = 0 the bandwidth is narrow to cope with the intermodulation requirements of FM stereo.
0	CH1MODE	Channel 1 receive mode: bit CH1MODE = 1 selects the hardware for the first sound carrier to operate in AM mode. If bit CH1MODE = 0 the FM mode is selected. This applies to both terrestrial and satellite FM reception.

Table 23 Identification mode

IDMOD1	IDMOD0	IDENTIFICATION MODE
0	0	slow
0	1	medium
1	0	fast
1	1	off/reset

Table 24 Channel 2 receive mode

CH2MOD1	CH2MOD0	CHANNEL 2
0	0	FM
0	1	AM
1	0	NICAM

7.3.6.1 Notes

It is recommended to switch the FM sound mode identification off whenever the received program is not a terrestrial 2-carrier sound. Switching the identification off will reset the associated hardware to a defined state.

Changing the FM identification mode during FM reception may cause a brief flickering of bit IDSTE or bit IDDUA in the device status register (see Section 7.4.1).

When channel 2 is used to receive FM sound carriers with the current application proposal (see Chapter 12), it is recommended to set bit TIMPOL to logic 1 (write subaddress 14; see Section 7.3.11) for best S/N performance.

7.3.7 FM DE-EMPHASIS REGISTER

This register is used to select the proper de-emphasis characteristics as appropriate for the standard of the received carrier. Bits B3 to B0 apply to sound carrier 1, bits B7 to B4 apply to sound carrier 2. In the event of A2 reception, both groups must be set to the same characteristics.

The default setting at power-up is 1000 1000.

Table 25 FM de-emphasis register (subaddress 10)

7	6	5	4	3	2	1	0
ADEEM2	FMDSC23	FMDSC22	FMDSC21	ADEEM1	FMDSC13	FMDSC12	FMDSC11

Table 26 Description of the FM de-emphasis register bits

BIT	SYMBOL	DESCRIPTION
7	ADEEM2	Adaptive de-emphasis on/off: bit ADEEM2 = 1 activates the adaptive de-emphasis function (for Wegener-Panda 1 encoded programs), which is required for certain satellite FM channels. The standard FM de-emphasis must then be set to 75 μs. If bit ADEEM2 = 0 the adaptive de-emphasis is off.
6	FMDSC23	FM de-emphasis: the state of these bits determine the FM de-emphasis for sound carrier 2 (see Table 27).
5	FMDSC22	
4	FMDSC21	
3	ADEEM1	Adaptive de-emphasis on/off: bit ADEEM1 = 1 activates the adaptive de-emphasis function (for Wegener-Panda 1 encoded programs), which is required for certain satellite FM channels. The standard FM de-emphasis must then be set to 75 μs. If bit ADEEM1 = 0 the adaptive de-emphasis is off.
2	FMDSC13	FM de-emphasis: the state of these bits determine the FM de-emphasis for sound carrier 1 (see Table 27).
1	FMDSC12	
0	FMDSC11	

Table 27 De-emphasis

FMDSC23	FMDSC22	FMDSC21	DE-EMPHASIS[1]
FMDSC13	FMDSC12	FMDSC11	
0	0	0	50 μs
0	0	1	60 μs
0	1	0	75 μs
0	1	1	J17
1	0	0	off

Note

1. The FM de-emphasis gain is 0 dB at 40 Hz.

7.3.8 FM DEMATRIX REGISTER

This register is used to select the proper dematrixing characteristics as appropriate for the standard of the received carrier and the related sound mode identification. For the dematrixing, it is assumed that the output from sound carrier 1 is on channel L input. The unused bits should be set to logic 0.

The default setting at power-up is 0000 0000.

Table 28 FM dematrix register (subaddress 11)

7	6	5	4	3	2	1	0
–	–	–	–	–	FDMS2	FDMS1	FDMS0

Table 29 Description of the FM dematrix register bits

BIT	SYMBOL	DESCRIPTION
7	–	these bits are not used and should be set to logic 0
6	–	
5	–	
4	–	
3	–	
2	FDMS2	Dematrixing characteristics select: the state of these 3 bits select the dematrixing characteristics (see Table 30).
1	FDMS1	
0	FDMS0	

Table 30 Selection of the dematrixing characteristics

FDMS2	FDMS1	FDMS0	L OUTPUT	R OUTPUT	MODE
0	0	0	L input	L input	forced mono
0	0	1	R input	R input	mono 2
0	1	0	L input	R input	dual
0	1	1	R input	L input	dual swapped
1	0	0	$2L\ input - R\ input$	R input	stereo Europe
1	0	1	$\frac{L\ input + R\ input}{2}$	$\frac{L\ input - R\ input}{2}$	stereo Korea

7.3.9 CHANNEL 1 OUTPUT LEVEL ADJUST REGISTER

This register is used to correct for standard and station-dependent differences of signal levels. Table 31 applies to sound carrier 1. The default setting at power-up is 0000 0000.

Table 31 Channel 1 output level adjust register (subaddress 12)

7	6	5	4	3	2	1	0	GAIN SETTING (dB)
B7	B6	B5	B4	B3	B2	B1	B0	
0	0	0	0	1	1	1	1	+15
0	0	0	0	1	1	1	0	+14
0	0	0	0	1	1	0	1	+13
0	0	0	0	1	1	0	0	+12
0	0	0	0	1	0	1	1	+11
0	0	0	0	1	0	1	0	+10
0	0	0	0	1	0	0	1	+9
0	0	0	0	1	0	0	0	+8
0	0	0	0	0	1	1	1	+7
0	0	0	0	0	1	1	0	+6
0	0	0	0	0	1	0	1	+5
0	0	0	0	0	1	0	0	+4
0	0	0	0	0	0	1	1	+3
0	0	0	0	0	0	1	0	+2
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1	not defined
0	0	0	1	1	1	1	0	−1
0	0	0	1	1	1	0	1	−2
0	0	0	1	1	1	0	0	−3
0	0	0	1	1	0	1	1	−4
0	0	0	1	1	0	1	0	−5
0	0	0	1	1	0	0	1	−6
0	0	0	1	1	0	0	0	−7
0	0	0	1	0	1	1	1	−8
0	0	0	1	0	1	1	0	−9
0	0	0	1	0	1	0	1	−10
0	0	0	1	0	1	0	0	−11
0	0	0	1	0	0	1	1	−12
0	0	0	1	0	0	1	0	−13
0	0	0	1	0	0	0	1	−14
0	0	0	1	0	0	0	0	−15

7.3.10 CHANNEL 2 OUTPUT LEVEL ADJUST REGISTER

This register is used to correct for standard and station-dependent differences of signal levels. Table 32 applies to sound carrier 2 in its FM and AM modes. In the event of FM stereo or FM dual language reception, channels 1 and 2 shall be adjusted to the same level. The default setting at power-up is 0000 0000.

Table 32 Channel 2 output level adjust register (subaddress 13)

7	6	5	4	3	2	1	0	GAIN SETTING (dB)
B7	B6	B5	B4	B3	B2	B1	B0	
0	0	0	0	1	1	1	1	+15
0	0	0	0	1	1	1	0	+14
0	0	0	0	1	1	0	1	+13
0	0	0	0	1	1	0	0	+12
0	0	0	0	1	0	1	1	+11
0	0	0	0	1	0	1	0	+10
0	0	0	0	1	0	0	1	+9
0	0	0	0	1	0	0	0	+8
0	0	0	0	0	1	1	1	+7
0	0	0	0	0	1	1	0	+6
0	0	0	0	0	1	0	1	+5
0	0	0	0	0	1	0	0	+4
0	0	0	0	0	0	1	1	+3
0	0	0	0	0	0	1	0	+2
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1	not defined
0	0	0	1	1	1	1	0	–1
0	0	0	1	1	1	0	1	–2
0	0	0	1	1	1	0	0	–3
0	0	0	1	1	0	1	1	–4
0	0	0	1	1	0	1	0	–5
0	0	0	1	1	0	0	1	–6
0	0	0	1	1	0	0	0	–7
0	0	0	1	0	1	1	1	–8
0	0	0	1	0	1	1	0	–9
0	0	0	1	0	1	0	1	–10
0	0	0	1	0	1	0	0	–11
0	0	0	1	0	0	1	1	–12
0	0	0	1	0	0	1	0	–13
0	0	0	1	0	0	0	1	–14
0	0	0	1	0	0	0	0	–15

7.3.11 NICAM CONFIGURATION REGISTER

The default setting at power-up is 0000 0000.

Table 33 NICAM configuration register (subaddress 14)

7	6	5	4	3	2	1	0
–	–	TIMPOL	DOUTEN	–	AMSEL	NDEEM	AMUTE

Table 34 Description of the NICAM configuration register bits

BIT	SYMBOL	DESCRIPTION
7	–	these bits are not used and should be set to logic 0
6	–	
5	TIMPOL	Timing loop polarity: bit TIMPOL = 1 inverts the polarity. This feature can be used to compensate for the phase shift that is introduced by an external inverting amplifier at the pin V_{tune}. Such an amplifier could be used to provide a larger tuning voltage swing for the VCXO. Bit TIMPOL = 0 sets the NICAM timing loop to normal polarity.
4	DOUTEN	Data output enable: bit DOUTEN = 1 enables the output of the NICAM serial data stream from the DQPSK demodulator and of the associated clock, PCLK. If bit DOUTEN = 0 both outputs will be 3-stated.
3	–	this bit is not used and should be set to logic 0
2	AMSEL	Auto-mute select: bit AMSEL = 1 will switch the auto-mute between NICAM sound and the analog mono input. This bit has only an effect if the auto-mute function is enabled and if the DAC has been selected in the Analog Output Select Register (see Section 7.3.17). If bit AMSEL = 0 the auto-mute will switch between NICAM sound and the sound on the first sound carrier (i.e. FM mono or AM).
1	NDEEM	De-emphasis on/off: bit NDEEM = 1 switches the NICAM J17 de-emphasis off. Bit NDEEM = 0 switches the NICAM J17 de-emphasis on.
0	AMUTE	Auto-muting on/off: bit AMUTE = 1 automatic muting is disabled. This bit has only an effect, if the second sound carrier is set to NICAM. Bit AMUTE = 0 enables the automatic switching between NICAM and the program on the first sound carrier (i.e. FM mono or AM), dependent on the NICAM bit error rate.

7.3.11.1 Notes

The decision of whether auto-muting is permitted shall be taken by the controlling microprocessor based on information contained in the TDA9874H status registers. Thus, it depends on the strategy implemented in the software whether the auto-mute function is in accordance with *"NICAM 728 ETS Revised for Data Applications"* or any other preference.

The NICAM de-emphasis gain is 0 dB at 40 Hz.

Bit AMSEL has only an effect on the analog sound outputs OUTL and OUTR. With regard to the digital sound output (I^2S), the auto-mute will only switch between NICAM and the first sound carrier.

When carrier 2 is in FM mode, bit TIMPOL should be set to logic 1, to achieve the best S/N performance with the current oscillator application proposal (see Chapter 12).

7.3.12 NICAM OUTPUT LEVEL ADJUST REGISTER

This register is used to correct for standard and station-dependent differences of signal levels. Table 35 applies to both NICAM sound outputs. The default setting at power-up is 0000 0000.

Table 35 NICAM output level adjust register (subaddress 15)

7	6	5	4	3	2	1	0	GAIN SETTING (dB)
B7	B6	B5	B4	B3	B2	B1	B0	
0	0	0	0	1	1	1	1	+15
0	0	0	0	1	1	1	0	+14
0	0	0	0	1	1	0	1	+13
0	0	0	0	1	1	0	0	+12
0	0	0	0	1	0	1	1	+11
0	0	0	0	1	0	1	0	+10
0	0	0	0	1	0	0	1	+9
0	0	0	0	1	0	0	0	+8
0	0	0	0	0	1	1	1	+7
0	0	0	0	0	1	1	0	+6
0	0	0	0	0	1	0	1	+5
0	0	0	0	0	1	0	0	+4
0	0	0	0	0	0	1	1	+3
0	0	0	0	0	0	1	0	+2
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1	not defined
0	0	0	1	1	1	1	0	−1
0	0	0	1	1	1	0	1	−2
0	0	0	1	1	1	0	0	−3
0	0	0	1	1	0	1	1	−4
0	0	0	1	1	0	1	0	−5
0	0	0	1	1	0	0	1	−6
0	0	0	1	1	0	0	0	−7
0	0	0	1	0	1	1	1	−8
0	0	0	1	0	1	1	0	−9
0	0	0	1	0	1	0	1	−10
0	0	0	1	0	1	0	0	−11
0	0	0	1	0	0	1	1	−12
0	0	0	1	0	0	1	0	−13
0	0	0	1	0	0	0	1	−14
0	0	0	1	0	0	0	0	−15

7.3.13 NICAM LOWER ERROR LIMIT REGISTER

When the auto-mute function is enabled (see Section 7.3.11) and the NICAM bit error count is lower than the value contained in this register, the NICAM signal is selected (again) for reproduction. See also Section 7.3.14.

The default setting at power-up is 0001 0100.

Table 36 NICAM lower error limit register (subaddress 16)

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

7.3.14 NICAM UPPER ERROR LIMIT REGISTER

When the auto-mute function is enabled and the NICAM bit error count is higher than the value contained in this register, the signal of the first sound carrier (i.e. FM mono or AM sound) or the analog mono input is selected for reproduction.

The difference between upper and lower error limit constitutes a hysteresis to avoid frequent switching between NICAM and the program on the first sound carrier.

The default setting at power-up is 0101 0000.

Table 37 NICAM upper error limit register (subaddress 17)

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

7.3.15 AUDIO MUTE CONTROL REGISTER

Only bits 6 and 2 are used. The unused bits should be set to logic 1. When any of these bits is set to logic 1, the corresponding pair of output channels will be muted. A bit set to logic 0 allows normal signal output.

The default setting at power-up is 1111 1111.

Table 38 Audio mute control register (subaddress 18)

7	6	5	4	3	2	1	0
–	MUTI^{2}S	–	–	–	MUTOUT	–	–

7.3.16 DAC OUTPUT SELECT REGISTER

This register is used to define the signal source to be entered into the DAC. The DAC is used for signal output from digital sources at analog outputs.

The two combinations of FM and NICAM shown in Table 41 apply to the (rare) condition that three different languages are being broadcast in an FM + NICAM system. They allow for a two-out-of-three selection for special applications. Note that the controlling microprocessor has to assure that the FM dematrix is set to the mono position.

Some extra gain can be introduced at the input to the DAC to provide a coarse level adjust function.

The default setting at power-up is 0000 0000.

The unused bits should be set to logic 0.

Table 39 DAC output select register (subaddress 19)

7	6	5	4	3	2	1	0
DGS1	–	–	–	DGS0	–	DOS1	DOS0

Table 40 Selection of DAC gain

DGS1	DGS0	DAC GAIN (dB)
0	0	0
0	1	3
1	0	6
1	1	9

Table 41 Signal source left and right

DOS1	DOS0	SIGNAL SOURCE	
		LEFT	RIGHT
0	0	FM/AM	FM/AM
0	1	NICAM left	NICAM right
1	0	FM/AM	NICAM M1
1	1	FM/AM	NICAM M2

7.3.17 Analog output select register

This register is used to define both the signal source to be output at the analog outputs and the output channel selector mode.

The DAC outputs are automatically muted, in case one of the analog inputs is selected for output.

The position $\frac{L+R}{2}$ of the matrix applies only to the DAC outputs, it is not available for analog input signals.

The default setting at power-up is 0000 0000.

Table 42 Analog output select register (subaddress 20)

7	6	5	4	3	2	1	0
–	CSM2	CSM1	CSM0	–	–	SS1	SS0

Table 43 Description of the analog output select register bits

BIT	SYMBOL	DESCRIPTION
7	–	this bit is not used and should be set to logic 0
6	CSM2	Output channel selection mode: these bits select the output channel selection mode (see Table 44).
5	CSM1	
4	CSM0	
3	–	these bits are not used and should be set to logic 0
2	–	
1	SS1	signal source: these bits select the signal source (see Table 45)
0	SS0	

Table 44 Output channel selection mode

CSM2	CSM1	CSM0	L OUTPUT	R OUTPUT
0	0	0	L input	R input
0	0	1	L input	L input
0	1	0	R input	R input
0	1	1	R input	L input
1	0	0	$\frac{L+R}{2}$	$\frac{L+R}{2}$

Table 45 Signal source selection

SS1	SS0	SIGNAL SOURCE
0	0	DAC
1	0	external input
1	1	mono input

7.3.18 Digital audio interface configuration register

The default setting at power-up is 0000 0000.

Table 46 Digital audio interface configuration register (subaddress 21)

7	6	5	4	3	2	1	0
–	–	–	SYSCL1	SYSCL0	SYSOUT	I2SFORM	I2SOUT

Table 47 Description of the digital audio interface configuration register bits

BIT	SYMBOL	DESCRIPTION
7	–	these bits are not used and should be set to logic 0
6	–	
5	–	
4	SYSCL1	System clock frequency select: these bits select the frequency of the system clock (see Table 48).
3	SYSCL0	
2	SYSOUT	System clock output on/off: bit SYSOUT = 1 enables the output of a system (or master) clock signal at pin SYSCLK. If bit SYSOUT = 0 the output will be off, thereby improving EMC performance.
1	I2SFORM	Serial output format: bit I2SFORM = 1 selects an MSB-aligned, MSB-first output format, i.e. a level change at the word select pin indicates the beginning of a new audio sample. If bit I2SFORM = 0 the standard I^2S-bus output format is selected.
0	I2SOUT	I^2S output on/off: bit I2SOUT = 1 enables the output of serial audio data (2 pins) plus serial bit clock and word select in a format determined by bit I2SFORM. The TDA9874H is then an I^2S-bus master. If bit I2SOUT = 0 the outputs mentioned will be 3-stated, thereby improving EMC performance.

Table 48 System clock frequency select

SYSCL1	SYSCL0	SYSCLK OUTPUT	FREQUENCY (MHz)
0	0	$256f_s$	8.192
0	1	$384f_s$	12.288
1	0	$512f_s$	16.384
1	1	$768f_s$	24.576

7.3.19 I²S-BUS OUTPUT SELECT REGISTER

This register is used to define both the signal source to be output at the I²S-bus port and the mode of the digital matrix for signal selection.

The two combinations of FM and NICAM shown in Table 52 apply to the (rare) condition that three different languages are being broadcast in an FM + NICAM system. They allow for a two-out-of-three selection for special applications. Note that the controlling microprocessor has to assure that the FM dematrix is set to the mono position.

The default setting at power-up is 0000 0000.

Table 49 I²S-bus output select register (subaddress 22)

7	6	5	4	3	2	1	0
–	ICSM2	ICSM1	ICSM0	–	–	ISS1	ISS0

Table 50 Description of the I²S-bus output select register bits

BIT	SYMBOL	DESCRIPTION
7	–	this bit is not used and should be set to logic 0
6	ICSM2	Output channel selection mode: these 3 bits select the output channel selection mode (see Table 51).
5	ICSM1	
4	ICSM0	
3	–	these bits are not used and should be set to logic 0
2	–	
1	ISS1	Signal source: these bits select the signal source (see Table 52).
0	ISS0	

Table 51 Mode of the digital matrix for signal selection

ICSM2	ICSM1	ICSM0	L OUTPUT	R OUTPUT
0	0	0	L input	R input
0	0	1	L input	L input
0	1	0	R input	R input
0	1	1	R input	L input
1	0	0	$\frac{L+R}{2}$	$\frac{L+R}{2}$

Table 52 Signal source left and right

ISS1	ISS0	SIGNAL SOURCE	
		LEFT	RIGHT
0	0	FM left	FM right
0	1	NICAM left	NICAM right
1	0	FM mono	NICAM M1
1	1	FM mono	NICAM M2

7.3.20 I²S-BUS OUTPUT LEVEL ADJUST REGISTER

This register is used to adjust the output level at the I²S-bus port. Left and right signal channels are treated identically. The default setting at power-up is 0000 0000.

Table 53 I²S-bus output level adjust register (subaddress 23)

7	6	5	4	3	2	1	0	GAIN SETTING (dB)
B7	B6	B5	B4	B3	B2	B1	B0	
0	0	0	0	1	1	1	1	+15
0	0	0	0	1	1	1	0	+14
0	0	0	0	1	1	0	1	+13
0	0	0	0	1	1	0	0	+12
0	0	0	0	1	0	1	1	+11
0	0	0	0	1	0	1	0	+10
0	0	0	0	1	0	0	1	+9
0	0	0	0	1	0	0	0	+8
0	0	0	0	0	1	1	1	+7
0	0	0	0	0	1	1	0	+6
0	0	0	0	0	1	0	1	+5
0	0	0	0	0	1	0	0	+4
0	0	0	0	0	0	1	1	+3
0	0	0	0	0	0	1	0	+2
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1	not defined
0	0	0	1	1	1	1	0	−1
0	0	0	1	1	1	0	1	−2
0	0	0	1	1	1	0	0	−3
0	0	0	1	1	0	1	1	−4
0	0	0	1	1	0	1	0	−5
0	0	0	1	1	0	0	1	−6
0	0	0	1	1	0	0	0	−7
0	0	0	1	0	1	1	1	−8
0	0	0	1	0	1	1	0	−9
0	0	0	1	0	1	0	1	−10
0	0	0	1	0	1	0	0	−11
0	0	0	1	0	0	1	1	−12
0	0	0	1	0	0	1	0	−13
0	0	0	1	0	0	0	1	−14
0	0	0	1	0	0	0	0	−15

7.4 Slave transmitter mode

As a slave transmitter, the TDA9874H provides 12 registers with status information and data, a part of which is for Philips internal purposes only. Each register is accessed by means of a subaddress.

Detailed descriptions of the slave transmitter registers are given in Sections 7.4.1 to 7.4.9.

Reading of data can start at any valid subaddress. It is allowed to read more than 1 data byte per transmission from the TDA9874H. In that case, the subaddress is automatically incremented after each data byte, resulting in reading the sequence of data bytes from successive register locations, starting at SUBADDRESS.

Each data byte in a read sequence, except for the last one, is acknowledged with Am. The subaddresses 'wrap around' from decimal 255 to 0. If an attempt is made to read from a non-existing subaddress, the device will send a data pattern of all ones, i.e. FF in hexadecimal notation.

Table 54 General format for reading data from the TDA9874H

S	SLAVE ADDRESS	0	A	SUBADDRESS	A	Sr	SLAVE ADDRESS	1	A	DATA	NAm	P

Table 55 Explanation of Tables 54 and 56

BIT	FUNCTION
S	START condition
SLAVE ADDRESS	7-bit device address
0	data direction bit (write to device)
A	acknowledge (by the slave)
SUBADDRESS	address of register to read from
Sr	repeated START condition
1	data direction bit (read from device)
DATA	data byte read from register
NAm	not acknowledge (by the master)
Am	acknowledge (by the master)
P	STOP condition

Table 56 Format of a transmission using automatic incrementing of subaddresses

S	SLAVE ADDRESS	0	A	SUBADDRESS	A	Sr	SLAVE ADDRESS	1	A	DATA BYTE Am(1)	DATA	NAm	P

Note

1. n data bytes with auto-increment of subaddresses.

Table 57 Overview of the slave transmitter registers

SUBADDRESS (DECIMAL)	DATA								FUNCTION
	7	6	5	4	3	2	1	0	
0	P2IN	P1IN	RSSF	AMSTAT	VDSP	IDDUA	IDSTE	–[1]	device status (identification, etc.)
1	C4	C3	C2	C1	OSB	CFC	S/MB	D/SB	NICAM status
2	B7	B6	B5	B4	B3	B2	B1	B0	NICAM error count
3	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	additional data (LSB)
4	OVW	SAD	–[1]	CI1	CI2	AD10	AD9	AD8	additional data (MSB)
5	B7	B6	B5	B4	B3	B2	B1	B0	level read out (MSB)
6	B7	B6	B5	B4	B3	B2	B1	B0	level read out (LSB)
7	–[1]	–[1]	–[1]	B4	B3	B2	B1	B0	SIF level
252[2]	B7	B6	B5	B4	B3	B2	B1	B0	test register 2
253[2]	B7	B6	B5	B4	B3	B2	B1	B0	test register 1
254[2]	B7	B6	B5	B4	B3	B2	B1	B0	device identification code
255[2]	B7	B6	B5	B4	B3	B2	B1	B0	software identification code

Notes

1. Value is undefined.
2. Registers from subaddress 252 to 255 are for Philips internal purposes only. They are considered as a set of registers for the identification of individual members and some key parameters in a family of devices.

7.4.1 DEVICE STATUS REGISTER

Table 58 Device status register (subaddress 0)

7	6	5	4	3	2	1	0
P2IN	P1IN	RSSF	AMSTAT	VDSP	IDDUA	IDSTE	–

Table 59 Description of the device status register bits

BIT	SYMBOL	DESCRIPTION
7	P2IN	Input from Port 2: this bit reflects the status of the general purpose port pin P2; see Section 7.3.2. If bit P2IN = 1 the general purpose port pin P2 is at HIGH level. If bit P2IN = 0 the general purpose port pin P2 is at LOW level.
6	P1IN	Input from Port 1: this bit reflects the status of the general purpose port pin P1; see Section 7.3.2. If bit P1IN = 1 the general purpose port pin P1 is at HIGH level. If bit P1IN = 0 the general purpose port pin P1 is at LOW level.
5	RSSF	Reserve Sound Switching Flag: if bit RSSF = 1 it is a copy of bit C4 in the NICAM Status Register (see Section 7.4.2). It indicates that the FM (or AM for standard L) sound matches the digital transmission and auto-muting should be enabled. If bit RSSF = 0 auto-muting should be disabled as analog and digital sound are different.
4	AMSTAT	Auto-mute Status: if this bit is 1, it indicates that the auto-muting function has switched from NICAM to the program of the first sound carrier (i.e. FM mono or AM in NICAM L systems).
3	VDSP	Identification of NICAM sound: bit VDSP = 1 indicates that digital transmission is a sound source. Bit VDSP = 0 indicates the transmission is either data or a currently undefined format.
2	IDDUA	Identification of FM dual sound; A2 systems: if bit IDDUA = 1, an FM dual-language signal has been identified. If neither bit IDSTE nor IDDUA = 1 the received signal is assumed to be FM mono (A2 systems only).
1	IDSTE	Identification of FM stereo; A2 systems; if bit IDSTE = 1 an FM stereo signal has been identified (A2 systems only).
0	–	value is undefined

7.4.2 NICAM STATUS REGISTER

Table 60 NICAM status register (subaddress 1)

7	6	5	4	3	2	1	0
C4	C3	C2	C1	OSB	CFC	S/MB	D/SB

Table 61 Description of the NICAM status register bits

BIT	SYMBOL	DESCRIPTION
7	C4	NICAM application control bits: these bits correspond to the control bits C1 to C4 in the NICAM transmission.
6	C3	
5	C2	
4	C1	
3	OSB	Synchronization bit: bit OSB = 1 indicates that the device has both frame and C0 (16 frame) synchronization. Bit OSB = 0 indicates the audio output from the NICAM part is digital silence.
2	CFC	Configuration change: bit CFC = 1 indicates a configuration change at the 16 frame (C0) boundary.
1	S/MB	Identification of NICAM stereo: bit S/MB = 1 indicates stereo mode.
0	D/SB	Identification of NICAM dual mono: bit D/SB = 1 indicates dual mono mode.

7.4.2.1 Notes

The TDA9874H does not support the extended control modes. Therefore, the program of the first sound carrier (i.e. FM mono or AM) is selected for reproduction in case bit C3 = 1, independent of bit AMUTE in the NICAM Configuration Register being set or not.

When a NICAM transmitter is switched off, the device will lose synchronization. In that case the program of the first sound carrier is selected for reproduction, independent of bit AMUTE being set or not.

7.4.3 NICAM ERROR COUNT REGISTER

Bits B7 to B0 contain the number of errors occurring in the previous 128 ms period. The register is updated every 128 ms.

Table 62 NICAM error count register (subaddress 2)

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

7.4.4 DATA REGISTERS DR1 AND DR2

The contents of these two registers provide information on the additional data bits. ADBYTE0 is stored at subaddress 3.

Table 63 Data register DR1 (subaddress 3)

7	6	5	4	3	2	1	0
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Table 64 Description of the data register DR1 bits

BIT	SYMBOL	DESCRIPTION
7	AD7	the lower 8 bits of the additional data word
6	AD6	
5	AD5	
4	AD4	
3	AD3	
2	AD2	
1	AD1	
0	AD0	

Table 65 Data register DR2 (subaddress 4)

7	6	5	4	3	2	1	0
OVW	SAD	–	CI1	CI2	AD10	AD9	AD8

Table 66 Description of the data register DR2 bits

BIT	SYMBOL	DESCRIPTION
7	OVW	If bit OVW = 1 new additional data bits are written to the IC without the previous bits being read.
6	SAD	If bit SAD = 1 new additional data is written into the IC. This bit is reset, if the additional data bits are read.
5	–	value is undefined
4	CI1	These bits are CI bits decoded by majority logic from the parity checks of the last ten samples in a frame.
3	CI2	
2	AD10	the upper 3 bits of the additional data word
1	AD9	
0	AD8	

7.4.5 Level read out registers A and B

These two bytes constitute a word that provides data from a location that has been specified with the FM Monitor Select Register (see Section 7.3.3). The most significant byte of the data is stored at subaddress 5.

Table 67 Level read out register A (subaddress 5)

7	6	5	4	3	2	1	0
B7[1]	B6	B5	B4	B3	B2	B1	B0

Note

1. B7 is the most significant bit or sign bit of the word.

Table 68 Level read out register B (subaddress 6)

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0[1]

Note

1. B0 is the least significant bit of the word.

7.4.6 SIF level register

When the SIF AGC is on, bits B4 to B0 of this register contain a number that gives an indication of the SIF input level. That number can be interpreted in the same way as the AGC Gain Register setting (see Section 7.3.1), i.e. if the SIF AGC were set to a fixed gain and the same number loaded into the AGC Gain Register, the current SIF input signal level would generate an SIF ADC output close to full-scale.

When the SIF AGC is off, this register returns the contents of the AGC Gain Register.

Bits B5 to B7 are not used and are undefined.

Table 69 SIF level register (subaddress 7)

7	6	5	4	3	2	1	0
–[1]	–[1]	–[1]	B4	B3	B2	B1	B0

Note

1. Value is undefined.

7.4.7 Test register 2

This register contains as a binary number the highest subaddress used for slave receiver registers.

The first version will have the identification 0010 1111.

Table 70 Test register 2 (subaddress 252)

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

7.4.8 Test register 1

This register contains as a binary number the highest subaddress used for slave transmitter (status) registers.

The first version will have the identification 0010 1111.

Table 71 Test register 1 (subaddress 253)

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

7.4.9 Device identification code

There will be several devices in the digital TV sound processor family, with TDA9874H being the second member. This byte is used to identify the individual family members.

The first version will have the identification 0000 0111.

Table 72 Device identification code (subaddress 254)

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

7.4.10 Software identification code

It is likely that during the life time of this family of devices several versions of the DSP software will be made, e.g. to take care of new application concepts, respond to customer wishes, etc. This byte is used to identify the different releases.

The first version will have the identification 0000 0111.

Table 73 Software identification code (subaddress 255)

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

8 I²S-BUS DESCRIPTION

The digital audio interface of the TDA9874H consists of a serial audio output and associated clock signals. It can be used to supply digital audio signals from received TV programs to a suitable output device, e.g. a DAC or an AES/EBU transmitter.

Two serial audio formats are supported at the digital audio interface, i.e. the I²S-bus format and a very similar MSB-aligned format. The difference is illustrated in Fig.6.

In both formats the left audio channel of a stereo sample pair is output first, and is placed on the Serial Data Output (SDO) line when the Word Select line (WS) is at LOW level. Data is written at the trailing edge of the Serial Clock (SCK) output and read at the leading edge of SCK. The most significant bit is sent first.

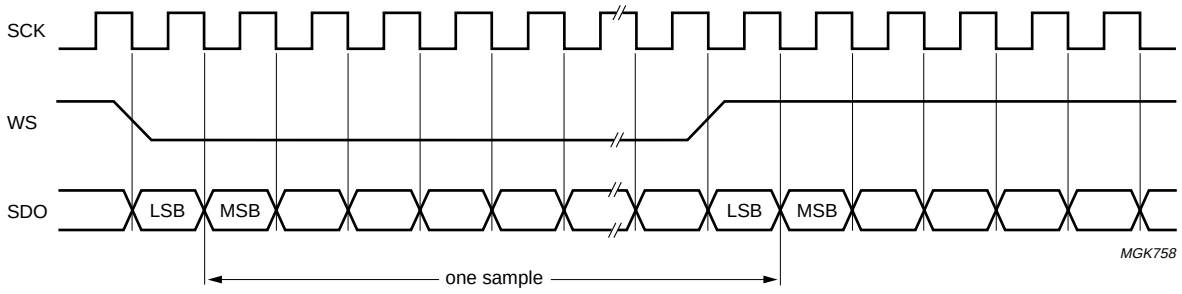
At power-up, the outputs of the digital audio interface are 3-stated to reduce EMC and allow for combinations with other ICs.

If output is desired, it has to be activated by means of an I²C-bus command.

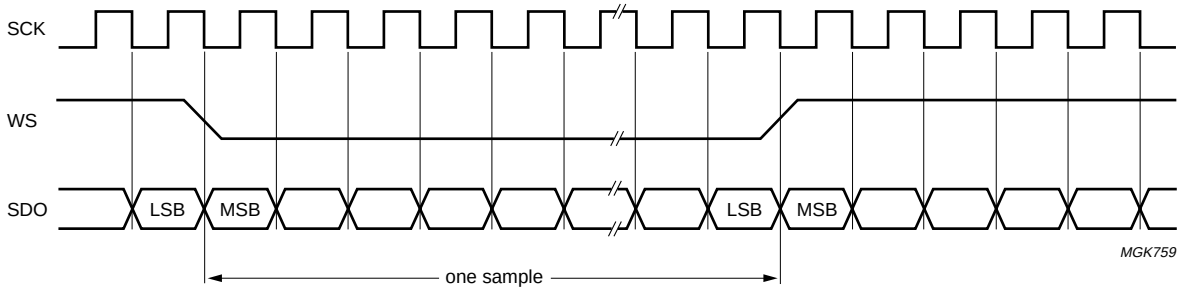
When the output is enabled, the serial audio data can be taken from pin SDO. Depending on the signal source, switch and matrix positions, the output can be either mono, stereo or dual language.

The Word Select output (WS) is clocked with the audio sample frequency of 32 kHz. The serial clock output is clocked at a frequency of 2048 MHz. This means, that there are 64 clock pulses per pair of stereo output samples, or 32 clock pulses per sample. There are 18 significant bits used on the serial data output.

A symmetrical system clock output (SYSCLK) is available from the TDA9874H as a master clock for external digital audio devices. At power-up, the clock is off. It can be enabled and the output frequency set via an I²C-bus command. Available output frequencies are 8192, 12288, 16384 and 24576 MHz.



a. I²S-bus format.



b. MSB-alignment format.

Fig.6 Serial audio interface formats.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDx}	DC supply voltage		–0.5	+6.5	V
ΔV_{DDx}	voltage differences between two V_{DD} pins		–	550	mV
I_{IK}	DC input clamp diode current	$V_i < –0.5$ V or $V_i > V_{DD} + 0.5$ V	–	±10	mA
I_{OK}	DC output clamp diode current; output type 4 mA	$V_o < –0.5$ V or $V_o > V_{DD} + 0.5$ V	–	±20	mA
I_o	DC output source or sink current; output type 4 mA	$–0.5 \text{ V} < V_o < V_{DD} + 0.5$ V	–	±20	mA
I_{DDD}, I_{SSD}	DC V_{DDD} or V_{SSD} current per digital supply pin		–	±62	mA
I_{DDA}, I_{SSA}	DC V_{DDA} or V_{SSA} current per analog supply pin		–	±28	mA
$I_{lu(prot)}$	latch-up protection current		100	–	mA
P/out	power dissipation per output		–	100	mW
P_{tot}	total power dissipation		–	0.9	W
T_{stg}	storage temperature		–55	+125	°C
T_{amb}	ambient temperature		–20	+70	°C
V_{es}	electrostatic handling	note 1	2000	–	V
		note 2	200	–	V

Notes

1. Human body model: C = 100 pF and R = 1.5 kΩ.
2. Machine model: C = 200 pF, L = 0.75 μH and R = 0 Ω.

10 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	70	K/W

11 CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = 25 °C; settings in accordance with B/G standard; FM deviation ±50 kHz; f_{mod} = 1 kHz; FM sound parameters in accordance with system A2; NICAM in accordance with *"EBU specification"*; 1 kΩ measurement source resistance for AF inputs; V_{SIF} = 300 mV (p-p); bit AGCOFF = 0; bit AGCSLOW = 1; level and gain settings according to note 2 with external components of Fig.7; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDD1}	digital supply voltage 1		4.5	5.0	5.5	V
V_{SSD1}	digital ground supply 1		–	0.0	–	V
I_{DDD1}	digital supply current 1	V_{DDD1} = 5.5 V	8	12	16	mA
		V_{DDD1} = 5.0 V	7	10	14	mA
V_{DDD2}	digital supply voltage 2		4.5	5.0	5.5	V
V_{SSD2}	digital ground supply 2		–	0.0	–	V
I_{DDD2}	digital supply current 2	V_{DDD2} = 5.5 V	25	32	37	mA
		V_{DDD2} = 5.0 V	22	28	33	mA
V_{DDD3}	digital supply voltage 3		4.5	5.0	5.5	V
V_{SSD3}	digital ground supply 3		–	0.0	–	V
I_{DDD3}	digital supply current 3	V_{DDD3} = 5.5 V; SYSCLK off	7	12	16	mA
		V_{DDD3} = 5.0 V; SYSCLK off	6	11	15	mA
Demodulator supplies and references						
V_{DDA2}	analog supply voltage 2 for demodulator part		4.5	5.0	5.5	V
V_{SSA2}	analog ground supply 2 for demodulator part		–	0.0	–	V
I_{DDA2}	analog supply current 2 for demodulator part	V_{DDA} = 5.5 V	20	24	28	mA
		V_{DDA} = 5.0 V	17	21.5	25	mA
V_{DDD4}	digital supply voltage 4		4.5	5.0	5.5	V
V_{SSD4}	digital ground supply 4		–	0.0	–	V
I_{DDD4}	digital supply current 4	V_{DDD2} = 5.5 V	40	50	60	mA
		V_{DDD2} = 5.0 V	34	44	54	mA
V_{ref1}	analog reference voltage 1 for demodulator part	referenced to V_{DDA2} and V_{SSA2}	35	50	65	%
$I_{ref1(sink)}$	sink current at pin V_{ref1}		170	220	260	µA
Audio supplies and references						
V_{DDA1}	analog supply voltage 1 for audio DAC part		4.5	5.0	5.5	V
V_{SSA1}	analog ground supply 1 for audio DAC part		–	0.0	–	V
I_{DDA1}	analog supply current 1 for audio DAC part	V_{DDA} = 5.5 V; digital silence	1.2	2.1	3.1	mA
		V_{DDA} = 5.0 V; digital silence	1.1	1.9	2.8	mA
V_{DDA3}	analog supply voltage 3 for operational amplifiers		4.5	5.0	5.5	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SSA3}	analog ground supply 3 for operational amplifiers		–	0.0	–	V
I_{DDA3}	analog supply current 3 for operational amplifiers	V_{DDA} = 5.5 V	1.3	1.8	2.4	mA
		V_{DDA} = 5.0 V	1.2	1.7	2.3	mA
V_{ref2}	reference voltage 2 for audio DACs and operational amplifiers	referenced to V_{DDA3} and V_{SSA3}	–	50	–	%
$Z_{(Vref2-VDDA3)}$	impedance between pins V_{ref2} and V_{DDA3}		–	20	–	kΩ
$Z_{(Vref2-VSSA3)}$	impedance between pins V_{ref2} and V_{SSA3}		–	20	–	kΩ
Digital inputs and outputs						
INPUTS						
CMOS level input, high drive, pull-down (pins TEST1, TEST2, TP1 and TP2)						
V_{IL}	LOW-level input voltage		–	–	1.6	V
V_{IH}	HIGH-level input voltage		3.0	–	–	V
C_i	input capacitance		–	–	10	pF
Z_i	input impedance		–	50	–	kΩ
CMOS level input, hysteresis, high drive, pull-up (pin CRESET)						
V_{IL}	LOW-level input voltage		–	–	1.0	V
V_{IH}	HIGH-level input voltage		4.0	–	–	V
V_{hys}	hysteresis voltage		–	$0.33V_{DDD}$	–	V
C_i	input capacitance		–	–	10	pF
Z_i	input impedance		–	50	–	kΩ
INPUTS/OUTPUTS						
I^2C level input with Schmitt trigger, open-drain output stage (pins SCL and SDA)						
V_{IL}	LOW-level input voltage		–	–	1.6	V
V_{IH}	HIGH-level input voltage		3.0	–	–	V
V_{hys}	hysteresis voltage		–	$0.33V_{DDD}$	–	V
I_{LI}	input leakage current		–	–	±10	µA
C_i	input capacitance		–	–	10	pF
V_{OL}	LOW-level output voltage		–	–	0.5	V
C_L	load capacitance	active pull-up	–	–	400	pF
		passive pull-up	–	–	200	pF
TTL/CMOS level, high drive, 4 mA 3-state output stage, pull-up (pins PCLK, NICAM, ADDR1, ADDR2, P1, P2, SCK, WS and SDO)						
V_{IL}	LOW-level input voltage		–	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	–	V
C_i	input capacitance		–	–	10	pF
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	–	–	0.5	V
V_{OH}	HIGH-level output voltage	I_{OH} = –3 mA	2.9	–	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_L	load capacitance	active pull-up	–	–	50	pF
Z_i	input impedance		–	50	–	kΩ
OUTPUTS						
4 mA 3-state output stage (pin SYSCLK)						
V_{OL}	LOW-level output voltage	I_{OL} = +2 mA	–	–	0.5	V
V_{OH}	HIGH-level output voltage	I_{OH} = –2 mA	2.9	–	–	V
C_L	load capacitance		–	–	50	pF
I_{LOZ}	3-state leakage current	V_i = 0 to V_{DDD}	–	–	±10	µA
SIF1 and SIF2 analog inputs						
$V_{SIF(p-p)}$	composite SIF input voltage (peak-to-peak value)	note 1	60	–	700	mV
f_i	input frequency		4	–	9.2	MHz
R_i	input resistance		10	13	16	kΩ
C_i	input capacitance		–	7.5	11	pF
Δf_{FM}	FM deviation	B/G standard; THD < 1%	±100	–	–	kHz
$\Delta f_{FM(FS)}$	FM deviation full-scale level	terrestrial FM; level adjust 0 dB	±150	–	–	kHz
C/N_{FM}	FM carrier-to-noise ratio	N_{FM} bandwidth = 6 MHz; white noise for S/N = 40 dB; *"CCIR468-2"*; quasi peak	–	77	–	$\frac{dB}{Hz}$
C/N_N	NICAM carrier-to-noise ratio	N_N bandwidth = 6 MHz; bit error rate = 10^{-3}; white noise	–	66	–	$\frac{dB}{Hz}$
Demodulator performance						
$V_{o(nom)(rms)}$	nominal level output voltage (RMS value)	note 2	400	500	600	mV
THD + N	total harmonic distortion plus noise	from FM source to any output with low-pass 30 kHz/3 dB; V_o = 1 V (RMS)	–	0.3	0.5	%
		from NICAM source to any output with low-pass 30 kHz/3 dB; V_o = 1 V (RMS)	–	0.1	0.3	%
S/N	signal-to-noise ratio	SC1 from FM source to any output; V_o = 1 V (RMS); *"CCIR468-2"*; quasi peak; bit TIMPOL = 1	61	65	–	dB
		SC2 from FM source to any output; V_o = 1 V (RMS); *"CCIR468-2"*; quasi peak; bit TIMPOL = 1	57	60	–	dB
		NICAM source; V_o = 1 V (RMS); *"CCIR468-2"*; quasi peak	NICAM in accordance with *"EBU specification"*; note 3			

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
B_{-3dB}	−3 dB bandwidth	from FM source to any output	14.5	15	–	kHz
		from NICAM source to any output	14.5	15	–	kHz
f_{res}	frequency response 20 Hz to 14 kHz	from FM/NICAM to any output; reference 1 kHz	−2	–	+1	dB
$\alpha_{cs(dual)}$	dual signal channel separation	note 4	65	70	–	dB
$\alpha_{cs(stereo)}$	stereo channel separation	note 5	40	45	–	dB
α_{AM}	AM suppression for FM	AM: 1 kHz, 30% modulation; reference: 1 kHz, 50 kHz deviation	50	–	–	dB
dm_{AM}	AM demodulation	SIF level 100 mV (RMS); 54% AM; 1 kHz AF; *"CCIR468-2"*; quasi peak	–	36	–	dB
IDENTIFICATION FOR FM SYSTEMS						
mod_p	pilot modulation for identification		25	50	75	%
C/N_p	pilot sideband carrier-to-noise ratio for identification start		–	32	–	$\frac{dB}{Hz}$
$hys_{(tun)}$	hysteresis		–	–	2	dB
f_{ident}	identification window	B/G stereo				
		slow mode	116.85	–	118.12	Hz
		medium mode	116.11	–	118.89	Hz
		fast mode	114.65	–	120.46	Hz
		B/G dual				
		slow mode	273.44	–	274.81	Hz
		medium mode	272.07	–	276.20	Hz
		fast mode	270.73	–	277.60	Hz
$t_{ident(on)}$	total identification time on	slow mode	–	–	2	s
		medium mode	–	–	1	s
		fast mode	–	–	0.5	s
$t_{ident(off)}$	total identification time off	slow mode	–	–	2	s
		medium mode	–	–	1	s
		fast mode	–	–	0.5	s
Mono and external inputs						
$V_{i(nom)(rms)}$	nominal level input voltage (RMS value)	note 2	–	500	–	mV
$V_{i(clip)(rms)}$	clipping level input voltage (RMS value)	THD < 3%; note 6	1250	1400	–	mV
R_i	input resistance	note 6	28	35	42	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog audio outputs						
$V_{o(clip)(rms)}$	clipping level output voltage (RMS value)	THD < 3%	1400	–	–	mV
R_o	output resistance		150	250	375	Ω
$R_{L(AC)}$	AC load resistor		10	–	–	kΩ
$R_{L(DC)}$	DC load resistor		10	–	–	kΩ
C_L	output load capacitor		–	10	12	nF
$V_{offset(DC)}$	static DC offset voltage		–	30	70	mV
α_{mute}	mute suppression	nominal input signal from any source; f_i = 1 kHz; note 2	80	–	–	dB
B_{line}	bandwidth	from external and mono source; –3 dB bandwidth	20	–	–	kHz
G_{ro}	roll-off gain at 14.5 kHz	from any source	–3	–2	–	dB
PSRR	power supply ripple rejection	f_{ripple} = 70 Hz; V_{ripple} = 100 mV (peak); C_{Vref} = 47 µF; signal from I^2S-bus	40	45	–	dB
Audio performance						
THD + N	total harmonic distortion plus noise	$V_i = V_o$ = 1 V (RMS); f_i = 1 kHz; bandwidth 20 Hz to 20 kHz; from external or mono input to output copy	–	0.1	0.3	%
S/N	signal-to-noise ratio	reference voltage V_o = 1.4 V (RMS); f_i = 1 kHz; *"CCIR468-2"*; quasi peak; from external or mono input to output copy	78	90	–	dB
α_{ct}	crosstalk attenuation	between any analog input pairs; f_i = 1 kHz	70	–	–	dB
α_{cs}	channel separation	between left and right of external input pair	65	–	–	dB
		between left and right of output pair	60	–	–	dB
VCXO and clock generation						
VCXO						
Crystal input						
C_i	input capacitance		–	–	10	pF
$V_{bias(DC)}$	DC bias voltage	R_i = 100 kΩ	3.5	3.63	3.7	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal output						
$V_{osc(p-p)}$	oscillation amplitude (peak-to-peak value)		–	1.4	–	V
$V_{bias(DC)}$	DC bias voltage		2.3	2.53	2.8	V
G_m	mutual conductance at 24.576 MHz		16.6	17.6	18.8	mS
C_o	output capacitance		–	–	10	pF
CRYSTAL SPECIFICATION (FUNDAMENTAL MODE)						
f_{xtal}	crystal frequency	note 7	–	24.576	–	MHz
C_L	load capacitance		–	20	–	pF
C_1	series capacitance		–	20	–	fF
C_0	parallel capacitance		–	–	7	pF
Φ_{pull}	pulling sensitivity	C_L changed from 18 to 16 pF	–	25	–	$\frac{10^{-6}}{pF}$
R_R	equivalent series resistance	at nominal frequency	–	–	30	Ω
R_N	equivalent series resistance of unwanted mode		$2R_R$	–	–	Ω
ΔT	temperature range		–20	+25	+70	°C
X_J	adjustment tolerance		–	–	±30	10^{-6}
X_D	drift	across temperature range	–	–	±30	10^{-6}
X_A	ageing		–	–	±5	$\frac{10^{-6}}{year}$

Notes

1. The demodulation/decoding is still functional above and below the limits given.
2. Definition of levels and level setting (see Tables 74 and 75):
   a) The full-scale level for analog audio signals is 1.4 V (RMS).
   b) The nominal level at the digital crossbar switch is defined at –15 dB (full-scale).
   c) Nominal audio input levels for external and mono: 500 mV (RMS) at –9 dB (full-scale).
3. Audio performance is limited by the dynamic range of the NICAM 728 system. Due to companding, the quantization noise is never lower than –62 dB referenced to the input level.
4. FM source; in dual mode only A (respectively B) signal modulated; measured at B (respectively A) channel output; V_o = 1 V (RMS) of modulated channel.
5. FM source; in stereo mode only L (respectively R) signal modulated; measured at R (respectively L) channel output; V_o = 1 V (RMS) of modulated channel.
6. If the supply voltage for the TDA9874H is switched off, because of the ESD protection circuitry all audio input pins are short-circuited.
7. The Philips crystal (order number 9922 520 20106) is suited for this application.

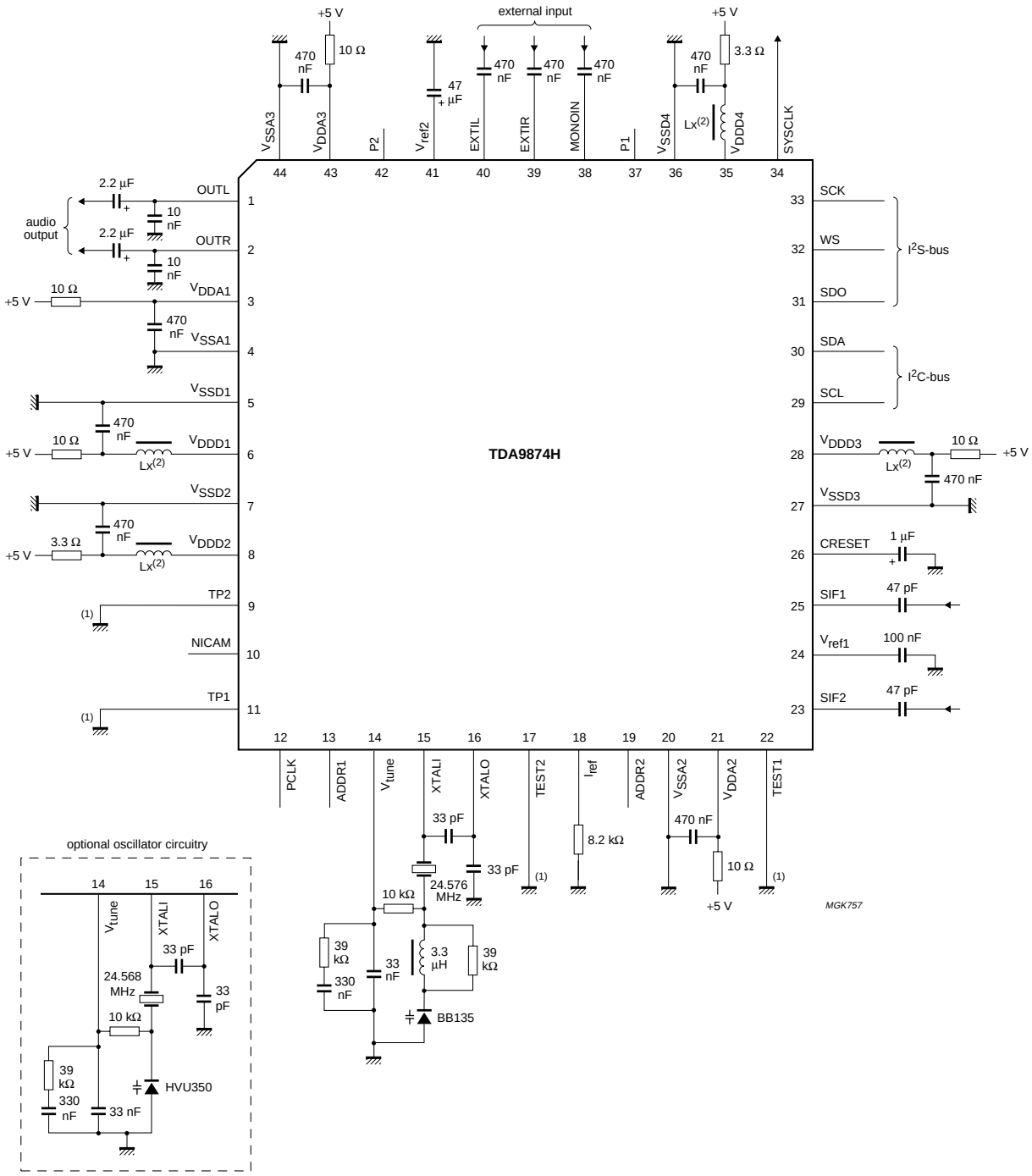
Table 74 Level setting FM, AM and NICAM at 0 dB (full-scale) = 1.4 V (RMS)

SOURCE	TRANSMITTER NOMINAL MODULATION DEPTH	NOMINAL LEVEL AT DEMODULATOR OUTPUT	LEVEL ADJUST SETTING	NOMINAL LEVEL AT CROSSBAR	DAC GAIN SETTING	NOMINAL OUTPUT VOLTAGE V_O
FM M standard	15 kHz deviation	–24 dB (full-scale)	+9 dB	–15 dB (full-scale) (spread of ±0.5 dB due to different transmitter references)	+6 dB	500 mV (RMS)
FM B/G, D/K, I standard	27 kHZ deviation	–19 dB (full-scale)	+4 dB			
AM L/L accent standard	54%	–19 dB (full-scale)	+4 dB			
NICAM B/G, D/K, L standard	–11.2 dB (full-scale)	–18 dB (full-scale)	+3 dB			
NICAM I standard	–15.8 dB (full-scale)	–23 dB (full-scale)	+8 dB			

Table 75 Level setting SAT FM at 0 dB (full-scale) = 1.4 V (RMS)

SOURCE	TRANSMITTER MAXIMUM MODULATION DEPTH	NOMINAL LEVEL AT DEMODULATOR OUTPUT	LEVEL ADJUST SETTING	MAXIMUM LEVEL AT CROSSBAR	DAC GAIN SETTING	MAXIMUM OUTPUT VOLTAGE V_O
SAT FM stereo	50 kHz deviation	–13 dB (full-scale)	+4 dB	–9 dB (full-scale)	+6 dB	1 V (RMS)
SAT FM mono	85 kHz deviation	–9 dB (full-scale)	0 dB			

12 APPLICATION DIAGRAM



All analog and digital supply ground pins are connected internally.

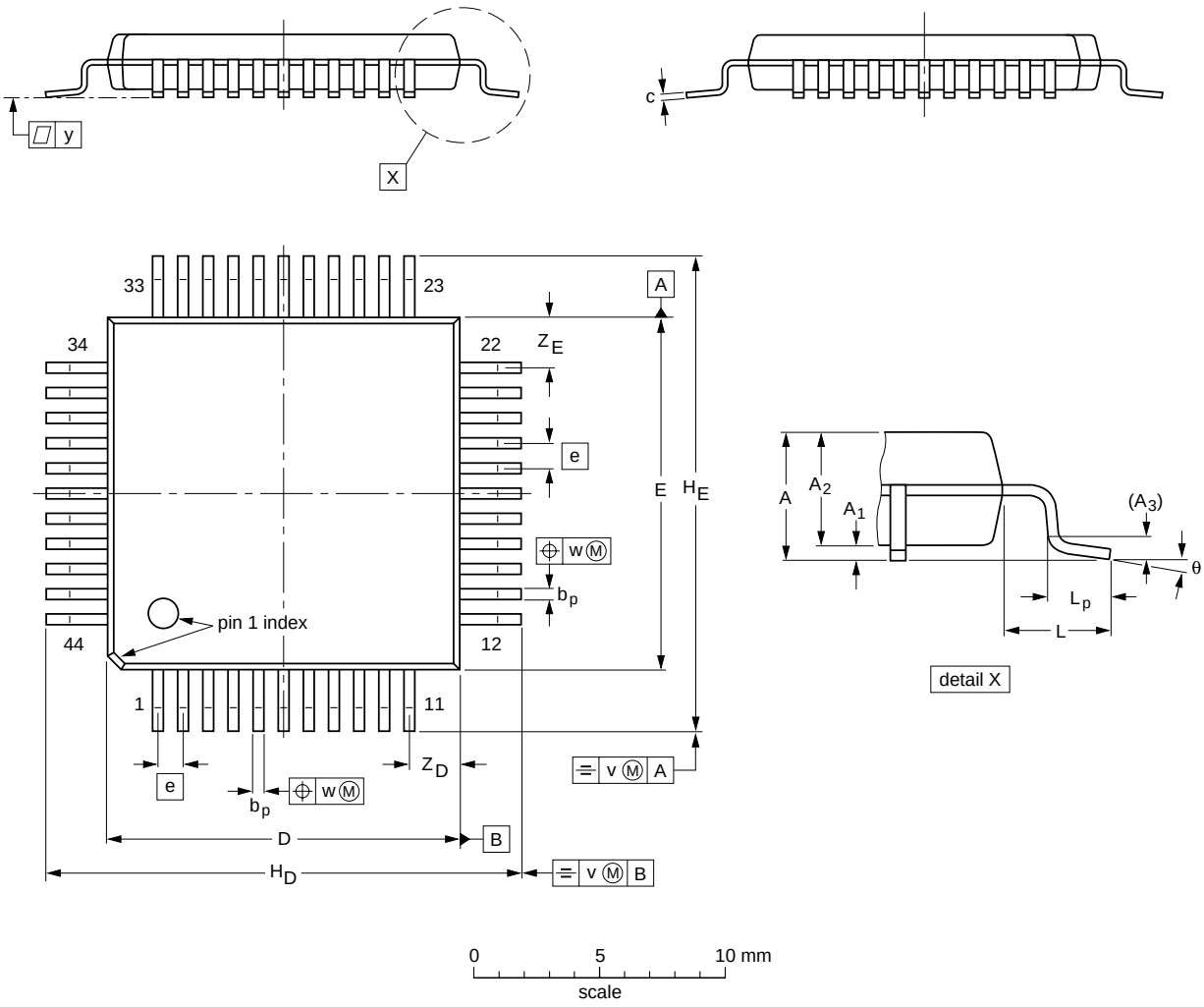
(1) TP1, TP2, TEST1 and TEST2 should be connected to V_{SS} during normal operation.

(2) Lx: ferrite bead, e.g. BLM 31A601S (Murata).

Fig.7 Application diagram.

13 PACKAGE OUTLINE

QFP44: plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 x 14 x 2.2 mm **SOT205-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.60	0.25 0.05	2.3 2.1	0.25	0.50 0.35	0.25 0.14	14.1 13.9	14.1 13.9	1	19.2 18.2	19.2 18.2	2.35	2.0 1.2	0.3	0.15	0.1	2.4 1.8	2.4 1.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT205-1	133E01					~~97-08-01~~ 99-12-27

14 SOLDERING

14.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

15 DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS (1)
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

16 DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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18 PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

NOTES

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