TDA9897; TDA9898

Multistandard hybrid IF processing

Rev. 03 — 11 January 2008 **Product data sheet**

1. General description

The Integrated Circuit (IC) is suitable for Intermediate Frequency (IF) processing including global multistandard Analog TV (ATV), Digital Video Broadcast (DVB) and mono FM radio using only 1 IC and 1 to 3 fixed Surface Acoustic Waves (SAWs) (application dependent). TDA9898 including L and L-accent standard. TDA9897 without L and L-accent standard.

2. Features

2.1 General

- 5 V supply voltage
- I^{2}C-bus control over all functions
- Four I^{2}C-bus addresses provided; selection by programmable Module Address (MAD)
- Three I^{2}C-bus voltage level supported; selection via pin BVS
- Separate gain controlled amplifiers with input selector and conversion for incoming IF [analog Vision IF (VIF) or Sound IF (SIF) or Digital TV (DTV)] allows the use of different filter shapes and bandwidths
- All conventional ATV standards applicable by using DTV bandwidth window [Band-Pass (BP)] filter
- Easy to use default settings for almost every standard provided, selectable via I^{2}C-bus
- Two 4 MHz reference frequency stages; the first one operates as crystal oscillator, the second one as external signal input
- Stabilizer circuit for ripple rejection and to achieve constant output signals
- Smallest size, simplest application
- ElectroStatic Discharge (ESD) protection for all pins

2.2 Analog TV processing

- Gain controlled wide-band VIF amplifier; AC-coupled
- Multistandard true synchronous demodulation with active carrier regeneration: very linear demodulation, good intermodulation figures, reduced harmonics and excellent pulse response
- Internal Nyquist slope processing; switch-off able for alternative use of inexpensive Nyquist slope SAW filter with additive video noise improvement
- Gated phase detector for L and L-accent standards
- Fully integrated VIF Voltage-Controlled Oscillator (VCO), alignment-free, frequencies switchable for all negative and positive modulated standards via I^{2}C-bus
- VIF Automatic Gain Control (AGC) detector for gain control; operating as a peak sync detector for negative modulated signals and as a peak white detector for positive modulated signals

founded by Philips

- Optimized AGC modes for negative modulation; e.g. very fast reaction time for VIF and SIF
- Precise fully digital Automatic Frequency Control (AFC) detector with 4-bit Digital-to-Analog Converter (DAC); AFC bits can be read-out via I^2C-bus
- High precise Tuner AGC (TAGC) TakeOver Point (TOP) for negative modulated standards; TOP adjust via I^2C-bus
- TAGC TOP for positive standards and Received Signal Strength Indication (RSSI); adjustable via I^2C-bus or alternatively by potentiometer
- Fully integrated Sound Carrier (SC) trap for any ATV standard (SC at 4.5 MHz, 5.5 MHz, 6.0 MHz and 6.5 MHz)
- SIF AGC for gain controlled SIF amplifier and high-performance single-reference Quasi Split Sound (QSS) mixer
- Fully integrated sound BP filter supporting any ATV standard
- Optional use of external FM sound BP filter
- AM sound demodulation for L and L-accent standard
- Alignment-free selective FM Phase-Locked Loop (PLL) demodulator with high linearity and low noise; external FM input
- VIF AGC voltage monitor output or port function
- VIF AFC current or tuner, SIF or FM AGC voltage monitor output
- 2nd SIF output, gain controlled by internal SIF AGC or by internal FM carrier AGC for Digital Signal Processor (DSP)
- Fully integrated BP filter for 2nd SIF at 4.5 MHz, 5.5 MHz, 6.0 MHz or 6.5 MHz

2.3 Digital TV processing

- Applicable for terrestrial and cable TV reception
- 70 dB variable gain wide-band IF amplifier (AC-coupled)
- Gain control via external control voltage (0 V to 3 V)
- 2 V (p-p) differential low IF (downconverted) output or 1 V (p-p) 1st IF output for direct Analog-to-Digital Converter (ADC) interfacing
- DVB downconversion with integrated selectivity for Low IF (LIF)/Zero IF (ZIF)
- Integrated anti-aliasing tracking low-pass filter
- Fully integrated synthesizer controlled oscillator with excellent phase noise performance
- Synthesizer frequencies for a wide range of world wide DVB standards (for IF center frequencies of 34.5 MHz, 36 MHz, 44 MHz and 57 MHz)
- All DVB bandwidth ranges supported (including ZIF I/Q)
- TAGC detector for independent tuner gain control loop applications
- TAGC operating as peak detector, fast reaction time due to additional speed-up detector
- Port function
- TAGC voltage monitor output

2.4 Dual mode

- Fully performed DTV processing and additional ATV video signal processing in parallel, but with reduced performance, for very fast channel scan
- VIF AGC voltage monitor output or port function
- VIF AFC current monitor output or TAGC voltage output

2.5 FM radio mode

- Gain controlled wide-band Radio IF (RIF) amplifier; AC-coupled
- Buffered RIF amplifier wide-band output, gain controlled by internal RIF AGC
- Fully integrated BP filter for 2nd RIF at 4.5 MHz, 5.5 MHz, 6.0 MHz, 6.5 MHz or 10.7 MHz
- 2nd RIF output, gain controlled by internal RIF AGC or by internal FM carrier AGC for DSP
- Alignment-free selective FM PLL demodulator with high linearity and low noise
- Precise fully digital AFC detector with 4-bit DAC; AFC bits read-out via I^2C-bus
- Port function
- Radio AFC current or tuner, RIF or FM AGC voltage monitor output

3. Applications

- Analog and digital TV front-end applications for TV sets, recording applications and personal computer cards

4. Quick reference data

Table 1. Quick reference data
V_P = 5 V; T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_P	supply voltage		[1]	4.5	5.0	5.5	V
I_P	supply current			-	-	190	mA
Analog TV signal processing							
Video part							
$V_{i(IF)(RMS)}$	RMS IF input voltage	lower limit at −1 dB video output signal		-	60	100	µV
$G_{VIF(cr)}$	control range VIF gain			60	66	-	dB
f_{VIF}	VIF frequency	see Table 25		-	-	-	MHz
$\Delta f_{VIF(dah)}$	digital acquisition help VIF frequency window	related to f_{VIF}					
		all standards except M/N		-	±2.3	-	MHz
		M/N standard		-	±1.8	-	MHz
$V_{o(video)(p-p)}$	peak-to-peak video output voltage	see Figure 10					
		positive or negative modulation; normal mode and sound carrier on	[2]	1.7	2.0	2.3	V
		trap bypass mode and sound carrier off	[3]	-	1.1	-	V

Table 1. Quick reference data *…continued*
V_P = 5 V; T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
G_{dif}	differential gain	*"ITU-T J.63 line 330"*	[2][4]				
		B/G standard		-	-	5	%
		L standard		-	-	7	%
φ_{dif}	differential phase	*"ITU-T J.63 line 330"*	[2][4]				
		B/G standard		-	2	4	deg
		L standard		-	2	4	deg
$B_{video(-3dB)}$	−3 dB video bandwidth	trap bypass mode and sound carrier off; AC load: C_L < 20 pF, R_L > 1 kΩ	[3]	6	8	-	MHz
α_{SC1}	first sound carrier attenuation	M/N standard; $f = f_{SC1}$ = 4.5 MHz; see Figure 21	[3]	38	-	-	dB
		B/G standard; $f = f_{SC1}$ = 5.5 MHz; see Figure 23	[3]	35	-	-	dB
$(S/N)_w$	weighted signal-to-noise ratio	normal mode and sound carrier on; B/G standard; 50 % grey video signal; unified weighting filter (*"ITU-T J.61"*); see Figure 20	[2][5]	53	57	-	dB
$PSRR_{CVBS}$	power supply ripple rejection on pin CVBS	normal mode and sound carrier on; f_{ripple} = 70 Hz; video signal; grey level; positive and negative modulation; see Figure 11	[2]	14	20	-	dB
$\Delta I_{AFC}/\Delta f_{VIF}$	change of AFC current with VIF frequency	AFC TV mode	[6]	0.85	1.05	1.25	μA/kHz
Audio part							
$V_{o(AF)(RMS)}$	RMS AF output voltage	FM: QSS mode; 27 kHz FM deviation; 50 μs de-emphasis		430	540	650	mV
		AM: 54 % modulation		400	500	600	mV
THD	total harmonic distortion	FM: 50 μs de-emphasis; FM deviation: for TV mode 27 kHz and for radio mode 22.5 kHz		-	0.15	0.50	%
		AM: 54 % modulation; BP on; see Figure 33		-	0.5	1.0	%
$f_{-3dB(AF)}$	AF cut-off frequency	W3[2] = 0; W3[4] = 0; without de-emphasis; FM window width = 237.5 kHz		80	100	-	kHz

Table 1. Quick reference data *...continued*
V_P = 5 V; T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$(S/N)_{w(AF)}$	AF weighted signal-to-noise ratio	*"ITU-R BS.468-4"*					
		FM: 27 kHz FM deviation; 50 μs de-emphasis; vision carrier unmodulated; FM PLL only		48	56	-	dB
		AM: BP off		44	50	-	dB
PSRR	power supply ripple rejection	f_{ripple} = 70 Hz; see Figure 11		14	20	-	dB
$V_{o(RMS)}$	RMS output voltage	IF intercarrier single-ended to GND; SC1 on; SC2 off		90	140	180	mV
		IF intercarrier single-ended to GND; L standard; without modulation; BP on; W7[5] = 0		45	70	90	mV
FM sound part							
$V_{i(FM)(RMS)}$	RMS FM input voltage	gain controlled operation; W1[1:0] = 10 or W1[1:0] = 11 or W1[1:0] = 01; see Figure 15		2	-	300	mV
$\Delta I_{AFC}/\Delta f_{RIF}$	change of AFC current with RIF frequency	AFC radio mode	[6]	0.85	1.05	1.25	μA/kHz
α_{AM}	AM suppression	referenced to 27 kHz FM deviation; 50 μs de-emphasis; AM: f = 1 kHz; m = 54 %		35	46	-	dB
Digital TV signal processing							
Digital direct IF							
$V_{o(dif)(p-p)}$	peak-to-peak differential output voltage	between pin OUT2A and pin OUT2B	[7]				
		W4[7] = 0		-	1.0	1.1	V
		W4[7] = 1		-	0.50	0.55	V
$G_{IF(max)}$	maximum IF gain	output peak-to-peak level to input RMS level ratio	[8]	-	83	-	dB
$G_{IF(cr)}$	control range IF gain		[8]	60	66	-	dB
PSRR	power supply ripple rejection	residual spurious at nominal differential output voltage dependent on power supply ripple	[8]				
		f_{ripple} = 70 Hz		-	60	-	dB
		f_{ripple} = 20 kHz		-	60	-	dB
Digital low IF							
$V_{o(dif)(p-p)}$	peak-to-peak differential output voltage	between pin OUT1A and pin OUT1B; W4[7] = 0	[7]	-	2	-	V
$G_{IF(max)}$	maximum IF gain	output peak-to-peak level to input RMS level ratio	[8]	-	89	-	dB
$G_{IF(cr)}$	control range IF gain		[8]	60	66	-	dB
f_{synth}	synthesizer frequency	see Table 35 and Table 36		-	-	-	MHz

Table 1. Quick reference data *...continued*

V_P = 5 V; T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$\varphi_{n(synth)}$	synthesizer phase noise	with 4 MHz crystal oscillator reference; f_{synth} = 31 MHz; f_{IF} = 36 MHz					
		at 1 kHz	[8]	89	99	-	dBc/Hz
		at 10 kHz	[8]	89	99	-	dBc/Hz
		at 100 kHz	[8]	98	102	-	dBc/Hz
		at 1.4 MHz	[8]	115	119	-	dBc/Hz
$\alpha_{ripple(pb)LIF}$	low IF pass-band ripple	6 MHz bandwidth		-	-	2.7	dB
		7 MHz bandwidth		-	-	2.7	dB
		8 MHz bandwidth		-	-	2.7	dB
α_{stpb}	stop-band attenuation	8 MHz band; f = 15.75 MHz		30	40	-	dB
α_{image}	image rejection	–10 MHz to 0 MHz; BP on		30	34	-	dB
C/N	carrier-to-noise ratio	at f_o = 4.9 MHz; $V_{i(IF)}$ = 10 mV (RMS); see Figure 37	[8][9][10]	112	118	-	dBc/Hz
Digital zero IF							
$V_{o(dif)(p-p)}$	peak-to-peak differential output voltage	between pin OUT1A and pin OUT1B or between pin OUT2A and pin OUT2B; W4[7] = 0	[7]	-	2	-	V
$G_{IF(max)}$	maximum IF gain	output peak-to-peak level to input RMS level ratio	[8]	-	89	-	dB
$G_{IF(cr)}$	control range IF gain		[8]	60	66	-	dB
f_{synth}	synthesizer frequency	see Table 35 and Table 36		-	-	-	MHz
$\varphi_{n(synth)}$	synthesizer phase noise	with 4 MHz crystal oscillator reference; f_{synth} = 31 MHz; f_{IF} = 36 MHz					
		at 1 kHz	[8]	89	99	-	dBc/Hz
		at 10 kHz	[8]	89	99	-	dBc/Hz
		at 100 kHz	[8]	98	102	-	dBc/Hz
		at 1.4 MHz	[8]	115	119	-	dBc/Hz
Reference frequency input from external source							
f_{ref}	reference frequency	W7[7] = 0	[11]	-	4	-	MHz
$V_{ref(RMS)}$	RMS reference voltage	W7[7] = 0; see Figure 34 and Figure 46		15	150	500	mV

[1] Values of video and sound parameters can be decreased at V_P = 4.5 V.

[2] AC load; C_L < 20 pF and R_L > 1 kΩ. The sound carrier frequencies (depending on TV standard) are attenuated by the integrated sound carrier traps.

[3] The sound carrier trap can be bypassed by setting the I2C-bus bit W2[0] to logic 0; see Table 24. In this way the full composite video spectrum appears at pin CVBS. The video amplitude is reduced to 1.1 V (p-p).

[4] Condition: luminance range (5 steps) from 0 % to 100 %. Measurement value is based on 4 of 5 steps.

[5] Measurement using 200 kHz high-pass filter, 5 MHz low-pass filter and subcarrier notch filter (*"ITU-T J.64"*).

[6] To match the AFC output signal to different tuning systems a current output is provided. The test circuit is given in Figure 19. The AFC steepness can be changed by resistors R1 and R2.

[7] With single-ended load for f_{IF} < 45 MHz $R_L \geq 1$ kΩ and $C_L \leq 5$ pF to ground and for f_{IF} = 45 MHz to 60 MHz $R_L = 1$ kΩ and $C_L \leq 3$ pF to ground.

[8] This parameter is not tested during production and is only given as application information.

[9] Noise level is measured without input signal but AGC adjusted corresponding to the given input level.

[10] Set with AGC nominal output voltage as reference. For C/N measurement switch input signal off.

[11] The tolerance of the reference frequency determines the accuracy of VIF AFC, RIF AFC, FM demodulator center frequency, maximum FM deviation, sound trap frequency, LIF band-pass cut-off frequency and ZIF low-pass cut-off frequency as well as the accuracy of the synthesizer.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDA9897HL/V2/S1	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
TDA9897HN/V2	HVQFN48	plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 × 7 × 0.85 mm	SOT619-1
TDA9898HL/V2/S1	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
TDA9898HN/V2	HVQFN48	plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 × 7 × 0.85 mm	SOT619-1

6. Block diagram

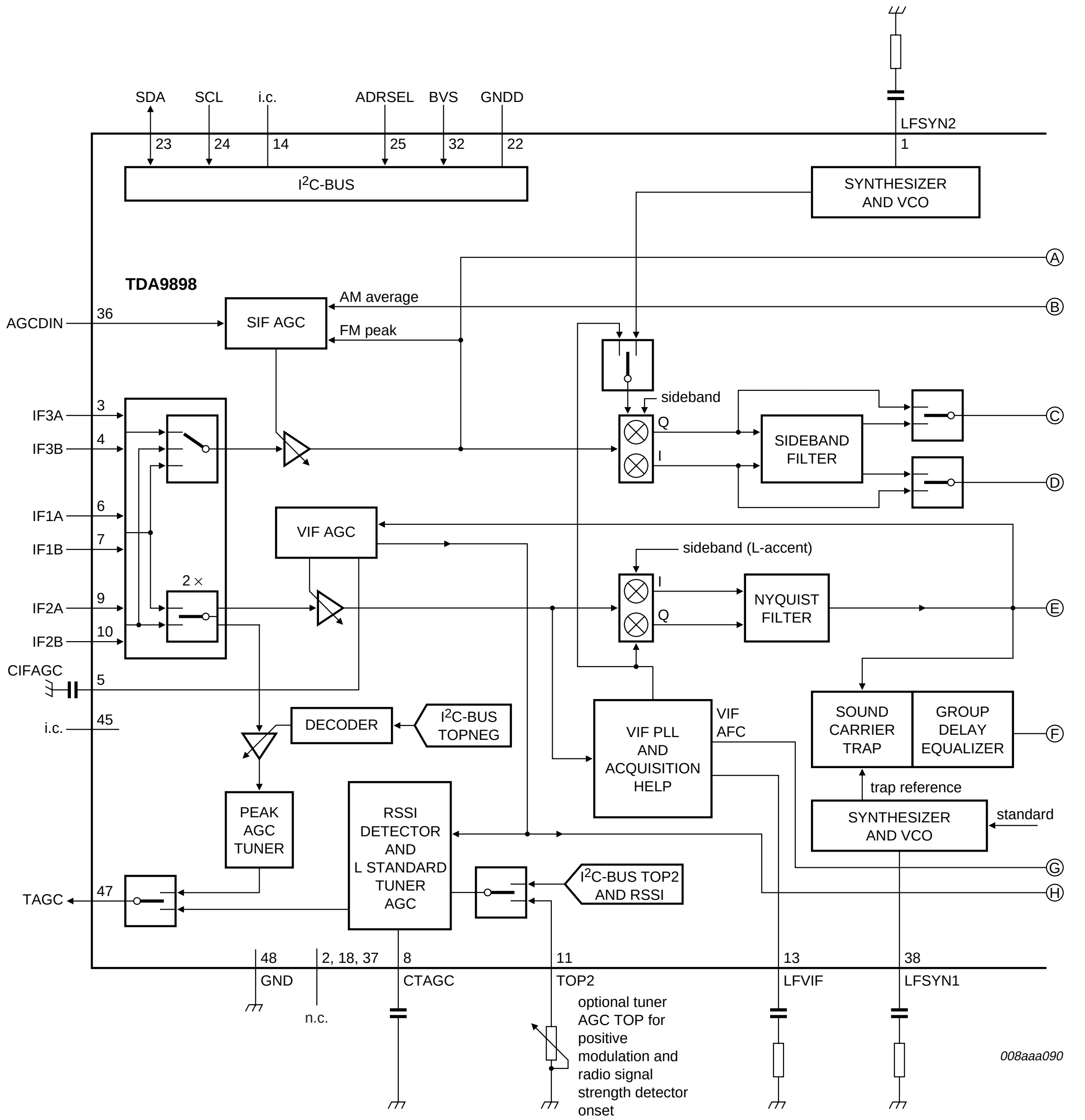
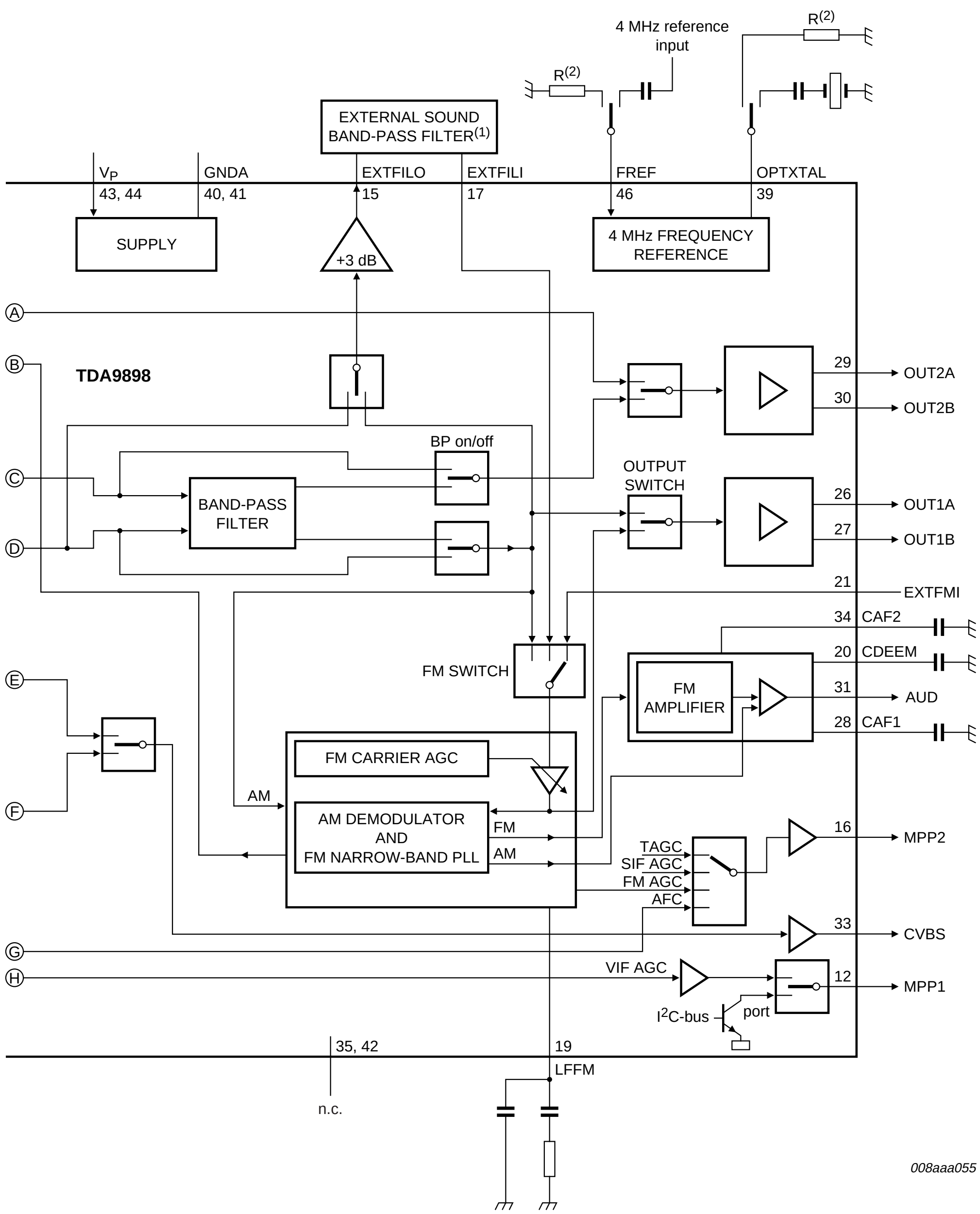


Fig 1. Block diagram of TDA9898 (continued in Figure 2)



(1) Optional.

(2) Connect resistor if input or crystal is not used.

Fig 2. Block diagram of TDA9898 (continued from Figure 1)

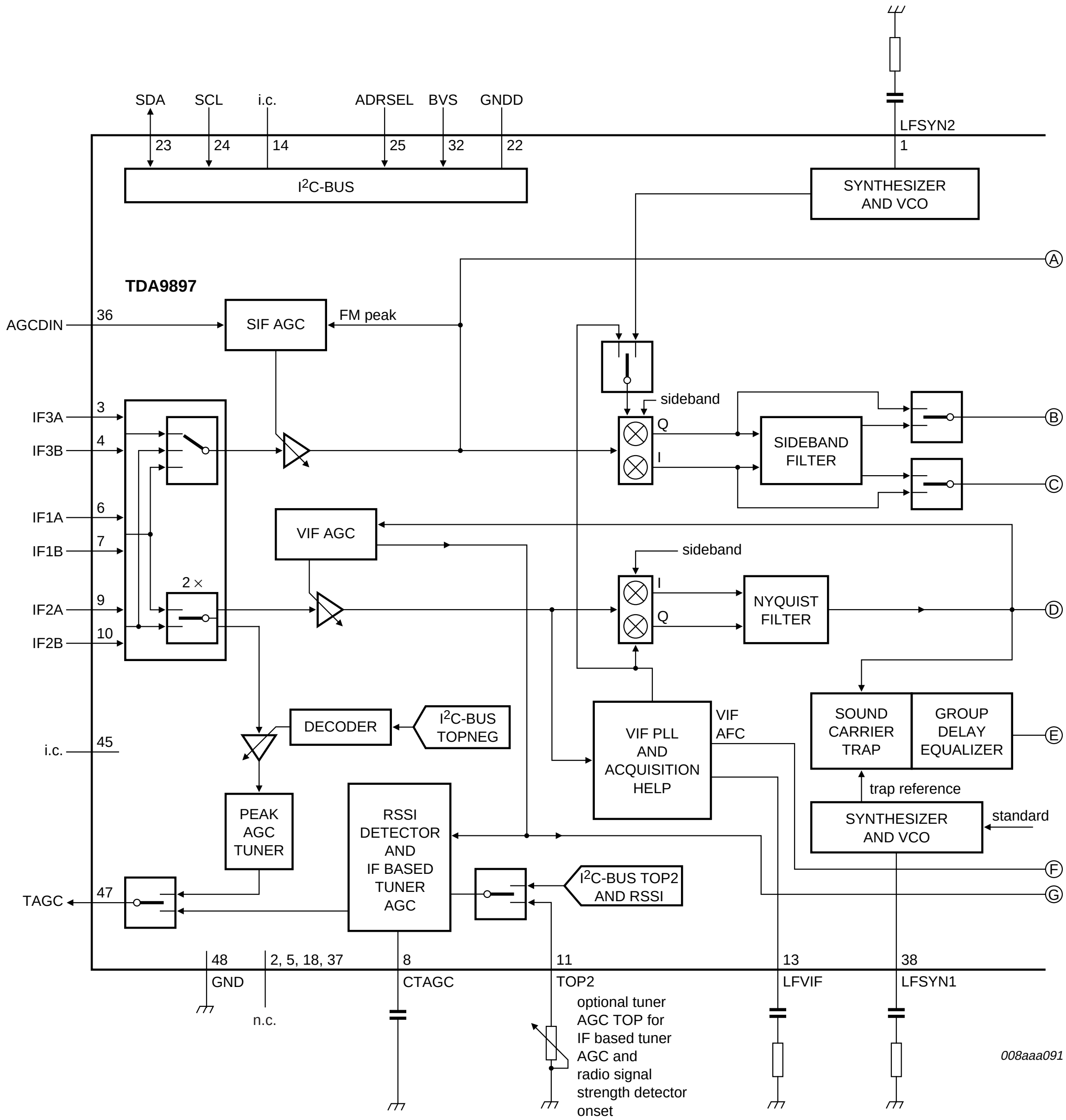
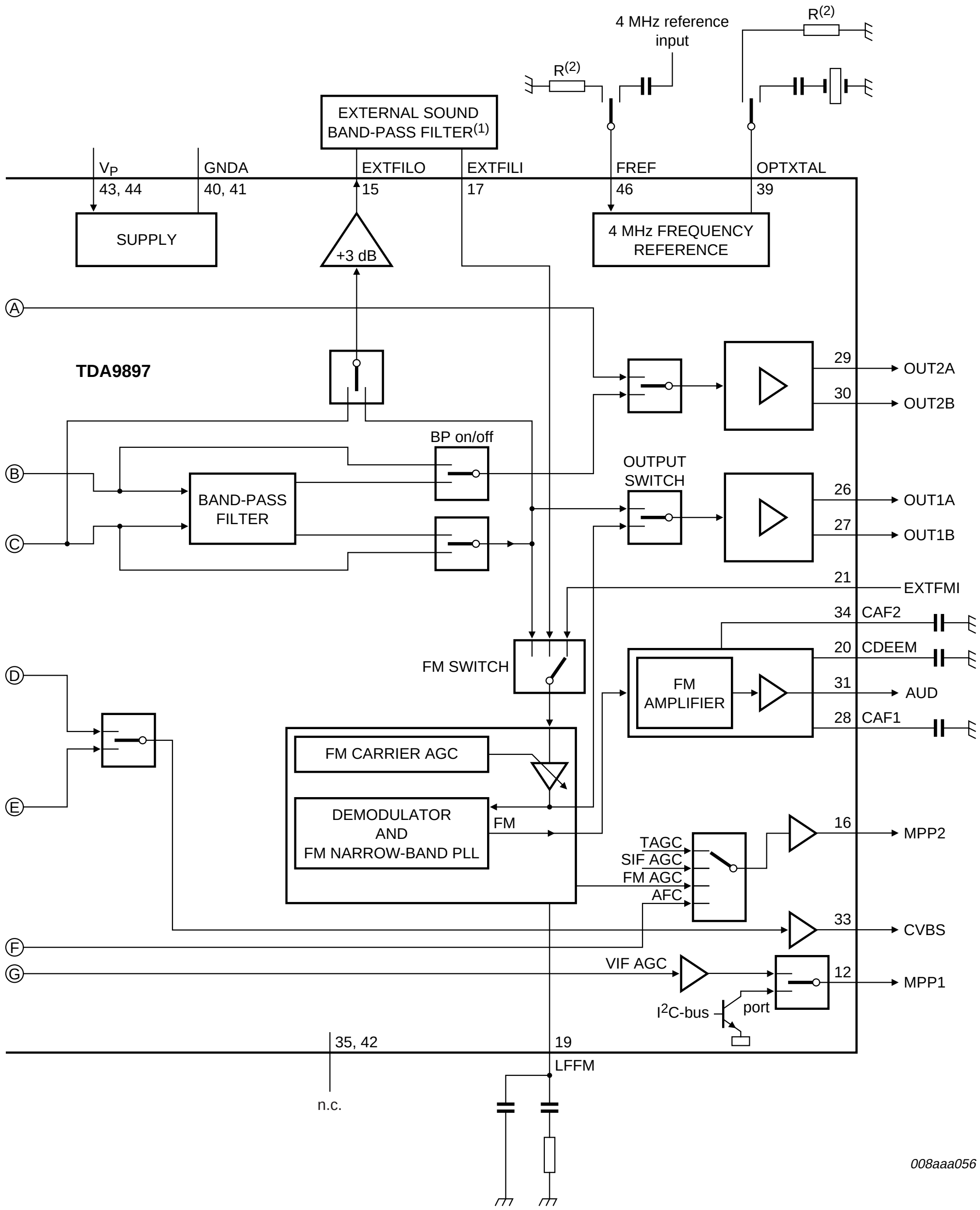


Fig 3. Block diagram of TDA9897 (continued in Figure 4)



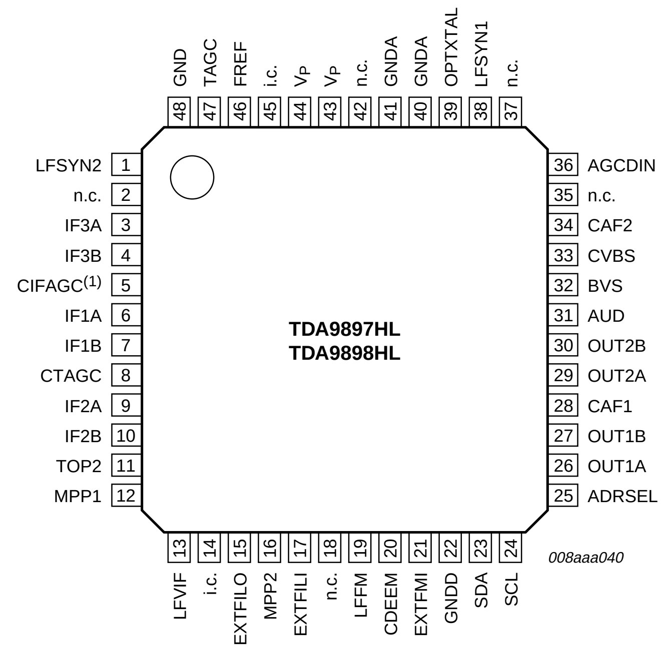
(1) Optional.

(2) Connect resistor if input or crystal is not used.

Fig 4. Block diagram of TDA9897 (continued from Figure 3)

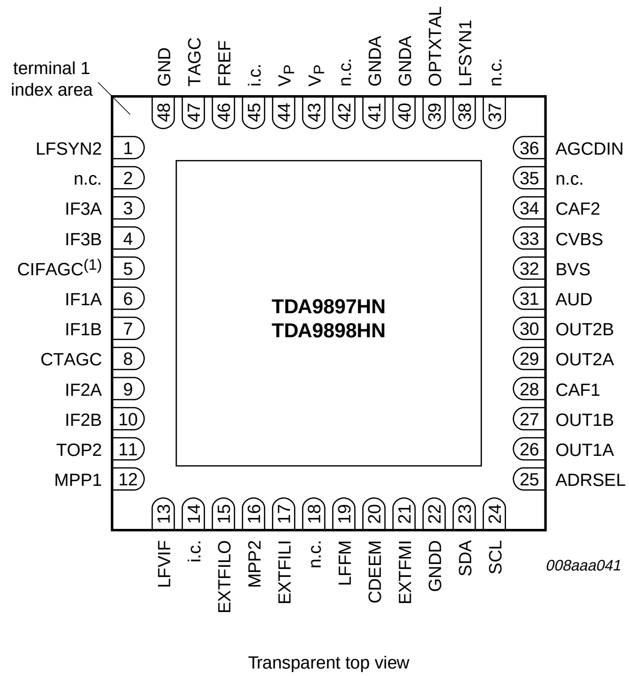
7. Pinning information

7.1 Pinning



(1) Not connected for TDA9897HL.

Fig 5. Pin configuration for LQFP48



(1) Not connected for TDA9897HN.

Fig 6. Pin configuration for HVQFN48

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
LFSYN2	1	loop filter synthesizer 2 (conversion synthesizer)
n.c.	2	not connected
IF3A	3	IF symmetrical input 3 for sound
IF3B	4	
CIFAGC	5	TDA9898: IF AGC capacitor; L standard
		TDA9897: not connected
IF1A	6	IF symmetrical input 1 for vision or digital
IF1B	7	
CTAGC	8	TAGC capacitor
IF2A	9	IF symmetrical input 2 for vision or digital
IF2B	10	
TOP2	11	TOP potentiometer for positive modulated standards and RSSI reference
MPP1	12	multipurpose pin 1: VIF AGC monitor output or port function
LFVIF	13	loop filter VIF PLL
i.c.	14	internally connected; connect to ground
EXTFILO	15	output to external filter

Table 3. Pin description *…continued*

Symbol	Pin	Description
MPP2	16	multipurpose pin 2: SIF AGC or FM AGC or TAGC or VIF AFC or FM AFC monitor output
EXTFILI	17	input from external filter
n.c.	18	not connected
LFFM	19	loop filter FM PLL
CDEEM	20	de-emphasis capacitor
EXTFMI	21	external FM input
GNDD	22	digital ground
SDA	23	I^2C-bus data input and output
SCL	24	I^2C-bus clock input
ADRSEL	25	address select
OUT1A	26	zero IF I or low IF or 2nd sound intercarrier symmetrical output
OUT1B	27	
CAF1	28	Direct Current (DC) decoupling capacitor 1
OUT2A	29	zero IF Q or 1st Digital IF (DIF) symmetrical output
OUT2B	30	
AUD	31	audio signal output
BVS	32	I^2C-bus voltage select
CVBS	33	composite video signal output
CAF2	34	DC decoupling capacitor 2
n.c.	35	not connected
AGCDIN	36	AGC input for DIF amplifier for e.g. input from channel decoder AGC
n.c.	37	not connected
LFSYN1	38	loop filter synthesizer 1 (filter control synthesizer)
OPTXTAL	39	optional quartz input
GNDA	40	analog ground
GNDA	41	analog ground
n.c.	42	not connected
V_P	43	supply voltage
V_P	44	supply voltage
i.c.	45	internally connected; connect to ground
FREF	46	4 MHz reference input
TAGC	47	TAGC output
GND	48	ground; plateau connection

8. Functional description

8.1 IF input switch

Different signal bandwidth can be handled by using two signal processing chains with individual gain control.

Switch configuration allows independent selection of filter for analog VIF and for analog SIF (used at same time) or DIF.

The switch takes into account correct signal selection for TAGC in the event of VIF and DIF signal processing.

8.2 VIF demodulator

ATV demodulation using 6 MHz DVB window (band-pass) filter (for 6 MHz, 7 MHz or 8 MHz channel width).

IF frequencies adapted to enable the use of different filter configurations. The Nyquist processing is integrated.

For optional use of standard Nyquist filter the integrated Nyquist processing can be switched off.

Sideband switch supplies selection of lower or upper sideband (e.g. for L-accent).

Equalizer provides optimum pulse response at different standards [e.g. to cope with higher demands for Liquid Crystal Display (LCD) TV].

Integrated sound traps.

Sound trap reference independent from received 2nd sound IF (reference taken from integrated reference synthesizer).

IF level selection provides an optimum adaptation of the demodulator to high linearity or low noise.

8.3 VIF AGC and tuner AGC

8.3.1 Mode selection of VIF AGC

Peak white AGC for positive modulation mode with adaptation for speed up and black level AGC (using proven system from TDA9886).

For negative modulation mode equal response times for increasing or decreasing input level (optimum for amplitude fading) **or** normal peak AGC **or** ultra fast peak AGC.

8.3.2 VIF AGC monitor

VIF AGC DC voltage monitor output (with expanded internal characteristic).

VIF AGC read out via I^2C-bus (for IF level indication) with zero-calibration via TOP setting (TOP setting either via I^2C-bus or via TOP potentiometer).

8.3.3 Tuner AGC

Independent integral tuner gain control loop (not nested with VIF AGC). Integral characteristic provides high control accuracy.

Accurate setting of tuner control onset (TOP) for integral tuner gain control loop via I^2C-bus.

For L standard, TAGC remains VIF AGC nested, as from field experience in the past this narrow-band TAGC gives best performance.

Thus two switchable TAGC systems for negative/DIF and positive modulation implemented.

L standard TAGC output changed from current output to voltage output, as it is not necessary to adapt for other than 5 V tuner.

L standard tuner time constant switching integrated (= speed up function in the event of step into high input levels), to minimize external application.

For high TOP accuracy at L standard, additional adjustment via optional potentiometer or I^2C-bus is provided.

Tuner AGC status bit provided. This function enables TOP alignment without need for TAGC voltage measurement (e.g. for TOP alignment in a complete set, where access to internal signals is not possible).

8.4 DIF/SIF FM and AM sound AGC

External AGC control input for DIF. DIF includes 1st IF, zero IF and low IF.

Integrated gain control loop for SIF.

Bandwidth of AGC control for FM SIF related to used SAW bandwidth.

Peak AGC control in the event of FM SIF.

Ultra fast SIF AGC time constant when VIF AGC set to ultra fast mode.

Slow average AGC control in the event of AM sound.

AM sound AGC related to AM sound carrier level.

Fast AM sound AGC in the event of fast VIF AGC (speed up).

SIF AGC DC voltage monitor output with expanded internal characteristic.

8.5 Frequency phase-locked loop for VIF

Basic function as previous TDA9887 design.

PLL gating mode for positive and negative modulation, optional.

PLL optimized for either overmodulation or strong multipath.

8.6 DIF/SIF converter stage

Frequency conversion with sideband suppression.

Selection mode of upper or lower sideband for pass or suppression.

Suppression around zero for frequency conversion.

I/Q output mode for zero IF conversion.

Conversion mode selection via synthesizer for DIF and radio mode or via VIF Frequency Phase-Locked Loop (FPLL) for TV QSS sound (FM/AM).

External BP filter (e.g. for 4.5 MHz) for additional filtering, optional.

Bypass mode selection for use of external filter.

Integrated SIF BP tracking filter for chroma suppression.

Integrated tracking filters for LIF and ZIF.

Symmetrical output stages for DIF, ZIF and 2nd SIF.

Second narrow-band gain control loop for 2nd SIF via FM PLL.

8.7 Mono sound demodulator

8.7.1 Narrow-band FM PLL demodulation

Additional external input for either TV or radio intercarrier signal.

FM carrier selection independent from VIF trap, because VIF trap uses reference via synthesizer.

FM wide and ultra wide mode with adapted loop bandwidth and different selectable FM acquisition window widths to cope with FM overmodulation conditions.

8.7.2 AM sound demodulation

Passive AM sound detector.

L and L-accent standard without SAW switching (done by sideband selection of SIF converter).

8.8 Audio amplifier

Different gain settings for FM sound to adapt to different FM deviation.

Switchable de-emphasis for FM sound.

Automatic mute function when FM PLL is unlocked.

Forced mute function.

Output amplifier for AM sound.

8.9 Synthesizer

In DIF mode, the synthesizer supports low and zero IF input frequencies for 34.5 MHz, 36 MHz, 44 MHz and 57 MHz center frequencies.

In radio mode, the synthesizer supports 2nd sound intercarrier conversion. A large set of synthesizer frequencies in steps of 0.5 MHz enables flexible combination of filter and 2nd IF frequencies.

Synthesizer loop internally adapted to divider ratio range for optimum phase noise requirement (loop bandwidth).

Synthesizer reference either via 4 MHz crystal or via an external source. Individual pins for crystal and external reference allows optimum interface definition and supports use of custom reference frequency offset.

8.10 I²C-bus transceiver and slave address

Four different I²C-bus device addresses to enable application with multi-IC use.

I²C-bus transceiver input ports can handle three different I²C-bus voltages.

Read-out functions as TDA9887 plus additional read out of VIF AGC and TAGC status.

Table 4. Slave address detection

Slave address	Selectable address bit		Pin ADRSEL
	A3	A0	
MAD1	0	1	GND
MAD2	0	0	V_P
MAD3	1	1	resistor to GND
MAD4	1	0	resistor to V_P

9. I²C-bus control

Table 5. Slave addresses[1]

Slave address		Bit						
Name	Value	A6	A5	A4	A3	A2	A1	A0
MAD1	43h	1	0	0	0	0	1	1
MAD2	42h	1	0	0	0	0	1	0
MAD3	4Bh	1	0	0	1	0	1	1
MAD4	4Ah	1	0	0	1	0	1	0

[1] For MAD activation via pin ADRSEL: see Table 4.

9.1 Read format

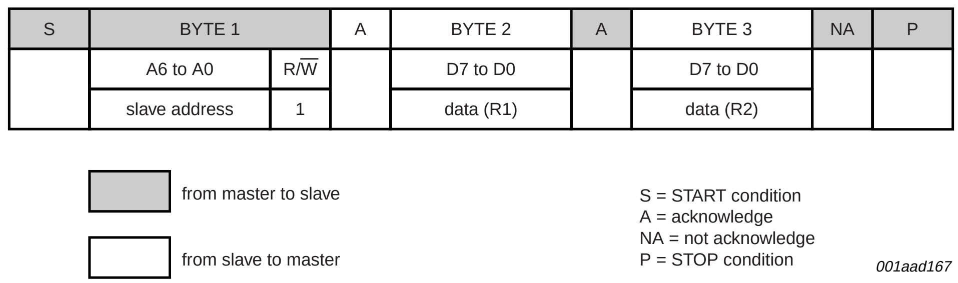


Fig 7. I^2C-bus read format (slave transmits data)

Table 6. R1 - data read register 1 bit allocation

7	6	5	4	3	2	1	0
AFCWIN	reserved	CARRDET	AFC4	AFC3	AFC2	AFC1	PONR

Table 7. R1 - data read register 1 bit description

Bit	Symbol	Description
7	AFCWIN	AFC window[1]
		1 = VCO in ±1.6 MHz AFC window[2]
		1 = VCO in ±0.8 MHz AFC window[3]
		0 = VCO out of ±1.6 MHz AFC window[2]
		0 = VCO out of ±0.8 MHz AFC window[3]
6	-	reserved
5	CARRDET	FM carrier detection[4]
		1 = detection (FM PLL is locked and level is less than 6 dB below gain controlled range of FM AGC)
		0 = no detection
4 to 1	AFC[4:1]	automatic frequency control; see Table 8
0	PONR	power-on reset
		1 = after power-on reset or after supply breakdown
		0 = after a successful reading of the status register

[1] If no IF input is applied, then bit AFCWIN can be logic 1 due to the fact that the VCO is forced to the AFC window border for fast lock-in behavior.

[2] All standards except M/N standard.

[3] M/N standard.

[4] Typical time constant of FM carrier detection is 50 ms. The minimal recommended wait time for read out is 80 ms.

Table 8. Automatic frequency control bits[1]

Bit				f[2]
AFC4	AFC3	AFC2	AFC1	
R1[4]	R1[3]	R1[2]	R1[1]	
0	1	1	1	≤ (f_{nom} – 187.5 kHz)
0	1	1	0	f_{nom} – 162.5 kHz
0	1	0	1	f_{nom} – 137.5 kHz
0	1	0	0	f_{nom} – 112.5 kHz
0	0	1	1	f_{nom} – 87.5 kHz
0	0	1	0	f_{nom} – 62.5 kHz
0	0	0	1	f_{nom} – 37.5 kHz
0	0	0	0	f_{nom} – 12.5 kHz
1	1	1	1	f_{nom} + 12.5 kHz
1	1	1	0	f_{nom} + 37.5 kHz
1	1	0	1	f_{nom} + 62.5 kHz
1	1	0	0	f_{nom} + 87.5 kHz
1	0	1	1	f_{nom} + 112.5 kHz
1	0	1	0	f_{nom} + 137.5 kHz
1	0	0	1	f_{nom} + 162.5 kHz
1	0	0	0	≥ (f_{nom} + 187.5 kHz)

[1] f_{nom} is the nominal frequency.

[2] In ATV mode f means vision intermediate frequency; in radio mode f means radio intermediate frequency.

Table 9. R2 - data read register 2 bit allocation

7	6	5	4	3	2	1	0
reserved	TAGC	VAGC5	VAGC4	VAGC3	VAGC2	VAGC1	VAGC0

Table 10. R2 - data read register 2 bit description

Bit	Symbol	Description
7	-	reserved
6	TAGC	tuner AGC
		1 = active
		0 = inactive
5 to 0	VAGC[5:0]	AGC level detector; VIF AGC in ATV mode, SIF AGC in radio mode and DIF AGC in DTV mode; see Table 11

Table 11. AGC bits (for corresponding AGC characteristic see Figure 12)

Bit						Typical $\Delta V_{AGC(VIF)}$ (V)
VAGC5	VAGC4	VAGC3	VAGC2	VAGC1	VAGC0	
R2[5]	R2[4]	R2[3]	R2[2]	R2[1]	R2[0]	
1	1	1	1	1	1	0 (TOP)[1]
1	1	1	1	1	0	–0.04
1	1	1	1	0	1	–0.08
1	1	1	1	0	0	–0.12
1	1	1	0	1	1	–0.16
1	1	1	0	1	0	–0.20
1	1	1	0	0	1	–0.24
1	1	1	0	0	0	–0.28
1	1	0	1	1	1	–0.32
1	1	0	1	1	0	–0.36
1	1	0	1	0	1	–0.40
1	1	0	1	0	0	–0.44
1	1	0	0	1	1	–0.48
1	1	0	0	1	0	–0.52
1	1	0	0	0	1	–0.56
1	1	0	0	0	0	–0.60
1	0	1	1	1	1	–0.64
1	0	1	1	1	0	–0.68
1	0	1	1	0	1	–0.72
1	0	1	1	0	0	–0.76
1	0	1	0	1	1	–0.80
1	0	1	0	1	0	–0.84
1	0	1	0	0	1	–0.88
1	0	1	0	0	0	–0.92
1	0	0	1	1	1	–0.96
1	0	0	1	1	0	–1.00
1	0	0	1	0	1	–1.04
1	0	0	1	0	0	–1.08
1	0	0	0	1	1	–1.12
1	0	0	0	1	0	–1.16
1	0	0	0	0	1	–1.20
1	0	0	0	0	0	–1.24
0	1	1	1	1	1	–1.28
0	1	1	1	1	0	–1.32
0	1	1	1	0	1	–1.36
0	1	1	1	0	0	–1.40
0	1	1	0	1	1	–1.44
0	1	1	0	1	0	–1.48
0	1	1	0	0	1	–1.52

Table 11. AGC bits (for corresponding AGC characteristic see Figure 12) *...continued*

Bit						Typical $\Delta V_{AGC(VIF)}$ (V)
VAGC5	VAGC4	VAGC3	VAGC2	VAGC1	VAGC0	
R2[5]	R2[4]	R2[3]	R2[2]	R2[1]	R2[0]	
0	1	1	0	0	0	–1.56
0	1	0	1	1	1	–1.60
0	1	0	1	1	0	–1.64
0	1	0	1	0	1	–1.68
0	1	0	1	0	0	–1.72
0	1	0	0	1	1	–1.76
0	1	0	0	1	0	–1.80
0	1	0	0	0	1	–1.84
0	1	0	0	0	0	–1.88
0	0	1	1	1	1	–1.92
0	0	1	1	1	0	–1.96
0	0	1	1	0	1	–2.00
0	0	1	1	0	0	–2.04
0	0	1	0	1	1	–2.08
0	0	1	0	1	0	–2.12
0	0	1	0	0	1	–2.16
0	0	1	0	0	0	–2.20
0	0	0	1	1	1	–2.24
0	0	0	1	1	0	–2.28
0	0	0	1	0	1	–2.32
0	0	0	1	0	0	–2.36
0	0	0	0	1	1	–2.40
0	0	0	0	1	0	–2.44
0	0	0	0	0	1	–2.48
0	0	0	0	0	0	–2.52

[1] The reference of 0 (TOP) can be adjusted via TOPPOS[4:0] (register W10; see Table 49 and Table 47) or via potentiometer at pin TOP2.

9.2 Write format

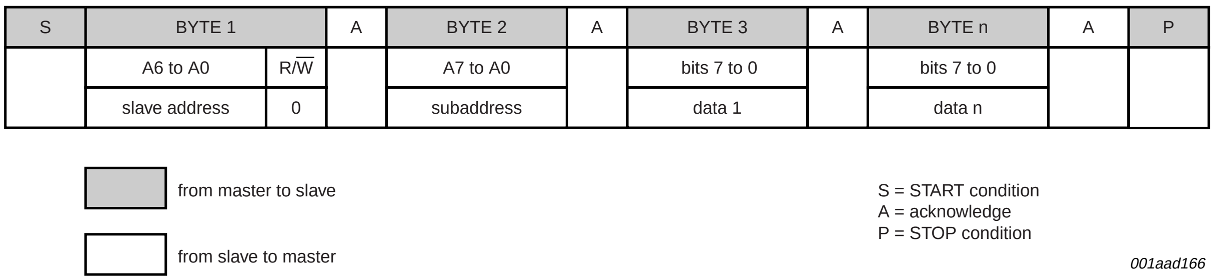


Fig 8. I²C-bus write format (slave receives data)

9.2.1 Subaddress

Table 12. W0 - subaddress register bit allocation

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

Table 13. W0 - subaddress register bit description

Bit	Symbol	Description
7 to 4	A[7:4]	has to be set to logic 0
3 to 0	A[3:0]	subaddress; see Table 14

Table 14. Subaddress control bits

Bit				Mode
A3	A2	A1	A0	
0	0	0	0	subaddress for register W1
0	0	0	1	subaddress for register W2
0	0	1	0	subaddress for register W3
0	0	1	1	subaddress for register W4
0	1	0	0	subaddress for register W5
0	1	0	1	subaddress for register W6
0	1	1	0	subaddress for register W7
0	1	1	1	subaddress for register W8
1	0	0	0	subaddress for register W9
1	0	0	1	subaddress for register W10

Table 15. I^2C-bus write register overview[1]

Register	7	6	5	4	3	2	1	0
W1[2]	RADIO	STD1	STD0	TV2	TV1	DUAL	FM	EXTFIL
W2[3]	MOD	STD4	STD3	STD2	SB	PLL	GATE	TRAP
W3[4]	RESCAR	AMUTE	FMUTE	FMWIDE0	DEEMT	DEEM	AGAIN1	AGAIN0
W4[5]	VIFLEVEL	BP	MPP2S1	MPP2S0	0	IFIN1	IFIN0	VIFIN
W5[6]	FSFREQ1	FSFREQ0	SFREQ5	SFREQ4	SFREQ3	SFREQ2	SFREQ1	SFREQ0
W6[7]	TAGC1	TAGC0	AGC2	AGC1	FMWIDE1	TWOFLO	0	DIRECT
W7[8]	0	0	SIFLEVEL	VIDLEVEL	OPSTATE	PORT	FILOUTBP	NYQOFF
W8[9]	0	0	0	0	EASY3	EASY2	EASY1	EASY0
W9[10]	DAGCSLOPE	TAGCIS	TAGCTC	TOPNEG4	TOPNEG3	TOPNEG2	TOPNEG1	TOPNEG0
W10[11]	0	0	XPOTPOS	TOPPOS4	TOPPOS3	TOPPOS2	TOPPOS1	TOPPOS0

[1] The register setting after power-on is not specified.

[2] See Table 17 for detailed description of W1.

[3] See Table 24 for detailed description of W2.

[4] See Table 28 for detailed description of W3.

[5] See Table 30 for detailed description of W4.

[6] See Table 34 for detailed description of W5.

[7] See Table 38 for detailed description of W6.

[8] See Table 41 for detailed description of W7.

[9] See Table 43 for detailed description of W8.

[10] See Table 46 for detailed description of W9.

[11] See Table 49 for detailed description of W10.

9.2.2 Description of data bytes

Table 16. W1 - data write register bit allocation

7	6	5	4	3	2	1	0
RADIO	STD1	STD0	TV2	TV1	DUAL	FM	EXTFIL

Table 17. W1 - data write register bit description

Bit	Symbol	Description
7	RADIO	FM mode
		1 = radio
		0 = ATV/DTV
6 and 5	STD[1:0]	2nd sound IF; see Table 18 and Table 19
4 and 3	TV[2:1]	TV mode
		00 = DTV and ZIF
		01 = DTV and LIF
		10 = not defined
		11 = ATV and QSS
2	DUAL	ATV and DTV dual mode for channel search; see Table 22
		1 = dual (TV2 = 0)
		0 = normal
1 and 0	FM and EXTFIL	FM and output switching; see Table 21

Table 18. Intercarrier sound BP and FM PLL frequency select for ATV, QSS mode[1]

Bit							f_{FMPLL} (MHz)	Sound BP
RADIO	MOD	STD1	STD0	FSFREQ1	FSFREQ0	TV1		
W1[7]	W2[7]	W1[6]	W1[5]	W5[7]	W5[6]	W1[3]		
0	1	0	0	X	X	1	4.5	M/N standard
0	1	0	1	X	X	1	5.5	B/G standard
0	1	1	0	X	X	1	6.0	I standard
0	1	1	1	X	X	1	6.5	D/K standard
0	0	1	1	X	X	1	off	L/L-accent standard

[1] For description of bit MOD refer to Table 24 and bits FSFREQ[1:0] are described in Table 34.

Table 19. Intercarrier sound BP and FM PLL frequency select for radio, QSS mode[1]

Bit							f_{FMPLL} (MHz)	Sound BP
RADIO	MOD	STD1	STD0	FSFREQ1	FSFREQ0	TV1		
W1[7]	W2[7]	W1[6]	W1[5]	W5[7]	W5[6]	W1[3]		
1	1	X	X	0	0	0	4.5	M/N standard
1	1	X	X	0	1	0	5.5	B/G standard
1	1	X	X	1	0	0	6.0	I standard
1	1	X	X	1	1	0	6.5	D/K standard
1	0	X	X	X	X	0	10.7	RADIO

[1] For description of bit MOD refer to Table 24 and bits FSFREQ[1:0] are described in Table 34.

Table 20. Second sound IF selection for 10.7 MHz[1]

Bit			f_{FMPLL} (MHz)
BP	MOD	RADIO	
W4[6]	W2[7]	W1[7]	
0	0	1	10.7

[1] For description of bit MOD refer to Table 24 and for BP refer to Table 30.

Table 21. 2nd intercarrier and sound input and output switching

MOD	FM	EXTFIL	Mode	Input signal selection (input switch)	Signal at OUT1A and OUT1B (output switch)	Mono sound demodulation
W2[7]	W1[1]	W1[0]				
1	0	0	FM sound	internal	internal BP via FM AGC	internal BP
1	0	1	FM sound	EXTFILI	internal BP	external BP
1	1	0	FM sound	EXTFMI	internal BP	external input
1	1	1	FM sound	EXTFILI	external BP via FM AGC	external BP
0	0	0	AM sound	not used		
0	0	1	AM sound	-	internal BP	internal BP
0	1	0	AM sound	-	internal BP	internal BP
0	1	1	AM sound	EXTFILI	external BP	internal BP

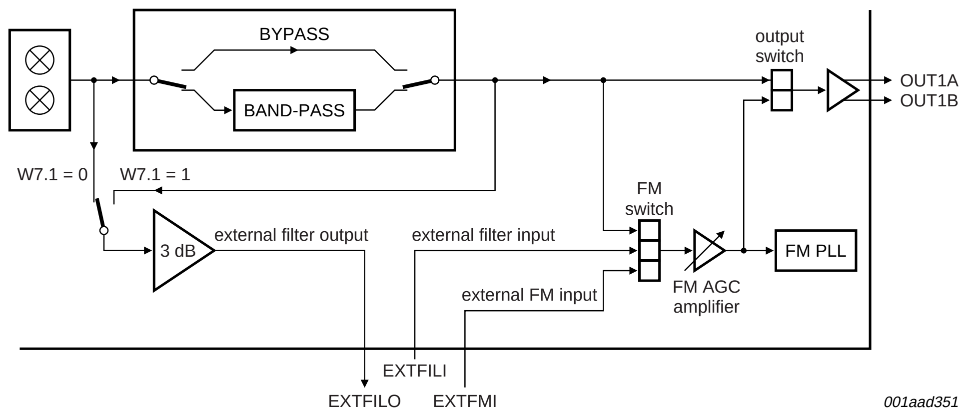


Fig 9. Signal path for intercarrier (2nd SIF) processing

Table 22. Dual mode options

Bit				Output mode
TV2	**TV1**	**DIRECT**	**DUAL**	
W1[4]	**W1[3]**	**W6[0]**	**W1[2]**	
X	X	X	0	all normal mode functions (ATV **OR** DTV)
0	X	1	1	analog CVBS at pin CVBS **AND** direct 1st DIF at pins OUT2A and OUT2B
0	0	0	1	analog CVBS at pin CVBS **AND** digital zero IF I/Q at pins OUT1A, OUT1B and OUT2A, OUT2B
0	1	0	1	analog CVBS at pin CVBS **AND** digital low IF at pins OUT1A and OUT1B

Table 23. W2 - data write register bit allocation

7	6	5	4	3	2	1	0
MOD	STD4	STD3	STD2	SB	PLL	GATE	TRAP

Table 24. W2 - data write register bit description

Bit	Symbol	Description
7	MOD	modulation
		1 = negative; FM mono sound at ATV and dual mode
		0 = positive; AM mono sound at ATV and dual mode
6 to 4	STD[4:2]	vision IF; see Table 25
3	SB	sideband for sound IF and digital low IF
		1 = upper
		0 = lower
2	PLL	operating modes; see Table 26
1	GATE	PLL gating
		1 = on
		0 = off
0	TRAP	sound trap
		1 = on
		0 = bypass

Table 25. Vision IF

Bit					f_{VIF} (MHz)	Sideband
NYQOFF	MOD	STD4	STD3	STD2	TV1 = 1 (QSS)	
W7[0]	W2[7]	W2[6]	W2[5]	W2[4]		
X	0	0	0	0	38.0	low
X	0	0	0	1	38.375	low
X	0	0	1	0	38.875	low
X	0	0	1	1	39.875	low
X	0	1	0	0	32.25	high
0	0	1	0	1	32.625	high
1	0	1	0	1	33.9	-
X	0	1	1	0	33.125	high
X	0	1	1	1	33.625	high
X	1	0	0	0	38.0	low
X	1	0	0	1	38.375	low
X	1	0	1	0	38.875	low
X	1	0	1	1	39.875	low
X	1	1	0	0	45.75	low
X	1	1	0	1	58.75	low
X	1	1	1	0	46.25	low
X	1	1	1	1	59.25	low

Table 26. VIF PLL gating and detector mode

Bit		Gating and detector mode
MOD	PLL	
W2[7]	W2[2]	
0	0	0 % gating in positive modulation mode (W2[1] = 1)
0	1	36 % gating in positive modulation mode (W2[1] = 1)
1	0	π mode on; optimized for overmodulation in negative modulation mode; f_{PC} = 0 kHz ± 187.5 kHz
1	1	π mode off; optimized for multipath in negative modulation mode; f_{PC} = 0 kHz ± 187.5 kHz

Table 27. W3 - data write register bit allocation

7	6	5	4	3	2	1	0
RESCAR	AMUTE	FMUTE	FMWIDE0	DEEMT	DEEM	AGAIN1	AGAIN0

Table 28. W3 - data write register bit description

Bit	Symbol	Description
7	RESCAR	video gain correction for residual carrier
		1 = 20 % residual carrier
		0 = 10 % residual carrier
6	AMUTE	auto mute
		1 = on
		0 = off
5	FMUTE	forced mute
		1 = on
		0 = off
4	FMWIDE0	FM window (W6[3] = 0)
		1 = 475 kHz; normal FM phase detector steepness
		0 = 237.5 kHz; high FM phase detector steepness
3	DEEMT	de-emphasis time
		1 = 50 μs
		0 = 75 μs
2	DEEM	de-emphasis
		1 = on
		0 = off
1 and 0	AGAIN[1:0]	audio gain
		00 = 0 dB
		01 = –6 dB
		10 = –12 dB (only for FM mode)
		11 = –18 dB (only for FM mode)

Table 29. W4 - data write register bit allocation

7	6	5	4	3	2	1	0
VIFLEVEL	BP	MPP2S1	MPP2S0	0	IFIN1	IFIN0	VIFIN

Table 30. W4 - data write register bit description

Bit	Symbol	Description
7	VIFLEVEL	control of internal VIF mixer input level (W1[4] = 1) and OUT1/OUT2 output level; see Table 31
		1 = reduced
		0 = normal
6	BP	SIF/DIF BP
		1 = on (bit W6[0] = 0; see Table 38)
		0 = bypass
5 and 4	MPP2S[1:0]	AGC or AFC output; see Table 32
3	-	0 = fixed value
2 and 1	IFIN[1:0]	DIF/SIF input
		00 = IF1A/B input
		01 = IF3A/B input
		10 = not used
		11 = IF2A/B input
0	VIFIN	VIF input
		1 = IF1A/B input
		0 = IF2A/B input

Table 31. List of output signals at OUT1 and OUT2

Bit					Output signal at	
TV2	TV1	DIRECT	FM	EXTFIL	OUT1A, OUT1B	OUT2A, OUT2B
W1[4]	W1[3]	W6[0]	W1[1]	W1[0]		
0	0	0	X	X	zero IF I	zero IF Q
0	1	0	X	X	low IF	off
0	X	1	X	X	off	direct IF
1	X	X	0	0	intercarrier[1]	off
1	X	X	0	1	intercarrier[2]	off
1	X	X	1	0	intercarrier[2]	off
1	X	X	1	1	intercarrier[1]	off

[1] Intercarrier output level based on wide-band AGC of SIF amplifier.

[2] Intercarrier output level based on narrow-band AGC of FM amplifier.

Table 32. Output mode at pin MPP2 for ATV; dual or radio mode

Bit			Pin MPP2 output mode
RADIO	MPP2S1	MPP2S0	
W1[7]	W4[5]	W4[4]	
X	0	0	gain control voltage of FM PLL
X	0	1	gain control voltage of SIF amplifier
X	1	0	TAGC monitor voltage
0	1	1	AFC current output, VIF PLL
1	1	1	AFC current output, radio mode

Table 33. W5 - data write register bit allocation

7	6	5	4	3	2	1	0
FSFREQ1	FSFREQ0	SFREQ5	SFREQ4	SFREQ3	SFREQ2	SFREQ1	SFREQ0

Table 34. W5 - data write register bit description[1]

Bit	Symbol	Description
7 and 6	FSFREQ[1:0]	DTV filter or sound trap selection for video
		ATV; sound trap; TV2 = 1
		00 = M/N standard (4.5 MHz)
		01 = B/G standard (5.5 MHz)
		10 = I standard (6.0 MHz)
		11 = D/K and L/L-accent standard (6.5 MHz)
		DTV (zero IF); low-pass cut-off frequency; TV2 = 0 and TV1 = 0
		00 = 3.0 MHz
		01 = 3.5 MHz
		10 = 4.0 MHz
		11 = not used
		DTV (low IF); upper BP cut-off frequency; TV2 = 0 and TV1 = 1
		00 = 7.0 MHz
		01 = 8.0 MHz
		10 = 9.0 MHz
		11 = not used
5 to 0	SFREQ[5:0]	synthesizer frequencies; see Table 35 and Table 36

[1] For bit description of TV1 and TV2 see Table 16 W1[3] and W1[4] and Table 17.

Table 35. DIF/SIF synthesizer frequencies (using bit TWOFLO = 0)

Bit						f_{synth} (MHz)
SFREQ5	SFREQ4	SFREQ3	SFREQ2	SFREQ1	SFREQ0	
W5[5]	W5[4]	W5[3]	W5[2]	W5[1]	W5[0]	
1	1	1	1	1	1	22.0
1	1	1	1	1	0	22.5
1	1	1	1	0	1	23.0
1	1	1	1	0	0	23.5
1	1	1	0	1	1	24.0
1	1	1	0	1	0	24.5
1	1	1	0	0	1	25.0
1	1	1	0	0	0	25.5
1	1	0	1	1	1	26.0
1	1	0	1	1	0	26.5
1	1	0	1	0	1	27.0
1	1	0	1	0	0	27.5
1	1	0	0	1	1	28.0
1	1	0	0	1	0	28.5
1	1	0	0	0	1	29.0
1	1	0	0	0	0	29.5
1	0	1	1	1	1	30.0
1	0	1	1	1	0	30.5
1	0	1	1	0	1	31.0
1	0	1	1	0	0	31.5
1	0	1	0	1	1	32.0
1	0	1	0	1	0	32.5
1	0	1	0	0	1	33.0
1	0	1	0	0	0	33.5
1	0	0	1	1	1	34.0
1	0	0	1	1	0	34.5
1	0	0	1	0	1	35.0
1	0	0	1	0	0	35.5
1	0	0	0	1	1	36.0
1	0	0	0	1	0	36.5
1	0	0	0	0	1	37.0
1	0	0	0	0	0	37.5
0	1	1	1	1	1	38.0
0	1	1	1	1	0	38.5
0	1	1	1	0	1	39.0
0	1	1	1	0	0	39.5
0	1	1	0	1	1	40.0
0	1	1	0	1	0	40.5
0	1	1	0	0	1	41.0

Table 35. DIF/SIF synthesizer frequencies (using bit TWOFLO = 0) *…continued*

Bit						f_{synth} (MHz)
SFREQ5	SFREQ4	SFREQ3	SFREQ2	SFREQ1	SFREQ0	
W5[5]	W5[4]	W5[3]	W5[2]	W5[1]	W5[0]	
0	1	1	0	0	0	41.5
0	1	0	1	1	1	42.0
0	1	0	1	1	0	42.5
0	1	0	1	0	1	43.0
0	1	0	1	0	0	43.5
0	1	0	0	1	1	44.0
0	1	0	0	1	0	44.5
0	1	0	0	0	1	45.0
0	1	0	0	0	0	45.5
0	0	1	1	1	1	46.0
0	0	1	1	1	0	46.5
0	0	1	1	0	1	47.0
0	0	1	1	0	0	47.5
0	0	1	0	1	1	48.0
0	0	1	0	1	0	48.5
0	0	1	0	0	1	49.0
0	0	1	0	0	0	49.5
0	0	0	1	1	1	50.0
0	0	0	1	1	0	50.5
0	0	0	1	0	1	51.0
0	0	0	1	0	0	51.5
0	0	0	0	1	1	52.0
0	0	0	0	1	0	52.5
0	0	0	0	0	1	53.0
0	0	0	0	0	0	53.5

Table 36. DIF/SIF synthesizer frequency for zero IF Japan (using bit TWOFLO = 1)

Bit						f_{synth} (MHz)
SFREQ5	SFREQ4	SFREQ3	SFREQ2	SFREQ1	SFREQ0	
W5[5]	W5[4]	W5[3]	W5[2]	W5[1]	W5[0]	
1	1	0	0	1	0	57

Table 37. W6 - data write register bit allocation

7	6	5	4	3	2	1	0
TAGC1	TAGC0	AGC2	AGC1	FMWIDE1	TWOFLO	0	DIRECT

Table 38. W6 - data write register bit description

Bit	Symbol	Description
7 and 6	TAGC[1:0]	tuner AGC mode[1]
		00 = TAGC integral loop mode; all currents off
		01 = TAGC integral loop mode; source current off
		10 = TAGC integral loop mode
		11 = TAGC derived from IF AGC; recommended for positive modulated signals
5 and 4	AGC[2:1]	AGC mode and behavior; see Table 39
3	FMWIDE1	FM window
		1 = 1 MHz
		0 = see Table 28 bit FMWIDE0
2	TWOFLO	synthesizer frequency selection
		1 = zero IF Japan mode (57 MHz)
		0 = synthesizer mode
1	-	0 = fixed value
0	DIRECT	direct IF at DTV mode; TV2 = 0[2]
		1 = direct IF output
		0 = zero IF or low IF output

[1] In integral TAGC loop mode the pin TAGC provides sink and source currents for control. TakeOver Point (TOP) is set via register W9 TOPNEG[4:0].

[2] For bit description refer to Table 16 and Table 17.

Table 39. AGC mode and behavior

Bit		VIF AGC; MOD = 1[1]	SIF AGC
AGC2	AGC1		
W6[5]	W6[4]		
0	0	normal	normal
0	1	off (minimum gain)	off (minimum gain)
1	0	fast	normal
1	1	2nd fast	fast

[1] For bit description of MOD refer to Table 23 W2[7] and Table 24.

Table 40. W7 - data write register bit allocation

7	6	5	4	3	2	1	0
0	0	SIFLEVEL	VIDLEVEL	OPSTATE	PORT	FILOUTBP	NYQOFF

Table 41. W7 - data write register bit description

Bit	Symbol	Description
7 and 6	-	0 = fixed value
5	SIFLEVEL	SIF level reduction
		1 = internal SIF level is reduced by 6 dB (only for AM sound)
		0 = internal SIF level is normal
4	VIDLEVEL	video level reduction
		1 = internal video level is reduced by 6 dB
		0 = internal video level is normal
3	OPSTATE	output state; PORT = 1
		1 = output port is HIGH (external pull-up resistor needed)
		0 = output port is LOW
2	PORT	port or VIF AGC monitor
		1 = pin MPP1 is logic output port; level depends on OPSTATE
		0 = pin MPP1 is VIF AGC monitor output; independent on OPSTATE
1	FILOUTBP	external filter output signal source; see Figure 9
		1 = signal for external filter is obtained behind internal BP filter
		0 = signal for external filter is obtained behind SIF mixer
0	NYQOFF	internal Nyquist processing
		1 = internal Nyquist processing off[1]
		0 = internal Nyquist processing on

[1] At internal Nyquist processing off (W7[0] = 1) it is mandatory to set the internal video level bit VIDLEVEL to normal (W7[4] = 0).

Table 42. W8 - data write register bit allocation

7	6	5	4	3	2	1	0
0	0	0	0	EASY3	EASY2	EASY1	EASY0

Table 43. W8 - data write register bit description

Bit	Symbol	Description
7 to 4	-	0 = fixed value
3 to 0	EASY[3:0]	easy setting; see Table 44

Table 44. Easy setting (to be used for fixed bit set-up only)[1]

Bit				Mode or standard	Name	Bit definition (hexadecimal)						
EASY3	EASY2	EASY1	EASY0			W1	W2	W3	W4	W5	W6	W7
W8[3]	W8[2]	W8[1]	W8[0]									
0	0	0	0	off	-	-	-	-	-	-	-	-
0	0	0	1	-	-	-	-	-	-	-	-	-
0	0	1	0	-	-	-	-	-	-	-	-	-
0	0	1	1	-	-	-	-	-	-	-	-	-
0	1	0	0	-	-	-	-	-	-	-	-	-
0	1	0	1	I 6.0	ES2	58	B1	CC	60	80	80	0C
0	1	1	0	B/G 5.5	ES3	38	B1	4C	60	40	80	0C
0	1	1	1	direct IF	ES4	08	E1	64	62	00	81	08
1	0	0	0	M Japan 4.5	ES5	18	F1	44	73	00	80	08
1	0	0	1	LIF 6/36	ES6	28	88	60	61	AD	00	0C
1	0	1	0	-	-	-	-	-	-	-	-	-
1	0	1	1	D/K 6.5	ES8	78	B1	4C	70	C0	80	0C
1	1	0	0	radio 5.5	ES9	BB	B8	40	26	6B	00	04
1	1	0	1	-	-	-	-	-	-	-	-	-
1	1	1	0	L 6.5	ES11	79	33	00	60	C0	C0	0C
1	1	1	1	-	-	-	-	-	-	-	-	-

[1] Access to register W1 to W6 after selection of an easy setting mode would require a transfer of all W1 to W6 register data.

Table 45. W9 - data write register bit allocation

7	6	5	4	3	2	1	0
DAGCSLOPE	TAGCIS	TAGCTC	TOPNEG4	TOPNEG3	TOPNEG2	TOPNEG1	TOPNEG0

Table 46. W9 - data write register bit description

Bit	Symbol	Description
7	DAGCSLOPE	AGCDIN input characteristic; see Figure 45
		1 = high voltage for high gain
		0 = low voltage for high gain
6	TAGCIS	tuner AGC IF input
		1 = inverse to VIF input
		0 = aligned to VIF input
5	TAGCTC	tuner AGC time constant
		1 = 2nd mode
		0 = normal
4 to 0	TOPNEG[4:0]	TOP adjustment for integral loop mode; see Table 47

Table 47. Tuner takeover point adjustment bits W9[4:0]

Bit					TOP adjustment (dBµV)
TOPNEG4	TOPNEG3	TOPNEG2	TOPNEG1	TOPNEG0	
W9[4]	W9[3]	W9[2]	W9[1]	W9[0]	
1	1	1	1	1	98.2 typical
:	:	:	:	:	see Figure 13
1	0	0	0	0	78.7[1]
:	:	:	:	:	see Figure 13
0	0	0	0	0	57.9 typical

[1] See Table 53 for parameter tuner takeover point accuracy ($\alpha_{acc(set)TOP}$).

Table 48. W10 - data write register bit allocation

7	6	5	4	3	2	1	0
0	0	XPOTPOS	TOPPOS4	TOPPOS3	TOPPOS2	TOPPOS1	TOPPOS0

Table 49. W10 - data write register bit description

Bit	Symbol	Description
7 and 6	-	0 = fixed value
5	XPOTPOS	TOP derived from IF AGC via I^2C-bus or potentiometer
		1 = TOP adjustment by external potentiometer at pin TOP2
		0 = see Table 50
4 to 0	TOPPOS[4:0]	TOP adjustment for TAGC derived from IF AGC; see Table 50

Table 50. Tuner takeover point adjustment bits W10[4:0]

Bit					TOP adjustment (dBµV)
TOPPOS4	TOPPOS3	TOPPOS2	TOPPOS1	TOPPOS0	
W10[4]	W10[3]	W10[2]	W10[1]	W10[0]	
1	1	1	1	1	99 typical
:	:	:	:	:	see Figure 13
1	0	0	0	0	81[1]
:	:	:	:	:	see Figure 13
0	0	0	0	0	61 typical

[1] See Table 53 for parameter tuner takeover point accuracy ($\alpha_{acc(set)TOP2}$).

10. Limiting values

Table 51. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_P	supply voltage			-	5.5	V
V_n	voltage on any other pin	all pins except ground		0	V_P	V
t_{sc}	short-circuit time	to ground or V_P		-	10	s
T_{stg}	storage temperature			–40	+150	°C
T_{amb}	ambient temperature			–20	+70	°C
T_{case}	case temperature	TDA9898HL (LQFP48)		-	105	°C
		TDA9898HN (HVQFN48)		-	115	°C
		TDA9897HL (LQFP48)		-	105	°C
		TDA9897HN (HVQFN48)		-	115	°C
V_{esd}	electrostatic discharge voltage	human body model	[1]	-	±3000	V
		machine model	[2]	-	±300	V

[1] Class 2 according to JESD22-A114.

[2] Class B according to EIA/JESD22-A115.

11. Thermal characteristics

Table 52. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; 2 layer board		
	TDA9898HL (LQFP48)		67	K/W
	TDA9898HN (HVQFN48)		48	K/W
	TDA9897HL (LQFP48)		67	K/W
	TDA9897HN (HVQFN48)		48	K/W
$R_{th(j-c)}$	thermal resistance from junction to case			
	TDA9898HL (LQFP48)		19	K/W
	TDA9898HN (HVQFN48)		10	K/W
	TDA9897HL (LQFP48)		19	K/W
	TDA9897HN (HVQFN48)		10	K/W

12. Characteristics

12.1 Analog TV signal processing

Table 53. Characteristics

V_P = 5 V; T_{amb} = 25 °C; see Table 25 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.375 MHz; f_{SC} = 32.875 MHz; PC / SC = 13 dB; f_{AF} = 400 Hz); input level $V_{i(IF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation: Vestigial SideBand (VSB); residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; internal Nyquist slope switched on (W7[0] = 0); not dual mode; measurements taken in test circuit of Figure 50 and Figure 51; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply; pin V_P							
V_P	supply voltage		[1]	4.5	5.0	5.5	V
I_P	supply current			-	-	190	mA
Power-on reset							
$V_{P(POR)}$	power-on reset supply voltage	for start of reset at decreasing supply voltage	[2]	2.5	3.0	3.5	V
		for end of reset at increasing supply voltage; I^2C-bus transmission enable	[2]	-	3.3	4.4	V
VIF amplifier; pins IF1A, IF1B, IF2A and IF2B							
V_I	input voltage			-	1.95	-	V
$R_{i(dif)}$	differential input resistance		[3]	-	2	-	kΩ
$C_{i(dif)}$	differential input capacitance		[3]	-	3	-	pF
$V_{i(IF)(RMS)}$	RMS IF input voltage	lower limit at −1 dB video output signal		-	60	100	μV
		upper limit at +1 dB video output signal		150	190	-	mV
		permissible overload	[4]	-	-	320	mV
ΔG_{IF}	IF gain variation	difference between picture and sound carrier; within AGC range; Δf = 5.5 MHz		-	0.7	-	dB
$G_{VIF(cr)}$	control range VIF gain			60	66	-	dB
$f_{-3dB(VIF)l}$	lower VIF cut-off frequency			-	15	-	MHz
$f_{-3dB(VIF)u}$	upper VIF cut-off frequency			-	80	-	MHz
FPLL and true synchronous video demodulator[5]							
V_{LFVIF}	voltage on pin LFVIF (DC)			0.9	-	3.6	V
$f_{VCO(max)}$	maximum VCO frequency	$f_{VCO} = 2f_{PC}$		120	140	-	MHz
f_{VIF}	VIF frequency	see Table 25		-	-	-	MHz
$\Delta f_{VIF(dah)}$	digital acquisition help VIF frequency window	related to f_{VIF}					
		all standards except M/N		-	±2.3	-	MHz
		M/N standard		-	±1.8	-	MHz
t_{acq}	acquisition time	$B_{LF(-3dB)}$ = 70 kHz	[6]	-	-	30	ms

Table 53. Characteristics *…continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 25 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.375 MHz; f_{SC} = 32.875 MHz; PC / SC = 13 dB; f_{AF} = 400 Hz); input level $V_{i(IF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation: Vestigial SideBand (VSB); residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; internal Nyquist slope switched on (W7[0] = 0); not dual mode; measurements taken in test circuit of Figure 50 and Figure 51; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{lock(min)(RMS)}$	RMS minimum lock-in voltage	measured on pins IF1A and IF1B or IF2A and IF2B; maximum IF gain; negative modulation mode W2[7] = 1 and PLL set to overmodulation mode W2[2] = 0 and W2[1] = 0	-	30	70	µV
$T_{cy(dah)}$	digital acquisition help cycle time		-	64	-	µs
$t_{w(dah)}$	digital acquisition help pulse width		64	-	-	µs
$I_{pul(acq)VIF}$	VIF acquisition pulse current	sink or source	21	-	33	µA
$K_{O(VIF)}$	VIF VCO steepness	$\Delta f_{VIF} / \Delta V_{LFVIF}$	-	26	-	MHz/V
$K_{D(VIF)}$	VIF phase detector steepness	$\Delta I_{VPLL} / \Delta \varphi_{VCO(VIF)}$	-	23	-	µA/rad
$I_{offset(VIF)}$	VIF offset current		–1	0	+1	µA
Video output 2 V; pin CVBS[7]						
Normal mode (sound carrier trap active) and sound carrier on						
$V_{o(video)(p-p)}$	peak-to-peak video output voltage	positive or negative modulation; see Figure 10				
		W4[7] = 0; W7[4] = 0	1.7	2.0	2.3	V
		W4[7] = 1; W7[4] = 0	1.7	2.0	2.3	V
		W4[7] = 0; W7[4] = 1	1.7	2.0	2.3	V
		W4[7] = 1; W7[4] = 1	-	2.0	-	V
$\Delta V_{o(CVBS)}$	CVBS output voltage difference	difference between L and B/G standard				
		W4[7] = 0; W7[4] = 0	–240	-	+240	mV
		W4[7] = 1; W7[4] = 0	–240	-	+240	mV
		W4[7] = 0; W7[4] = 1	–240	-	+240	mV
V_{video}/V_{sync}	video voltage to sync voltage ratio		2.0	2.33	2.75	
V_{syncl}	sync level voltage	W4[7] = 0; W7[4] = 0	1.0	1.2	1.4	V
		W4[7] = 1; W7[4] = 0	0.9	1.2	1.5	V
		W4[7] = 0; W7[4] = 1	0.9	1.2	1.5	V
$V_{clip(video)u}$	upper video clipping voltage		V_P – 1.2	V_P – 1	-	V
$V_{clip(video)l}$	lower video clipping voltage		-	0.4	0.9	V
R_O	output resistance	[3]	-	-	30	Ω
$I_{bias(int)}$	internal bias current (DC)	for emitter-follower	1.5	2.0	-	mA
$I_{sink(o)(max)}$	maximum output sink current	AC and DC	1	-	-	mA

Table 53. Characteristics *...continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 25 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.375 MHz; f_{SC} = 32.875 MHz; PC / SC = 13 dB; f_{AF} = 400 Hz); input level $V_{i(IF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation: Vestigial SideBand (VSB); residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; internal Nyquist slope switched on (W7[0] = 0); not dual mode; measurements taken in test circuit of Figure 50 and Figure 51; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{source(o)(max)}$	maximum output source current	AC and DC		3.9	-	-	mA
$\Delta V_{o(CVBS)}$	CVBS output voltage difference	50 dB gain control		-	-	0.5	dB
		30 dB gain control		-	-	0.1	dB
$\Delta V_{blt}/V_{CVBS}$	black level tilt to CVBS voltage ratio	negative modulation		-	-	1	%
$\Delta V_{blt(v)}/V_{CVBS}$	vertical black level tilt to CVBS voltage ratio	worst case in L standard; vision carrier modulated by test line [Vertical Interval Test Signal (VITS)] only		-	-	3	%
G_{dif}	differential gain	*"ITU-T J.63 line 330"*	[8]				
		B/G standard		-	-	5	%
		L standard		-	-	7	%
φ_{dif}	differential phase	*"ITU-T J.63 line 330"*	[8]				
		B/G standard		-	2	4	deg
		L standard		-	2	4	deg
$(S/N)_w$	weighted signal-to-noise ratio	B/G standard; 50 % grey video signal; unified weighting filter (*"ITU-T J.61"*); see Figure 20	[9]	53	57	-	dB
$(S/N)_{unw}$	unweighted signal-to-noise ratio	M/N standard; 50 IRE grey video signal; see Figure 20		47	51	-	dB
$V_{PC(rsd)(RMS)}$	RMS residual picture carrier voltage	fundamental wave and harmonics		-	2	5	mV
$\Delta f_{PC(p-p)}$	peak-to-peak picture carrier frequency variation	3 % residual carrier; 50 % serration pulses; L standard	[3]	-	-	12	kHz
$\Delta\varphi$	phase difference	0 % residual carrier; 50 % serration pulses; L standard; L-gating = 0 %	[3]	-	-	3	%
$\alpha_{H(video)}$	video harmonics suppression	AC load: C_L < 20 pF, R_L > 1 kΩ	[10]	35	40	-	dB
α_{sp}	spurious suppression		[11]	40	-	-	dB
$PSRR_{CVBS}$	power supply ripple rejection on pin CVBS	f_{ripple} = 70 Hz; video signal; grey level; positive and negative modulation; see Figure 11		14	20	-	dB

Table 53. Characteristics *...continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 25 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.375 MHz; f_{SC} = 32.875 MHz; PC / SC = 13 dB; f_{AF} = 400 Hz); input level $V_{i(IF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation: Vestigial SideBand (VSB); residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; internal Nyquist slope switched on (W7[0] = 0); not dual mode; measurements taken in test circuit of Figure 50 and Figure 51; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
M/N standard inclusive Korea; see Figure 21[12]							
$\alpha_{ripple(resp)f}$	frequency response ripple	0.5 MHz to 2.5 MHz		–1	-	+1	dB
		2.5 MHz to 3.6 MHz		–2	-	+2	dB
		3.6 MHz to 3.8 MHz		–3	-	+2	dB
		3.8 MHz to 4.2 MHz		–16	-	+2	dB
α_{SC1}	first sound carrier attenuation	$f = f_{SC1}$ = 4.5 MHz		38	-	-	dB
		$f = f_{SC1} \pm 60$ kHz		29	-	-	dB
α_{SC2}	second sound carrier attenuation	$f = f_{SC2}$ = 4.724 MHz		25	-	-	dB
		$f = f_{SC2} \pm 60$ kHz		16	-	-	dB
$t_{d(grp)CC}$	color carrier group delay time	f = 3.58 MHz; including transmitter pre-correction; see Figure 22	[13]	–75	–50	+75	ns
B/G standard; see Figure 23[12]							
$\alpha_{ripple(resp)f}$	frequency response ripple	0.5 MHz to 3.2 MHz		–1	-	+1	dB
		3.2 MHz to 4.5 MHz		–2	-	+2	dB
		4.5 MHz to 4.8 MHz		–4	-	+2	dB
		4.8 MHz to 5 MHz		–12	-	+2	dB
α_{SC1}	first sound carrier attenuation	$f = f_{SC1}$ = 5.5 MHz		35	-	-	dB
		$f = f_{SC1} \pm 60$ kHz		26	-	-	dB
α_{SC2}	second sound carrier attenuation	$f = f_{SC2}$ = 5.742 MHz		25	-	-	dB
		$f = f_{SC2} \pm 60$ kHz		16	-	-	dB
$\alpha_{SC(NICAM)}$	NICAM sound carrier attenuation	$f_{car(NICAM)}$ = 5.85 MHz; $f = f_{car(NICAM)} \pm 250$ kHz		12	-	-	dB
α	attenuation	$f = f_{(N+1)ch}$ = 7 MHz		21	-	-	dB
		$f = f_{(N+1)ch} \pm 750$ kHz		5	-	-	dB
$t_{d(grp)CC}$	color carrier group delay time	f = 4.43 MHz; including transmitter pre-correction; see Figure 24	[13]	–75	–10	+75	ns
I standard; see Figure 25[12]							
$\alpha_{ripple(resp)f}$	frequency response ripple	0.5 MHz to 3.2 MHz		–1	-	+1	dB
		3.2 MHz to 4.5 MHz		–2	-	+2	dB
		4.5 MHz to 5 MHz		–4	-	+2	dB
		5 MHz to 5.5 MHz		–12	-	+2	dB
α_{SC1}	first sound carrier attenuation	$f = f_{SC1}$ = 6.0 MHz		35	-	-	dB
		$f = f_{SC1} \pm 60$ kHz		26	-	-	dB
$\alpha_{SC(NICAM)}$	NICAM sound carrier attenuation	$f_{car(NICAM)}$ = 6.55 MHz; $f = f_{car(NICAM)} \pm 250$ kHz		12	-	-	dB

Table 53. Characteristics *…continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 25 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.375 MHz; f_{SC} = 32.875 MHz; PC / SC = 13 dB; f_{AF} = 400 Hz); input level $V_{i(IF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation: Vestigial SideBand (VSB); residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; internal Nyquist slope switched on (W7[0] = 0); not dual mode; measurements taken in test circuit of Figure 50 and Figure 51; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{d(grp)CC}$	color carrier group delay time	f = 4.43 MHz; see Figure 26	[13]	–75	–15	+75	ns
D/K standard; see Figure 27[12]							
$\alpha_{ripple(resp)f}$	frequency response ripple	0.5 MHz to 3.1 MHz		–1	-	+1	dB
		3.1 MHz to 4.5 MHz		–2	-	+2	dB
		4.5 MHz to 4.8 MHz		–4	-	+2	dB
		4.8 MHz to 5.1 MHz		–6	-	+2	dB
α_{SC1}	first sound carrier attenuation	f = f_{SC1} = 6.5 MHz		35	-	-	dB
		f = f_{SC1} ± 60 kHz		26	-	-	dB
$\alpha_{SC2(us)}$	second sound carrier attenuation (upper side)	f = f_{SC2} = 6.742 MHz		25	-	-	dB
		f = f_{SC2} ± 60 kHz		16	-	-	dB
$\alpha_{SC2(ls)}$	second sound carrier attenuation (lower side)	f = f_{SC2} = 6.258 MHz		25	-	-	dB
		f = f_{SC2} ± 60 kHz		16	-	-	dB
$\alpha_{SC(NICAM)}$	NICAM sound carrier attenuation	$f_{car(NICAM)}$ = 5.85 MHz; f = $f_{car(NICAM)}$ ± 250 kHz		6	-	-	dB
$t_{d(grp)CC}$	color carrier group delay time	f = 4.28 MHz; including transmitter pre-correction; see Figure 28	[13]	–50	0	+100	ns
L standard; see Figure 29[12]							
$\alpha_{ripple(resp)f}$	frequency response ripple	0.5 MHz to 3.2 MHz		–1	-	+1	dB
		3.2 MHz to 4.5 MHz		–2	-	+2	dB
		4.5 MHz to 4.8 MHz		–4	-	+2	dB
		4.8 MHz to 5.3 MHz		–12	-	+2	dB
$\alpha_{SC(NICAM)}$	NICAM sound carrier attenuation	$f_{car(NICAM)}$ = 5.85 MHz; f = $f_{car(NICAM)}$ ± 250 kHz		5	-	-	dB
$\alpha_{SC(AM)}$	AM sound carrier attenuation	f = $f_{SC(AM)}$ = 6.5 MHz		38	-	-	dB
		f = $f_{SC(AM)}$ ± 30 kHz		29	-	-	dB
$t_{d(grp)CC}$	color carrier group delay time	f = 4.28 MHz; including transmitter pre-correction; see Figure 30		–75	–5	+75	ns
Video output 1.1 V; pin CVBS							
Trap bypass mode and sound carrier off[12]							
$V_{o(video)(p-p)}$	peak-to-peak video output voltage	see Figure 10		-	1.1	-	V
V_{syncl}	sync level voltage			-	1.5	-	V
$V_{clip(video)u}$	upper video clipping voltage			V_P – 1.1	V_P – 1	-	V
$V_{clip(video)l}$	lower video clipping voltage			-	0.4	0.9	V
$B_{video(-3dB)}$	–3 dB video bandwidth	AC load: C_L < 20 pF, R_L > 1 kΩ		6	8	-	MHz

Table 53. Characteristics *…continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 25 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.375 MHz; f_{SC} = 32.875 MHz; PC / SC = 13 dB; f_{AF} = 400 Hz); input level $V_{i(IF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation: Vestigial SideBand (VSB); residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; internal Nyquist slope switched on (W7[0] = 0); not dual mode; measurements taken in test circuit of Figure 50 and Figure 51; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$(S/N)_w$	weighted signal-to-noise ratio	B/G standard; 50 % grey video signal; unified weighting filter (*"ITU-T J.61"*); see Figure 20	[9]	54	-	-	dB
$(S/N)_{unw}$	unweighted signal-to-noise ratio	M/N standard; 50 IRE grey video signal; see Figure 20	[9]	47	51	-	dB
Loop filter synthesizer; pin LFSYN1							
V_{LFSYN1}	voltage on pin LFSYN1			1.0	-	3.5	V
$I_{source(o)PD(max)}$	maximum phase detector output source current			-	-	65	µA
$I_{sink(o)PD(max)}$	maximum phase detector output sink current			-	-	65	µA
K_O	VCO steepness			-	3.75	-	MHz/V
K_D	phase detector steepness			-	9	-	µA/rad
Pin MPP1 operating as VIF AGC voltage monitor							
$V_{monitor(VIFAGC)}$	VIF AGC monitor voltage		[3]	0.5	-	4.5	V
V_{AGC}	AGC voltage	see Figure 12; $V_{i(IF)}$ set to					
		1 mV (60 dBµV)		2.2	-	2.6	V
		10 mV (80 dBµV)		2.5	-	3.1	V
		200 mV (106 dBµV)		3	-	4	V
$I_{o(max)}$	maximum output current	sink or source		10	-	-	µA

Table 53. Characteristics *…continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 25 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.375 MHz; f_{SC} = 32.875 MHz; PC / SC = 13 dB; f_{AF} = 400 Hz); input level $V_{i(IF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation: Vestigial SideBand (VSB); residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; internal Nyquist slope switched on (W7[0] = 0); not dual mode; measurements taken in test circuit of Figure 50 and Figure 51; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{resp}	response time	increasing VIF step; negative modulation	[14]				
		normal mode		-	4.3	-	μs/dB
		fast mode		-	1.5	-	μs/dB
		increasing VIF step; positive modulation; normal mode	[14]	-	130	-	μs/dB
		decreasing VIF step; negative modulation	[14]				
		normal mode		-	1.9	-	ms/dB
		fast normal mode		-	0.08	-	ms/dB
		2nd mode		-	0.25	-	ms/dB
		fast 2nd mode		-	0.01	-	ms/dB
		decreasing VIF step; positive modulation	[14]				
		20 dB		-	890	-	ms
		fast mode		-	2.6	-	ms/dB
		normal mode		-	143	-	ms/dB
$\alpha_{th(fast)VIF}$	VIF fast mode threshold	L standard		–10	–6	–2	dB
$\Delta V_{VAGC(step)}$	VIF AGC voltage difference (step)	see Table 11		-	40	-	mV/bit
Pin MPP1 operating as open-collector output port							
V_{OL}	LOW-level output voltage	I = 2 mA (sink)		-	-	0.4	V
$I_{sink(o)}$	output sink current	W7[3] = 0		-	-	3	mA
		W7[3] = 1		-	-	10	μA
V_{OH}	HIGH-level output voltage			-	-	V_P + 0.5	V
VIF AGC; pin CIFAGC							
$I_{ch(max)}$	maximum charge current	L standard		75	100	125	μA
$I_{ch(add)}$	additional charge current	L standard: in the event of missing VITS pulses and no white video content		-	100	-	nA
I_{dch}	discharge current	L standard; normal mode		-	35	-	nA
		L standard; fast mode		-	1.8	-	μA

Table 53. Characteristics *...continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 25 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.375 MHz; f_{SC} = 32.875 MHz; PC / SC = 13 dB; f_{AF} = 400 Hz); input level $V_{i(IF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation: Vestigial SideBand (VSB); residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; internal Nyquist slope switched on (W7[0] = 0); not dual mode; measurements taken in test circuit of Figure 50 and Figure 51; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Tuner AGC; pin TAGC							
Integral TAGC loop mode (W6[7:6] = 10); TAGC is current output; applicable for negative modulation only; unmodulated VIF; see Table 46 and Figure 13							
$V_{i(IF)(RMS)}$	RMS IF input voltage	at starting point of tuner AGC takeover; $I_{sink(TAGC)}$ = 100 μA					
		W9[4:0] = 0 0000		-	57.9	-	dBμV
		W9[4:0] = 1 0000		-	78.7	-	dBμV
		W9[4:0] = 1 1111		-	98.2	-	dBμV
$\alpha_{acc(set)TOP}$	TOP setting accuracy			–2	-	+2	dB
I_{source}	source current	TAGC charge current					
		normal mode; W9[5] = 0		0.2	0.3	0.4	μA
		2nd normal mode; W9[5] = 1		1.9	2.3	2.7	μA
		fast mode activated by internal level detector; W9[5] = 0		7	11	15	μA
		2nd fast mode activated by internal level detector; W9[5] = 1		60	90	120	μA
I_{sink}	sink current	TAGC discharge current; V_{TAGC} = 1 V		400	500	600	μA
$\Delta\alpha_{acc(set)TOP}/\Delta T$	TOP setting accuracy variation with temperature	W9[4:0] = 1 0000		-	-	0.02	dB/K
R_L	load resistance		[3]	50	-	-	MΩ
$V_{sat(u)}$	upper saturation voltage	pin operating as current output		V_P – 0.3	-	-	V
$V_{sat(l)}$	lower saturation voltage	pin operating as current output		-	-	0.3	V
$\alpha_{th(fast)AGC}$	AGC fast mode threshold	activated by internal fast AGC detector; I^2C-bus setting corresponds to W9[4:0] = 1 0000	[3]	6	8	10	dB
t_d	delay time	before activating; $V_{i(IF)}$ below $\alpha_{th(fast)AGC}$		40	60	80	ms

Table 53. Characteristics *…continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 25 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.375 MHz; f_{SC} = 32.875 MHz; PC / SC = 13 dB; f_{AF} = 400 Hz); input level $V_{i(IF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation: Vestigial SideBand (VSB); residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; internal Nyquist slope switched on (W7[0] = 0); not dual mode; measurements taken in test circuit of Figure 50 and Figure 51; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TAGC loop based on VIF AGC (W6[7:6] = 11); TAGC is voltage output; applicable for TV mode: positive modulation and optional for negative modulation); see Table 49; Figure 13 and Figure 14							
$V_{i(IF)(RMS)}$	RMS IF input voltage	at starting point of tuner AGC takeover; V_{TAGC} = 3.5 V					
		R_{TOP2} = 22 kΩ or W10[5:0] = 00 0000		-	61	-	dBμV
		R_{TOP2} = 10 kΩ or W10[5:0] = 01 0000		-	81	-	dBμV
		R_{TOP2} = 0 kΩ		-	96	-	dBμV
		W10[5:0] = 01 1111		-	99	-	dBμV
$\alpha_{acc(set)TOP2}$	TOP2 setting accuracy			–6	-	+6	dB
$\Delta\alpha_{acc(set)TOP2}/\Delta T$	TOP2 setting accuracy variation with temperature	V_{TAGC} = 3.5 V		-	0.03	0.07	dB/K
V_O	output voltage	no tuner gain reduction		4.5	-	V_P	V
		maximum tuner gain reduction		0.2	-	0.6	V
$\Delta G_{slip(TAGC)}$	TAGC slip gain offset	tuner gain voltage from 0.6 V to 3.5 V		3	5	8	dB
TOP adjust 2; pin TOP2; IF based TAGC loop mode; see Figure 14							
V_{TOP2}	voltage on pin TOP2 (DC)	pin open-circuit		-	3.5	-	V
R_I	input resistance			-	27	-	kΩ
R_{TOP2}	resistance on pin TOP2	adjustment of VIF AGC based TAGC loop					
		W10[5] = 1; external resistor operation		0	-	22	kΩ
		W10[5] = 0; forced I²C-bus operation		100	-	-	kΩ
Pin CTAGC							
V_{CTAGC}	voltage on pin CTAGC		[3]	0.2	-	$0.55V_P$	V
I_L	leakage current	sink	[3]	-	-	10	nA
		source	[3]	-	-	10	nA
Control current or voltage monitor output; pin MPP2							
General							
$V_{sat(u)}$	upper saturation voltage			V_P – 0.8	V_P – 0.5	-	V
$V_{sat(l)}$	lower saturation voltage			-	0.5	0.8	V

Table 53. Characteristics *…continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 25 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.375 MHz; f_{SC} = 32.875 MHz; PC / SC = 13 dB; f_{AF} = 400 Hz); input level $V_{i(IF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation: Vestigial SideBand (VSB); residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; internal Nyquist slope switched on (W7[0] = 0); not dual mode; measurements taken in test circuit of Figure 50 and Figure 51; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
AFC (current output)							
I_o	output current	sink or source; see Figure 17 and Figure 18	[15][16]				
		100 kHz VIF deviation		80	-	160	µA
		200 kHz VIF deviation		160	200	240	µA
		1.5 MHz VIF deviation		160	-	240	µA
AFC TV mode							
$\Delta I_{AFC}/\Delta f_{VIF}$	change of AFC current with VIF frequency		[16]	0.85	1.05	1.25	µA/kHz
$f_{VIFacc(dig)}$	digital accuracy of VIF frequency	read-out via I²C-bus; R1[4:1] = f_0; f_{ref} = 4 MHz	[17]	−20	-	+20	kHz
$f_{VIFacc(a)}$	analog accuracy of VIF frequency	I_{AFC} = 0 A; f_{ref} = 4 MHz	[17]	−20	-	+20	kHz
AFC radio mode							
$\Delta I_{AFC}/\Delta f_{RIF}$	change of AFC current with RIF frequency		[16]	0.85	1.05	1.25	µA/kHz
$f_{RIFacc(dig)}$	digital accuracy of RIF frequency	read-out via I²C-bus; R1[4:1] = f_0; f_{ref} = 4 MHz	[17]	−10	-	+10	kHz
$f_{RIFacc(a)}$	analog accuracy of RIF frequency	I_{AFC} = 0 A; f_{ref} = 4 MHz	[17]	−10	-	+10	kHz
AGC monitor (voltage output)							
G_v	voltage gain	voltage on pin MPP2 to internal control voltage; see Table 32		-	0	-	dB
		SIF AGC		-	6	-	dB
		FM AGC		-	6	-	dB
		TAGC		-	0	-	dB
$I_{o(max)}$	maximum output current	sink or source		350	-	-	µA
SIF amplifier; pins IF3A and IF3B or pins IF1A and IF1B or pins IF2A and IF2B							
V_I	input voltage			-	1.95	-	V
$R_{i(dif)}$	differential input resistance			-	2	-	kΩ
$C_{i(dif)}$	differential input capacitance			-	3	-	pF

Table 53. Characteristics *…continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 25 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.375 MHz; f_{SC} = 32.875 MHz; PC / SC = 13 dB; f_{AF} = 400 Hz); input level $V_{i(IF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation: Vestigial SideBand (VSB); residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; internal Nyquist slope switched on (W7[0] = 0); not dual mode; measurements taken in test circuit of Figure 50 and Figure 51; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{i(SIF)(RMS)}$	RMS SIF input voltage	FM mode; –3 dB at intercarrier output pins OUT1A and OUT1B; without FM AGC; see Table 21	-	60	100	µV
		AM mode; –3 dB at AF output pin AUD	-	40	70	µV
		FM mode; +1 dB at intercarrier output pins OUT1A and OUT1B; without FM AGC; see Table 21	150	190	-	mV
		AM mode; +1 dB at AF output pin AUD	70	140	-	mV
		permissible overload	-	-	320	mV
$G_{SIF(cr)}$	control range SIF gain	FM and AM mode	60	66	-	dB
$f_{-3dB(SIF)l}$	lower SIF cut-off frequency		-	7	-	MHz
$f_{-3dB(SIF)u}$	upper SIF cut-off frequency		-	80	-	MHz
SIF AGC detector; pin MPP2; see Figure 16						
t_{resp}	response time	increasing or decreasing SIF step of 20 dB; AM mode; fast AGC				
		increasing	-	8	-	ms
		decreasing	-	25	-	ms
		increasing or decreasing SIF step of 20 dB; AM mode; slow AGC				
		increasing	-	80	-	ms
		decreasing	-	250	-	ms
		increasing or decreasing SIF step of 20 dB; FM mode; normal AGC				
		increasing	-	0.3	-	ms
		decreasing	-	20	-	ms
		increasing or decreasing SIF step of 20 dB; FM mode; fast AGC				
		increasing	-	0.1	-	ms
		decreasing	-	4	-	ms

Table 53. Characteristics *...continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 25 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.375 MHz; f_{SC} = 32.875 MHz; PC / SC = 13 dB; f_{AF} = 400 Hz); input level $V_{i(IF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation: Vestigial SideBand (VSB); residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; internal Nyquist slope switched on (W7[0] = 0); not dual mode; measurements taken in test circuit of Figure 50 and Figure 51; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{AGC(SIF)}$	SIF AGC voltage	FM mode					
		V_{SIF} = 100 μV		1.5	-	2.4	V
		V_{SIF} = 10 mV		2.6	-	3.4	V
		V_{SIF} = 140 mV		3.3	-	V_P	V
		AM mode					
		V_{SIF} = 100 μV		1.5	-	2.4	V
		V_{SIF} = 10 mV		2.9	-	3.9	V
		V_{SIF} = 140 mV		3.3	-	V_P	V
Conversion synthesizer PLL; pin LFSYN2 (radio mode)							
V_{LFSYN2}	voltage on pin LFSYN2			1	-	3	V
K_O	VCO steepness	$\Delta f_{VCO} / \Delta V_{LFSYN2}$		-	31	-	MHz/V
K_D	phase detector steepness	$\Delta I_{LFSYN2} / \Delta\varphi_{VCO}$; see Table 57; f_{VCO} selection:					
		22 MHz to 29.5 MHz		-	32	-	μA/rad
		30 MHz to 37.5 MHz		-	38	-	μA/rad
		38 MHz to 45.5 MHz		-	47	-	μA/rad
		46 MHz to 53.5 MHz		-	61	-	μA/rad
		57 MHz		-	61	-	μA/rad
$I_{o(PD)}$	phase detector output current	sink or source; f_{VCO} selection:					
		22 MHz to 29.5 MHz		-	200	-	μA
		30 MHz to 37.5 MHz		-	238	-	μA
		38 MHz to 45.5 MHz		-	294	-	μA
		46 MHz to 53.5 MHz		-	384	-	μA
		57 MHz		-	384	-	μA
$\varphi_{n(synth)}$	synthesizer phase noise	with 4 MHz crystal oscillator reference					
		at 1 kHz	[3]	89	99	-	dBc/Hz
		at 10 kHz	[3]	89	99	-	dBc/Hz
		at 100 kHz	[3]	98	102	-	dBc/Hz
		at 1.4 MHz	[3]	115	119	-	dBc/Hz
α_{sp}	spurious suppression	multiple of Δf = 500 kHz	[3]	50	-	-	dBc
I_L	leakage current	synthesizer spurious performance > 50 dBc	[3]	-	-	10	nA

Table 53. Characteristics *...continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 25 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.375 MHz; f_{SC} = 32.875 MHz; PC / SC = 13 dB; f_{AF} = 400 Hz); input level $V_{i(IF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation: Vestigial SideBand (VSB); residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; internal Nyquist slope switched on (W7[0] = 0); not dual mode; measurements taken in test circuit of Figure 50 and Figure 51; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PSRR	power supply ripple rejection	residual spurious at nominal differential output voltage dependent on power supply ripple at 70 Hz; see Figure 11	-	50	-	dB
Single reference QSS intercarrier mixer; pins OUT1A and OUT1B						
V_{OUT1A}	voltage on pin OUT1A (DC)		1.8	2.0	2.2	V
V_{OUT1B}	voltage on pin OUT1B (DC)		1.8	2.0	2.2	V
$I_{bias(int)}$	internal bias current (DC)	for emitter-follower	2.0	2.5	-	mA
$I_{sink(o)(max)}$	maximum output sink current	DC and AC	1.4	1.7	-	mA
$I_{source(o)(max)}$	maximum output source current	DC and AC; with external resistor to GND	3.0	-	-	mA
R_O	output resistance	output active; single-ended to GND	-	-	25	Ω
		output inactive; internal resistance to GND	-	800	-	Ω
$V_{o(RMS)}$	RMS output voltage	IF intercarrier single-ended to GND; SC1 on; SC2 off	90	140	180	mV
		IF intercarrier single-ended to GND; L standard; without modulation; BP on				
		W7[5] = 0	45	70	90	mV
		W7[5] = 1	20	35	45	mV
$f_{-3dB(ic)u}$	upper intercarrier cut-off frequency	internal sound band-pass off	11	15	-	MHz
α_{image}	image rejection	band-pass off; –8 MHz to 0 MHz	24	28	-	dB
$V_{interf(RMS)}$	RMS interference voltage	fundamental wave and harmonics	-	2	5	mV
AM intercarrier from pin EXTFILI to pins OUT1A and OUT1B						
G	gain	IF intercarrier; L standard; without modulation	-	5	-	dB

Table 53. Characteristics *...continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 25 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.375 MHz; f_{SC} = 32.875 MHz; PC / SC = 13 dB; f_{AF} = 400 Hz); input level $V_{i(IF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation: Vestigial SideBand (VSB); residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; internal Nyquist slope switched on (W7[0] = 0); not dual mode; measurements taken in test circuit of Figure 50 and Figure 51; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Band-pass mode						
f_c	center frequency	QSS mode; BP selection for standard				
		M/N	-	4.7	-	MHz
		B/G	-	5.75	-	MHz
		I	-	6.25	-	MHz
		D/K	-	6.25	-	MHz
		L/L-accent	-	6.05	-	MHz
		radio mode; BP selection for standard				
		M/N	-	4.7	-	MHz
		B/G	-	5.75	-	MHz
		I	-	6.25	-	MHz
		D/K	-	6.78	-	MHz
		RADIO	-	10.7	-	MHz
$f_{-3dB(BP)u}$	upper BP cut-off frequency	M/N, B/G, I, D/K or L/L-accent standard	f_c + 0.5	f_c + 0.65	f_c + 0.8	MHz
		RADIO 10.7	f_c + 0.25	f_c + 0.4	f_c + 0.55	MHz
$f_{-3dB(BP)l}$	lower BP cut-off frequency	M/N, B/G, I, D/K or L/L-accent standard	f_c – 0.5	f_c – 0.65	f_c – 0.8	MHz
		RADIO 10.7	f_c – 0.25	f_c – 0.4	f_c – 0.55	MHz
α_{stpb}	stop-band attenuation	at f_c ± 1.5 MHz				
		M/N, B/G, I, D/K or L/L-accent standard	20	30	-	dB
		RADIO 10.7	15	25	-	dB
α_{CC}	color carrier attenuation	QSS mode; BP selection for standard				
		M/N; f_{CC} = 3.58 MHz	15	23	-	dB
		B/G; f_{CC} = 4.43 MHz	22	30	-	dB
		I; f_{CC} = 4.43 MHz	20	28	-	dB
		D/K; f_{CC} = 4.28 MHz	20	28	-	dB
		L/L-accent; f_{CC} = 4.28 MHz	20	28	-	dB
External filter output; pin EXTFILO						
$V_{EXTFILO}$	voltage on pin EXTFILO (DC)		1.8	2.0	2.2	V

Table 53. Characteristics *…continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 25 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.375 MHz; f_{SC} = 32.875 MHz; PC / SC = 13 dB; f_{AF} = 400 Hz); input level $V_{i(IF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation: Vestigial SideBand (VSB); residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; internal Nyquist slope switched on (W7[0] = 0); not dual mode; measurements taken in test circuit of Figure 50 and Figure 51; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{EXTFILO(p-p)}$	peak-to-peak voltage on pin EXTFILO	IF intercarrier; SC1 on; SC2 off	420	620	820	mV
		IF intercarrier; L standard; without modulation				
		W7[5] = 0	210	310	410	mV
		W7[5] = 1	105	155	205	mV
$I_{o(max)}$	maximum output current	AC and DC	1	-	-	mA
FM PLL demodulator						
f_{FMPLL}	FM PLL frequency	see Table 18 and Table 20	-	4.5	-	MHz
			-	5.5	-	MHz
			-	6.0	-	MHz
			-	6.5	-	MHz
			-	10.7	-	MHz
FM PLL filter; pin LFFM						
V_{LFFM}	voltage on pin LFFM	f_{FMPLL} = 4.5 MHz	1.5	1.9	3.3	V
		f_{FMPLL} = 5.5 MHz	1.5	2.2	3.3	V
		f_{FMPLL} = 6.0 MHz	1.5	2.35	3.3	V
		f_{FMPLL} = 6.5 MHz	1.5	2.5	3.3	V
		f_{FMPLL} = 10.7 MHz	1.5	2.4	3.3	V
$T_{cy(dah)}$	digital acquisition help cycle time		-	64	-	µs
$t_{w(dah)}$	digital acquisition help pulse width		-	16	-	µs
$I_{o(dah)}$	digital acquisition help output current	sink or source				
		W3[4] = 0; W6[3] = 0; FM window width = 237.5 kHz	14	18	22	µA
		W3[4] = 1; W6[3] = 0; FM window width = 475 kHz	28	36	44	µA
		W3[4] = 0; W6[3] = 1; FM window width = 1 MHz	14	18	22	µA
		W3[4] = 1; W6[3] = 1; FM window width = 1 MHz	28	36	44	µA

Table 53. Characteristics *…continued*
V_P = 5 V; T_{amb} = 25 °C; see Table 25 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.375 MHz; f_{SC} = 32.875 MHz; PC / SC = 13 dB; f_{AF} = 400 Hz); input level $V_{i(IF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation: Vestigial SideBand (VSB); residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with “ITU-T J.63 line 17 and line 330” or “NTC-7 Composite”; internal Nyquist slope switched on (W7[0] = 0); not dual mode; measurements taken in test circuit of Figure 50 and Figure 51; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$K_{D(FM)}$	FM phase detector steepness	ΔI_{FMPLL} / $\Delta \varphi_{VCO(FM)}$				
		W3[4] = 0; W6[3] = 0; FM window width = 237.5 kHz	-	4	-	μA/rad
		W3[4] = 1; W6[3] = 0; FM window width = 475 kHz	-	10	-	μA/rad
		W3[4] = 0; W6[3] = 1; FM window width = 1 MHz	-	4	-	μA/rad
		W3[4] = 1; W6[3] = 1; FM window width = 1 MHz	-	10	-	μA/rad
$K_{O(FM)}$	FM VCO steepness	Δf_{FMPLL} / ΔV_{LFFM}				
		f < 10 MHz	-	3.3	-	MHz/V
		f = 10.7 MHz	-	5.9	-	MHz/V
$I_{offset(FM)}$	FM offset current	W6[3] = 0; W3[4] = 0	–1.5	0	+1.5	μA
		W6[3] = 0; W3[4] = 1	–2.5	0	+2.5	μA
FM intercarrier input; pins EXTFMI and EXTFILI; see Figure 15						
$\|Z_i\|$	input impedance	AC-coupled via 4 pF	-	20	-	kΩ
$V_{i(FM)(RMS)}$	RMS FM input voltage	gain controlled operation; W1[1:0] = 10 or W1[1:0] = 11 or W1[1:0] = 01	2	-	300	mV
$V_{lock(min)(RMS)}$	RMS minimum lock-in voltage	W1[1:0] = 10 or W1[1:0] = 11 or W1[1:0] = 01	-	-	1.5	mV
$V_{det(FM)min(RMS)}$	RMS minimum FM carrier detection voltage	W1[1:0] = 10 or W1[1:0] = 11 or W1[1:0] = 01	-	-	1.8	mV
FM demodulator part; audio output; pin AUD						
$V_{o(AF)(RMS)}$	RMS AF output voltage	QSS mode; 25 kHz FM deviation; 75 μs de-emphasis	400	500	600	mV
		QSS mode; 27 kHz FM deviation; 50 μs de-emphasis	430	540	650	mV
		QSS mode; 55 kHz FM deviation; 50 μs de-emphasis	900	-	1300	mV
		radio mode; 22.5 kHz FM deviation; 75 μs de-emphasis	360	450	540	mV

Table 53. Characteristics *…continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 25 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.375 MHz; f_{SC} = 32.875 MHz; PC / SC = 13 dB; f_{AF} = 400 Hz); input level $V_{i(IF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation: Vestigial SideBand (VSB); residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; internal Nyquist slope switched on (W7[0] = 0); not dual mode; measurements taken in test circuit of Figure 50 and Figure 51; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$\Delta V_{o(AF)}/\Delta T$	AF output voltage variation with temperature			-	3×10^{-3}	7×10^{-3}	dB/K
THD	total harmonic distortion	50 μs de-emphasis; FM deviation: for TV mode 27 kHz and for radio mode 22.5 kHz		-	0.15	0.50	%
$\Delta f_{AF(max)}$	maximum AF frequency deviation	THD < 2 %; pre-emphasis off; f_{AF} = 400 Hz	[18]				
		W3[1:0] = 00 (audio gain = 0 dB)		±55	-	-	kHz
		W3[1:0] = 01 (audio gain = –6 dB)		±110	-	-	kHz
		W3[1:0] = 10 (audio gain = –12 dB)		±170	-	-	kHz
		W3[1:0] = 11 (audio gain = –18 dB) and W3[4] = 1 (FM window width = 475 kHz)		±380	-	-	kHz
$f_{AF(max)}$	maximum AF frequency	THD < 2 %; pre-emphasis off	[3]				
		FM window width = 237.5 kHz; –6 dB audio gain; FM deviation 100 kHz		15	-	-	kHz
		FM window width = 475 kHz; –18 dB audio gain; FM deviation 300 kHz		15	-	-	kHz
$f_{-3dB(AF)}$	AF cut-off frequency	W3[2] = 0; W3[4] = 0; without de-emphasis; FM window width = 237.5 kHz		80	100	-	kHz
$(S/N)_{w(AF)}$	AF weighted signal-to-noise ratio	27 kHz FM deviation; 50 μs de-emphasis; vision carrier unmodulated; FM PLL only; *"ITU-R BS.468-4"*		48	56	-	dB
$(S/N)_{unw(AF)}$	AF unweighted signal-to-noise ratio	radio mode (10.7 MHz); 22.5 kHz FM deviation; 75 μs de-emphasis		-	58	-	dB
$V_{SC(rsd)(RMS)}$	RMS residual sound carrier voltage	fundamental wave and harmonics; without de-emphasis		-	-	2	mV

Table 53. Characteristics *…continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 25 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.375 MHz; f_{SC} = 32.875 MHz; PC / SC = 13 dB; f_{AF} = 400 Hz); input level $V_{i(IF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation: Vestigial SideBand (VSB); residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; internal Nyquist slope switched on (W7[0] = 0); not dual mode; measurements taken in test circuit of Figure 50 and Figure 51; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
α_{AM}	AM suppression	referenced to 27 kHz FM deviation; 50 µs de-emphasis; AM: f = 1 kHz; m = 54 %		35	46	-	dB
PSRR	power supply ripple rejection	f_{ripple} = 70 Hz; see Figure 11		14	20	-	dB
Audio amplifier							
Audio output; pin AUD							
R_O	output resistance		[3]	-	-	300	Ω
V_O	output voltage			2.0	2.4	2.7	V
R_L	load resistance	AC-coupled	[3]	10	-	-	kΩ
		DC-coupled	[3]	100	-	-	kΩ
C_L	load capacitance		[3]	-	-	1	nF
$V_{o(AF)(RMS)}$	RMS AF output voltage	25 kHz FM deviation; 75 µs de-emphasis; see Table 28					
		0 dB		400	500	600	mV
		–6 dB		-	250	-	mV
		–12 dB		-	125	-	mV
		–18 dB		-	62.5	-	mV
		AM; m = 54 %; see Table 28					
		0 dB		400	500	600	mV
		–6 dB		-	250	-	mV
$f_{-3dB(AF)u}$	upper AF cut-off frequency	W3[2] = 0 (without de-emphasis)	[19]	-	150	-	kHz
$f_{-3dB(AF)l}$	lower AF cut-off frequency	W3[2] = 0 (without de-emphasis)	[20]	-	20	-	Hz
α_{mute}	mute attenuation	of AF signal		70	-	-	dB
ΔV_{jmp}	jump voltage difference (DC)	switching AF output to mute state or vice versa; activated by digital acquisition help W3[6] = 1 or via W3[5]		-	±50	±150	mV
PSRR	power supply ripple rejection	f_{ripple} = 70 Hz; see Figure 11		14	20	-	dB
De-emphasis network; pin CDEEM							
V_O	output voltage			-	2.4	-	V

Table 53. Characteristics *…continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 25 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.375 MHz; f_{SC} = 32.875 MHz; PC / SC = 13 dB; f_{AF} = 400 Hz); input level $V_{i(IF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation: Vestigial SideBand (VSB); residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; internal Nyquist slope switched on (W7[0] = 0); not dual mode; measurements taken in test circuit of Figure 50 and Figure 51; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_O	output resistance	W3[3:2] = 11 (50 µs de-emphasis)	8.5	-	14	kΩ
		W3[3:2] = 01 (75 µs de-emphasis)	13	-	21	kΩ
$V_{AF(RMS)}$	RMS AF voltage	f_{AF} = 400 Hz; $V_{o(AF)}$ = 500 mV (RMS); 0 dB attenuation	-	170	-	mV
AF decoupling						
Pin CAF1						
V_{dec}	decoupling voltage (DC)	f_{FMPLL} = 4.5 MHz	1.5	1.9	3.3	V
		f_{FMPLL} = 5.5 MHz	1.5	2.2	3.3	V
		f_{FMPLL} = 6.0 MHz	1.5	2.35	3.3	V
		f_{FMPLL} = 6.5 MHz	1.5	2.5	3.3	V
		f_{FMPLL} = 10.7 MHz	1.5	2.4	3.3	V
I_L	leakage current	ΔV_{AUD} < ±50 mV (p-p); 0 dB attenuation	-	-	±25	nA
$I_{o(max)}$	maximum output current	sink or source	1.15	1.5	1.85	µA
Pin CAF2						
V_O	output voltage		-	2.4	-	V
FM operation[21][22]						
Single reference QSS AF performance; pin AUD[23]						
$(S/N)_{w(SC1)}$	first sound carrier weighted signal-to-noise ratio	PC / SC1 > 40 dB at pins IF1A and IF1B or IF2A and IF2B; 27 kHz FM deviation; BP off; *"ITU-R BS.468-4"*				
		black picture	45	50	-	dB
		white picture	45	50	-	dB
		6 kHz sine wave (black-to-white modulation)	43	47	-	dB
		250 kHz square wave (black-to-white modulation)	45	50	-	dB

Table 53. Characteristics *…continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 25 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.375 MHz; f_{SC} = 32.875 MHz; PC / SC = 13 dB; f_{AF} = 400 Hz); input level $V_{i(IF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation: Vestigial SideBand (VSB); residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; internal Nyquist slope switched on (W7[0] = 0); not dual mode; measurements taken in test circuit of Figure 50 and Figure 51; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Single reference QSS AF performance with external FM demodulator connected to OUT1A and OUT1B[24]						
$(S/N)_{w(SC1)}$	first sound carrier weighted signal-to-noise ratio	PC / SC1 > 40 dB at pins IF1A and IF1B or IF2A and IF2B; 27 kHz FM deviation; BP off; *"ITU-R BS.468-4"*				
		black picture	53	58	-	dB
		white picture	50	53	-	dB
		6 kHz sine wave (black-to-white modulation)	44	48	-	dB
		250 kHz square wave (black-to-white modulation)	40	45	-	dB
		sound carrier subharmonics; f = 2.75 MHz ± 3 kHz	45	51	-	dB
		sound carrier subharmonics; f = 2.87 MHz ± 3 kHz	46	52	-	dB
$(S/N)_{w(SC2)}$	second sound carrier weighted signal-to-noise ratio	with external reference FM demodulator; PC / SC2 > 40 dB at pins IF1A and IF1B or IF2A and IF2B; 27 kHz (54 % FM deviation); BP off; *"ITU-R BS.468-4"*				
		black picture	48	55	-	dB
		white picture	46	51	-	dB
		6 kHz sine wave (black-to-white modulation)	42	46	-	dB
		250 kHz square wave (black-to-white modulation)	29	34	-	dB
		sound carrier subharmonics; f = 2.75 MHz ± 3 kHz	44	50	-	dB
		sound carrier subharmonics; f = 2.87 MHz ± 3 kHz	45	51	-	dB

Table 53. Characteristics *...continued*
V_P = 5 V; T_{amb} = 25 °C; see Table 25 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.375 MHz; f_{SC} = 32.875 MHz; PC / SC = 13 dB; f_{AF} = 400 Hz); input level $V_{i(IF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation: Vestigial SideBand (VSB); residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; internal Nyquist slope switched on (W7[0] = 0); not dual mode; measurements taken in test circuit of Figure 50 and Figure 51; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
AM operation							
L standard; pin AUD							
$V_{o(AF)(RMS)}$	RMS AF output voltage	54 % modulation		400	500	600	mV
THD	total harmonic distortion	54 % modulation; BP on; see Figure 33		-	0.5	1.0	%
$B_{AF(-3dB)}$	–3 dB AF bandwidth			12	18	-	kHz
$(S/N)_{w(AF)}$	AF weighted signal-to-noise ratio	*"ITU-R BS.468-4"*					
		BP on		38	42	-	dB
		BP off		44	50	-	dB
		composite IF; VIF modulation = color bar; *"ITU-R BS.468-4"*; BP on	[3]	-	40	-	dB
Reference frequency							
General							
f_{ref}	reference frequency		[25]	-	4	-	MHz
Reference frequency generation with crystal; pin OPTXTAL							
$V_{OPTXTAL}$	voltage on pin OPTXTAL (DC)	pin open-circuit		2.3	2.6	2.9	V
R_i	input resistance		[3]	-	2	-	kΩ
$R_{rsn(xtal)}$	crystal resonance resistance			-	-	200	Ω
C_{pull}	pull capacitance		[26]	-	-	-	pF
$R_{swoff(OPTXTAL)}$	switch-off resistance on pin OPTXTAL	to switch off crystal input by external resistor wired between pin OPTXTAL and GND		0.22	-	4.7	kΩ
I_{swoff}	switch-off current	$R_{swoff(OPTXTAL)}$ = 0.22 kΩ		-	-	1600	µA
		$R_{swoff(OPTXTAL)}$ = 3.3 kΩ		-	500	-	µA
Reference frequency input from external source; pin OPTXTAL							
$V_{OPTXTAL}$	voltage on pin OPTXTAL (DC)	pin open-circuit		2.3	2.6	2.9	V
R_i	input resistance		[3]	-	2	-	kΩ
$V_{ref(RMS)}$	RMS reference voltage			80	-	400	mV
R_O	output resistance	of external reference signal source	[3]	-	2	4.7	kΩ
C_{dec}	decoupling capacitance	to external reference signal source	[3]	22	100	-	pF
Reference frequency input from external source; W7[7] = 0; pin FREF							
V_{FREF}	voltage on pin FREF (DC)	pin open-circuit		2.2	2.5	2.8	V
R_i	input resistance		[3]	50	-	-	kΩ

Table 53. Characteristics *…continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 25 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.375 MHz; f_{SC} = 32.875 MHz; PC / SC = 13 dB; f_{AF} = 400 Hz); input level $V_{i(IF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation: Vestigial SideBand (VSB); residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; internal Nyquist slope switched on (W7[0] = 0); not dual mode; measurements taken in test circuit of Figure 50 and Figure 51; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ref}	reference frequency	[25]	-	4	-	MHz
$V_{ref(RMS)}$	RMS reference voltage	see Figure 34	15	150	500	mV
R_O	output resistance	of external reference signal source; AC-coupled	-	-	4.7	kΩ
C_{dec}	decoupling capacitance	to external reference signal source	22	100	-	pF
$R_{swoff(FREF)}$	switch-off resistance on pin FREF	to switch off reference signal input by external resistor wired between pin FREF and GND	3.9	-	27	kΩ
I_{swoff}	switch-off current	$R_{swoff(FREF)}$ = 3.9 kΩ	-	-	100	µA
		$R_{swoff(FREF)}$ = 22 kΩ	-	75	-	µA
I²C-bus transceiver[27]						
Address select; pin ADRSEL						
V_{ADRSEL}	voltage on pin ADRSEL (DC)	pin open-circuit	-	$0.5V_P$	-	V
		for address select				
		MAD1; pin connected to GND	0	-	$0.04V_P$	V
		MAD3; pin connected to GND via R_{ADRSEL}	$0.12V_P$	-	$0.30V_P$	V
		MAD4; pin connected to V_P via R_{ADRSEL}	$0.66V_P$	-	$0.86V_P$	V
		MAD2; pin connected to V_P	$0.96V_P$	-	V_P	V
R_i	input resistance	[3]	-	35	-	kΩ
R_{ADRSEL}	resistance on pin ADRSEL		42.3	47	51.7	kΩ
I²C-bus voltage select; pin BVS						
V_{BVS}	voltage on pin BVS (DC)	pin open-circuit	-	$0.52V_P$	-	V
$I_{sink(I)}$	input sink current	pin connected to V_P	-	-	10	µA
$I_{source(I)}$	input source current	pin connected to GND	-	-	60	µA
V_I	input voltage	$V_{CC(I2C-bus)}$ = 5.0 V; pin connected to V_P	$0.88V_P$	-	V_P	V
		$V_{CC(I2C-bus)}$ = 3.3 V; pin open-circuit	$0.46V_P$	-	$0.58V_P$	V
		$V_{CC(I2C-bus)}$ = 2.5 V; pin connected to GND	0	-	$0.12V_P$	V

Table 53. Characteristics *...continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 25 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.375 MHz; f_{SC} = 32.875 MHz; PC / SC = 13 dB; f_{AF} = 400 Hz); input level $V_{i(IF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation: Vestigial SideBand (VSB); residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; internal Nyquist slope switched on (W7[0] = 0); not dual mode; measurements taken in test circuit of Figure 50 and Figure 51; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I^2C-bus transceiver; pins SCL and SDA[28]							
V_{IH}	HIGH-level input voltage	$V_{CC(I2C-bus)}$ = 5.0 V	[29]	$0.6V_P$	-	V_P	V
		$V_{CC(I2C-bus)}$ = 3.3 V	[30]	2.3	-	V_P	V
		$V_{CC(I2C-bus)}$ = 2.5 V	[30]	1.75	-	V_P	V
V_{IL}	LOW-level input voltage	$V_{CC(I2C-bus)}$ = 5.0 V	[29]	–0.3	-	$+0.3V_P$	V
		$V_{CC(I2C-bus)}$ = 3.3 V	[30]	–0.3	-	+1.0	V
		$V_{CC(I2C-bus)}$ = 2.5 V	[30]	–0.3	-	+0.75	V
I_{IH}	HIGH-level input current			–10	-	+10	µA
I_{IL}	LOW-level input current			–10	-	+10	µA
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA; for data transmission (SDA)		-	-	0.4	V
f_{SCL}	SCL clock frequency			0	-	400	kHz

[1] Values of video and sound parameters can be decreased at V_P = 4.5 V.

[2] Condition for secure POR is a rise or fall time greater than 2 µs.

[3] This parameter is not tested during the production and is only given as application information for designing the receiver circuit.

[4] Level headroom for input level jumps during gain control setting.

[5] $B_{LF(-3dB)}$ = 100 kHz (damping factor d = 1.9; calculated with sync level within gain control range). Calculation of the VIF PLL filter can be done by use of the following formula:

$$B_{LF(-3dB)} = \frac{1}{2\pi} K_O K_D R \text{, valid for } d \geq 1.2$$

$$d = \frac{1}{2} R \sqrt{K_O K_D C},$$

where:

K_O is the VCO steepness $\left(\frac{rad}{sV}\right)$ or $\left(2\pi\frac{Hz}{V}\right)$; K_D is the phase detector steepness $\left(\frac{A}{rad}\right)$;

R is the loop filter serial resistor (Ω); C is the loop filter serial capacitor (F); $B_{LF(-3dB)}$ is the –3 dB LF bandwidth (Hz); d is the damping factor.

[6] The VCO frequency offset related to the PC frequency is set to 1 MHz with white picture video modulation.

[7] AC load; C_L < 20 pF and R_L > 1 kΩ. The sound carrier frequencies (depending on TV standard) are attenuated by the integrated sound carrier traps.

[8] Condition: luminance range (5 steps) from 0 % to 100 %. Measurement value is based on 4 of 5 steps.

[9] Measurement using 200 kHz high-pass filter, 5 MHz low-pass filter and subcarrier notch filter (*"ITU-T J.64"*).

[10] Modulation VSB; sound carrier off; f_{video} > 0.5 MHz.

[11] Sound carrier on; f_{video} = 10 kHz to 10 MHz.

[12] The sound carrier trap can be bypassed by setting the I^2C-bus bit W2[0] to logic 0; see Table 24. In this way the full composite video spectrum appears at pin CVBS. The video amplitude is reduced to 1.1 V (p-p).

[13] Measurement condition: with transformer, transmitter pre-correction on; reference is at 1 MHz.

[14] The response time is valid for a VIF input level range from 200 µV to 70 mV.

[15] See Figure 19 to smooth current pulses.

[16] To match the AFC output signal to different tuning systems a current output is provided. The test circuit is given in Figure 19. The AFC steepness can be changed by resistors R1 and R2.

[17] The AFC value of the VIF and RIF frequency is generated by using digital counting methods. The used counter resolution is provided with an uncertainty of ±1 bit corresponding to ±25 kHz. This uncertainty of ±25 kHz has to be added to the frequency accuracy parameter.

[18] Measured with an FM deviation of 25 kHz and the typical AF output voltage of 500 mV (RMS). The audio signal processing stage provides headroom of 6 dB with THD < 1.5 %. The I^2C-bus bits W3[0] and W3[1] control the AF output signal amplitude from 0 dB to −18 dB in steps of −6 dB. Reducing the audio gain for handling a frequency deviation of more than 55 kHz avoids AF output signal clipping.

[19] Amplitude response depends on dimensioning of FM PLL loop filter.

[20] The lower AF cut-off frequency depends on the value of the capacitor at pin CAF1. A value of C_{AF1} = 470 nF leads to $f_{-3dB(AF)l}$ ≈ 20 Hz and C_{AF1} = 220 nF leads to $f_{-3dB(AF)l}$ ≈ 40 Hz.

[21] For all signal-to-noise measurements the used VIF modulator has to meet the following specifications:

a) Incidental phase modulation for black-to-white jump less than 0.5 degrees.

b) QSS AF performance, measured with the television demodulator AMF2 (audio output, weighted signal-to-noise ratio) better than 60 dB (at deviation 27 kHz) for 6 kHz sine wave black-to-white video modulation.

c) Picture-to-sound carrier ratio PC / SC1 = 13 dB (transmitter).

[22] The PC / SC ratio is calculated as the addition of TV transmitter PC / SC1 ratio and SAW filter PC / SC1 ratio. This PC / SC ratio is necessary to achieve the weighted signal-to-noise values as noted. A different PC / SC ratio will change these values.

[23] Measurement condition is SC1 / SC2 ≥ 7 dB.

[24] The differential QSS signal output on pins OUT1A and OUT1B is analyzed by a test demodulator TDA9820. The signal-to-noise ratio of this device is better than 60 dB. The measurement is related to an FM deviation of ±27 kHz and in accordance with *"ITU-R BS.468-4"*.

[25] The tolerance of the reference frequency determines the accuracy of VIF AFC, RIF AFC, FM demodulator center frequency, maximum FM deviation, sound trap frequency, LIF band-pass cut-off frequency and ZIF low-pass cut-off frequency as well as the accuracy of the synthesizer.

[26] The value of C_{pull} determines the accuracy of the resonance frequency of the crystal. It depends on the used type of crystal.

[27] The AC characteristics are in accordance with the I^2C-bus specification for fast mode (maximum clock frequency is 400 kHz). Information about the I^2C-bus can be found in the brochure *"The I^2C-bus and how to use it"* (order number 9398 393 40011).

[28] The SDA and SCL lines will not be pulled down if V_P is switched off.

[29] The threshold is dependent on V_P.

[30] The threshold is independent of V_P.

Table 54. Examples to the FM PLL filter

$B_{LF(-3dB)}$ (kHz)	C_s (nF)	C_{par} (pF)	R_s (kΩ)	Comment
210	2.2	100	8.2	recommended for single-carrier-sound, FM narrow
410	2.2	47	5.6	recommended for single-carrier-sound, FM wide
130	2.2	470	5.6	recommended for two-carrier-sound, FM narrow
210	2.2	47	8.2	used for test circuit

Table 55. Input frequencies and carrier ratios (examples)

Symbol	Parameter	B/G standard	M/N standard	L standard	L-accent standard	Unit
f_{PC}	picture carrier frequency	38.375	38.375	38.375	33.625	MHz
f_{SC1}	sound carrier frequency 1	32.825	33.825	31.825	40.125	MHz
f_{SC2}	sound carrier frequency 2	32.583	-	-	-	MHz
PC / SC1	picture to first sound carrier ratio	13	7	10	10	dB
PC / SC2	picture to second sound carrier ratio	20	-	-	-	dB

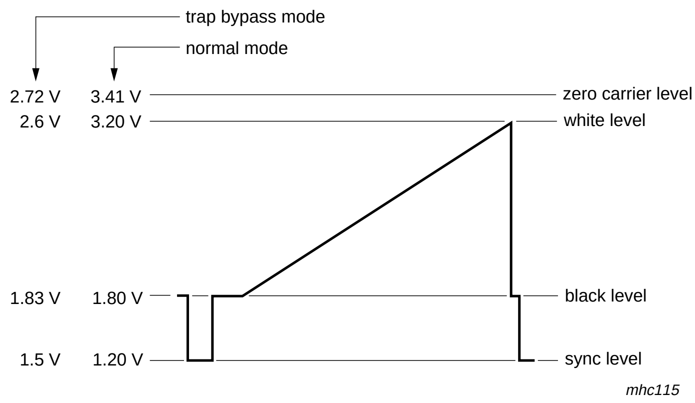


Fig 10. Typical video signal levels on output pin CVBS (sound carrier off)

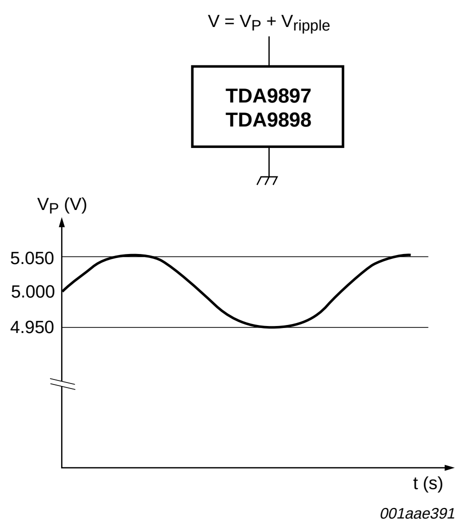
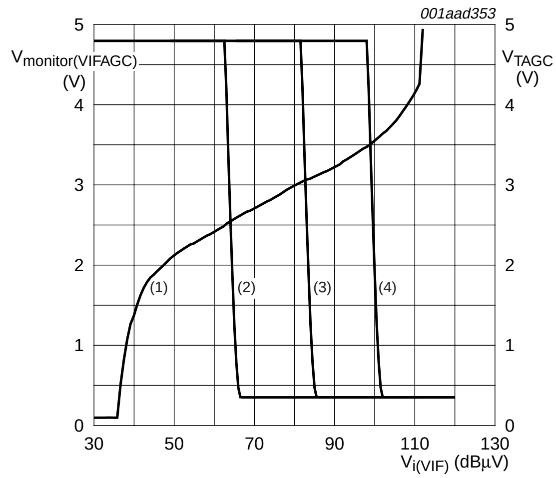


Fig 11. Ripple rejection condition



(1) VIF AGC.

(2) TAGC; W10 = 00h.

(3) TAGC; W10 = 10h.

(4) TAGC; W10 = 1Fh.

Fig 12. Typical VIF monitor and TAGC characteristic

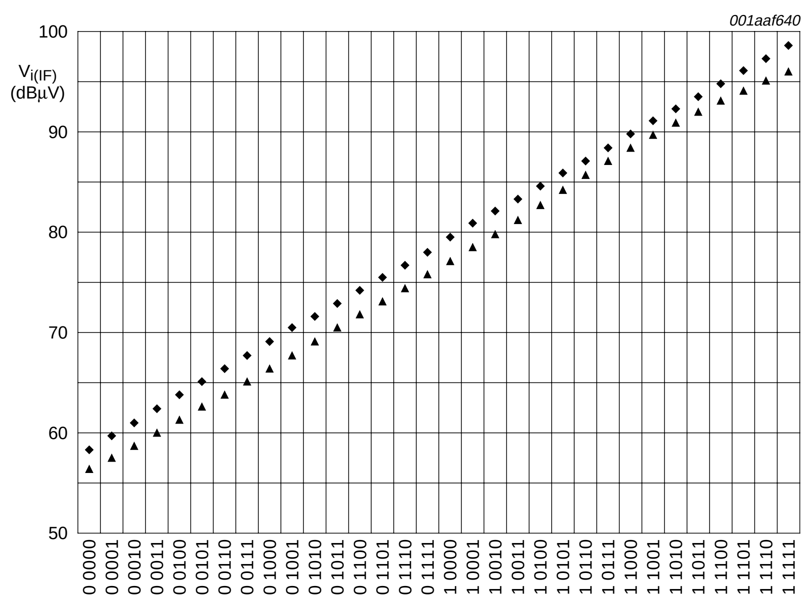
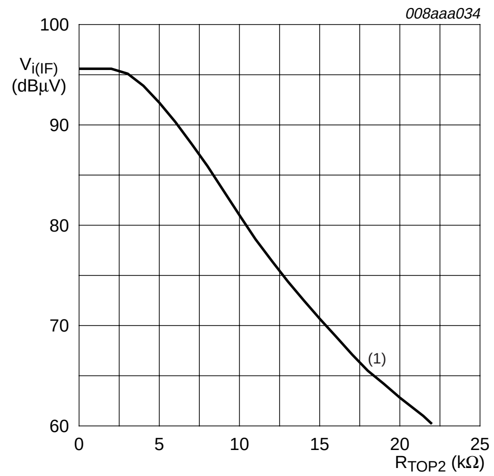


Fig 13. Typical tuner takeover point as a function of I²C-bus register W9 or W10



(1) IF based TAGC (TOP2).

Fig 14. Typical tuner takeover point as a function of resistor R_{TOP2}

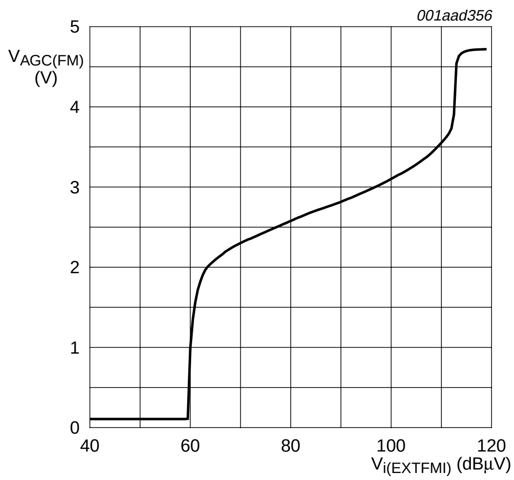
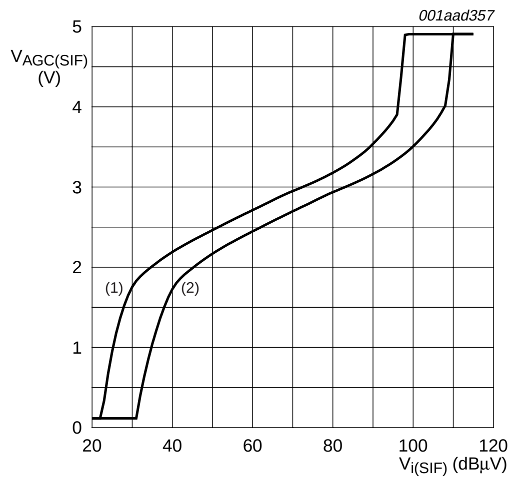


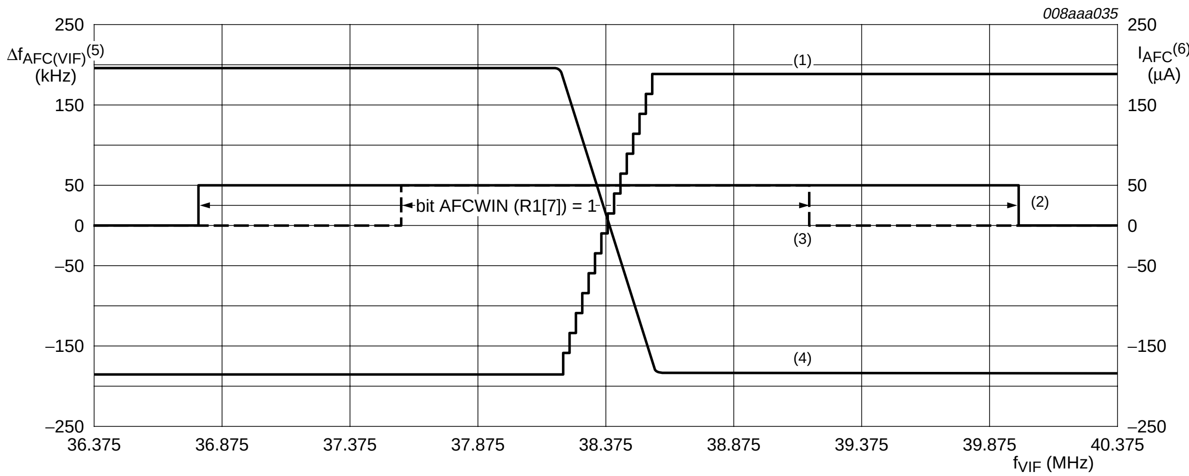
Fig 15. Typical FM AGC characteristic measured at pin MPP2



(1) AM.

(2) FM.

Fig 16. Typical SIF AGC characteristic measured at pin MPP2



(1) VIF AFC via I2C-bus; accuracy is ±1 digit.

(2) Bit AFCWIN via I2C-bus (VCO is in ±1.6 MHz window) for all standards except M/N standard.

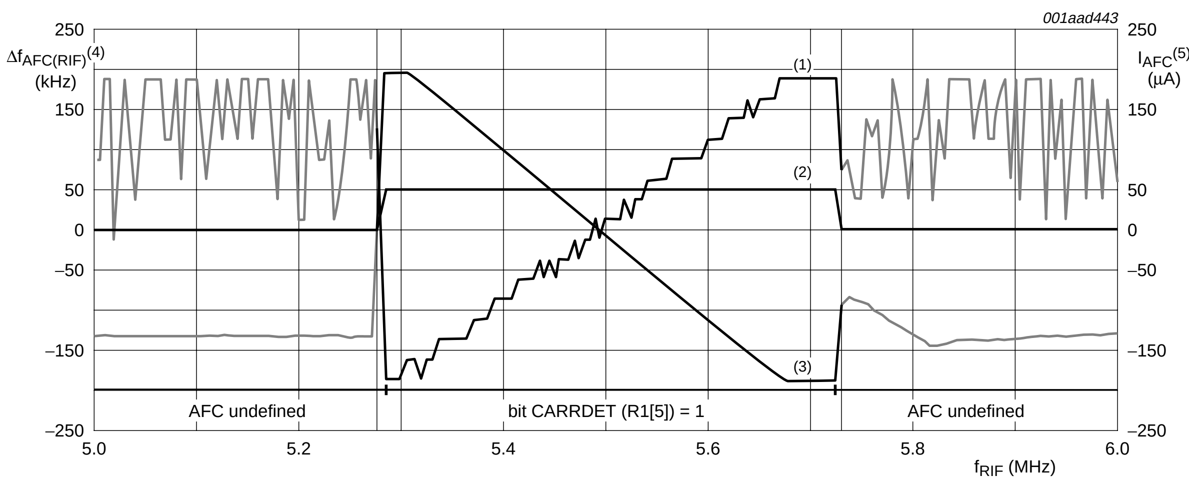
(3) Bit AFCWIN via I2C-bus (VCO is in ±0.8 MHz window) for M/N standard.

(4) VIF AFC average current.

(5) Reading via I2C-bus.

(6) Average; RC network at pin MPP2.

Fig 17. Typical analog and digital AFC characteristic for VIF



Characteristics of digital and analog radio AFC is mirrored with respect to center frequency when lower sideband is used (W2[3] = 0).

(1) RIF AFC via I2C-bus.

(2) FM carrier detection via I2C-bus.

(3) RIF AFC average current.

(4) Reading via I2C-bus.

(5) Average; RC network at pin MPP2.

Fig 18. Typical analog and digital AFC characteristic for RIF

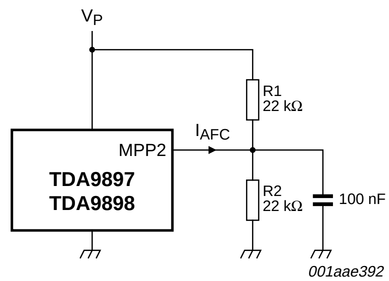
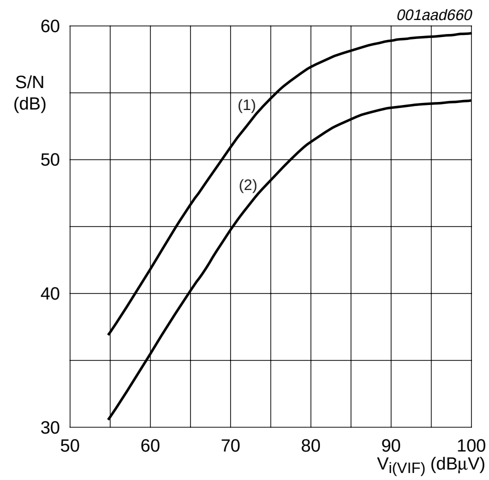


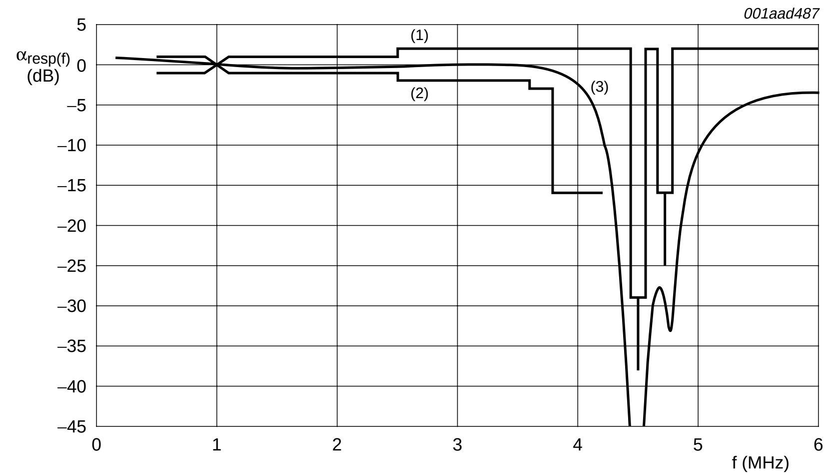
Fig 19. RC network for measurement of analog AFC characteristic



(1) B/G standard; weighted video S/N; using 50 % grey picture.

(2) M/N standard; unweighted video S/N; using 50 IRE grey picture.

Fig 20. Typical signal-to-noise ratio as a function of VIF input voltage

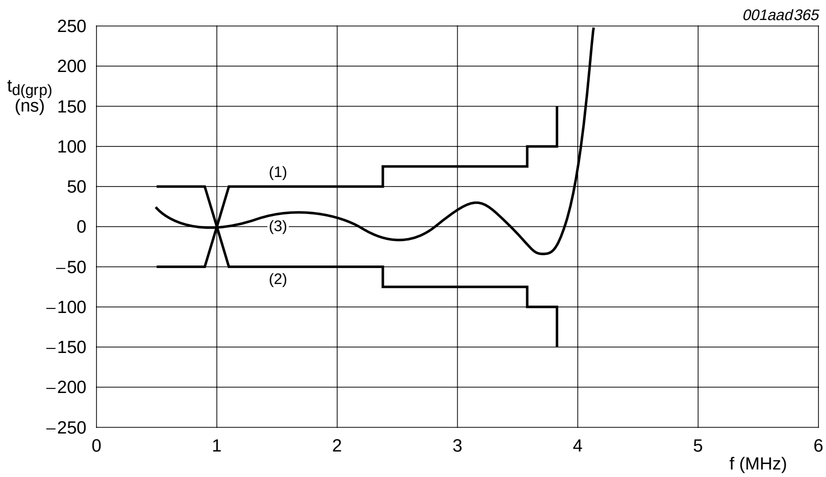


(1) Minimum requirements upper limit.

(2) Minimum requirements lower limit.

(3) Typical trap amplitude frequency response.

Fig 21. Typical amplitude frequency response for sound trap at M/N standard (including Korea)

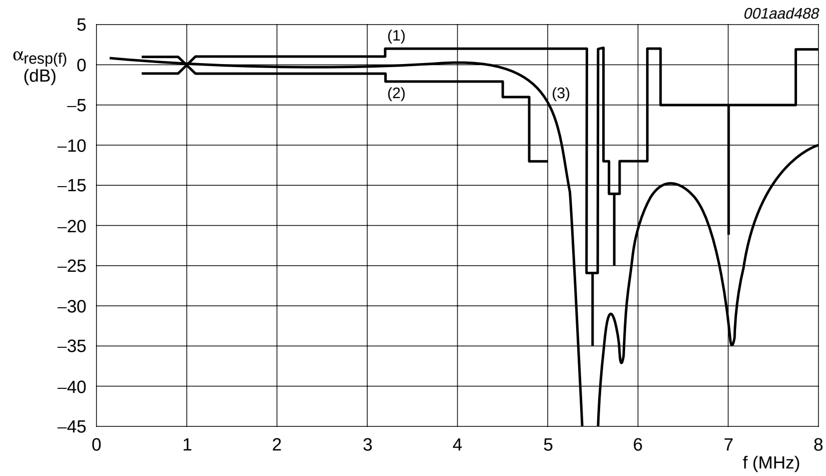


(1) Minimum requirements upper limit.

(2) Minimum requirements lower limit.

(3) Typical trap group delay response.

Fig 22. Typical group delay response for sound trap at M/N standard

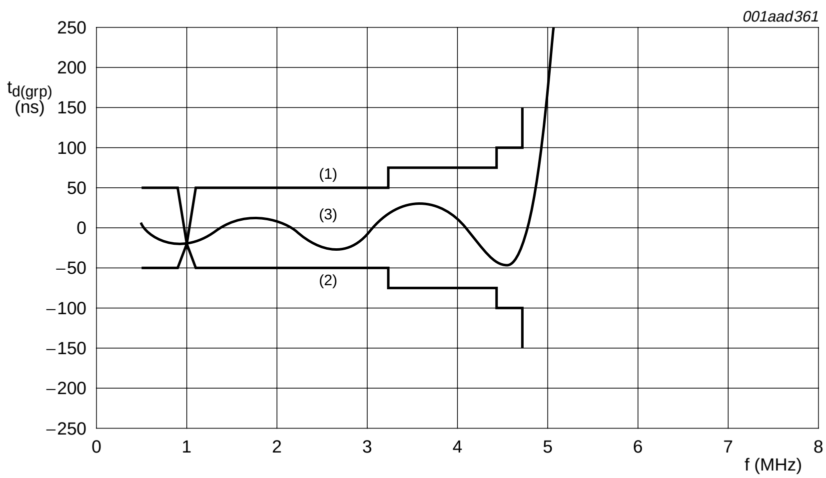


(1) Minimum requirements upper limit.

(2) Minimum requirements lower limit.

(3) Typical trap amplitude frequency response.

Fig 23. Typical amplitude frequency response for sound trap at B/G standard

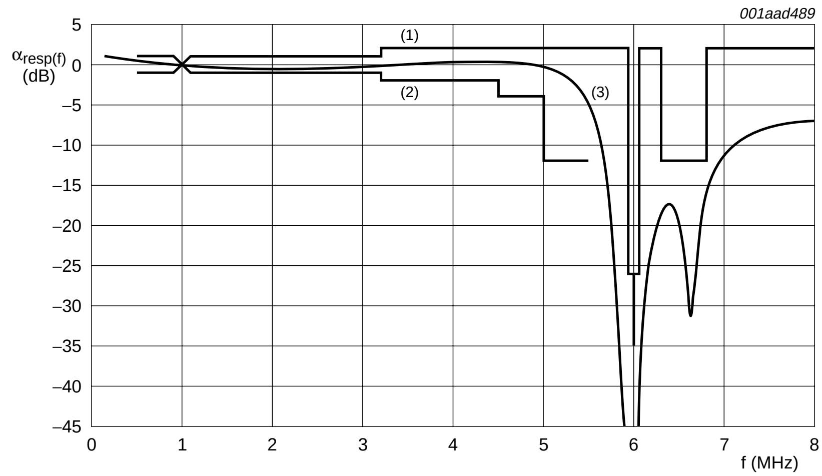


(1) Minimum requirements upper limit.

(2) Minimum requirements lower limit.

(3) Typical trap group delay response.

Fig 24. Typical group delay response for sound trap at B/G standard

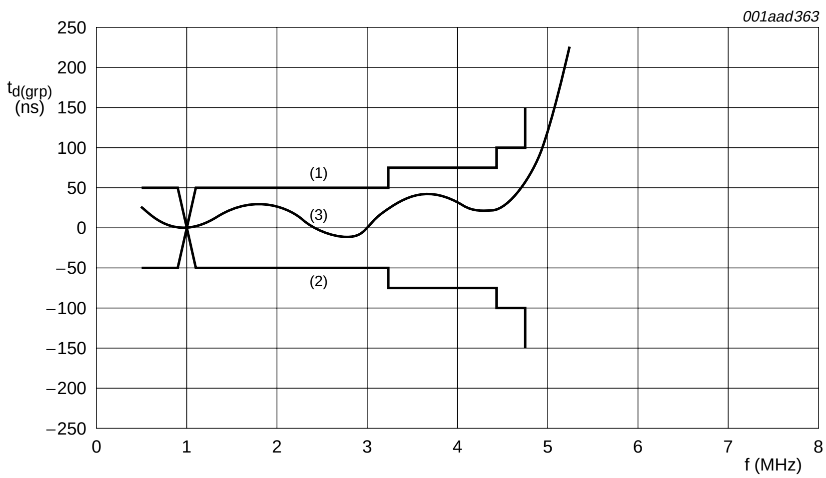


(1) Minimum requirements upper limit.

(2) Minimum requirements lower limit.

(3) Typical trap amplitude frequency response.

Fig 25. Typical amplitude frequency response for sound trap at I standard

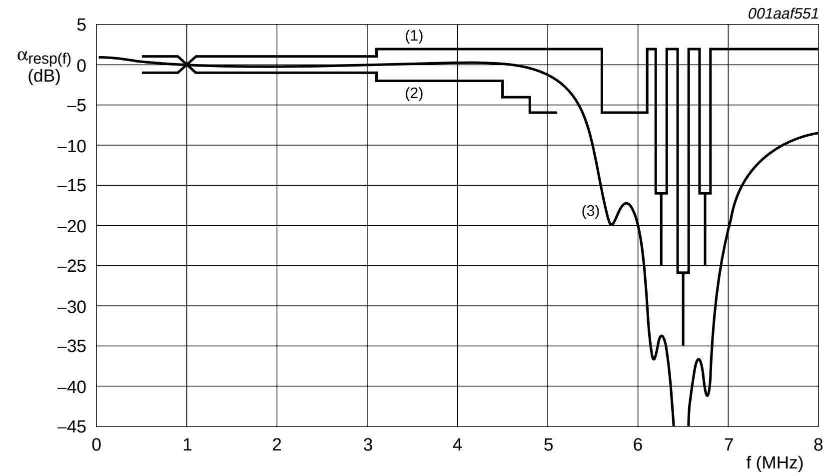


(1) Minimum requirements upper limit.

(2) Minimum requirements lower limit.

(3) Typical trap group delay response.

Fig 26. Typical group delay response for sound trap at I standard

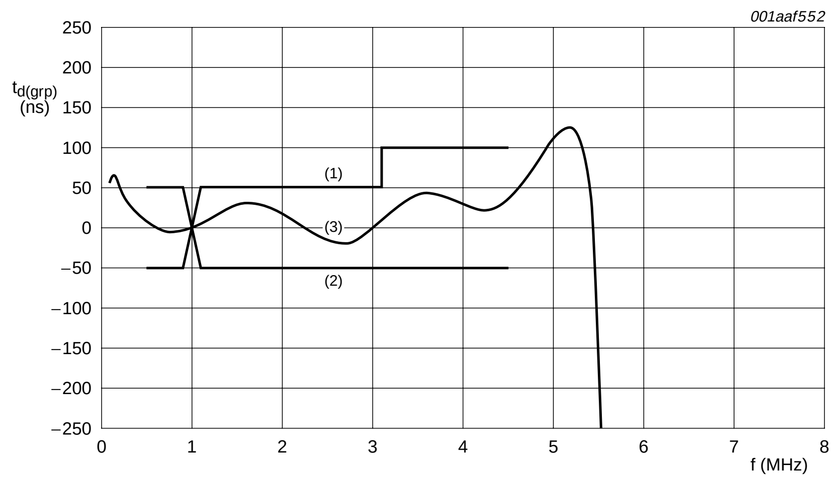


(1) Minimum requirements upper limit.

(2) Minimum requirements lower limit.

(3) Typical trap amplitude frequency response.

Fig 27. Typical amplitude frequency response for sound trap at D/K standard

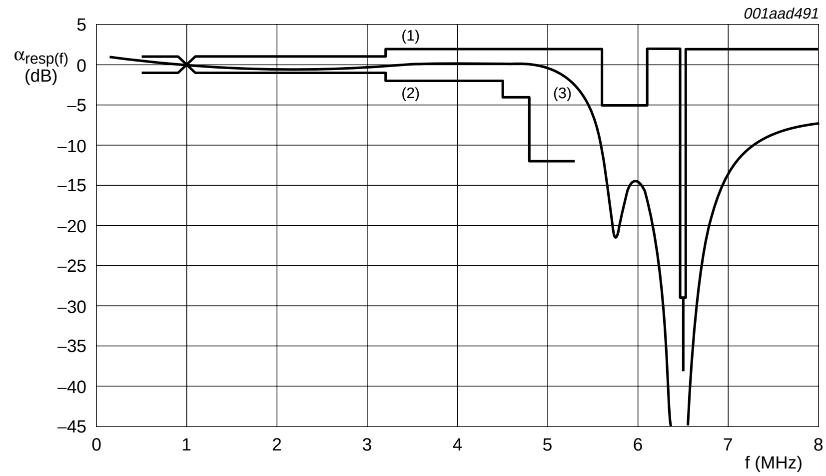


(1) Minimum requirements upper limit.

(2) Minimum requirements lower limit.

(3) Typical trap group delay response.

Fig 28. Typical group delay response for sound trap at D/K standard

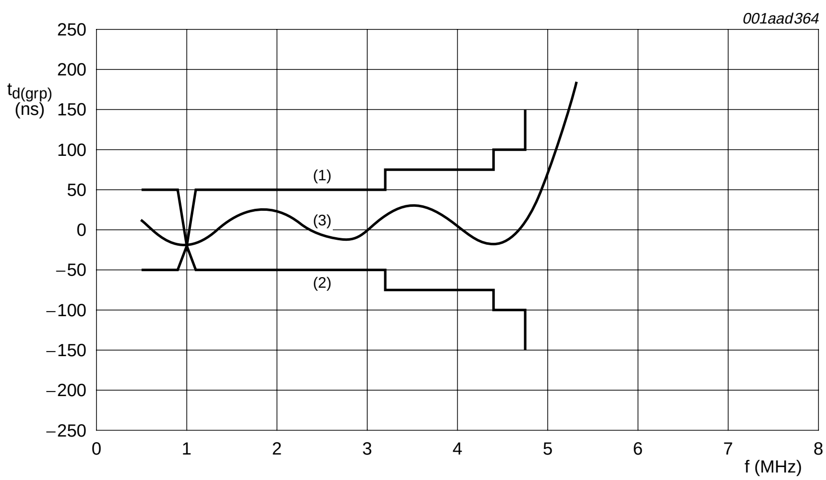


(1) Minimum requirements upper limit.

(2) Minimum requirements lower limit.

(3) Typical trap amplitude frequency response.

Fig 29. Typical amplitude frequency response for sound trap at L standard

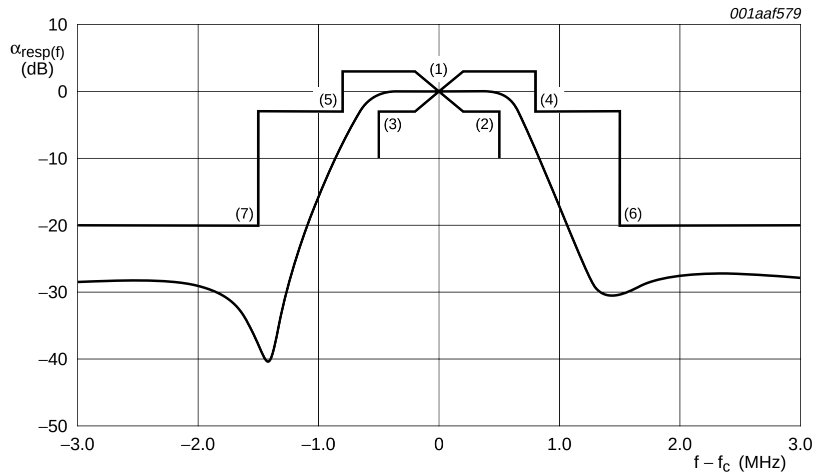


(1) Minimum requirements upper limit.

(2) Minimum requirements lower limit.

(3) Typical trap group delay response.

Fig 30. Typical group delay response for sound trap at L standard



(1) Center frequency.

(2) Minimum upper cut-off frequency.

(3) Minimum lower cut-off frequency.

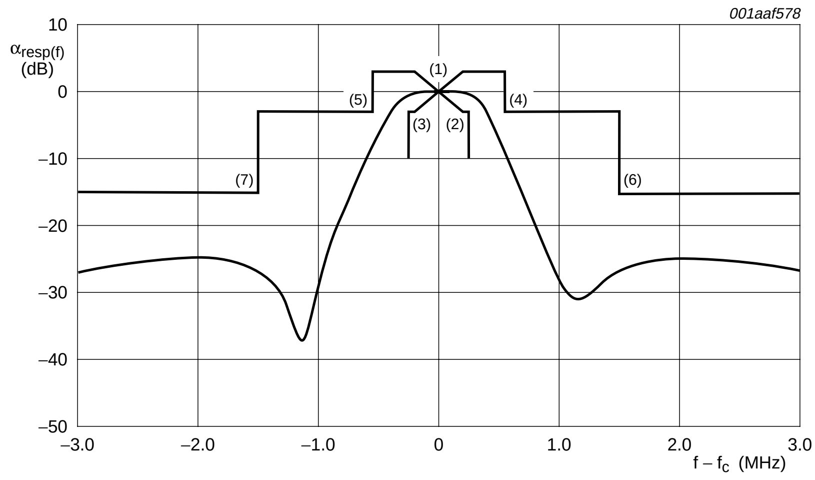
(4) Maximum upper cut-off frequency.

(5) Maximum lower cut-off frequency.

(6) Minimum upper stop-band attenuation.

(7) Minimum lower stop-band attenuation.

Fig 31. Typical sound BP amplitude frequency response at TV mode, normalized to BP center frequency



(1) Center frequency.

(2) Minimum upper cut-off frequency.

(3) Minimum lower cut-off frequency.

(4) Maximum upper cut-off frequency.

(5) Maximum lower cut-off frequency.

(6) Minimum upper stop-band attenuation.

(7) Minimum lower stop-band attenuation.

Fig 32. Typical sound BP amplitude frequency response at radio 10.7 mode, normalized to BP center frequency

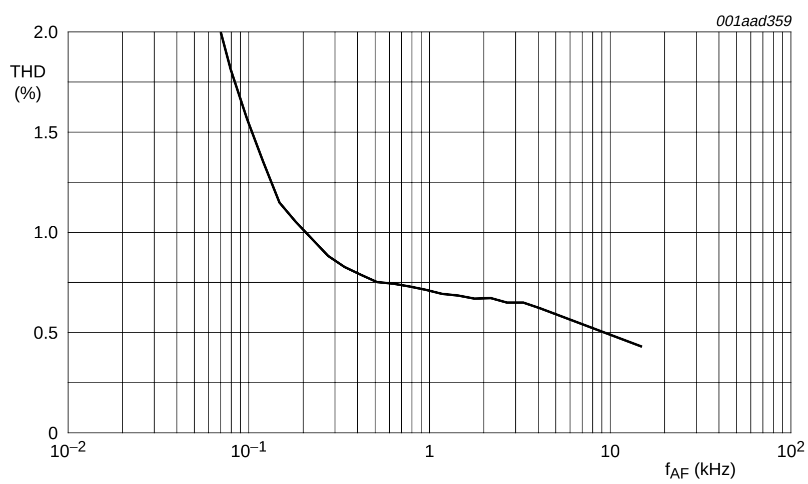
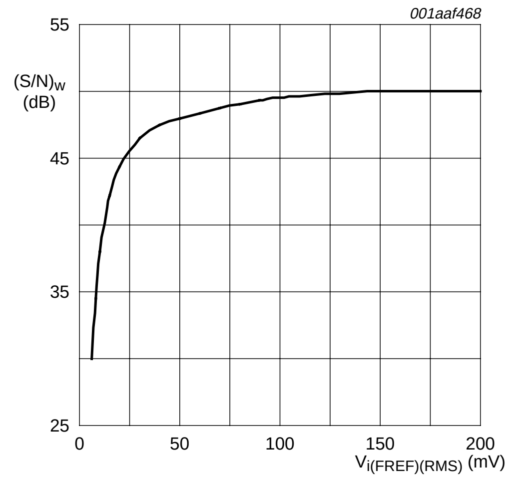
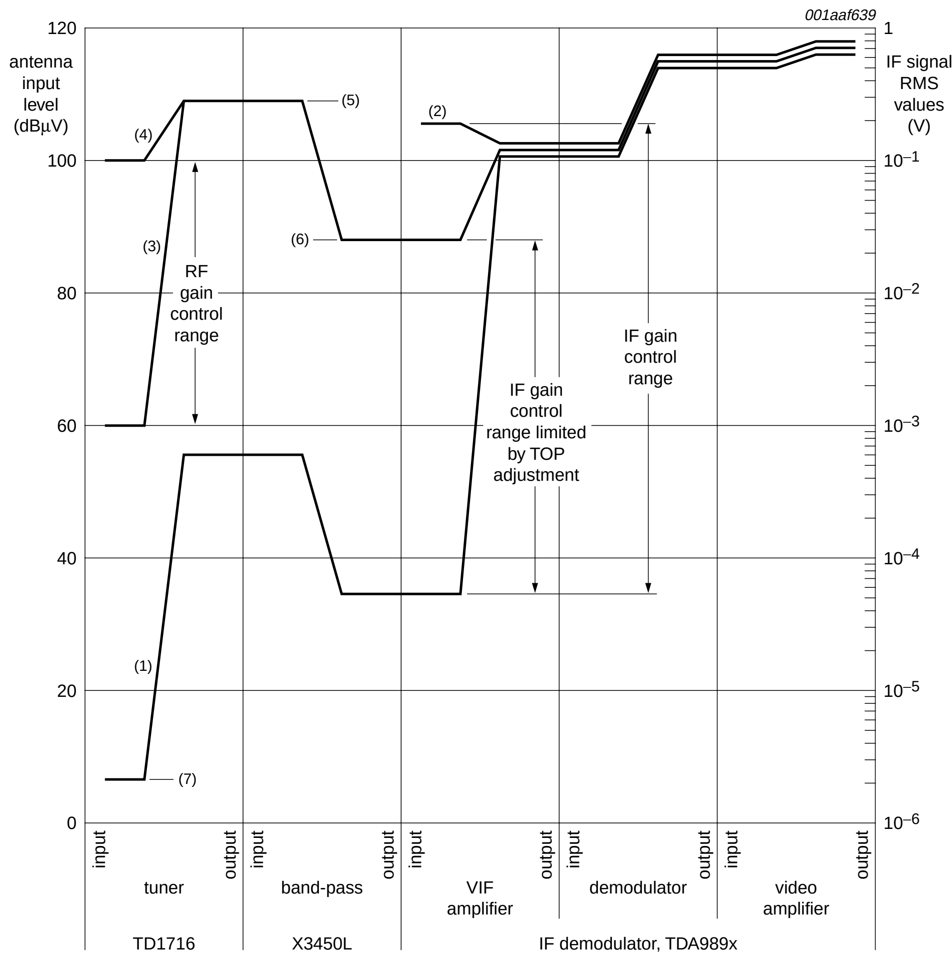


Fig 33. Typical total harmonic distortion as a function of audio frequency at AM standard



Reference frequency input signal taken from external quartz circuit.

Fig 34. Weighted FM audio S/N versus reference frequency input level using radio mode



Video signal related peak-to-peak levels are divided by factor $2\sqrt{2}$ in order to conform with the RMS value scale of the secondary y-axis, but disregarding the none sine wave signal content.

(1) Signal levels for –1 dB video output level using maximum RF gain and maximum IF gain.

(2) Signal levels for +1 dB video output level using minimum IF gain.

(3) Signal levels for TOP-adjusted tuner output level using maximum RF gain and adjustment-related minimum IF gain.

(4) Signal levels for TOP-adjusted tuner output level using minimum RF gain and adjustment-related minimum IF gain.

(5) TOP-adjusted tuner output level.

(6) TOP-adjusted VIF amplifier input level.

(7) Minimum antenna input level at –1 dB video level.

Fig 35. Front-end level diagram

12.2 Digital TV signal processing

Table 56. Characteristics

V_P = 5 V[1]; T_{amb} = 25 °C; 8 MHz system; see Table 34 and Table 35; CW test input signal is used for specification; $V_{i(IF)}$ = 10 mV (RMS); f_{IF} = 36 MHz for low IF output of 5 MHz; IF input from 50 Ω via broadband transformer 1 : 1; gain controlled amplifier adjusted to typical specified output level; measurements taken in test circuit of Figure 50 and Figure 51 with 4 MHz crystal oscillator reference; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
IF amplifier; pins IF3A and IF3B or IF1A and IF1B or IF2A and IF2B							
V_I	input voltage			1.8	1.93	2.2	V
$R_{i(dif)}$	differential input resistance		[2]	-	2	-	kΩ
$C_{i(dif)}$	differential input capacitance		[2]	-	3	-	pF
$G_{IF(cr)}$	control range IF gain		[2]	60	66	-	dB
DTV differential output; pins OUT1A, OUT1B, OUT2A and OUT2B							
V_O	output voltage	pin open-circuit		1.8	2.0	2.2	V
$I_{bias(int)}$	internal bias current (DC)	for emitter-follower		2.0	2.5	-	mA
$I_{sink(o)(max)}$	maximum output sink current	DC and AC; see Figure 36	[3]	1.4	1.7	-	mA
$I_{source(o)(max)}$	maximum output source current	DC and AC; see Figure 36	[3]	6.0	-	-	mA
R_O	output resistance	differential; output active	[2]	-	-	50	Ω
		output inactive; internal resistance to GND	[2]	-	800	-	Ω
$V_{i(IF)(RMS)}$	RMS IF input voltage	minimum input sine wave level for nominal output level		-	70	100	µV
		maximum input sine wave level for nominal output level		130	170	-	mV
		permissible overload	[2]	-	-	320	mV
Direct IF; pins OUT2A and OUT2B							
$G_{IF(max)}$	maximum IF gain	output peak-to-peak level to input RMS level ratio	[2]	-	83	-	dB
$V_{o(dif)(p-p)}$	peak-to-peak differential output voltage	between pin OUT2A and pin OUT2B	[4]				
		W4[7] = 0		-	1.0	1.1	V
		W4[7] = 1		-	0.50	0.55	V
C/N	carrier-to-noise ratio	at f_o = 33.4 MHz; see Figure 37	[2][5][6]				
		$V_{i(IF)}$ = 10 mV (RMS)		115	124	-	dBc/Hz
		$V_{i(IF)}$ = 0.5 mV (RMS)		90	104	-	dBc/Hz
α_{IM}	intermodulation suppression	input signals: f_i = 47.0 MHz and 57.5 MHz; output signals: f_o = 36.5 MHz or 68.0 MHz; see Figure 38	[2]				
		W4[7] = 0		40	-	-	dB
		W4[7] = 1		40	-	-	dB

Table 56. Characteristics *…continued*

V_P = 5 V[1]; T_{amb} = 25 °C; 8 MHz system; see Table 34 and Table 35; CW test input signal is used for specification; $V_{i(IF)}$ = 10 mV (RMS); f_{IF} = 36 MHz for low IF output of 5 MHz; IF input from 50 Ω via broadband transformer 1 : 1; gain controlled amplifier adjusted to typical specified output level; measurements taken in test circuit of Figure 50 and Figure 51 with 4 MHz crystal oscillator reference; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$f_{IF(-1dB)l}$	lower −1 dB IF cut-off frequency		[2]	-	7	-	MHz
$f_{-3dB(IF)u}$	upper IF cut-off frequency	W4[7] = 0	[4]	60	-	-	MHz
		W4[7] = 1	[7]	60	-	-	MHz
PSRR	power supply ripple rejection	residual spurious at nominal differential output voltage dependent on power supply ripple	[2]				
		f_{ripple} = 70 Hz		-	60	-	dB
		f_{ripple} = 20 kHz		-	60	-	dB
Low or zero IF output signal; pins OUT1A and OUT1B or pins OUT2A and OUT2B; differential							
$G_{IF(max)}$	maximum IF gain	output peak-to-peak level to input RMS level ratio	[2]	-	89	-	dB
f_{synth}	synthesizer frequency	see Table 35 and Table 36		-	-	-	MHz
$V_{o(dif)(p-p)}$	peak-to-peak differential output voltage	W4[7] = 0	[4]	-	2	-	V
		W4[7] = 1	[4]	-	1	-	V
PSRR	power supply ripple rejection	residual spurious at nominal differential output voltage dependent on power supply ripple	[2]				
		f_{ripple} = 70 Hz		-	50	-	dB
		f_{ripple} = 20 kHz		-	30	-	dB
Low IF output signal; pins OUT1A and OUT1B							
$\alpha_{ripple(pb)LIF}$	low IF pass-band ripple	6 MHz bandwidth		-	-	2.7	dB
		7 MHz bandwidth		-	-	2.7	dB
		8 MHz bandwidth		-	-	2.7	dB
B_{-3dB}	−3 dB bandwidth	BP off	[4]	11	15	-	MHz
		6 MHz bandwidth	[4]	-	7.8	-	MHz
		7 MHz bandwidth	[4]	-	8.8	-	MHz
		8 MHz bandwidth	[4]	-	9.8	-	MHz
α_{stpb}	stop-band attenuation	6 MHz band; f = 11.75 MHz		30	40	-	dB
		6 MHz band; f = 20 MHz		28	35	-	dB
		7 MHz band; f = 13.75 MHz		30	40	-	dB
		7 MHz band; f = 20 MHz		28	35	-	dB
		8 MHz band; f = 15.75 MHz		30	40	-	dB
		8 MHz band; f = 20 MHz		28	35	-	dB

Table 56. Characteristics *…continued*

V_P = 5 V[1]; T_{amb} = 25 °C; 8 MHz system; see Table 34 and Table 35; CW test input signal is used for specification; $V_{i(IF)}$ = 10 mV (RMS); f_{IF} = 36 MHz for low IF output of 5 MHz; IF input from 50 Ω via broadband transformer 1 : 1; gain controlled amplifier adjusted to typical specified output level; measurements taken in test circuit of Figure 50 and Figure 51 with 4 MHz crystal oscillator reference; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$\Delta t_{d(grp)}$	group delay time variation	from 1 MHz to 2 MHz	[2]	-	90	200	ns
		from 2 MHz to end of band with a bandwidth of	[2]				
		6 MHz		-	90	160	ns
		7 MHz		-	90	160	ns
		8 MHz		-	90	160	ns
α_{image}	image rejection	−10 MHz to 0 MHz					
		BP on		30	34	-	dB
		BP off		24	28	-	dB
C/N	carrier-to-noise ratio	at f_o = 4.9 MHz; see Figure 37	[2][5][6]				
		$V_{i(IF)}$ = 10 mV (RMS)		112	118	-	dBc/Hz
		$V_{i(IF)}$ = 0.5 mV (RMS)		90	104	-	dBc/Hz
$\alpha_{H(ib)}$	in-band harmonics suppression	low IF = multiple of 1.31 MHz; $f_i = f_{synth}$ + 1.31 MHz; see Figure 41	[2]				
		W4[7] = 0		40	-	-	dB
		W4[7] = 1		40	-	-	dB
α_{IM}	intermodulation suppression	input signals: $f_i = f_{synth}$ + 4.7 MHz and f_{synth} + 5.3 MHz; output signals: f_o = 4.1 MHz or 5.9 MHz; see Figure 40	[2]				
		W4[7] = 0		40	-	-	dB
		W4[7] = 1		40	-	-	dB
$\alpha_{sp(ib)}$	in-band spurious suppression	single-ended AC load; R_L = 1 kΩ; C_L = 5 pF; 1 MHz to end of band; BP on	[2]	50	-	-	dB
$\alpha_{sp(ob)}$	out-band spurious suppression	single-ended AC load; R_L = 1 kΩ; C_L = 5 pF; BP on	[2]	50	-	-	dB
Zero IF output signal; pins OUT1A and OUT1B or pins OUT2A and OUT2B							
$\alpha_{ripple(pb)ZIF}$	zero IF pass-band ripple	3.0 MHz bandwidth		-	-	1.8	dB
		3.5 MHz bandwidth		-	-	1.8	dB
		4.0 MHz bandwidth		-	-	1.8	dB
B_{-3dB}	−3 dB bandwidth	BP off	[4]	11	15	-	MHz
		3.0 MHz bandwidth	[4]	-	3.7	-	MHz
		3.5 MHz bandwidth	[4]	-	4.2	-	MHz
		4.0 MHz bandwidth	[4]	-	4.7	-	MHz

Table 56. Characteristics *…continued*

V_P = 5 V[1]; T_{amb} = 25 °C; 8 MHz system; see Table 34 and Table 35; CW test input signal is used for specification; $V_{i(IF)}$ = 10 mV (RMS); f_{IF} = 36 MHz for low IF output of 5 MHz; IF input from 50 Ω via broadband transformer 1 : 1; gain controlled amplifier adjusted to typical specified output level; measurements taken in test circuit of Figure 50 and Figure 51 with 4 MHz crystal oscillator reference; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
α_{stpb}	stop-band attenuation	3.0 MHz band; f = 7.75 MHz		30	40	-	dB
		3.5 MHz band; f = 9.25 MHz		30	40	-	dB
		4.0 MHz band; f = 10.75 MHz		30	40	-	dB
		any band; f = 15 MHz		28	35	-	dB
$\Delta t_{d(grp)}$	group delay time variation	from 0 MHz to end of band with a bandwidth of	[2]				
		3.0 MHz		-	60	100	ns
		3.5 MHz		-	50	100	ns
		4.0 MHz		-	45	100	ns
C/N	carrier-to-noise ratio	at f_o = 1.9 MHz; see Figure 37	[2][5][6]				
		$V_{i(IF)}$ = 10 mV (RMS)		112	121	-	dBc/Hz
		$V_{i(IF)}$ = 0.5 mV (RMS)		87	101	-	dBc/Hz
α_{IM}	intermodulation suppression	input signals: $f_i = f_{synth}$ + 1.7 MHz and f_{synth} + 2.3 MHz; output signals: f_o = 1.1 MHz or 2.9 MHz; see Figure 39		40	-	-	dB
$\alpha_{sp(ib)}$	in-band spurious suppression	0.437 MHz to end of band; BP on	[2][4]	40	-	-	dB
$\alpha_{sp(ob)}$	out-band spurious suppression	BP on	[2][4]	50	-	-	dB
$\Delta\varphi$	phase difference	mismatch between I and Q channel	[2]	-	-	6	deg
ΔG	gain mismatch	mismatch between I and Q channel		-	-	2	dB
IF AGC control; pin AGCDIN							
$I_{sink(i)(max)}$	maximum input sink current		[2]	-	-	2	µA
$V_{i(max)}$	maximum input voltage		[2]	-	-	V_P	V
V_{AGCDIN}	voltage on pin AGCDIN		[2]	0	-	3	V
$\Delta G_{IF}/\Delta V_{AGCDIN}$	change of IF gain with voltage on pin AGCDIN	V_{AGCDIN} = 0.8 V to 2.2 V		-	–45	-	dB/V

Table 56. Characteristics *…continued*

V_P = 5 V[1]; T_{amb} = 25 °C; 8 MHz system; see Table 34 and Table 35; CW test input signal is used for specification; $V_{i(IF)}$ = 10 mV (RMS); f_{IF} = 36 MHz for low IF output of 5 MHz; IF input from 50 Ω via broadband transformer 1 : 1; gain controlled amplifier adjusted to typical specified output level; measurements taken in test circuit of Figure 50 and Figure 51 with 4 MHz crystal oscillator reference; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Tuner AGC; pin TAGC							
Integral TAGC loop mode (W6[7:6] = 10); TAGC is current output; unmodulated IF							
$V_{i(IF)(RMS)}$	RMS IF input voltage	at starting point of tuner AGC takeover; $I_{sink(TAGC)}$ = 100 µA					
		W9[4:0] = 0 0000		-	57.9	-	dBµV
		W9[4:0] = 1 0000		-	78.7	-	dBµV
		W9[4:0] = 1 1111		-	98.2	-	dBµV
$\alpha_{acc(set)TOP}$	TOP setting accuracy			–2	-	+2	dB
I_{source}	source current	TAGC charge current					
		normal mode		0.20	0.27	0.34	µA
		fast mode activated by internal level detector		7	10	13	µA
I_{sink}	sink current	TAGC discharge current; V_{TAGC} = 1 V		400	500	600	µA
$\Delta\alpha_{acc(set)TOP}/\Delta T$	TOP setting accuracy variation with temperature	$I_{sink(TAGC)}$ = 100 µA; W9[4:0] = 1 0000	[2]	-	-	0.02	dB/K
R_L	load resistance		[2]	50	-	-	MΩ
$V_{sat(u)}$	upper saturation voltage	pin operating as current output	[2]	V_P – 0.3	-	-	V
$V_{sat(l)}$	lower saturation voltage	pin operating as current output	[2]	-	-	0.3	V
$\alpha_{th(fast)AGC}$	AGC fast mode threshold	activated by internal fast AGC detector; I^2C-bus setting corresponds to W9[4:0] = 1 0000	[2]	6	8	10	dB
t_d	delay time	before activating; $V_{i(IF)}$ below $\alpha_{th(fast)AGC}$	[2]	40	60	80	ms
Filter synthesizer PLL; pin LFSYN1							
V_{LFSYN1}	voltage on pin LFSYN1			1.0	-	3.5	V
K_O	VCO steepness	$\Delta f_{VCO} / \Delta V_{LFSYN1}$		-	3.75	-	MHz/V
K_D	phase detector steepness	$\Delta I_{LFSYN1} / \Delta\varphi_{VCO}$		-	9	-	µA/rad
$I_{sink(o)PD(max)}$	maximum phase detector output sink current			-	-	65	µA
$I_{source(o)PD(max)}$	maximum phase detector output source current			-	-	65	µA

Table 56. Characteristics *...continued*

V_P = 5 V[1]; T_{amb} = 25 °C; 8 MHz system; see Table 34 and Table 35; CW test input signal is used for specification; $V_{i(IF)}$ = 10 mV (RMS); f_{IF} = 36 MHz for low IF output of 5 MHz; IF input from 50 Ω via broadband transformer 1 : 1; gain controlled amplifier adjusted to typical specified output level; measurements taken in test circuit of Figure 50 and Figure 51 with 4 MHz crystal oscillator reference; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Conversion synthesizer PLL; pin LFSYN2							
V_{LFSYN2}	voltage on pin LFSYN2			1	-	3	V
K_O	VCO steepness	$\Delta f_{VCO} / \Delta V_{LFSYN2}$		-	31	-	MHz/V
K_D	phase detector steepness	$\Delta I_{LFSYN2} / \Delta\varphi_{VCO}$; see Table 57; f_{VCO} selection:					
		22 MHz to 29.5 MHz		-	32	-	µA/rad
		30 MHz to 37.5 MHz		-	38	-	µA/rad
		38 MHz to 45.5 MHz		-	47	-	µA/rad
		46 MHz to 53.5 MHz		-	61	-	µA/rad
		57 MHz		-	61	-	µA/rad
$I_{o(PD)}$	phase detector output current	sink or source; f_{VCO} selection:					
		22 MHz to 29.5 MHz		-	200	-	µA
		30 MHz to 37.5 MHz		-	238	-	µA
		38 MHz to 45.5 MHz		-	294	-	µA
		46 MHz to 53.5 MHz		-	384	-	µA
		57 MHz		-	384	-	µA
$\varphi_{n(synth)}$	synthesizer phase noise	f_{synth} = 31 MHz; f_{IF} = 36 MHz					
		at 1 kHz	[2]	89	99	-	dBc/Hz
		at 10 kHz	[2]	89	99	-	dBc/Hz
		at 100 kHz	[2]	98	102	-	dBc/Hz
		at 1.4 MHz	[2]	115	119	-	dBc/Hz
		f_{synth} = 40 MHz; f_{IF} = 44 MHz; external 4 MHz reference signal of 265 mV (RMS) and phase noise better than 120 dBc/Hz; see Figure 46					
		at 1 kHz	[2]	89	96	-	dBc/Hz
		at 10 kHz	[2]	89	100	-	dBc/Hz
		at 100 kHz	[2]	96	100	-	dBc/Hz
		at 1.4 MHz	[2]	115	118	-	dBc/Hz
α_{sp}	spurious suppression	multiple of Δf = 500 kHz	[2]	50	-	-	dBc
I_L	leakage current	synthesizer spurious performance > 50 dBc	[2]	-	-	10	nA
Reference frequency							
General							
f_{ref}	reference frequency		[8]	-	4	-	MHz

Table 56. Characteristics *…continued*

V_P = 5 V[1]; T_{amb} = 25 °C; 8 MHz system; see Table 34 and Table 35; CW test input signal is used for specification; $V_{i(IF)}$ = 10 mV (RMS); f_{IF} = 36 MHz for low IF output of 5 MHz; IF input from 50 Ω via broadband transformer 1 : 1; gain controlled amplifier adjusted to typical specified output level; measurements taken in test circuit of Figure 50 and Figure 51 with 4 MHz crystal oscillator reference; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Reference frequency generation with crystal; pin OPTXTAL							
$V_{OPTXTAL}$	voltage on pin OPTXTAL (DC)	pin open-circuit		2.3	2.6	2.9	V
R_i	input resistance		[2]	-	2	-	kΩ
$R_{rsn(xtal)}$	crystal resonance resistance			-	-	200	Ω
C_{pull}	pull capacitance		[9]	-	-	-	pF
$R_{swoff(OPTXTAL)}$	switch-off resistance on pin OPTXTAL	to switch off crystal input by external resistor wired between pin OPTXTAL and GND		0.22	-	4.7	kΩ
I_{swoff}	switch-off current	$R_{swoff(OPTXTAL)}$ = 0.22 kΩ		-	-	1600	µA
		$R_{swoff(OPTXTAL)}$ = 3.3 kΩ		-	500	-	µA
Reference frequency input from external source; pin OPTXTAL							
$V_{OPTXTAL}$	voltage on pin OPTXTAL (DC)	pin open-circuit		2.3	2.6	2.9	V
R_i	input resistance		[2]	-	2	-	kΩ
$V_{ref(RMS)}$	RMS reference voltage			80	-	400	mV
R_O	output resistance	of external reference signal source	[2]	-	2	4.7	kΩ
C_{dec}	decoupling capacitance	to external reference signal source	[2]	22	100	-	pF
Reference frequency input from external source; W7[7] = 0; pin FREF							
V_{FREF}	voltage on pin FREF (DC)	pin open-circuit		2.2	2.5	2.8	V
R_i	input resistance		[2]	50	-	-	kΩ
f_{ref}	reference frequency		[8]	-	4	-	MHz
$V_{ref(RMS)}$	RMS reference voltage	see Figure 46		15	150	500	mV
R_O	output resistance	of external reference signal source; AC-coupled		-	-	4.7	kΩ
C_{dec}	decoupling capacitance	to external reference signal source		22	100	-	pF
$R_{swoff(FREF)}$	switch-off resistance on pin FREF	to switch off reference signal input by external resistor wired between pin FREF and GND		3.9	-	27	kΩ
I_{swoff}	switch-off current	$R_{swoff(FREF)}$ = 3.9 kΩ		-	-	100	µA
		$R_{swoff(FREF)}$ = 22 kΩ		-	75	-	µA

[1] Some parameters can be decreased at V_P = 4.5 V.

[2] This parameter is not tested during production and is only given as application information.

[3] Output current can be increased by application of single-ended resistor from each output pin to GND. Recommended resistor value is minimum 1 kΩ.

[4] With single-ended load for f_{IF} < 45 MHz $R_L \geq 1$ kΩ and $C_L \leq 5$ pF to ground and for f_{IF} = 45 MHz to 60 MHz $R_L = 1$ kΩ and $C_L \leq 3$ pF to ground.

[5] Noise level is measured without input signal but AGC adjusted corresponding to the given input level.

[6] Set with AGC nominal output voltage as reference. For C/N measurement switch input signal off.

[7] With single-ended load $R_L \geq 1$ kΩ and $C_L \leq 5$ pF to ground.

[8] The tolerance of the reference frequency determines the accuracy of VIF AFC, RIF AFC, FM demodulator center frequency, maximum FM deviation, sound trap frequency, LIF band-pass cut-off frequency and ZIF low-pass cut-off frequency as well as the accuracy of the synthesizer.

[9] The value of C_{pull} determines the accuracy of the resonance frequency of the crystal. It depends on the used type of crystal.

Table 57. Conversion synthesizer PLL; loop filter dimensions[1]

f_{VCO} (MHz)	R_{LFSYN2} (kΩ)[2]	C_{LFSYN2} (nF)
22 to 29.5	1.5	4.7
30 to 37.5	1.8	4.7
38 to 45.5	2.2	4.7
46 to 53.5	2.7	4.7
57	3.3	4.7

[1] Calculation of the PLL loop filter by using the following formulae, valid under the condition for the damping factor d ≥ 1.2. $B_{LF(-3dB)} = \frac{K_O}{N} K_D R_{LFSYN2}$ and $d = \frac{1}{2} R_{LFSYN2} \sqrt{2\pi \frac{K_O}{N} K_D C_{LFSYN2}}$ with the following parameters

K_O = VCO steepness (MHz/V),

N = divider ratio: $N = \frac{f_{VCO}}{0.5\ MHz}$,

K_D = phase frequency detector steepness (μA/rad),

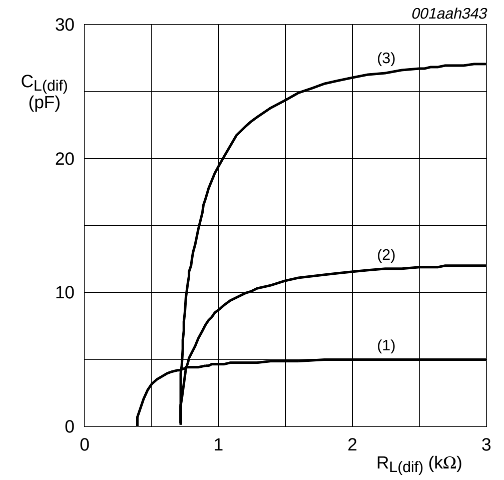
R_{LFSYN2} = synthesizer loop filter serial resistor (Ω),

C_{LFSYN2} = synthesizer loop filter serial capacitor (F),

$B_{LF(-3dB)}$ = −3 dB LF bandwidth (Hz),

d = damping factor.

[2] If more than one frequency range is used in the application, then the smallest resistor value should be applied.



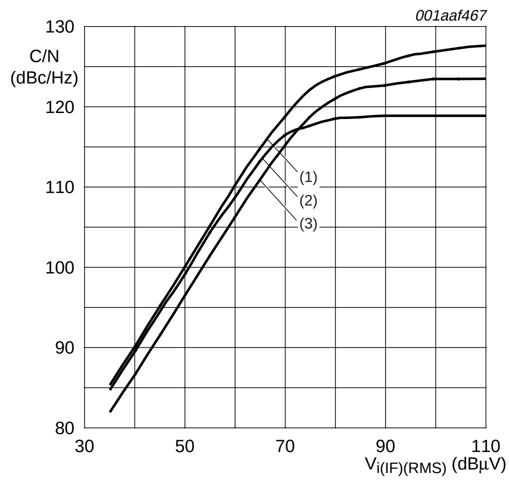
W4[7] = 0; nominal output level

(1) Direct IF, f_{max} = 40 MHz, with single-ended resistors of 1 kΩ to GND.

(2) Low IF, f_{max} = 9 MHz.

(3) Zero IF, f_{max} = 4 MHz.

Fig 36. Maximum differential load figures at OUT1/OUT2

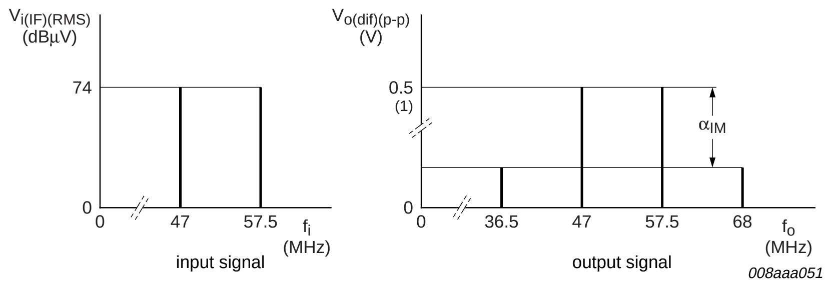


(1) Direct IF.

(2) Low IF.

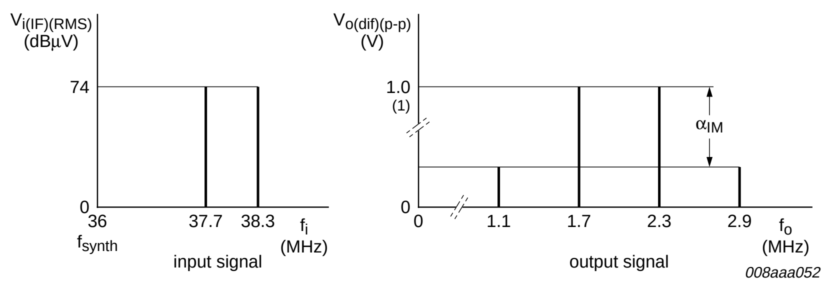
(3) Zero IF.

Fig 37. Typical C/N ratio as a function of IF input voltage



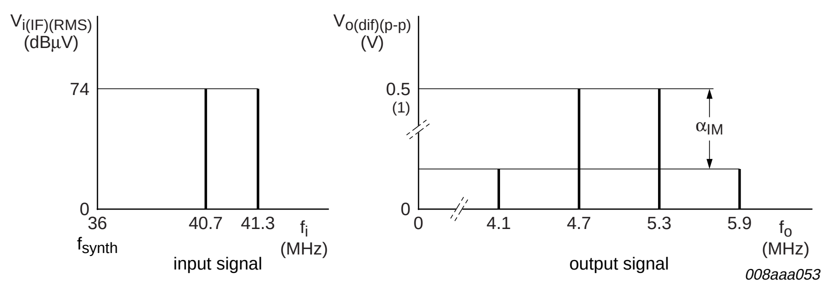
(1) 0.25 V for W4[7] = 1.

Fig 38. Direct IF signal conditions for measurement of intermodulation at OUT2



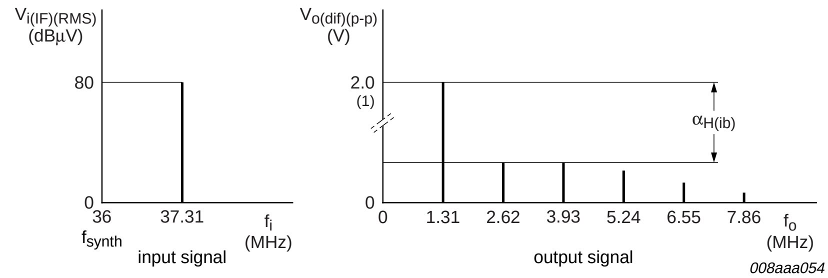
(1) 0.5 V for W4[7] = 1.

Fig 39. Zero IF signal conditions for measurement of intermodulation at OUT1 and OUT2



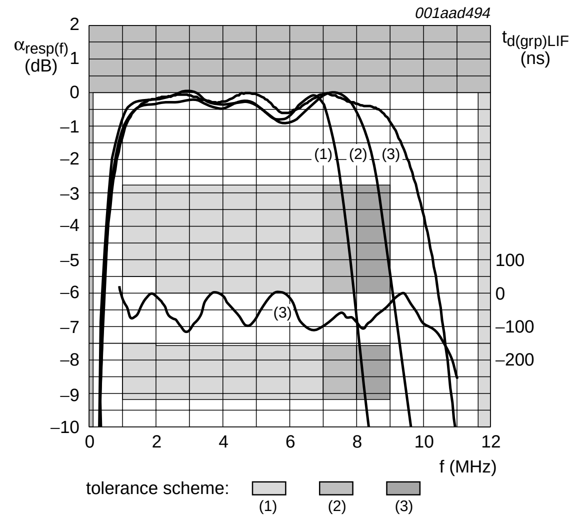
(1) 0.25 V for W4[7] = 1.

Fig 40. Low IF signal conditions for measurement of intermodulation at OUT1



(1) 1.0 V for W4[7] = 1.

Fig 41. Low IF signal conditions for measurement of harmonics at OUT1

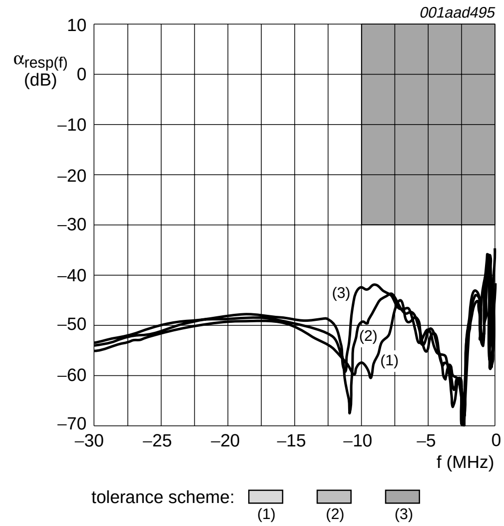


(1) Channel bandwidth = 6 MHz.

(2) Channel bandwidth = 7 MHz.

(3) Channel bandwidth = 8 MHz.

Fig 42. Detailed low IF amplitude and group delay pass-band tolerance scheme

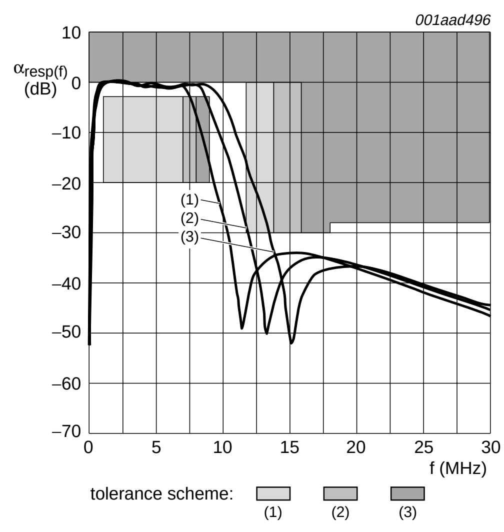


(1) Channel bandwidth = 6 MHz.

(2) Channel bandwidth = 7 MHz.

(3) Channel bandwidth = 8 MHz.

Fig 43. Low IF amplitude stop-band tolerance scheme

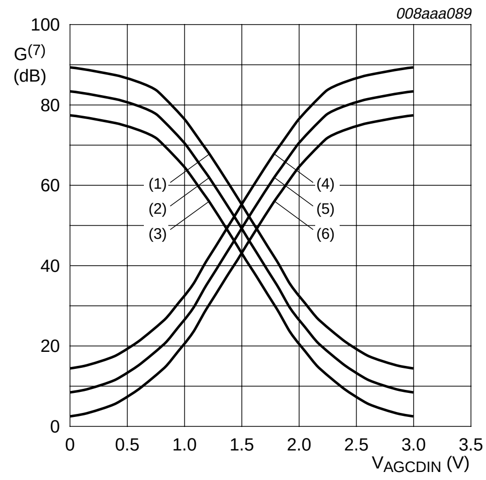


(1) Channel bandwidth = 6 MHz.

(2) Channel bandwidth = 7 MHz.

(3) Channel bandwidth = 8 MHz.

Fig 44. Low IF amplitude pass-band tolerance scheme



(1) 2.0 V (p-p) differential output voltage (LIF or ZIF, W9[7] = 0, W4[7] = 0).

(2) 1.0 V (p-p) differential output voltage (LIF or ZIF, W9[7] = 0, W4[7] = 1; DIF, W9[7] = 0, W4[7] = 0).

(3) 0.5 V (p-p) differential output voltage (DIF, W9[7] = 0, W4[7] = 1).

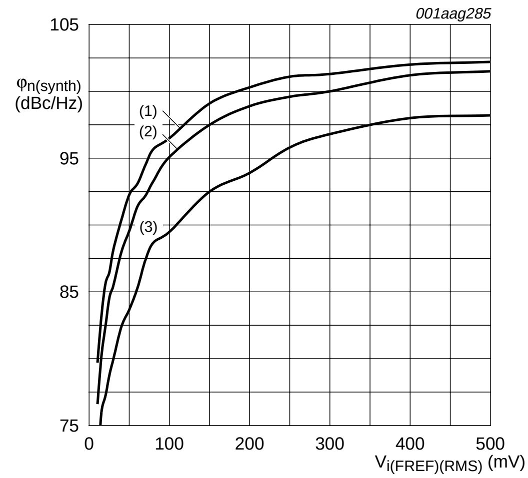
(4) 2.0 V (p-p) differential output voltage (LIF or ZIF, W9[7] = 1, W4[7] = 0).

(5) 1.0 V (p-p) differential output voltage (LIF or ZIF, W9[7] = 1, W4[7] = 1; DIF, W9[7] = 1, W4[7] = 0).

(6) 0.5 V (p-p) differential output voltage (DIF, W9[7] = 1, W4[7] = 1).

(7) Ratio of output peak-to-peak level to input RMS level.

Fig 45. Typical gain characteristic for AGCDIN control voltage



f_{synth} = 40 MHz; f_{IF} = 44 MHz

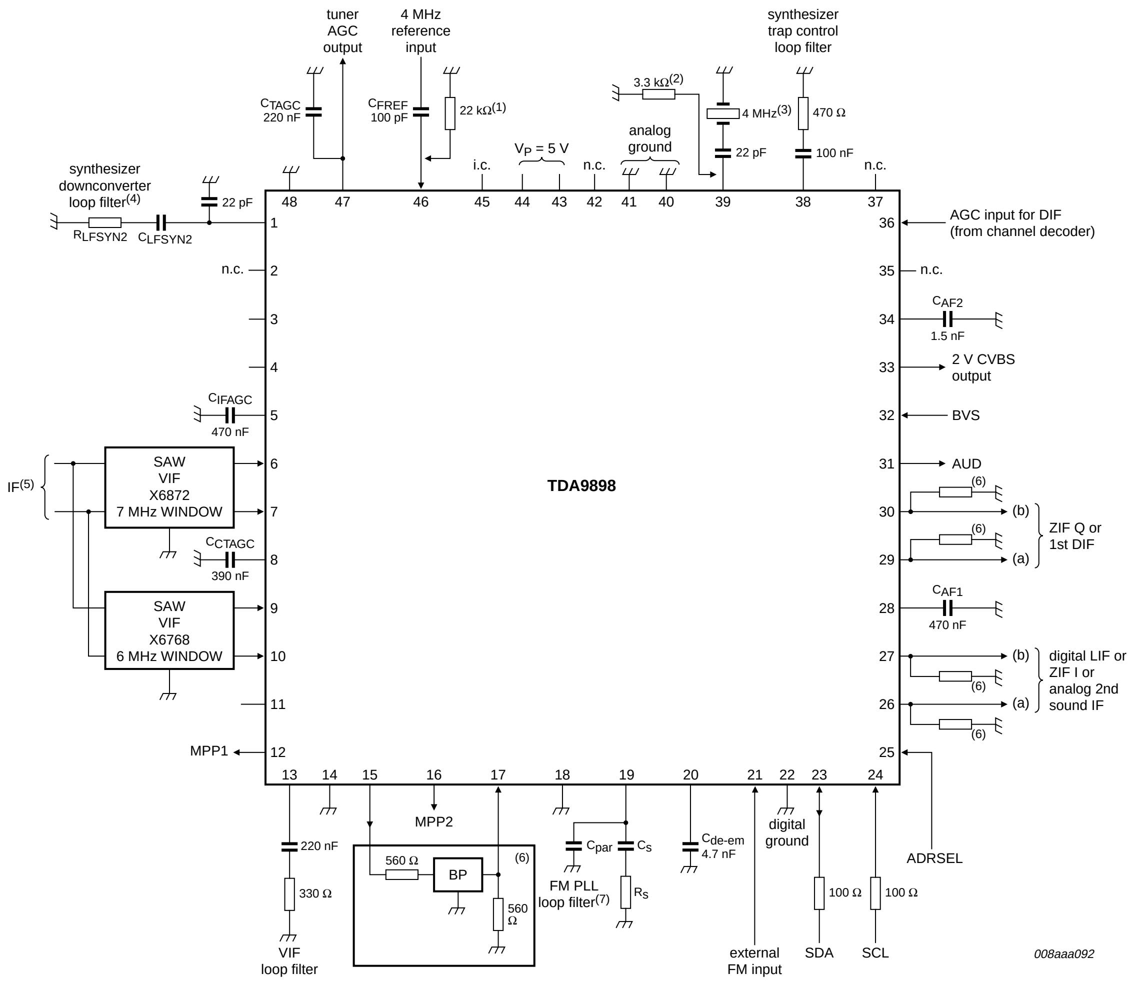
(1) Δf = 100 kHz.

(2) Δf = 10 kHz.

(3) Δf = 1 kHz.

Fig 46. Typical synthesizer phase noise at carrier frequency plus Δf on LIF output versus input voltage on pin FREF

13. Application information



(1) Connect resistor if external reference signal is not used.

(2) Connect resistor if crystal is not used.

(3) Use of crystal is optional.

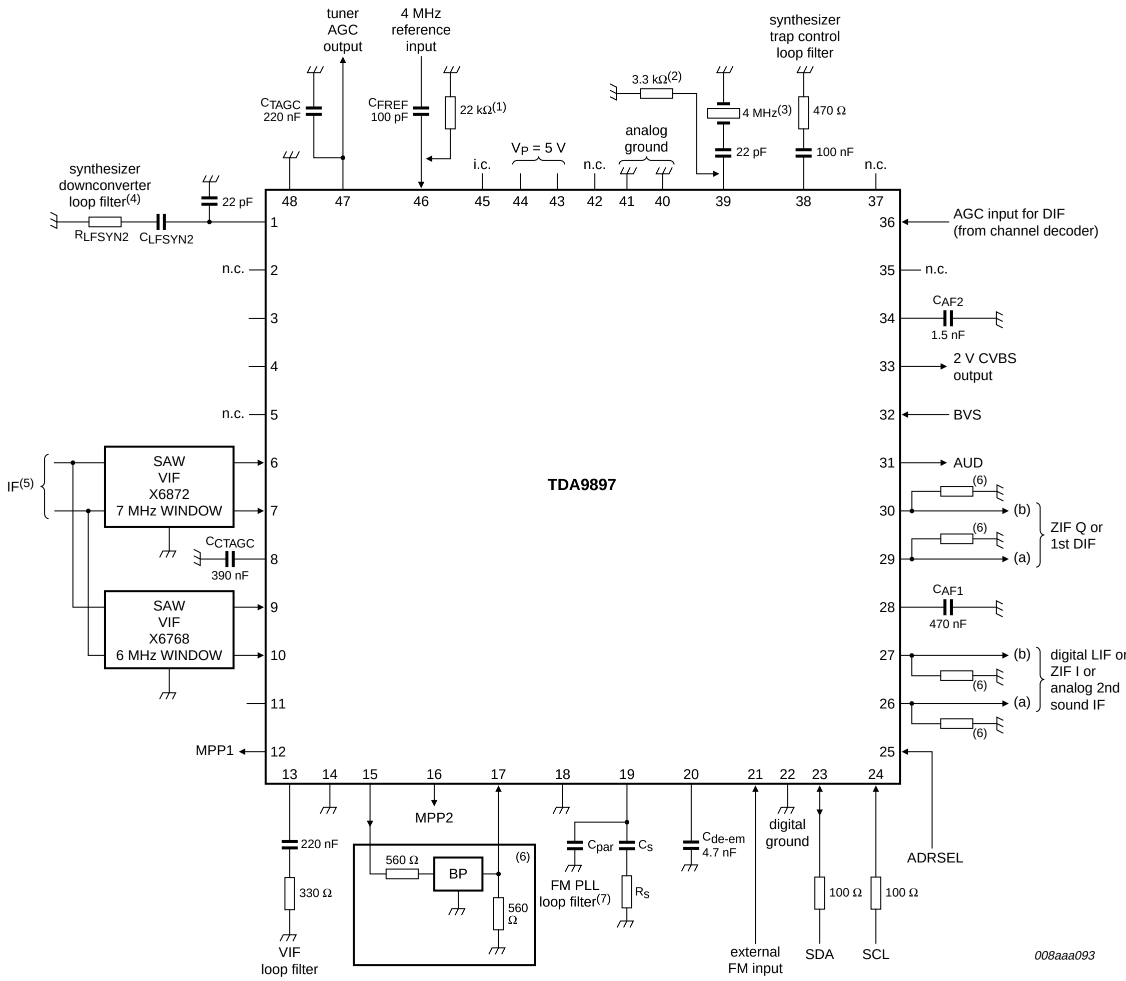
(4) Application depends on synthesizer frequency; see Table 57.

(5) Optional single-ended IF input possible.

(6) Optional.

(7) See Table 54.

Fig 47. Application diagram of TDA9898



(1) Connect resistor if external reference signal is not used.

(2) Connect resistor if crystal is not used.

(3) Use of crystal is optional.

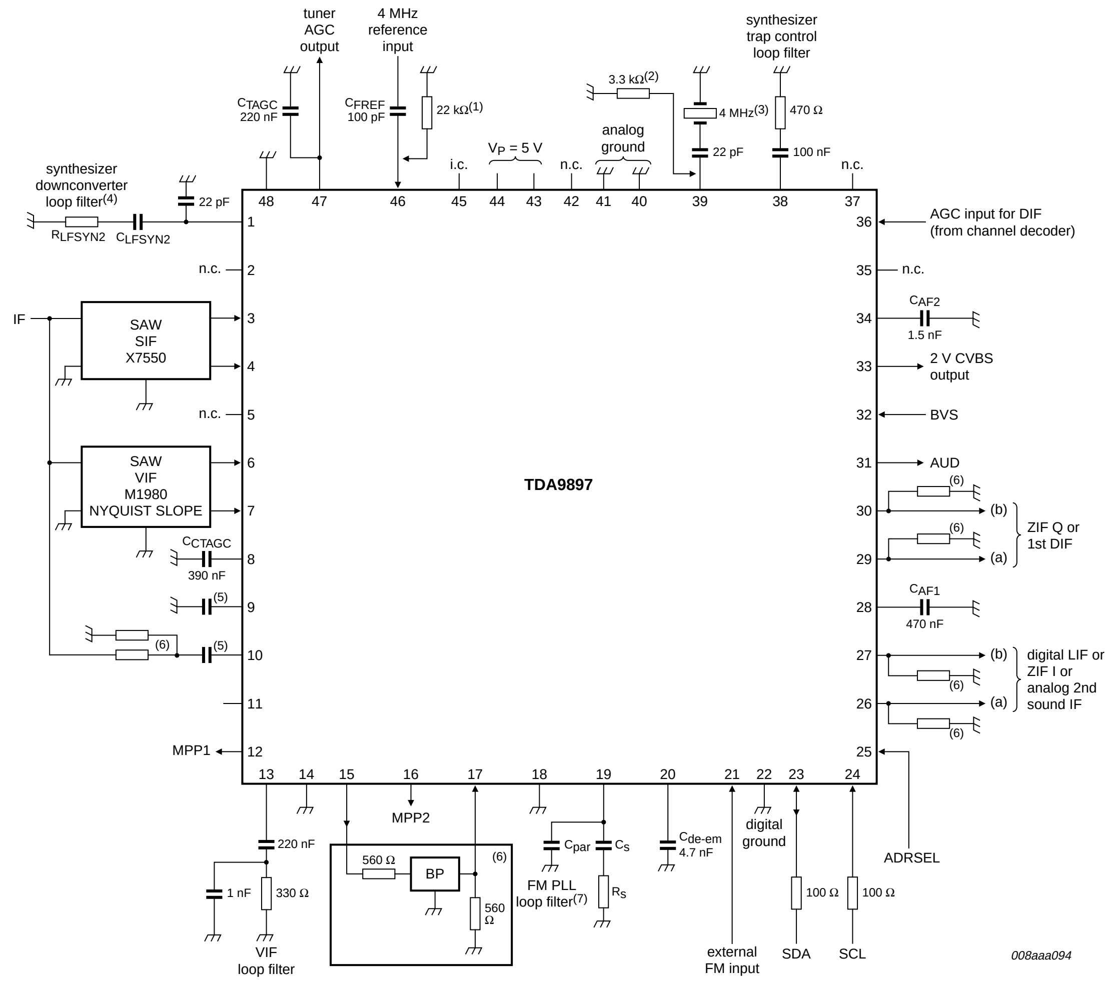
(4) Application depends on synthesizer frequency; see Table 57.

(5) Optional single-ended IF input possible.

(6) Optional.

(7) See Table 54.

Fig 48. Application diagram of TDA9897



(1) Connect resistor if external reference signal is not used.

(2) Connect resistor if crystal is not used.

(3) Use of crystal is optional.

(4) Application depends on synthesizer frequency; see Table 57.

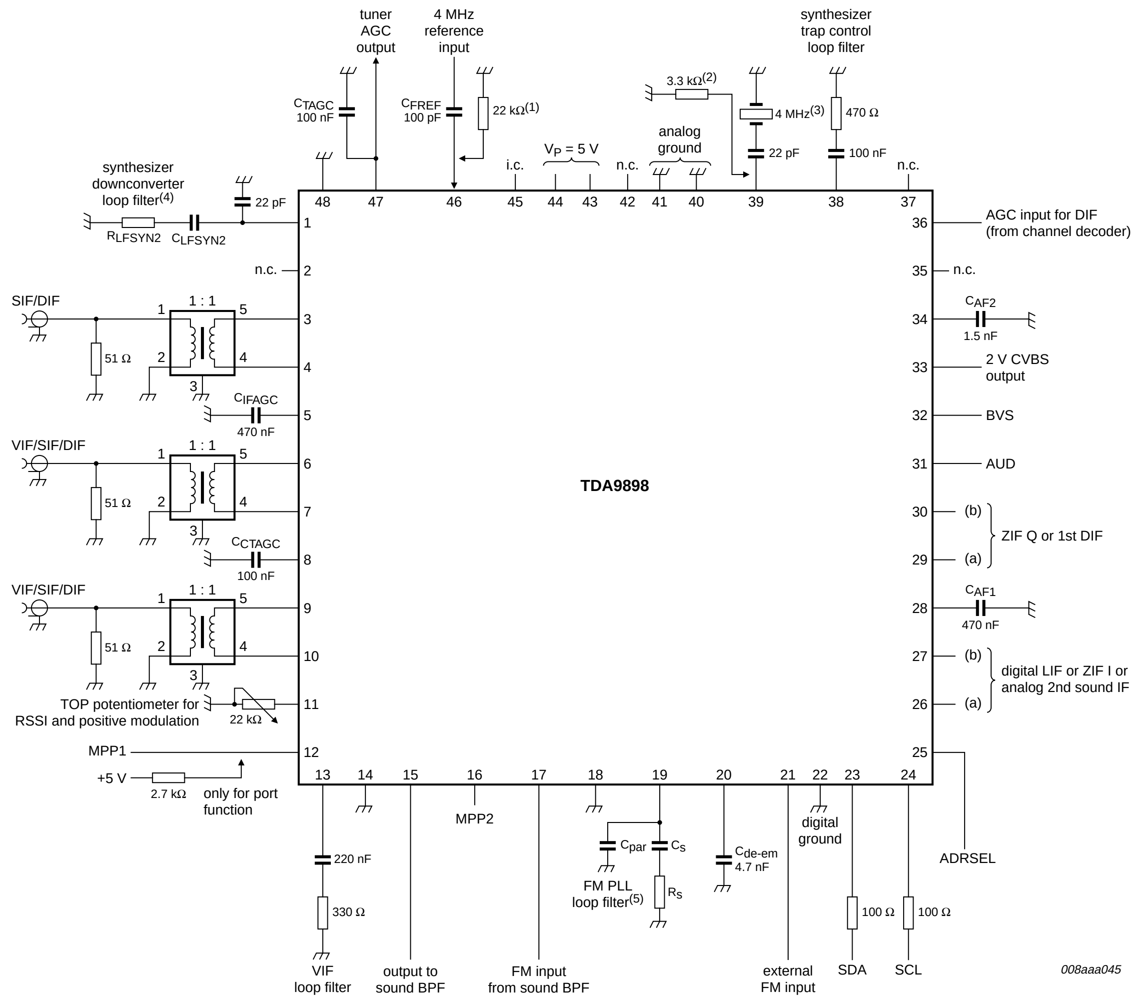
(5) Value depends on application.

(6) Optional.

(7) See Table 54.

Fig 49. Application diagram of TDA9897 using SAW filter with Nyquist slope

14. Test information



(1) Connect resistor if external reference signal is not used.

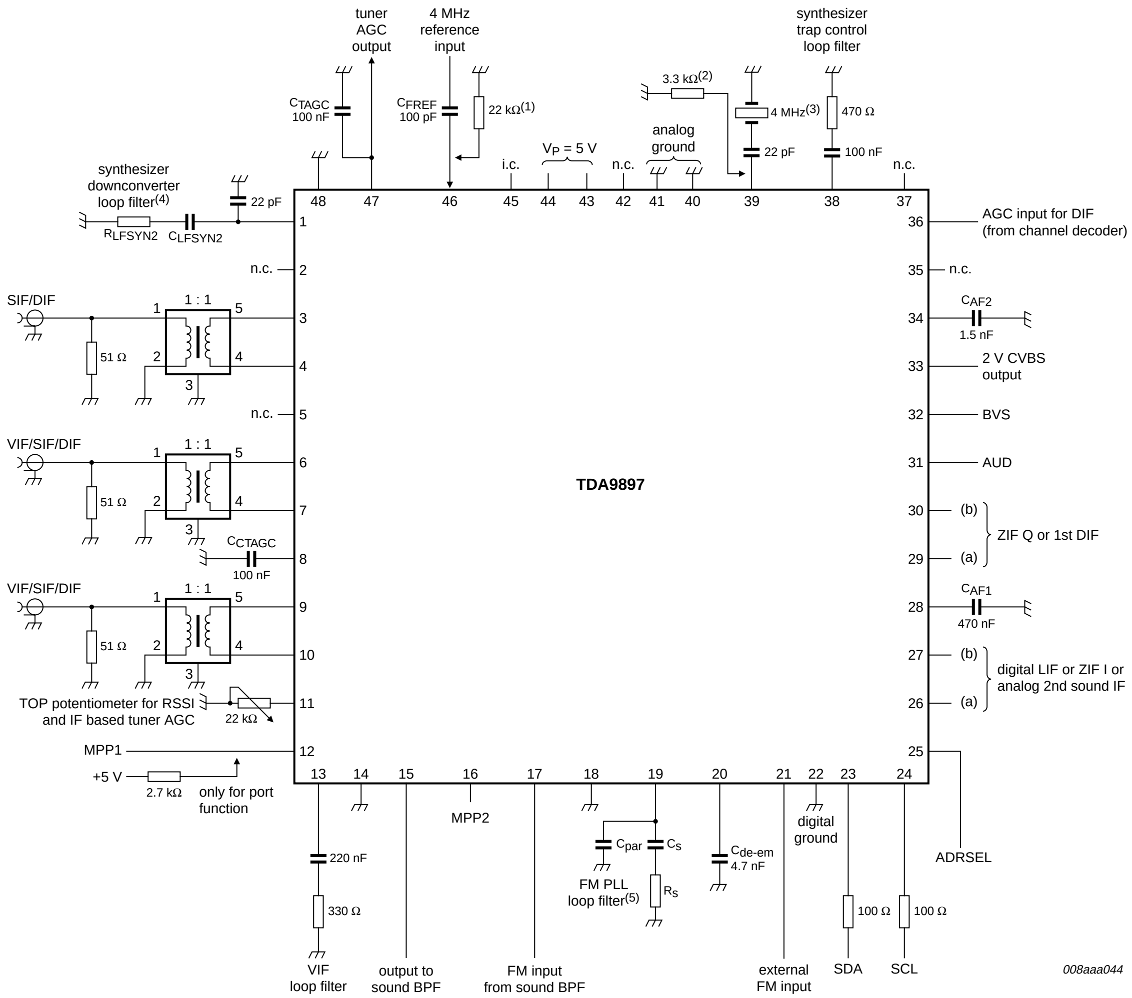
(2) Connect resistor if crystal is not used.

(3) Use of crystal is optional.

(4) Application depends on synthesizer frequency; see Table 57.

(5) See Table 54.

Fig 50. Test circuit of TDA9898



(1) Connect resistor if external reference signal is not used.

(2) Connect resistor if crystal is not used.

(3) Use of crystal is optional.

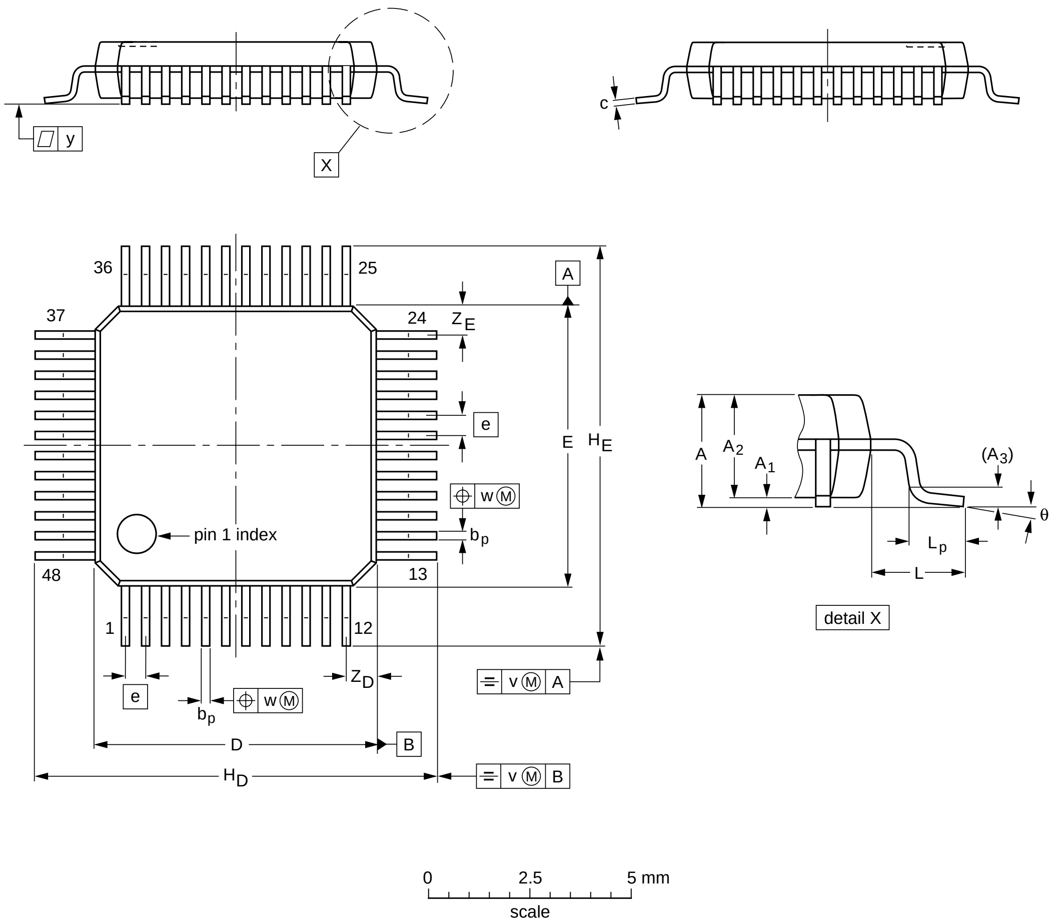
(4) Application depends on synthesizer frequency; see Table 57.

(5) See Table 54.

Fig 51. Test circuit of TDA9897

15. Package outline

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_D	H_E	L	L_p	v	w	y	Z_D(1)	Z_E(1)	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°

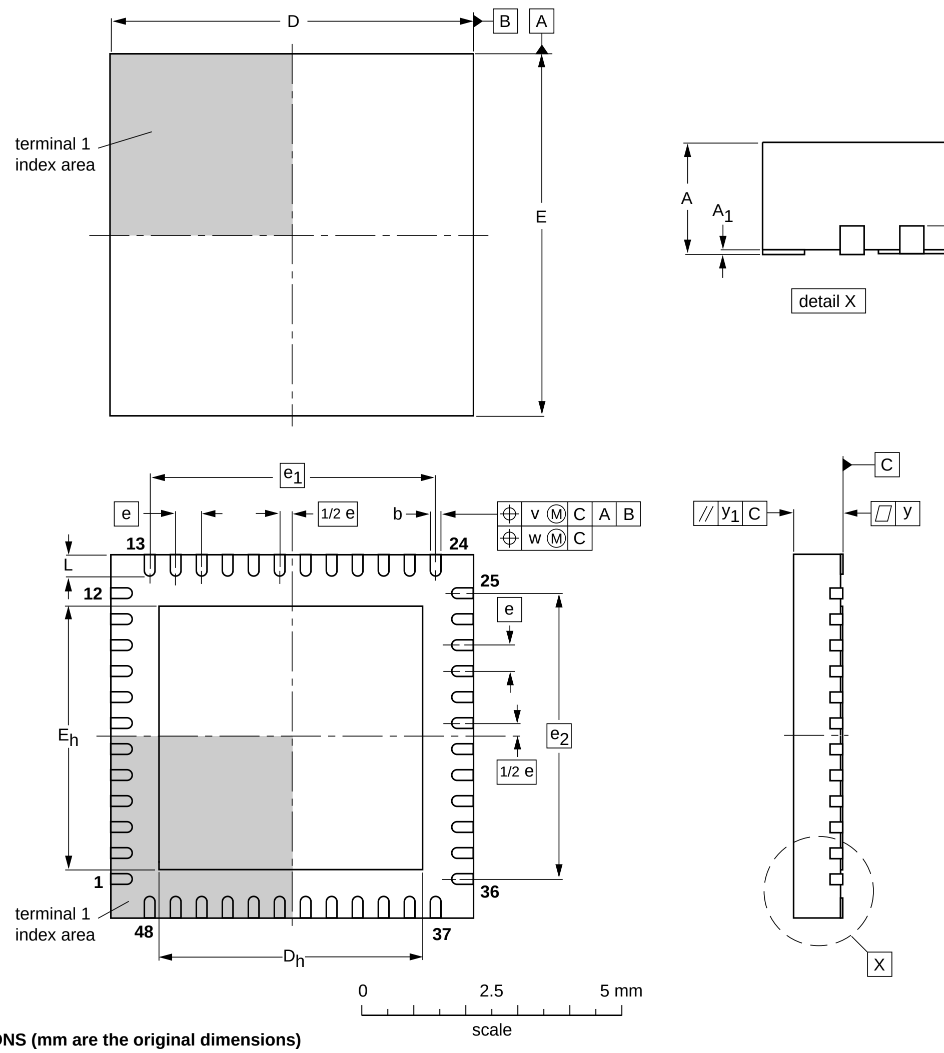
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT313-2	136E05	MS-026				~~00-01-19~~ 03-02-25

Fig 52. Package outline SOT313-2 (LQFP48)

HVQFN48: plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 x 7 x 0.85 mm **SOT619-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	7.1 6.9	5.25 4.95	7.1 6.9	5.25 4.95	0.5	5.5	5.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT619-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-18

Fig 53. Package outline SOT619-1 (HVQFN48)

16. Soldering

16.1 Introduction

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

16.2 Through-hole mount packages

16.2.1 Soldering by dipping or by solder wave

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

16.2.2 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 °C and 400 °C, contact may be up to 5 seconds.

16.3 Surface mount packages

16.3.1 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 54) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 58 and 59

Table 58. SnPb eutectic process (from J-STD-020C)

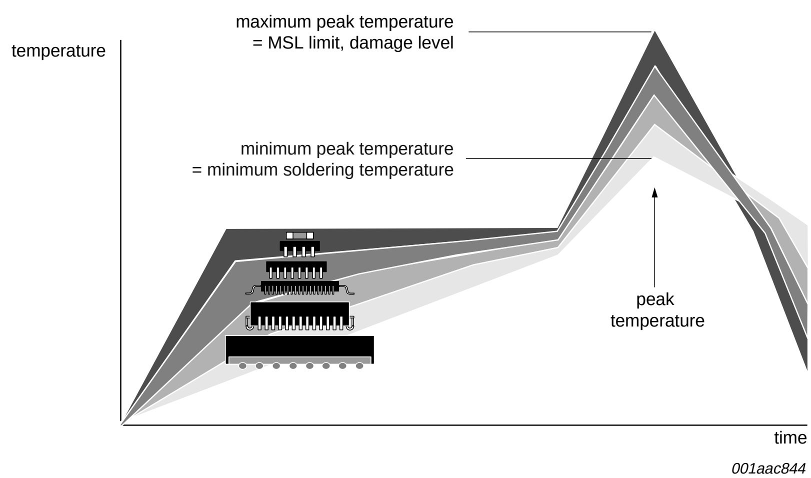
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 59. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 54.



MSL: Moisture Sensitivity Level

Fig 54. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

16.3.2 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  – larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  – smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

16.3.3 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

16.4 Package related soldering information

Table 60. Suitability of IC packages for wave, reflow and dipping soldering methods

Mounting	Package[1]	Soldering method		
		Wave	Reflow[2]	Dipping
Through-hole mount	CPGA, HCPGA	suitable	–	–
	DBS, DIP, HDIP, RDBS, SDIP, SIL	suitable[3]	–	suitable
Through-hole-surface mount	PMFP[4]	not suitable	not suitable	–

Table 60. Suitability of IC packages for wave, reflow and dipping soldering methods *…continued*

Mounting	Package[1]	Soldering method		
		Wave	Reflow[2]	Dipping
Surface mount	BGA, HTSSON..T[5], LBGA, LFBGA, SQFP, SSOP..T[5], TFBGA, VFBGA, XSON	not suitable	suitable	–
	DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[6]	suitable	–
	PLCC[7], SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended[7][8]	suitable	–
	SSOP, TSSOP, VSO, VSSOP	not recommended[9]	suitable	–
	CWQCCN..L[10], WQCCN..L[10]	not suitable	not suitable	–

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your NXP Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect).

[3] For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

[4] Hot bar soldering or manual soldering is suitable for PMFP packages.

[5] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[6] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[7] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[8] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[9] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[10] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

17. Abbreviations

Table 61. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AFC	Automatic Frequency Control
AGC	Automatic Gain Control
ATV	Analog TV
BP	Band-Pass
CW	Continuous Wave
DAC	Digital-to-Analog Converter
DC	Direct Current

Table 61. Abbreviations *…continued*

Acronym	Description
DIF	Digital Intermediate Frequency
DSP	Digital Signal Processor
DTV	Digital TV
DVB	Digital Video Broadcast
ESD	ElectroStatic Discharge
FPLL	Frequency Phase-Locked Loop
IC	Integrated Circuit
IF	Intermediate Frequency
LCD	Liquid Crystal Display
LIF	Low Intermediate Frequency
MAD	Module Address
NICAM	Near Instantaneous Companded Audio Multiplex
PLL	Phase-Locked Loop
POR	Power-On Reset
QSS	Quasi Split Sound
RIF	Radio Intermediate Frequency
RSSI	Received Signal Strength Indication
SAW	Surface Acoustic Wave
SC	Sound Carrier
SIF	Sound Intermediate Frequency
TAGC	Tuner Automatic Gain Control
TOP	TakeOver Point
VCO	Voltage-Controlled Oscillator
VIF	Vision Intermediate Frequency
VITS	Vertical Interval Test Signal
ZIF	Zero Intermediate Frequency

18. Revision history

Table 62. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA9897_TDA9898_3	20080111	Product data sheet	-	TDA9897_TDA9898_2
Modifications:	• Additional specification of features for V2/S1 version			
TDA9897_TDA9898_2	20070411	Product data sheet	-	TDA9897_TDA9898_1
TDA9897_TDA9898_1	20060922	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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