PCA9691

8-bit A/D and D/A converter

Rev. 01 — 8 April 2008 Product data sheet

1. General description

The PCA9691 is a single chip, single supply, low power, 8-bit CMOS data acquisition device with four analog inputs, one analog output and a serial I^2C-bus interface. Three address pins (A0, A1 and A2) are used for programming the hardware address, allowing the use of up to 64 PCA9691 devices connected to the I^2C-bus without additional hardware. Address, control and data to and from the PCA9691 are transferred via the serial two-line bidirectional I^2C-bus.

The functions of the PCA9691 include:

- Analog input multiplexing
- On-chip sample and hold
- 8-bit Analog-to-Digital (A/D) conversion
- 8-bit Digital-to-Analog (D/A) conversion

The maximum conversion rate is given by the maximum frequency of the I^2C-bus.

2. Features

- 8-bit successive approximation A/D conversion
- Four analog inputs programmable as single-ended or differential inputs
- 64 different addresses by three hardware address pins
- 1 MHz Fast-mode Plus (Fm+) I^2C-bus via serial input/output
- Sampling rate given by I^2C-bus frequency
- Single supply voltage; operating from 2.5 V to 5.5 V
- Low standby current
- Analog voltage from V_{SS} to V_{DD}
- Multiplying D/A Converter (DAC) with one analog output
- On-chip sample and hold circuit
- Auto-incremented channel selection

founded by Philips

3. Ordering information

Table 1. Ordering information

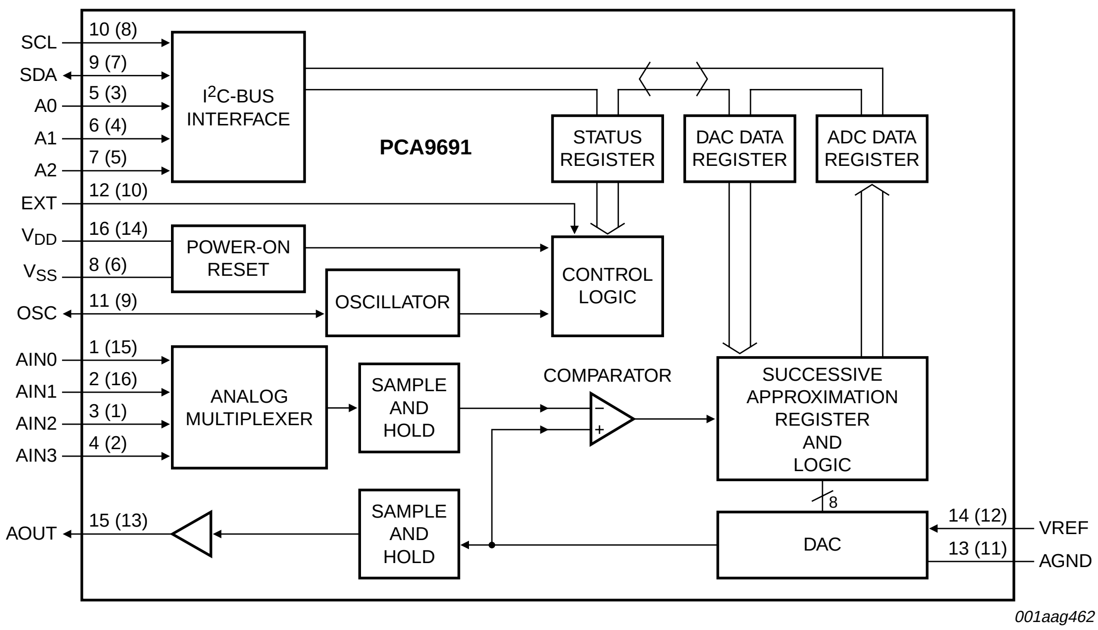
Type number	Package		
	Name	Description	Version
PCA9691BS	HVQFN16	plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 4 × 4 × 0.85 mm	SOT629-1
PCA9691TS	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4. Marking

Table 2. Marking codes

Type number	Marking code
PCA9691BS	9691
PCA9691TS	PCA9691

5. Block diagram



The numbers in brackets refer to HVQFN16 package.

Fig 1. Block diagram of PCA9691

6. Pinning information

6.1 Pinning

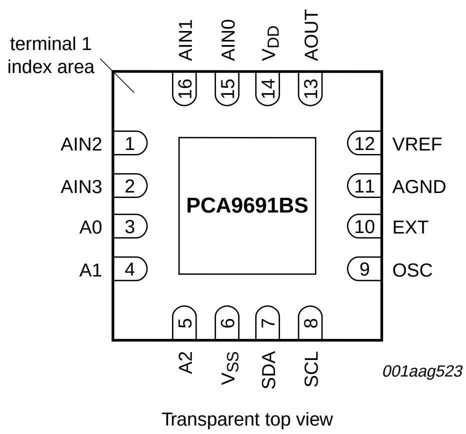


Fig 2. Pin configuration for HVQFN16

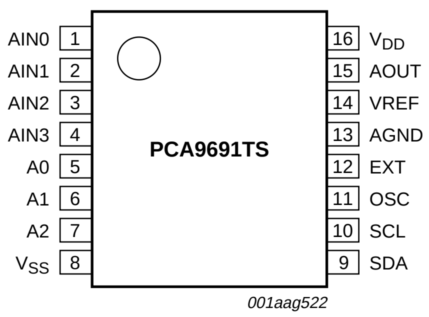


Fig 3. Pin configuration for TSSOP16

6.2 Pin description

Table 3. Pin description

Symbol	Pin		Type	Description
	TSSOP16	HVQFN16		
AIN0	1	15	input	analog input 0
AIN1	2	16	input	analog input 1
AIN2	3	1	input	analog input 2
AIN3	4	2	input	analog input 3
A0	5	3	input	address input 0
A1	6	4	input	address input 1
A2	7	5	input	address input 2
V_{SS}	8	6	ground	analog and digital ground
SDA	9	7	input/output	I^2C-bus data input and output
SCL	10	8	input	I^2C-bus clock input
OSC	11	9	input/output	oscillator sgnal selection: input, if pin EXT = HIGH output, if pin EXT = LOW
EXT	12	10	input	oscillator selection input: HIGH = external oscillator LOW = internal oscillator
AGND	13	11	ground	DAC analog ground
VREF	14	12	input	DAC reference voltage input
AOUT	15	13	output	analog output
V_{DD}	16	14	supply	supply voltage

7. Functional description

7.1 Addressing

Each PCA9691 device in an I²C-bus system is activated by sending a valid address to the device. The address consists of seven programmable bits and one read/write bit. The address must be set according to Table 4. The three input pins (A2, A1 and A0) are used to encode the seven address bits (A[6:0]), where each of the pins can be connected to V_{DD}, V_{SS}, SCL or SDA. The address is always sent as the first byte after the start condition in the I²C-bus protocol. The last bit of the address byte is the read/write-bit which sets the direction of the following data transfer (see Figure 4, Figure 17 and Figure 18).

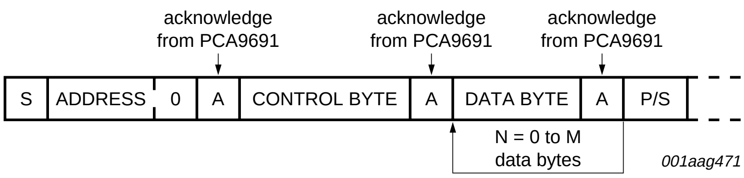


Fig 4. Address byte

7.1.1 Address map

Table 4. PCA9691 address map

Pin			Bit								Address	Nr
A2	A1	A0	A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$		
V_{SS}	V_{SS}	SDA	0	1	0	0	0	0	0	0	40h	1
V_{SS}	V_{DD}	SDA	0	1	0	0	0	0	1	0	42h	2
V_{DD}	V_{SS}	SDA	0	1	0	0	0	1	0	0	44h	3
V_{DD}	V_{DD}	SDA	0	1	0	0	0	1	1	0	46h	4
V_{SS}	SDA	V_{SS}	0	1	0	0	1	0	0	0	48h	5
V_{SS}	SDA	V_{DD}	0	1	0	0	1	0	1	0	4Ah	6
V_{DD}	SDA	V_{SS}	0	1	0	0	1	1	0	0	4Ch	7
V_{DD}	SDA	V_{DD}	0	1	0	0	1	1	1	0	4Eh	8
SDA	V_{SS}	V_{SS}	0	1	0	1	0	0	0	0	50h	9
SDA	V_{SS}	V_{DD}	0	1	0	1	0	0	1	0	52h	10
SDA	V_{DD}	V_{SS}	0	1	0	1	0	1	0	0	54h	11
SDA	V_{DD}	V_{DD}	0	1	0	1	0	1	1	0	56h	12
V_{SS}	SDA	SDA	0	1	0	1	1	0	0	0	58h	13
V_{DD}	SDA	SDA	0	1	0	1	1	0	1	0	5Ah	14
SDA	V_{SS}	SDA	0	1	0	1	1	1	0	0	5Ch	15
SDA	V_{DD}	SDA	0	1	0	1	1	1	1	0	5Eh	16
SDA	SDA	V_{SS}	0	1	1	0	0	0	0	0	60h	17
SDA	SDA	V_{DD}	0	1	1	0	0	0	1	0	62h	18
SDA	SDA	SDA	0	1	1	0	0	1	0	0	64h	19
SCL	SCL	SCL	0	1	1	0	0	1	1	0	66h	20

Table 4. PCA9691 address map *...continued*

Pin			Bit								Address	Nr
A2	A1	A0	A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$		
V_{SS}	V_{SS}	SCL	0	1	1	0	1	0	0	0	68h	21
V_{SS}	V_{DD}	SCL	0	1	1	0	1	0	1	0	6Ah	22
V_{DD}	V_{SS}	SCL	0	1	1	0	1	1	0	0	6Ch	23
V_{DD}	V_{DD}	SCL	0	1	1	0	1	1	1	0	6Eh	24
V_{SS}	SCL	V_{SS}	0	1	1	1	0	0	0	0	70h	25
V_{SS}	SCL	V_{DD}	0	1	1	1	0	0	1	0	72h	26
V_{DD}	SCL	V_{SS}	0	1	1	1	0	1	0	0	74h	27
V_{DD}	SCL	V_{DD}	0	1	1	1	0	1	1	0	76h	28
SCL	V_{SS}	V_{SS}	0	1	1	1	1	0	0	0	78h	29
SCL	V_{SS}	V_{DD}	0	1	1	1	1	0	1	0	7Ah	30
SCL	V_{DD}	V_{SS}	0	1	1	1	1	1	0	0	7Ch	31
SCL	V_{DD}	V_{DD}	0	1	1	1	1	1	1	0	7Eh	32
V_{SS}	SCL	SCL	1	0	0	0	0	0	0	0	80h	33
V_{DD}	SCL	SCL	1	0	0	0	0	0	1	0	82h	34
SCL	V_{SS}	SCL	1	0	0	0	0	1	0	0	84h	35
SCL	V_{DD}	SCL	1	0	0	0	0	1	1	0	86h	36
SCL	SCL	V_{SS}	1	0	0	0	1	0	0	0	88h	37
SCL	SCL	V_{DD}	1	0	0	0	1	0	1	0	8Ah	38
V_{SS}	SCL	SDA	1	0	0	0	1	1	0	0	8Ch	39
V_{DD}	SCL	SDA	1	0	0	0	1	1	1	0	8Eh	40
V_{SS}	V_{SS}	V_{SS}	1	0	0	1	0	0	0	0	90h	41
V_{SS}	V_{SS}	V_{DD}	1	0	0	1	0	0	1	0	92h	42
V_{SS}	V_{DD}	V_{SS}	1	0	0	1	0	1	0	0	94h	43
V_{SS}	V_{DD}	V_{DD}	1	0	0	1	0	1	1	0	96h	44
V_{DD}	V_{SS}	V_{SS}	1	0	0	1	1	0	0	0	98h	45
V_{DD}	V_{SS}	V_{DD}	1	0	0	1	1	0	1	0	9Ah	46
V_{DD}	V_{DD}	V_{SS}	1	0	0	1	1	1	0	0	9Ch	47
V_{DD}	V_{DD}	V_{DD}	1	0	0	1	1	1	1	0	9Eh	48
V_{SS}	SDA	SCL	1	0	1	0	0	0	0	0	A0h	49
V_{DD}	SDA	SCL	1	0	1	0	0	0	1	0	A2h	50
SCL	SDA	V_{SS}	1	0	1	0	0	1	0	0	A4h	51
SCL	SDA	V_{DD}	1	0	1	0	0	1	1	0	A6h	52
SDA	SCL	V_{SS}	1	0	1	0	1	0	0	0	A8h	53
SDA	SCL	V_{DD}	1	0	1	0	1	0	1	0	AAh	54
SDA	V_{SS}	SCL	1	0	1	0	1	1	0	0	ACh	55
SDA	V_{DD}	SCL	1	0	1	0	1	1	1	0	AEh	56
SCL	V_{SS}	SDA	1	0	1	1	0	0	0	0	B0h	57
SCL	V_{DD}	SDA	1	0	1	1	0	0	1	0	B2h	58
SDA	SCL	SCL	1	0	1	1	0	1	0	0	B4h	59
SCL	SDA	SCL	1	0	1	1	0	1	1	0	B6h	60

Table 4. PCA9691 address map *...continued*

Pin			Bit								Address	Nr
A2	A1	A0	A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$		
SCL	SCL	SDA	1	0	1	1	1	0	0	0	B8h	61
SCL	SDA	SDA	1	0	1	1	1	0	1	0	BAh	62
SDA	SCL	SDA	1	0	1	1	1	1	0	0	BCh	63
SDA	SDA	SCL	1	0	1	1	1	1	1	0	BEh	64

7.2 Control byte

The second byte sent to a PCA9691 is stored in its control register and is required to control the PCA9691 function.

The upper nibble of the control register is used for enabling the analog output, and for programming the analog inputs as single-ended or differential inputs. The lower nibble selects one of the analog input channels defined by the upper nibble (see Figure 5).

If the auto-increment flag is set, the channel number is incremented automatically after each A/D conversion.

If the auto-increment mode is selected and the internal oscillator is used, the analog output enable flag in the control byte (bit 6) must be set. This allows the internal oscillator to run continuously, thereby preventing conversion errors resulting from oscillator start-up delay. The analog output enable flag can be reset at other times to reduce quiescent power consumption.

The selection of a non-existing input channel results in the highest available channel number being allocated. Therefore, if the auto-increment flag is set, the next selected channel is always channel 0.

After power-on all bits of the control register are reset to logic 0. The DAC and the oscillator are disabled for power saving. The analog output is switched to a high-impedance state.

The most significant bits of both nibbles are reserved for oscillator control. Bit 7 and bit 3 can be set when the interface frequency is $f_{SCL} \leq 400$ kHz (see Figure 5). Setting these two bits to logic 1 sets the internal frequency to half and the accuracy of the A/D and D/A conversion is 1 LSB as indicated in Table 8 and Table 9.

The oscillator output is disabled in normal operation (pin OSC = LOW). Setting bit 7 to logic 0 and bit 3 to logic 1 will enable this output in order to observe the oscillator frequency (divided by 4).

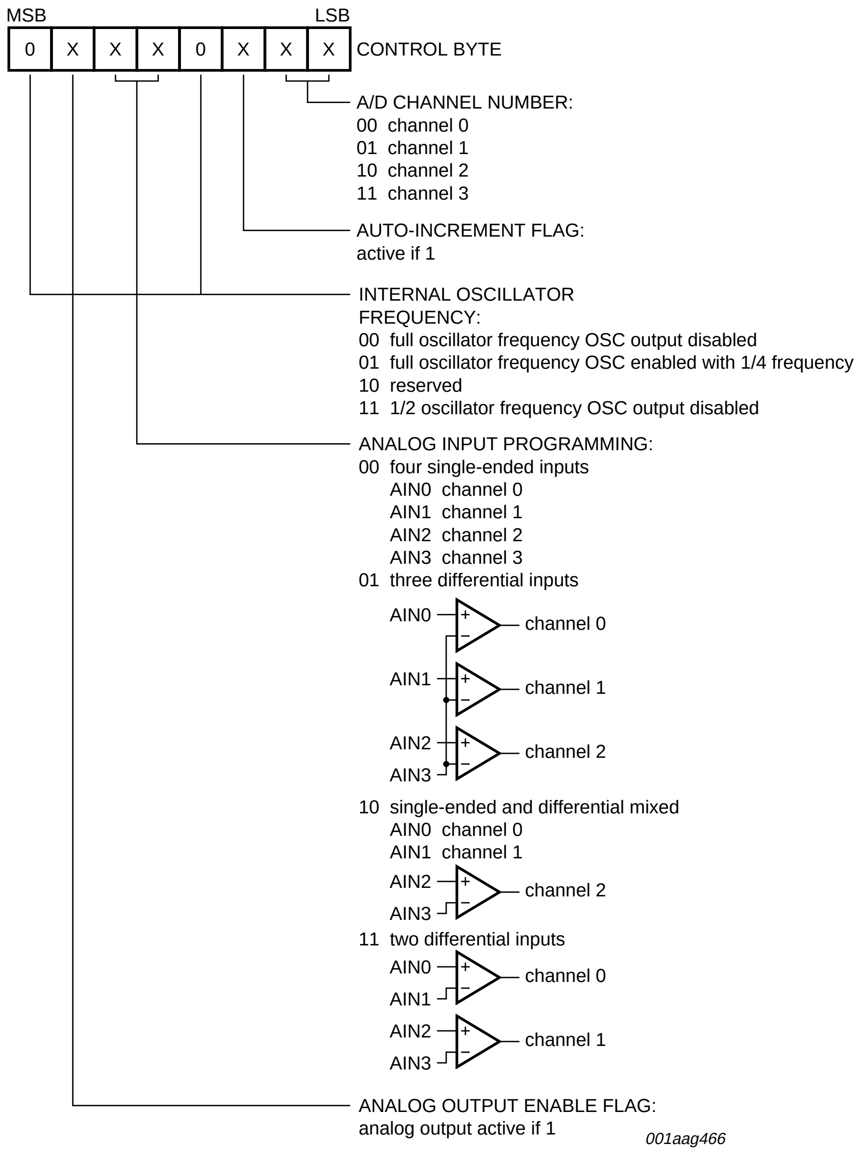


Fig 5. Control byte

7.3 D/A conversion

The third byte sent to a PCA9691 is stored in the DAC data register and is converted to the corresponding analog voltage using the on-chip DAC. This DAC consists of a resistor divider chain connected to the external reference voltage (pin VREF) with 256 taps and selection switches. The tap-decoder switches one of these taps to the DAC output line (see Figure 6).

The analog output voltage is buffered by an auto-zeroed unity gain amplifier. Setting the analog output enable flag of the control register switches this buffer amplifier on or off. In the active state the output voltage is held until a further data byte is sent.

In order to release the DAC for a successive approximation A/D conversion cycle, the unity gain amplifier is equipped with a sample and hold circuit. This circuit holds the output voltage while executing the A/D conversion.

The formula for the output voltage supplied to the analog output pin AOUT is shown in Figure 7.

The waveforms of a D/A conversion sequence are shown in Figure 8.

With the rising edge of the 8th clock bit the DAC register is filled with a new value D7 to D0. After some delay the voltage at the analog output starts to change from the previous value to the new value.

This delay is random but stays within the following limits:

- Minimum $8T_{osc}$ from the rising edge of the 8th bit
- Maximum $18T_{osc}$ from the rising edge of the acknowledge bit (9th bit)

Where T_{osc} is the oscillator period (oscillator frequency is given in Table 6).

Remark: When AOUT starts changing, the DAC settling time $t_{s(DAC)}$ (specified in Table 8), is required for AOUT to reach a new accurate value.

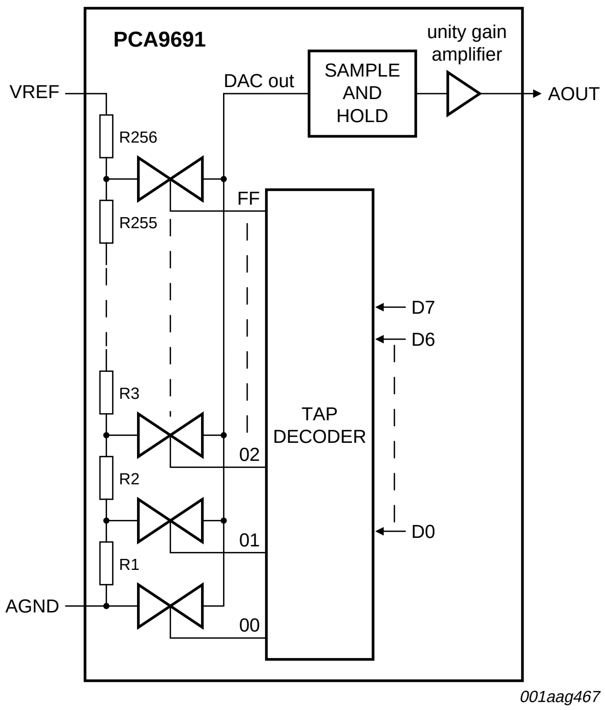


Fig 6. DAC resistor divider chain

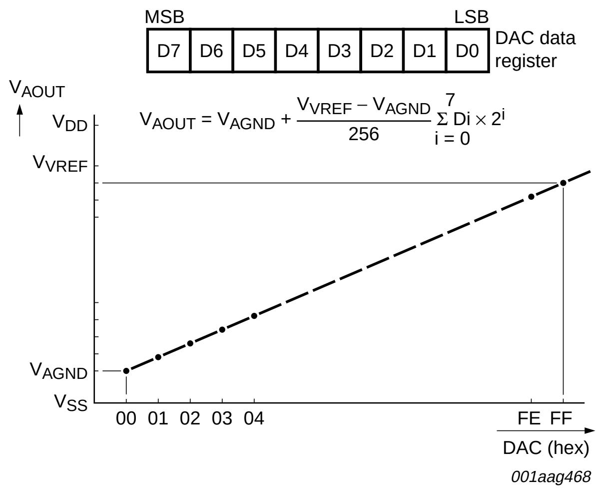


Fig 7. DAC data and DC conversion characteristics

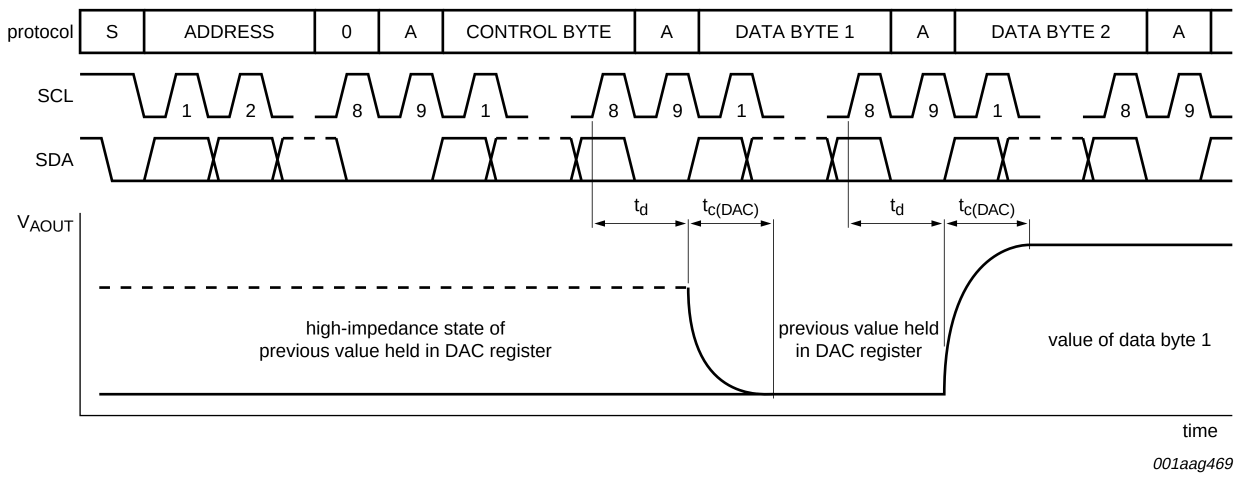


Fig 8. D/A conversion sequence

7.3.1 Worst case example

An example of the worst case is shown in Figure 9. The delay time can have a value between $8T_{osc}$ and $18T_{osc}$.

When the I^{2}C-bus is driven at 1 MHz (full speed) then the DAC is operating at a rate of 9 µs.

The previous AOUT value is valid at least until the rising edge of the acknowledge bit ($8T_{osc} \geq 1.23$ µs).

The latest start time of the new value is 5.6 µs from the rising edge of the acknowledge bit: ($18T_{osc} \leq 5.6$ µs) so AOUT is stable after $t_{s(DAC)} \leq 2.4$ µs.

The new AOUT value is valid, at the latest, after 8.0 μs so before the rising edge of the 8th bit of the next transferred byte. Therefore, at the full speed of the I^2C-bus, the analog output is valid under all circumstances between the rising edges of the 8th bit and the acknowledge bit.

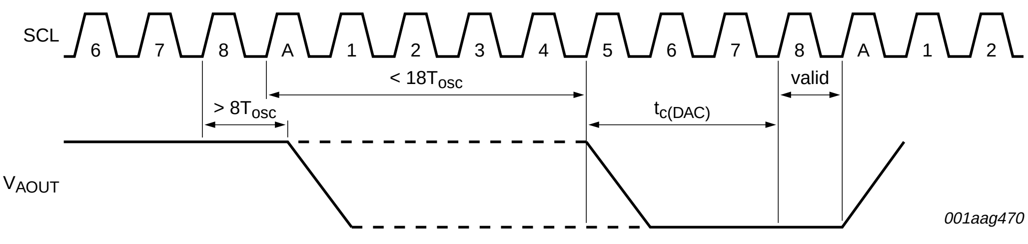


Fig 9. D/A conversion sequence, example of worst case

7.4 A/D conversion

The A/D Converter (ADC) makes use of the successive approximation conversion technique. The on-chip DAC and a high-gain comparator are used temporarily during an A/D conversion cycle.

An A/D conversion cycle is always started after sending a valid read mode address to a PCA9691. The A/D conversion cycle is triggered at the trailing edge of the acknowledge clock pulse and is executed while transmitting the result of the previous conversion (see Figure 10).

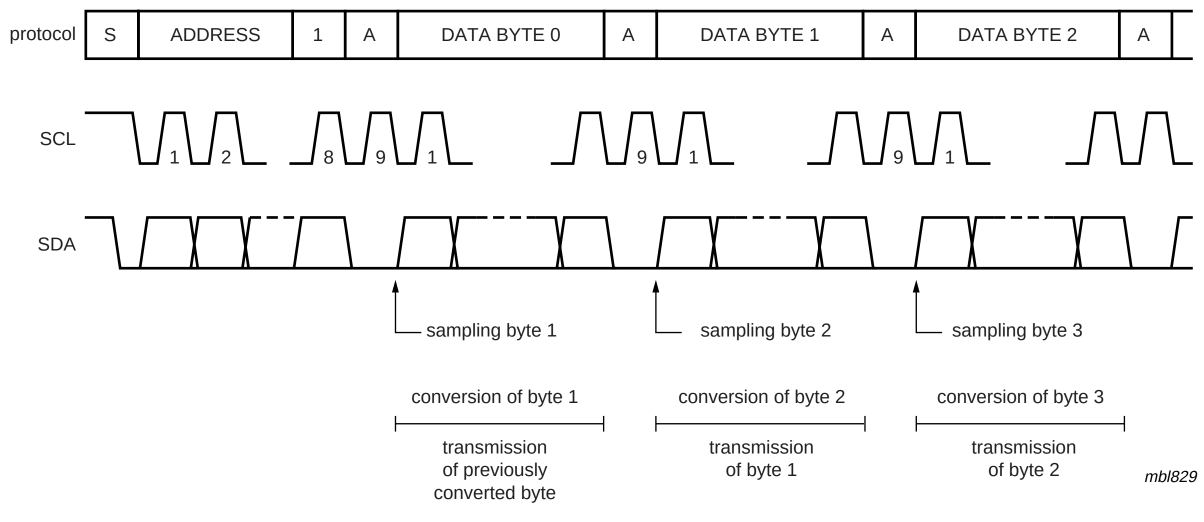


Fig 10. A/D conversion sequence

Once a conversion cycle is triggered, an input voltage sample of the selected channel is stored on the chip and is converted to the corresponding 8-bit binary code. Samples picked up from differential inputs are converted to an 8-bit two's complement code (see Figure 11 and Figure 12).

The conversion result is stored in the ADC data register and awaits transmission. If the auto-increment flag is set the next channel is selected.

The first byte transmitted in a read cycle contains the conversion result code of the previous read cycle. After a power-on reset condition the first byte read is 80h. The protocol of an I^{2}C-bus read cycle is shown in Figure 18.

The actual speed of the I^{2}C-bus provides the maximum A/D conversion rate.

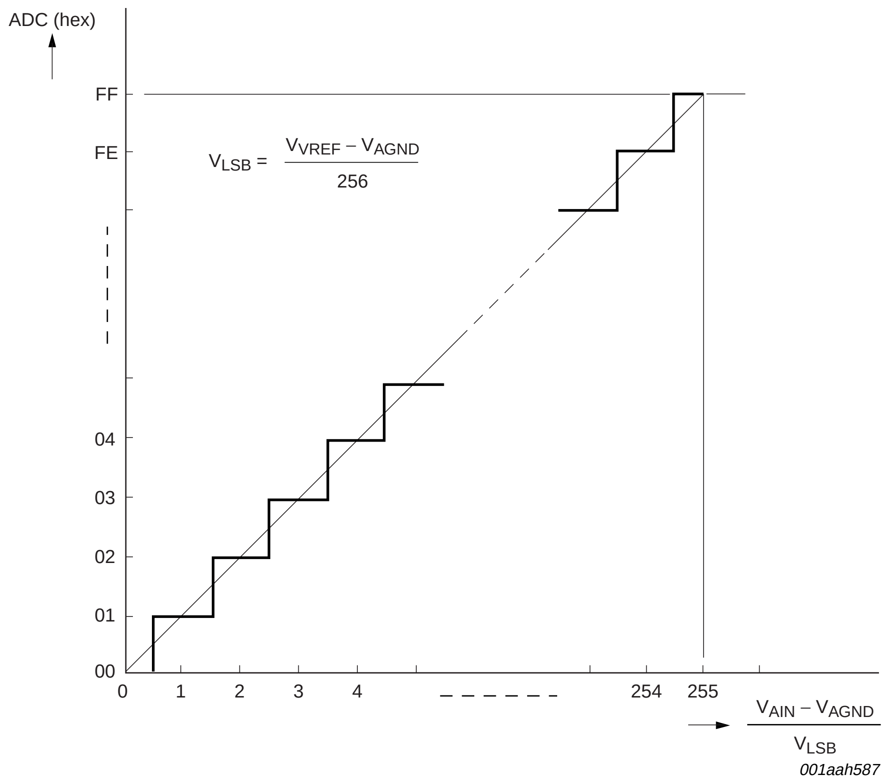


Fig 11. A/D conversion characteristics of single-ended inputs

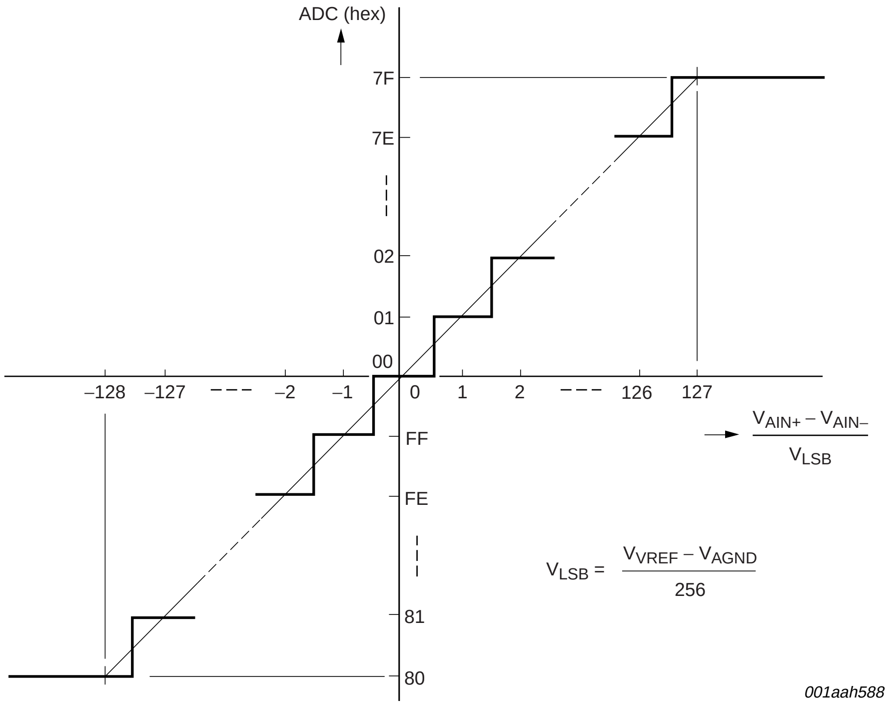


Fig 12. A/D conversion characteristics of differential inputs

7.5 Reference voltage

For the D/A and A/D conversion either a stable external voltage reference or the supply voltage has to be applied to the resistor divider chain (pins VREF and AGND). Pin AGND has to be connected to the system analog ground and may have a DC off-set with reference to V_{SS}.

A low frequency may be applied to pins VREF and AGND. This allows the use of the DAC as a one-quadrant multiplier (see Figure 11 and Figure 23).

The ADC may also be used as a one- or two-quadrant analog divider. The analog input voltage is divided by the reference voltage. The result is converted to a binary code. In this application the user has to keep the reference voltage stable during the conversion cycle.

7.6 Oscillator

An on-chip oscillator generates the clock signal required for the A/D conversion cycle and for refreshing the auto-zeroed buffer amplifier. When using this oscillator pin EXT has to be connected to V_{SS}. The oscillator frequency divided by 4 is available at output pin OSC (see Section 7.2). However, in normal operation it is recommended that output pin OSC is disabled. In this case the output pin OSC = LOW.

The oscillator starts when a start condition is sent via the I^2C-bus interface. If the received address is recognized as valid the oscillator continues to run. If the received address is not recognized the oscillator stops.

If a stop condition occurs the oscillator is stopped unless pin AOUT is enabled.

It is recommended that if the I^2C-bus speed $f_{SCL} \leq 400$ kHz, you must reduce the oscillator frequency by half (see the definition of the control byte in Figure 5).

If pin EXT is connected to V_{DD} the oscillator output OSC is switched to a high-impedance state allowing to feed an external clock signal to the OSC input. The frequency of the external clock must be in the specified range.

7.7 Characteristics of the I^2C-bus

The I^2C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines are connected to a positive supply via a pull-up resistor. Data transfer is initiated only when the bus is not busy.

7.7.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line remains stable during the HIGH period of the clock pulse as changes in the data line at this time are interpreted as control signals (see Figure 13).

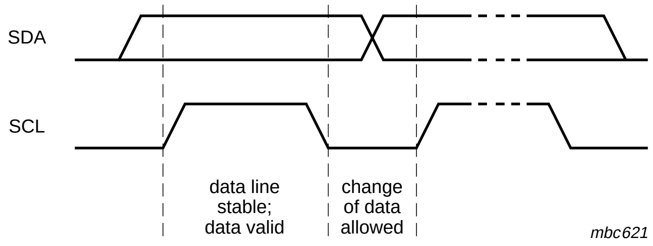


Fig 13. Bit transfer

7.7.2 Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition [S]. A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition [P] (see Figure 14).

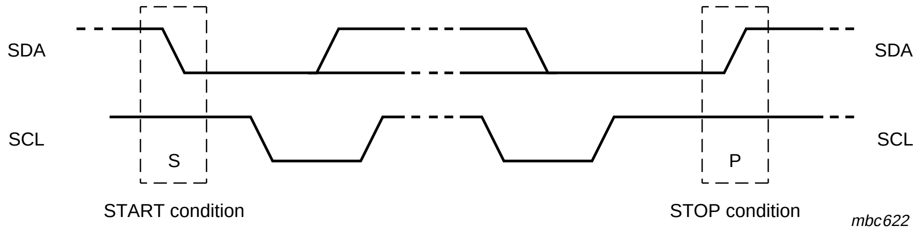


Fig 14. Definition of start and stop condition

7.7.3 System configuration

A device generating a message is a ‘transmitter’, a device receiving a message is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’.

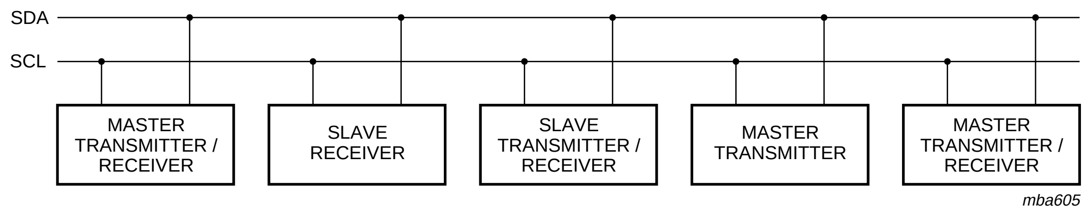


Fig 15. System configuration

7.7.4 Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master also generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition (see Figure 16).

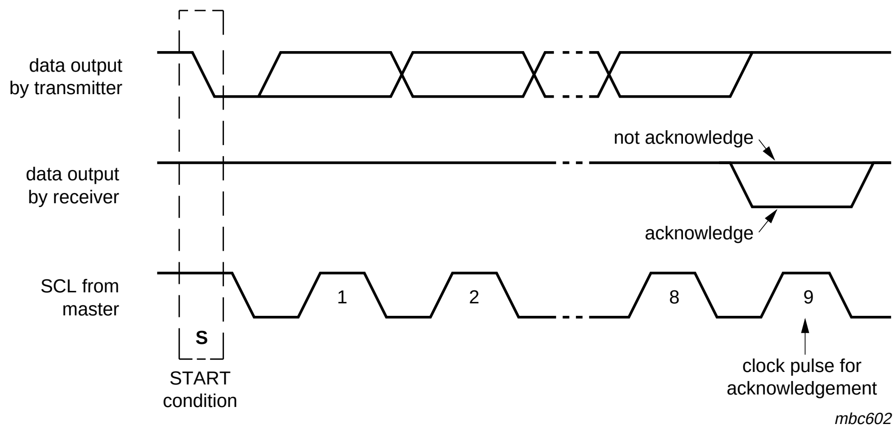


Fig 16. Acknowledgement on the I²C-bus

7.7.5 I²C-bus protocol

After a start condition a valid hardware address has to be sent to a PCA9691 device. The read/write bit defines the direction of the following single or multiple byte data transfer. For the format and the timing of the start condition (S), the stop condition (P) and the acknowledge bit (A) refer to the I²C-bus characteristics. In the write mode a data transfer is terminated by sending either a stop condition or the start condition of the next data transfer.

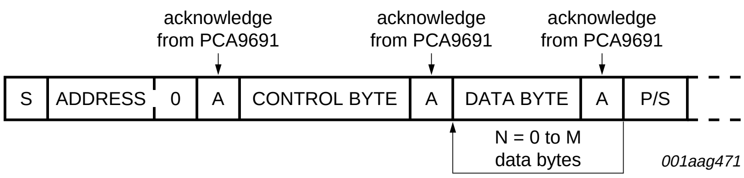


Fig 17. Bus protocol for write mode, D/A conversion

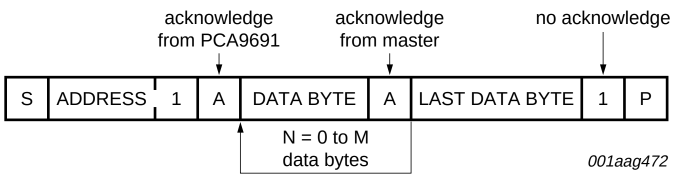


Fig 18. Bus protocol for read mode, A/D conversion

8. Internal circuitry

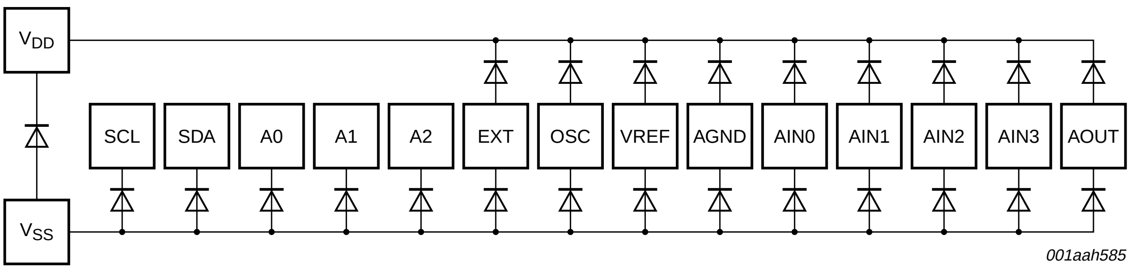


Fig 19. Device protection

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+6.5	V
V_I	input voltage		–0.5	V_{DD} + 0.5	V
I_I	input current		-	±10	mA
I_O	output current		-	±20	mA
I_{DD}	supply current		-	+50	mA
I_{SS}	negative supply current		-	–50	mA
P_{tot}	total power dissipation		-	300	mW
P_o	output power		-	100	mW
T_{amb}	ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–65	+150	°C

Table 5. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{esd}	electrostatic discharge voltage	HBM	[1]	-	±1500	V
		MM	[2]	-	±200	V
I_{lu}	latch-up current		[3]	-	100	mA

[1] HBM: Human Body Model per JESD22-A114.

[2] MM: Machine Model per JESD22-A115.

[3] Latch-up testing is done to JEDEC standard JESD78.

10. Characteristics

10.1 Static characteristics

Table 6. Static characteristic

V_{DD} = 2.5 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

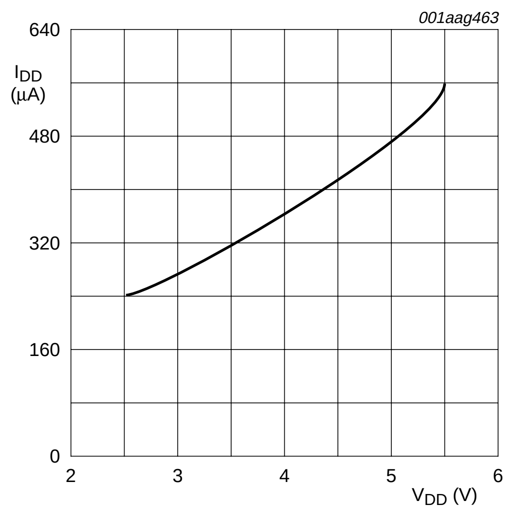
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
V_{DD}	supply voltage			2.5	5.0	5.5	V
I_{DD}	supply current	$V_I = V_{SS}$ or V_{DD}; no load					
		standby					
		no bus activity		-	1.5	10	µA
		bus activity		-	10	100	µA
		operating; f_{SCL} = 1 MHz					
		pin AOUT off		-	500	1400	µA
		pin AOUT active		-	1400	2500	µA
V_{POR}	power-on reset voltage		[1]	0.8	-	2.0	V
Digital inputs: pins SCL, SDA, A0, A1, A2, OSC and EXT							
V_{IL}	LOW-level input voltage			0	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
I_L	leakage current	$V_I = V_{SS}$ to V_{DD}		−100	-	+100	nA
C_i	input capacitance			-	-	550	pF
Digital output: pin SDA							
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{DD} = 5 V; C_L = 550 pF; f_{SCL} = 1 MHz		24	-	-	mA
Reference inputs: pins VREF and AGND							
V_{VREF}	voltage on pin VREF	$V_{VREF} - V_{AGND} \geq 1.6$ V		1.6	-	V_{DD}	V
V_{AGND}	voltage on pin AGND	$V_{VREF} - V_{AGND} \geq 1.6$ V		V_{SS}	-	$V_{DD} - 1.6$	V
I_{LI}	input leakage current			−100	-	+100	nA
R_{ref}	reference resistance	resistance between pin VREF and pin AGND		-	40	-	kΩ

Table 6. Static characteristic *...continued*

V_{DD} = 2.5 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

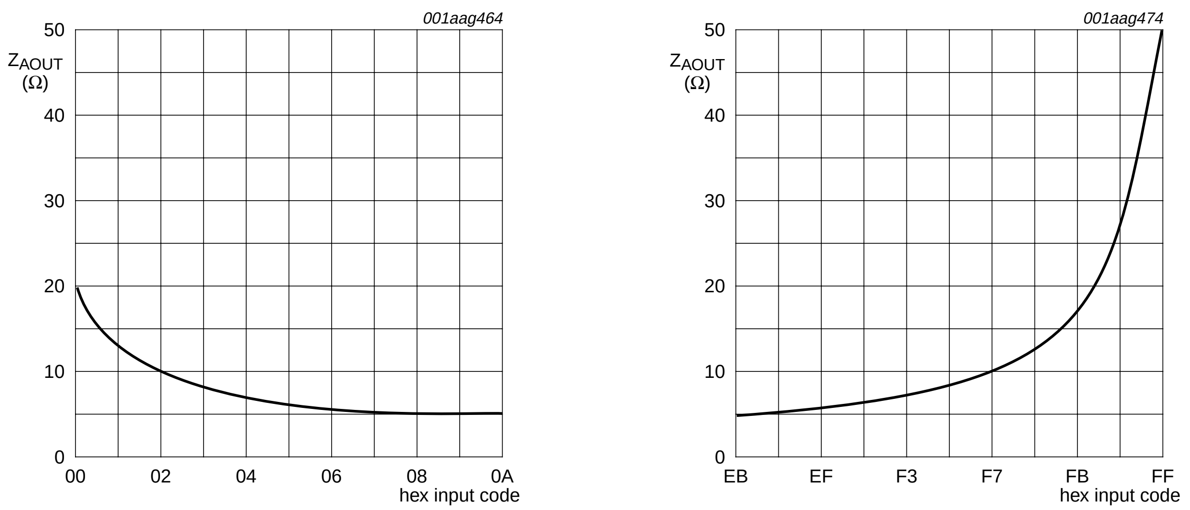
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Oscillator: pin OSC						
$f_{osc(int)}$	internal oscillator frequency	pin EXT = LOW	3.2	-	8.0	MHz
$f_{osc(ext)}$	external oscillator frequency	pin EXT = HIGH	3.5	-	5.5	MHz

[1] The power-on reset circuit resets the I²C-bus logic when $V_{DD} < V_{POR}$.



Internal oscillator on; analog output disabled; T_{amb} = 27 °C

Fig 20. Operating supply current as a function of supply voltage (typical)



a. Output impedance near negative power rail (V_{SS})

b. Output impedance near positive power rail (V_{DD})

T_{amb} = 27 °C; V_{DD} = 5 V; V_{VREF} = 5 V; V_{AGND} = 0 V, (typical values)

Fig 21. Output impedance of analog output buffer (near power rails)

10.2 Dynamic characteristics

Table 7. I²C-bus characteristics

V_{DD} = 2.5 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; reference to 30 % and 70 % with an input voltage swing of V_{SS} to V_{DD} (see Figure 22).

Symbol	Parameter	Conditions	Standard mode		Fast mode		Fast-mode Plus		Unit
			Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	[1]	0	100	0	400	0	1000	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	0.5	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		4.0	-	0.6	-	0.26	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	0.26	-	µs
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	0.26	-	µs
$t_{HD;DAT}$	data hold time		0	-	0	-	0	-	ns
$t_{VD;ACK}$	data valid acknowledge time	[2]	0.1	3.45	0.1	0.9	0.05	0.45	µs
$t_{VD;DAT}$	data valid time	[3]	300	-	75	-	75	450	ns
$t_{SU;DAT}$	data set-up time		250	-	100	-	50	-	ns
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	0.26	-	µs
t_f	fall time of both SDA and SCL signals	[4][5][6]	-	300	20 + 0.1C_b	300	-	120	ns
t_r	rise time of both SDA and SCL signals	[4][5][6]	-	1000	20 + 0.1C_b	300	-	120	ns
$t_{w(spike)}$	spike pulse width	[7]	-	50	-	50	-	50	ns

[1] The minimum SCL clock frequency is limited by the bus time-out feature which resets the serial bus interface if either the SDA or SCL is held LOW for a minimum of 25 ms. You must disable the bus time-out feature for DC operation.

[2] $t_{VD;ACK}$ = time for acknowledgement signal from SCL LOW to SDA (out) LOW.

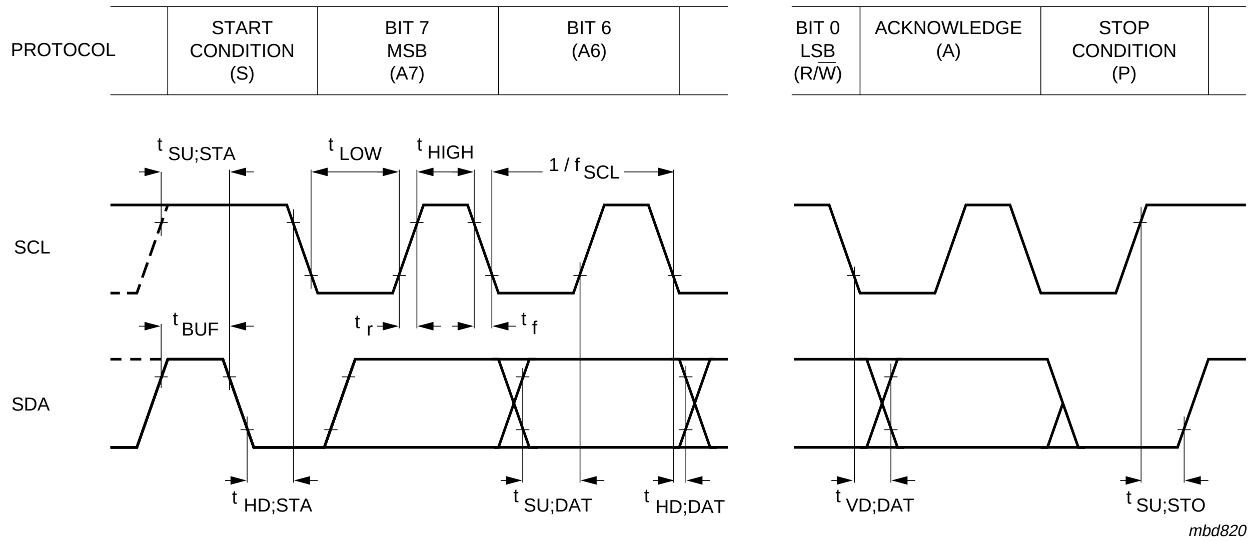
[3] $t_{VD;DAT}$ = minimum time for valid SDA (out) data following SCL LOW.

[4] A master device must internally provide a hold time of at least 300 ns for the SDA signal (refer to the V_{IL} of the SCL signal) in order to bridge the undefined region of the SCL's falling edge.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is 300 ns. The maximum fall time for the SDA output stage, t_f is 250 ns. This allows series protection resistors to be connected between the SDA pin and the SDA bus line and between the SCL pin and the SCL bus line without exceeding the maximum t_f.

[7] Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.



Rise and fall times refer to 30 % and 70 %

Fig 22. I^2C-bus timing diagram

Table 8. D/A characteristics

V_{DD} = 5.0 V; V_{SS} = 0 V; V_{VREF} = 5.0 V; V_{AGND} = 0 V; T_{amb} = −40 °C to +85 °C; R_L = 10 kΩ; C_L = 50 pF; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Analog output							
V_{AOUT}	voltage on pin AOUT	no resistive load		V_{SS}	-	V_{DD}	V
		R_L = 10 kΩ		V_{SS}	-	$0.9V_{DD}$	V
I_{LO}	output leakage current	pin AOUT disabled		−100	-	+100	nA
Accuracy							
E_G	gain error	no resistive load		-	-	1	%
E_O	offset error			-	-	±20	mV
E_L	linearity error	$f_{SCL} \leq 400$ kHz	[1]	-	-	±1.0	LSB
		$f_{SCL} > 400$ kHz	[1]	-	-	±1.5	LSB
$t_{s(DAC)}$	DAC settling time		[2]	-	-	2.4	µs
$f_{c(DAC)}$	DAC conversion frequency			-	-	44	kHz
$\alpha_{sup(n)}$	noise suppression	f = 100 Hz; $V_{n(VDD)(p-p)}$ = 100 mV		-	40	-	dB

[1] The linearity error is assured if the internal frequency is changed by setting bit 7 and bit 3 of the control byte to logic 1 (see Figure 5).

[2] The time from the start of AOUT to a change of ½ LSB full scale (see Section 7.3).

Table 9. A/D characteristics

V_{DD} = 5.0 V; V_{SS} = 0 V; V_{VREF} = 5.0 V; V_{AGND} = 0 V; T_{amb} = –40 °C to +85 °C; R_L = 10 kΩ; C_L = 50 pF; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Analog inputs							
V_{AIN}	voltage on pin AIN	pins AIN0 to AIN3		V_{SS}	-	V_{DD}	V
I_{LI}	input leakage current			–100	-	+100	nA
$C_{i(a)}$	analog input capacitance			-	10	-	pF
$C_{i(dif)}$	differential input capacitance			-	10	-	pF
$V_{i(se)}$	single-ended input voltage	measuring range		V_{AGND}	-	V_{VREF}	V
$V_{i(dif)}$	differential input voltage	measuring range: $V_{FS} = V_{VREF} - V_{AGND}$		$-0.5V_{FS}$	-	$+0.5V_{FS}$	V
Accuracy							
E_G	gain error	$f_{SCL} \leq 400$ kHz		-	-	1	%
		$f_{SCL} > 400$ kHz		-	-	3	%
E_O	offset error			-	-	±20	mV
E_L	linearity error	$f_{SCL} \leq 400$ kHz	[1]	-	-	±1.0	LSB
		$f_{SCL} > 400$ kHz	[1]	-	-	±2.0	LSB
CMRR	common-mode rejection ratio			-	40	-	dB
$\alpha_{sup(n)}$	noise suppression	f = 100 Hz; $V_{n(VDD)(p-p)}$ = 100 mV		-	40	-	dB
$t_{c(ADC)}$	ADC conversion time			-	-	8.5	µs
$f_{c(ADC)}$	ADC conversion frequency	f_{SCL} = 1 MHz		-	-	111	kHz

[1] The linearity error is assured if the internal frequency is changed by setting bit 7 and bit 3 of the control byte to logic 1 (see Figure 5).

11. Application information

Inputs must be connected to V_{SS} or V_{DD} when not in use. Analog inputs may also be connected to pins AGND or VREF.

In order to prevent excessive ground and supply noise and to minimize crosstalk of the digital-to-analog signal paths the printed-circuit board layout must be designed very carefully. Noisy digital circuits and ground loops must be avoided on the supply lines common to the PCA9691 device. Decoupling capacitors (> 10 µF) are recommended for power supply and reference voltage inputs.

During data transfer the first bit written out is the MSB and the last bit is the LSB.

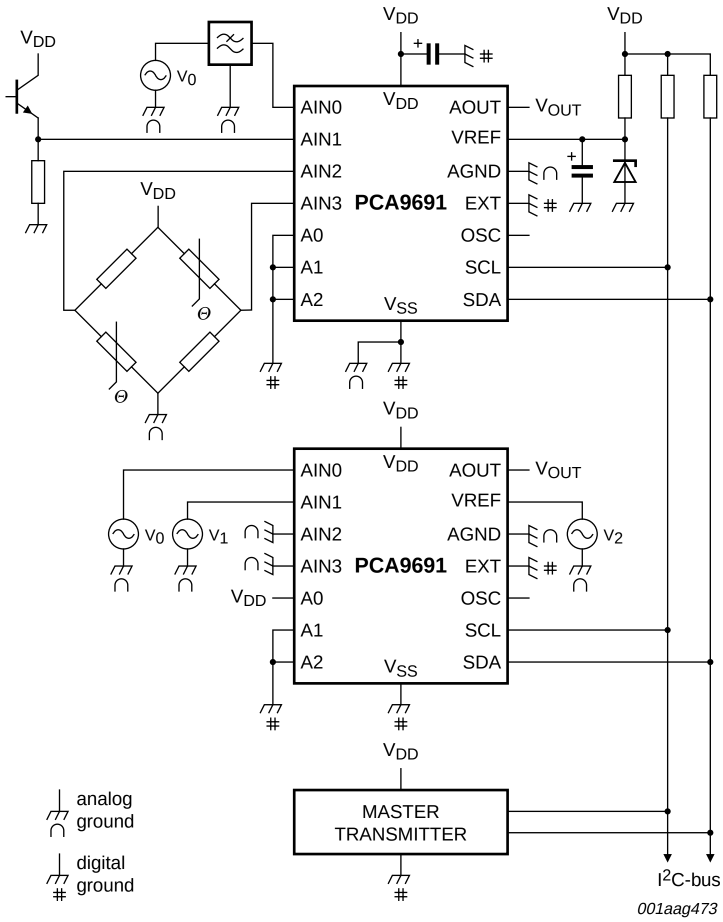
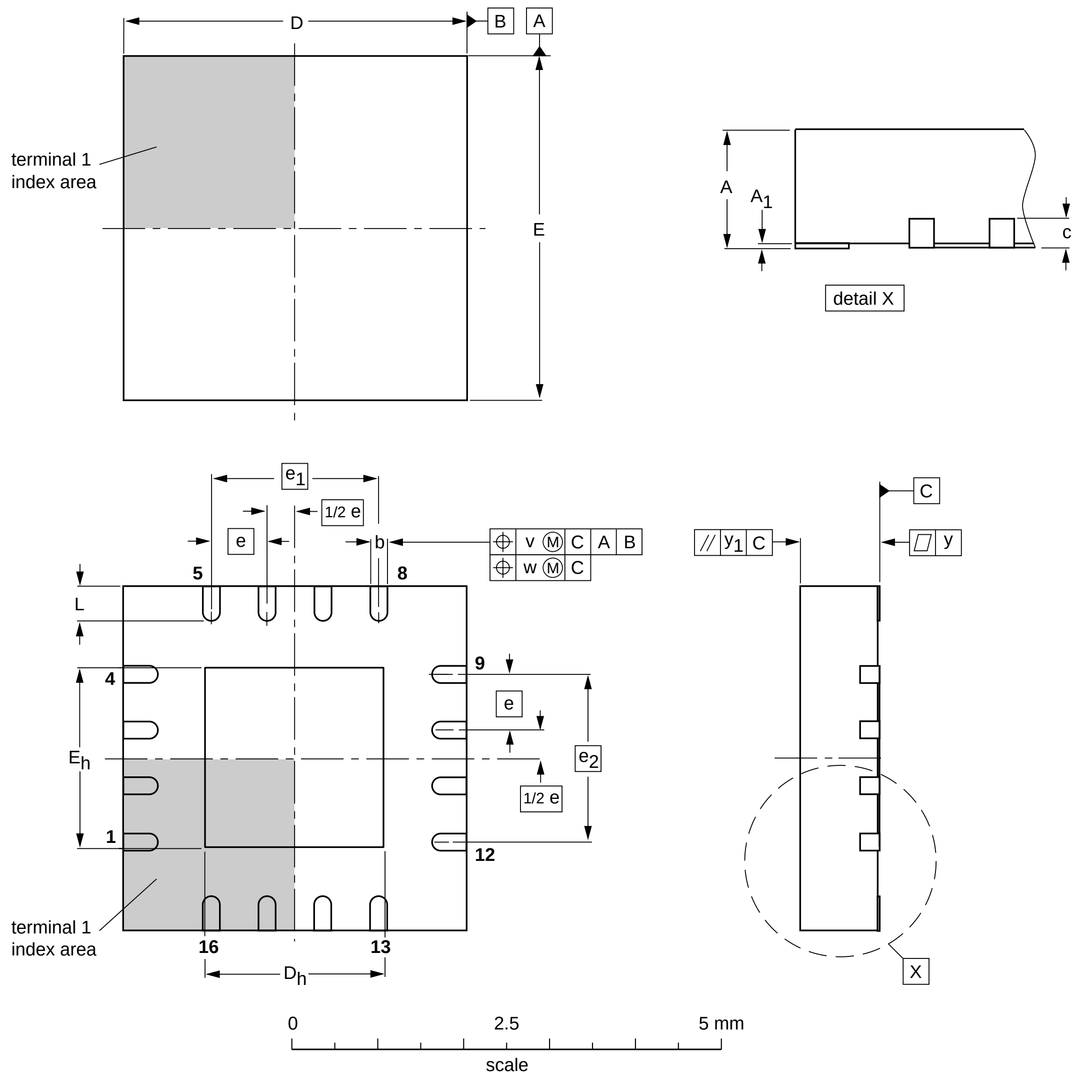


Fig 23. Application diagram

12. Package outline

HVQFN16: plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 4 x 4 x 0.85 mm **SOT629-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.38 0.23	0.2	4.1 3.9	2.25 1.95	4.1 3.9	2.25 1.95	0.65	1.95	1.95	0.75 0.50	0.1	0.05	0.05	0.1

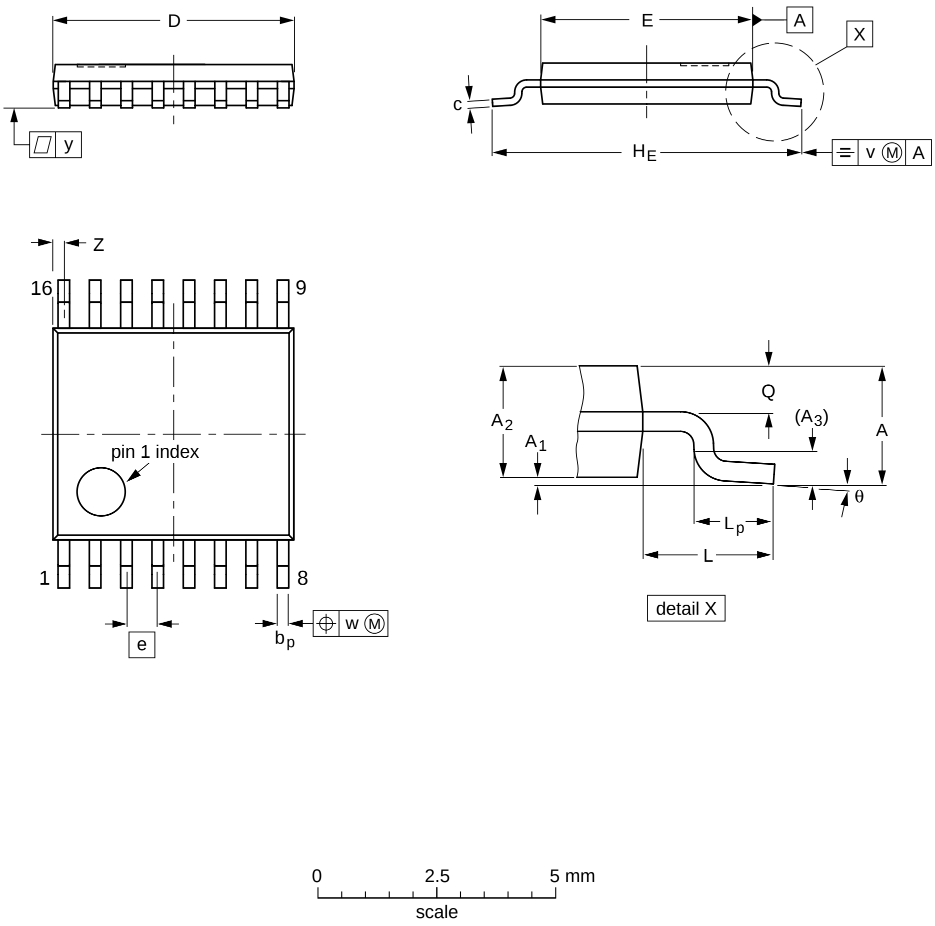
Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT629-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

Fig 24. Package outline SOT629-1 (HVQFN16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 25. Package outline SOT403-1 (TSSOP16)

13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 26) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 10 and 11

Table 10. SnPb eutectic process (from J-STD-020C)

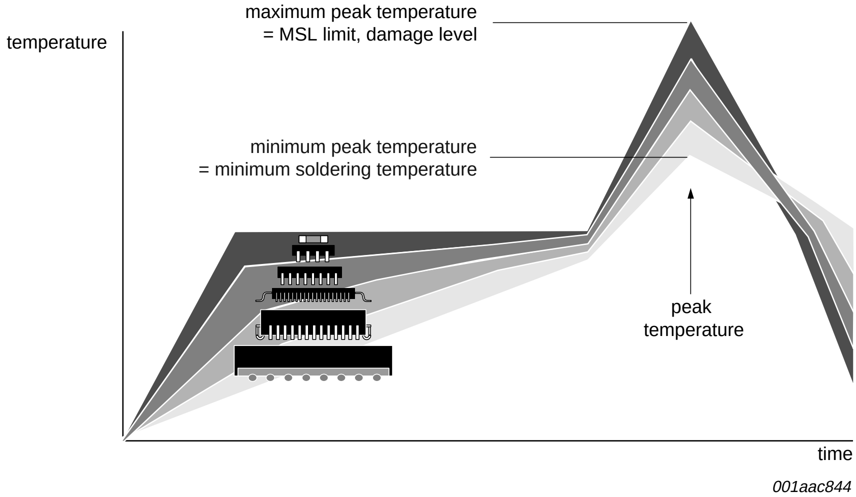
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 11. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 26.



MSL: Moisture Sensitivity Level

Fig 26. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9691_1	20080408	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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17. Contents

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