



# PCA9575

16-bit I<sup>2</sup>C-bus and SMBus, level translating, low voltage GPIO with reset and interrupt

Rev. 01 — 2 October 2008

Product data sheet

## 1. General description

The PCA9575 is a CMOS device that provides 16 bits of General Purpose parallel Input/Output (GPIO) expansion in low voltage processor and handheld battery powered mobile applications and was developed to enhance the NXP family of I<sup>2</sup>C-bus I/O expanders. The improvements include lower supply current, lower operating voltage of 1.1 V to 3.6 V, separate supply rails to allow voltage level translation anywhere between 1.1 V and 3.6 V with 3.6 V tolerant I/Os, 400 kHz clock frequency, and smaller packaging. Any of the 16 I/O ports can be configured as an input or output independent of each other and default on start-up to inputs.

I/O expanders provide a simple solution when additional I/Os are needed while keeping interconnections to a minimum; for example in battery powered mobile applications and clamshell devices for interfacing to sensors, push buttons, keypad, etc. In addition to providing a flexible set of GPIOs, it simplifies interconnection of a processor running at one voltage level to I/O devices operating at a different (usually higher) voltage level. PCA9575 has built-in level shifting feature that makes these devices extremely flexible in mixed signal environments where communication between incompatible I/Os is required. The core of PCA9575 can operate at a voltage as low as 1.1 V while each I/O bank can operate in the range 1.1 V to 3.6 V. Bus hold with programmable on-chip pull-up or pull-down feature for I/Os is also provided.

The output stage consists of two banks each of 8-bit configuration registers, input registers, interrupt mask registers, output registers, bus-hold and pull-up/pull-down registers and polarity inversion registers. These registers allow the system master to program and configure 16 GPIOs through the I<sup>2</sup>C-bus.

The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration register bits. The data for each input or output is kept in the corresponding Input or Output register. The polarity of the read registers can be inverted with the Polarity Inversion register (active HIGH or active LOW operation). Either a bus-hold function or pull-up/pull-down feature can be selected by programming corresponding registers. The bus-hold provides a valid logic level when the I/O bus is not actively driven. When bus-hold feature is not selected, the I/O ports can be configured to have pull-up or pull-down by programming the pull-up/pull-down configuration register.

An open-drain interrupt output pin ( $\overline{\text{INT}}$ ) allows monitoring of the input pins and is asserted each time a change occurs on an input port unless that port is masked (default = masked). A 'GPIO All Call' command allows programming multiple PCA9575s at the same time even if they have different individual I<sup>2</sup>C-bus addresses. This allows optimal code programming when more than one device needs to be programmed with the same instruction or if all outputs need to be turned on or off at the same time. The internal

Power-On Reset (POR) or hardware reset pin ( $\overline{\text{RESET}}$ ) initializes the two banks of 8 I/Os as inputs, sets the registers to their default values and initializes the device state machine. The I/O banks are held in its default state when the logic supply ( $V_{DD}$ ) is off.

The PCA9575 is available in 24-pin TSSOP, 28-pin TSSOP and HWQFN24 packages, and is specified over the  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  industrial temperature range.

The 28-pin package provides four address select pins, allowing up to 16 PCA9575 devices to be connected with 16 different addresses on the same I<sup>2</sup>C-bus.

## 2. Features

- Separate supply rails for core logic and each of the two I/O banks provides voltage level shifting
- 1.1 V to 3.6 V operation with level shifting feature and 3.6 V tolerant
- Very low standby current:  $< 2\text{ }\mu\text{A}$
- 16 configurable I/O pins organized as 2 banks that default to inputs at power-up
- Outputs:
  - ◆ Programmable totem pole or open-drain (1 mA source and 3 mA sink)
  - ◆ Independently programmable 100 k $\Omega$  pull-up or pull-down for each I/O pin
  - ◆ Open-drain active LOW interrupt ( $\overline{\text{INT}}$ ) output pin allows monitoring of logic level change of pins programmed as inputs
- Inputs:
  - ◆ Programmable bus hold provides valid logic level when inputs are not actively driven
  - ◆ Programmable Interrupt Mask Control for input pins that do not require an interrupt when their states change or to prevent spurious interrupts default to mask at power-up
  - ◆ Polarity Inversion register allows inversion of the polarity of the I/O pins when read
- 400 kHz I<sup>2</sup>C-bus serial interface
- Compliant with I<sup>2</sup>C-bus Standard-mode (100 kHz)
- Active LOW reset ( $\overline{\text{RESET}}$ ) input pin resets device to power-up default state
- GPIO All Call address allows programming of more than one device at the same time with the same parameters
- 16 programmable slave addresses using 4 address pins (28-pin TSSOP only)
- $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  operation
- ESD protection exceeds 6000 V HBM per JESD22-A114, 500 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: TSSOP28, TSSOP24, HWQFN24

### 3. Applications

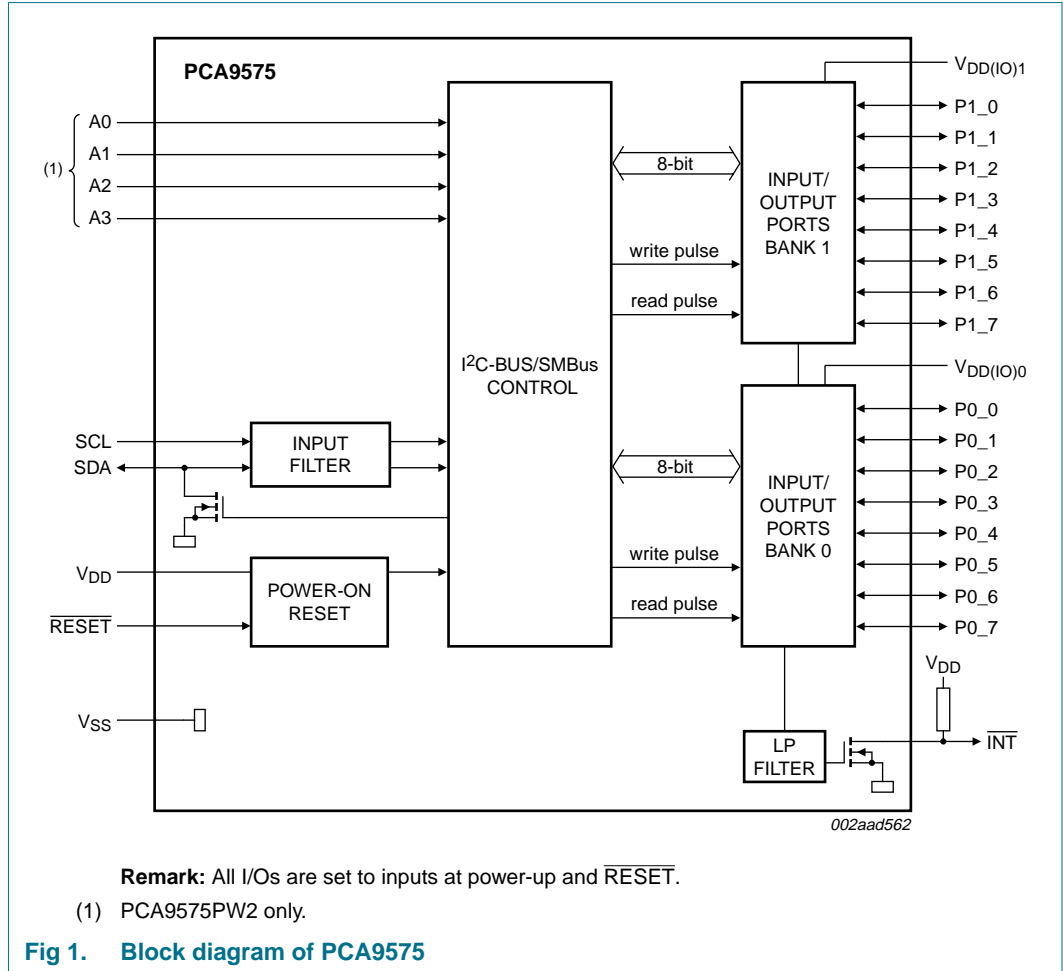
- Cell phones
- Media players
- Multi-voltage environments
- Battery operated mobile gadgets
- Motherboards
- Servers
- RAID systems
- Industrial control
- Medical equipment
- PLCs
- Gaming machines
- Instrumentation and test measurement

### 4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PCA9575PW2	PCA9575PW2	TSSOP28	plastic thin shrink small outline package; 28 leads; body width 4.4 mm	SOT361-1
PCA9575PW1	PA9575PW1	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
PCA9575HF	575F	HWQFN24	plastic thermal enhanced very very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.75 mm	SOT994-1

5. Block diagram



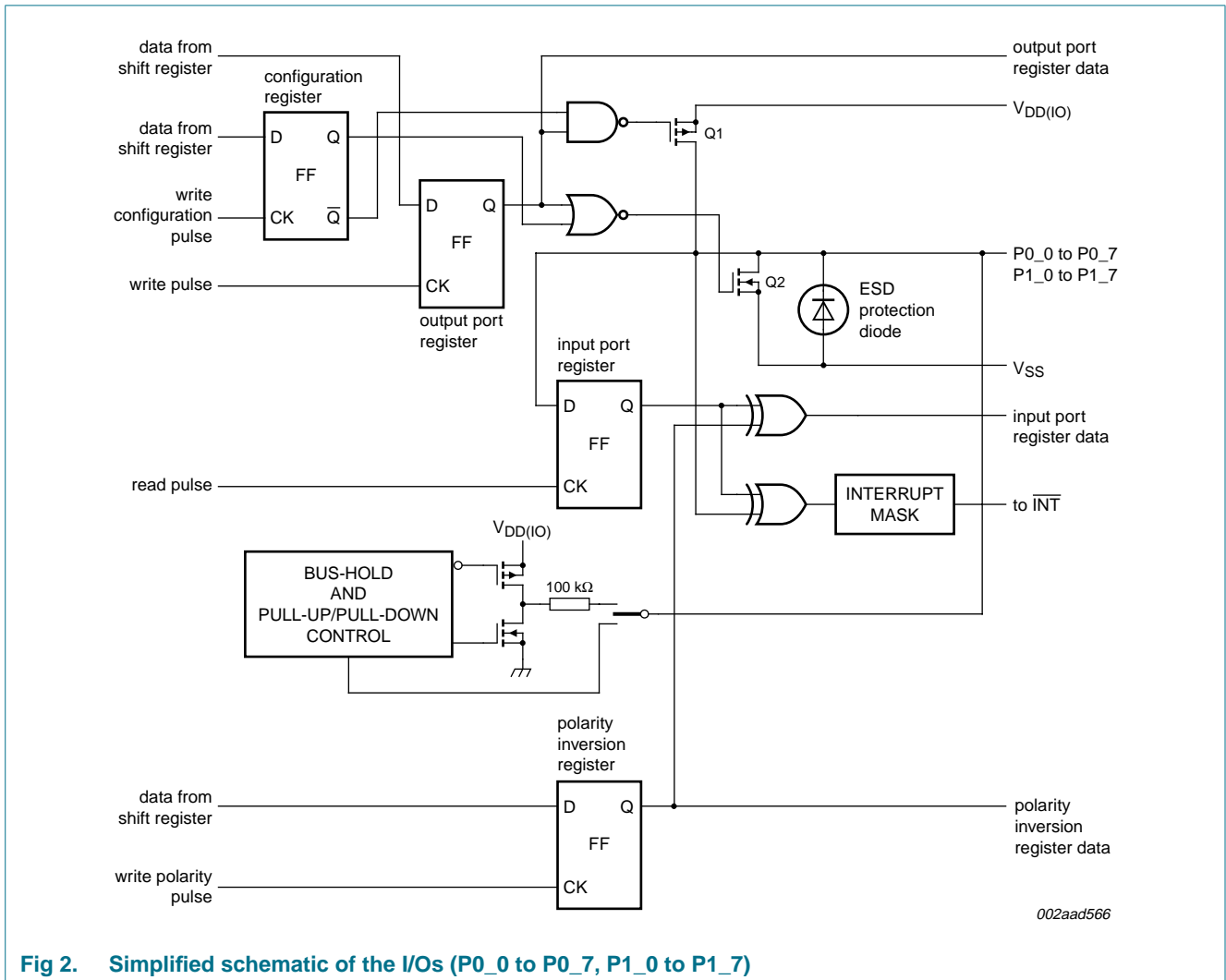


Fig 2. Simplified schematic of the I/Os (P0\_0 to P0\_7, P1\_0 to P1\_7)

## 6. Pinning information

### 6.1 Pinning

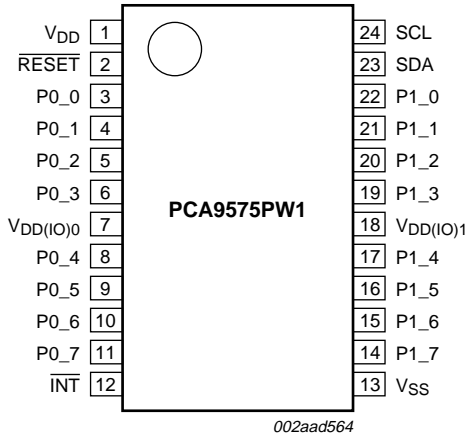


Fig 3. Pin configuration for TSSOP24

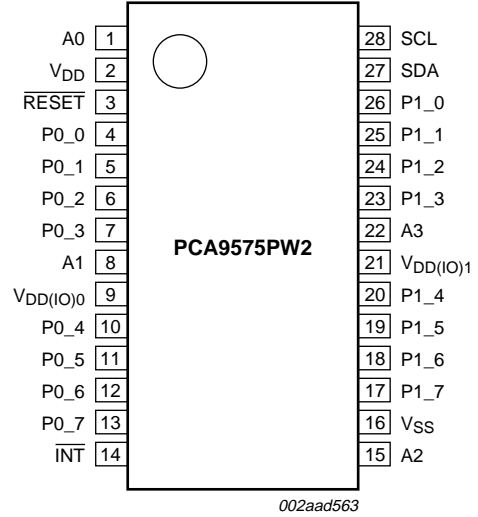


Fig 4. Pin configuration for TSSOP28

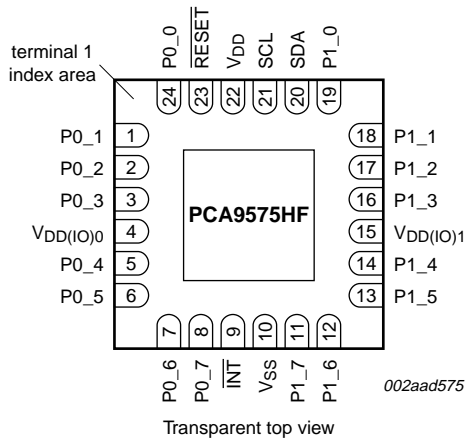


Fig 5. Pin configuration for HWQFN24

## 6.2 Pin description

Table 2. Pin description

Symbol	Pin			Type	Description
	TSSOP28	TSSOP24	HWQFN24		
A0	1	-	-	I	address input 0
V <sub>DD</sub>	2	1	22	power supply	supply voltage
$\overline{\text{RESET}}$	3	2	23	I	active LOW reset input
P0_0	4	3	24	I/O	port 0 input/output 0
P0_1	5	4	1	I/O	port 0 input/output 1
P0_2	6	5	2	I/O	port 0 input/output 2
P0_3	7	6	3	I/O	port 0 input/output 3
A1	8	-	-	I	address input 1
V <sub>DD(I/O)0</sub>	9	7	4	power supply	I/O supply voltage for bank 0
P0_4	10	8	5	I/O	port 0 input/output 0
P0_5	11	9	6	I/O	port 0 input/output 1
P0_6	12	10	7	I/O	port 0 input/output 2
P0_7	13	11	8	I/O	port 0 input/output 3
$\overline{\text{INT}}$	14	12	9	O	interrupt output (open-drain; active LOW)
A2	15	-	-	I	address input 2
V <sub>SS</sub>	16	13	10 <sup>[1]</sup>	ground	supply ground
P1_7	17	14	11	I/O	port 1 input/output 4
P1_6	18	15	12	I/O	port 1 input/output 5
P1_5	19	16	13	I/O	port 1 input/output 6
P1_4	20	17	14	I/O	port 1 input/output 7
V <sub>DD(I/O)1</sub>	21	18	15	power supply	I/O supply voltage for bank 1
A3	22	-	-	I	address input 3
P1_3	23	19	16	I/O	port 1 input/output 3
P1_2	24	20	17	I/O	port 1 input/output 2
P1_1	25	21	18	I/O	port 1 input/output 1
P1_0	26	22	19	I/O	port 1 input/output 0
SDA	27	23	20	I/O	serial data line
SCL	28	24	21	I	serial clock line

[1] HWQFN24 package die supply ground is connected to both V<sub>SS</sub> pin and exposed center pad. V<sub>SS</sub> pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the PCB in the thermal pad region.

## 7. Functional description

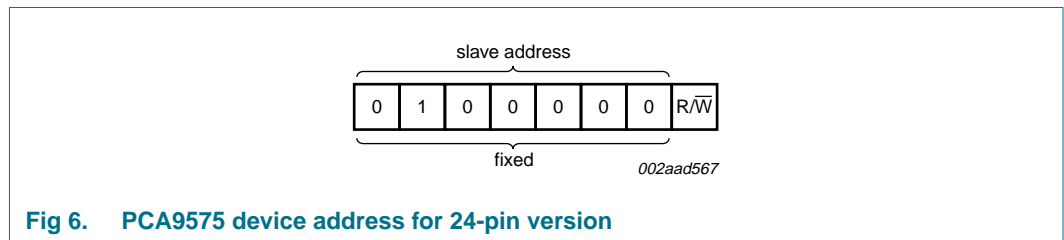
### 7.1 I/O ports

The 16 I/O ports are organized as two banks of 8 ports each. The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration register bits. The data for each input or output is kept in the corresponding Input or Output register. The polarity of the read register can be inverted with the Polarity Inversion register. Either a bus-hold function or pull-up/pull-down feature can be selected by programming corresponding registers. A bus-hold provides a valid logic level when the I/O bus is not actively driven. It consists of a pair of buffers, one being weak (low drive-strength), that latch the input at the last driven value. This prevents the input from floating while it is being driven by a 3-state output. Latching the last valid logic state of input prevents it from settling at a midpoint between V<sub>DD</sub> and ground that in turn consumes power. An active bus driver can easily override the logic level set by the bus-keeper.

When bus-hold feature is not selected, the I/O ports can be configured to have pull-up or pull-down by programming the pull-up/pull-down configuration register.

### 7.2 Device address

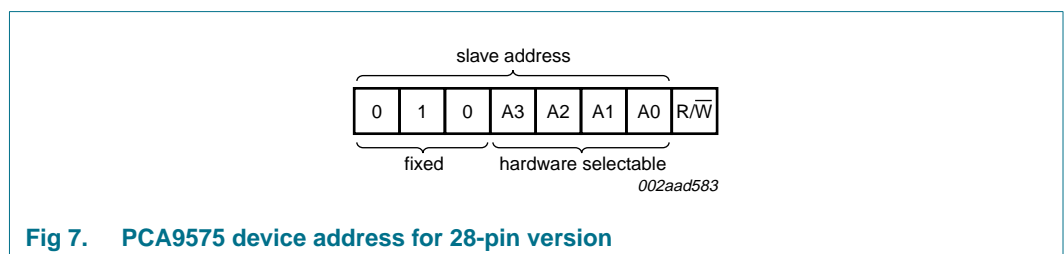
Following a START condition, the bus master must send the address of the slave it is accessing and the operation it wants to perform (read or write). Address configuration for the device depends on the package type chosen. The device offered in a 24-pin package will have a fixed slave address for the PCA9575 as shown in [Figure 6](#).



**Fig 6. PCA9575 device address for 24-pin version**

The last bit of the first byte defines the operation to be performed. When set to logic 1 a read is selected, while logic 0 selects a write operation.

The slave address for the 28-pin version of the PCA9575 is shown in [Figure 7](#).



**Fig 7. PCA9575 device address for 28-pin version**



### 7.3 Command register

Following the successful acknowledgement of the slave address + R/W bit, the bus master will send a byte to the PCA9575, which will be stored in the Command register.

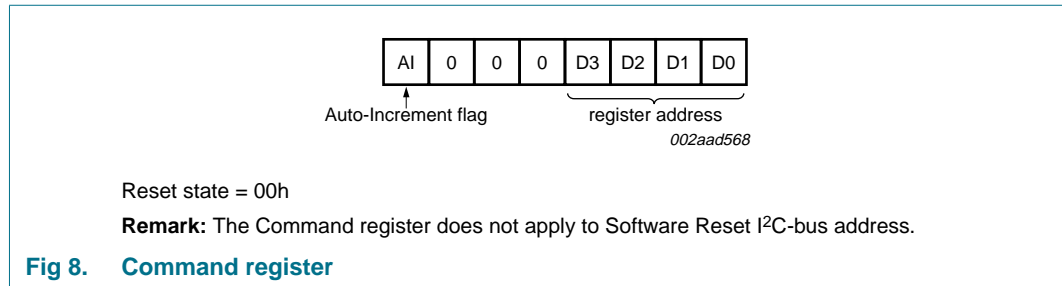


Fig 8. Command register

The lowest 4 bits are used as a pointer to determine which register will be accessed. Only a Command register code with the 4 least significant bits equal to the 16 allowable values as defined in [Table 3 “Register summary”](#) will be acknowledged. Reserved or undefined command codes will not be acknowledged. At power-up, this register defaults to 00h, with the AI bit set to logic 0, and the lowest 4 bits set to logic 0.

### 7.4 Register definitions

Table 3. Register summary

Register number	D3	D2	D1	D0	Name	Type	Function
00h	0	0	0	0	IN0	read only	Input port 0 register
01h	0	0	0	1	IN1	read only	Input port 1 register
02h	0	0	1	0	INVRT0	read/write	Polarity inversion port 0 register
03h	0	0	1	1	INVRT1	read/write	Polarity inversion port 1 register
04h	0	1	0	0	BKEN0	read/write	Bus-hold enable 0 register
05h	0	1	0	1	BKEN1	read/write	Bus-hold enable 1 register
06h	0	1	1	0	PUPD0	read/write	Pull-up/pull-down selector port 0 register
07h	0	1	1	1	PUPD1	read/write	Pull-up/pull-down selector port 1 register
08h	1	0	0	0	CFG0	read/write	Configuration port 0 register
09h	1	0	0	1	CFG1	read/write	Configuration port 1 register
0Ah	1	0	1	0	OUT0	read/write	Output port 0 register
0Bh	1	0	1	1	OUT1	read/write	Output port 1 register
0Ch	1	1	0	0	MSK0	read/write	Interrupt mask port 0 register
0Dh	1	1	0	1	MSK1	read/write	Interrupt mask port 1 register
0Eh	1	1	1	0	INTS0	read only	Interrupt status port 0 register
0Fh	1	1	1	1	INTS1	read only	Interrupt status port 1 register

### 7.5 Writing to port registers

Data is transmitted to the PCA9575 by sending the device address and setting the least significant bit to logic 0 (see [Figure 6](#) or [Figure 7](#) for device address). The command byte is sent after the address and determines which register will receive the data following the command byte. Each 8-bit register may be updated independently of the other registers.

## 7.6 Reading the port registers

In order to read data from the PCA9575, the bus master must first send the PCA9575 address with the least significant bit set to a logic 0 (see [Figure 6](#) or [Figure 7](#) for device address). The command byte is sent after the address and determines which register will be accessed. After a restart, the device address is sent again but this time, the least significant bit is set to logic 1. Data from the register defined by the command byte will then be sent by the PCA9575. Data is clocked into the register on the falling edge of the acknowledge clock pulse. After the first byte is read, additional bytes may be read using the auto-increment feature.

### 7.6.1 Register 0 - Input port 0 register

This register is read-only. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. Writes to this register will be acknowledged but will have no effect.

The default 'X' is determined by the externally applied logic level.

**Table 4. Register 0 - Input port 0 register (address 00h) bit description**

Bit	Symbol	Access	Value	Description
7	IO0.7	read only	X	determined by externally applied logic level
6	IO0.6	read only	X	
5	IO0.5	read only	X	
4	IO0.4	read only	X	
3	IO0.3	read only	X	
2	IO0.2	read only	X	
1	IO0.1	read only	X	
0	IO0.0	read only	X	

### 7.6.2 Register 1 - Input port 1 register

This register is read-only. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. Writes to this register will be acknowledged but will have no effect.

The default 'X' is determined by the externally applied logic level.

**Table 5. Register 1 - Input port 1 register (address 01h) bit description**

Bit	Symbol	Access	Value	Description
7	IO1.7	read only	X	determined by externally applied logic level
6	IO1.6	read only	X	
5	IO1.5	read only	X	
4	IO1.4	read only	X	
3	IO1.3	read only	X	
2	IO1.2	read only	X	
1	IO1.1	read only	X	
0	IO1.0	read only	X	

**7.6.3 Register 2 - Polarity inversion port 0 register**

This register allows the user to invert the polarity of the Input port register data. If a bit in this register is set (written with '1'), the corresponding Input port data is inverted. If a bit in this register is cleared (written with a '0'), the Input port data polarity is retained.

**Table 6. Register 2 - Polarity Inversion port 0 register (address 02h) bit description**

Legend: \* default value.

Bit	Symbol	Access	Value	Description
7	N0.7	R/W	0*	inverts polarity of Input port 0 register data
6	N0.6	R/W	0*	0 = Input port 0 register data retained (default value)
5	N0.5	R/W	0*	1 = Input port 0 register data inverted
4	N0.4	R/W	0*	
3	N0.3	R/W	0*	
2	N0.2	R/W	0*	
1	N0.1	R/W	0*	
0	N0.0	R/W	0*	

**7.6.4 Register 3 - Polarity inversion port 1 register**

This register allows the user to invert the polarity of the Input port register data. If a bit in this register is set (written with '1'), the corresponding Input port data is inverted. If a bit in this register is cleared (written with a '0'), the Input port data polarity is retained.

**Table 7. Register 3 - Polarity Inversion port 1 register (address 03h) bit description**

Legend: \* default value.

Bit	Symbol	Access	Value	Description
7	N1.7	R/W	0*	inverts polarity of Input port 1 register data
6	N1.6	R/W	0*	0 = Input port 1 register data retained (default value)
5	N1.5	R/W	0*	1 = Input port 1 register data inverted
4	N1.4	R/W	0*	
3	N1.3	R/W	0*	
2	N1.2	R/W	0*	
1	N1.1	R/W	0*	
0	N1.0	R/W	0*	

**7.6.5 Register 4 - Bus-hold/pull-up/pull-down enable 0 register**

Bit 0 of this register allows the user to enable/disable the bus-hold feature for the I/O pins. Setting the bit 0 to logic 1 enables bus-hold feature for the I/O bank 0. In this mode, the pull-up/pull-downs will be disabled for I/O bank 0. Setting the bit 0 to logic 0 disables bus-hold feature.

Bit 1 of this register allows the user to enable/disable pull-up/pull-downs on the I/O pins. Setting the bit 1 to logic 1 enables selection of pull-up/pull-down using Register 6. Setting the bit 1 to logic 0 disables pull-up/pull-downs on the I/O bank 0 pins and contents of Register 6 will have no effect on the I/O.

**Table 8. Register 4 - Bus-hold/pull-up/pull-down enable 0 register (address 04h) bit description**

Legend: \* default value.

Bit	Symbol	Access	Value	Description
7	E0.7	R/W	X	not used
6	E0.6	R/W	X	
5	E0.5	R/W	X	
4	E0.4	R/W	X	
3	E0.3	R/W	X	
2	E0.2	R/W	X	
1	E0.1	R/W	0*	allows the user to enable/disable pull-up/pull-downs on the I/O bank 0 pins 0 = disables pull-up/pull-downs on the I/O bank 0 pins and contents of Register 6 will have no effect on the I/O bank 0 (default value) 1 = enables selection of pull-up/pull-down using Register 6
0	E0.0	R/W	0*	allows user to enable/disable the bus-hold feature for the I/O bank 0 pins 0 = disables bus-hold feature (default value) 1 = enables bus-hold feature

**7.6.6 Register 5 - Bus-hold/pull-up/pull-down enable 1 register**

Bit 0 of this register allows the user to enable/disable the bus-hold feature for the I/O pins. Setting the bit 0 to logic 1 enables bus-hold feature for the I/O bank 1. In this mode, the pull-up/pull-downs will be disabled for I/O bank 1. Setting the bit 0 to logic 0 disables bus-hold feature.

Bit 1 of this register allows the user to enable/disable pull-up/pull-downs on the I/O pins. Setting the bit 1 to logic 1 enables selection of pull-up/pull-down using Register 7. Setting the bit 1 to logic 0 disables pull-up/pull-downs on the I/O bank 1 pins and contents of Register 7 will have no effect on the I/O.

**Table 9. Register 5 - Bus-hold/pull-up/pull-down enable 1 register (address 05h) bit description**

Legend: \* default value.

Bit	Symbol	Access	Value	Description
7	E1.7	R/W	X	not used
6	E1.6	R/W	X	
5	E1.5	R/W	X	
4	E1.4	R/W	X	
3	E1.3	R/W	X	
2	E1.2	R/W	X	
1	E1.1	R/W	0*	allows the user to enable/disable pull-up/pull-downs on the I/O bank 1 pins 0 = disables pull-up/pull-downs on the I/O bank 1 pins and contents of Register 7 will have no effect on the I/O bank 0 (default value) 1 = enables selection of pull-up/pull-down using Register 7
0	E1.0	R/W	0*	allows user to enable/disable the bus-hold feature for the I/O bank 1 pins 0 = disables bus-hold feature (default value) 1 = enables bus-hold feature

**7.6.7 Register 6 - Pull-up/pull-down select port 0 register**

When bus-hold feature is not selected and bit 1 of Register 4 is set to logic 1, the I/O port 0 can be configured to have pull-up or pull-down by programming the pull-up/pull-down register. Setting a bit to logic 1 will select a 100 kΩ pull-up resistor for that I/O pin. Setting a bit to logic 0 will select a 100 kΩ pull-down resistor for that I/O pin. If the bus-hold feature is enabled, writing to this register will have no effect on pull-up/pull-down selection.

**Table 10. Register 6 - Pull-up/pull-down select port 0 register (address 06h) bit description**  
 Legend: \* default value.

Bit	Symbol	Access	Value	Description
7	P0.7	R/W	1*	configures I/O port 0 pin to have pull-up or pull-down when bus-hold feature not selected and bit 1 of Register 4 is logic 1 0 = selects a 100 kΩ pull-down resistor for that I/O pin 1 = selects a 100 kΩ pull-up resistor for that I/O pin (default value)
6	P0.6	R/W	1*	
5	P0.5	R/W	1*	
4	P0.4	R/W	1*	
3	P0.3	R/W	1*	
2	P0.2	R/W	1*	
1	P0.1	R/W	1*	
0	P0.0	R/W	1*	

**7.6.8 Register 7 - Pull-up/pull-down select port 1 register**

When bus-hold feature is not selected and bit 1 of Register 5 is set to logic 1, the I/O port 1 can be configured to have pull-up or pull-down by programming the pull-up/pull-down register. Setting a bit to logic 1 will select a 100 kΩ pull-up resistor for that I/O pin. Setting a bit to logic 0 will select a 100 kΩ pull-down resistor for that I/O pin. If the bus-hold feature is enabled, writing to this register will have no effect on pull-up/pull-down selection.

**Table 11. Register 7 - Pull-up/pull-down select port 1 register (address 07h) bit description**  
 Legend: \* default value.

Bit	Symbol	Access	Value	Description
7	P1.7	R/W	1*	configures I/O port 1 pin to have pull-up or pull-down when bus-hold feature not selected and bit 1 of Register 5 is logic 1 0 = selects a 100 kΩ pull-down resistor for that I/O pin 1 = selects a 100 kΩ pull-up resistor for that I/O pin (default value)
6	P1.6	R/W	1*	
5	P1.5	R/W	1*	
4	P1.4	R/W	1*	
3	P1.3	R/W	1*	
2	P1.2	R/W	1*	
1	P1.1	R/W	1*	
0	P1.0	R/W	1*	

**7.6.9 Register 8 - Configuration port 0 register**

This register configures the direction of the I/O pins. If a bit in this register is set (written with logic 1), the corresponding port 0 pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared (written with logic 0), the corresponding port 0 pin is enabled as an output. At reset, the device's ports are inputs.

**Table 12. Register 8 - Configuration port 0 register (address 08h) bit description**

Legend: \* default value.

Bit	Symbol	Access	Value	Description
7	C0.7	R/W	1*	configures the direction of the I/O pins
6	C0.6	R/W	1*	0 = corresponding port pin enabled as an output
5	C0.5	R/W	1*	1 = corresponding port pin configured as input (default value)
4	C0.4	R/W	1*	
3	C0.3	R/W	1*	
2	C0.2	R/W	1*	
1	C0.1	R/W	1*	
0	C0.0	R/W	1*	

**7.6.10 Register 9 - Configuration port 1 register**

This register configures the direction of the I/O pins. If a bit in this register is set (written with logic 1), the corresponding port 1 pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared (written with logic 0), the corresponding port 1 pin is enabled as an output. At reset, the device's ports are inputs.

**Table 13. Register 9 - Configuration port 1 register (address 09h) bit description**

Legend: \* default value.

Bit	Symbol	Access	Value	Description
7	C1.7	R/W	1*	configures the direction of the I/O pins
6	C1.6	R/W	1*	0 = corresponding port pin enabled as an output
5	C1.5	R/W	1*	1 = corresponding port pin configured as input (default value)
4	C1.4	R/W	1*	
3	C1.3	R/W	1*	
2	C1.2	R/W	1*	
1	C1.1	R/W	1*	
0	C1.0	R/W	1*	

### 7.6.11 Register 10 - Output port 0 register

This register is an output-only port. It reflects the outgoing logic levels of the pins defined as outputs by Register 8. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, **not** the actual pin value.

**Table 14. Register 10 - Output port 0 register (address 0Ah) bit description**

Legend: \* default value.

Bit	Symbol	Access	Value	Description
7	O0.7	R/W	0*	reflects outgoing logic levels of pins defined as outputs by Register 8
6	O0.6	R/W	0*	
5	O0.5	R/W	0*	
4	O0.4	R/W	0*	
3	O0.3	R/W	0*	
2	O0.2	R/W	0*	
1	O0.1	R/W	0*	
0	O0.0	R/W	0*	

### 7.6.12 Register 11 - Output port 1 register

This register is an output-only port. It reflects the outgoing logic levels of the pins defined as outputs by Register 9. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, **not** the actual pin value.

**Table 15. Register 11 - Output port 1 register (address 0Bh) bit description**

Legend: \* default value.

Bit	Symbol	Access	Value	Description
7	O1.7	R/W	0*	reflects outgoing logic levels of pins defined as outputs by Register 9
6	O1.6	R/W	0*	
5	O1.5	R/W	0*	
4	O1.4	R/W	0*	
3	O1.3	R/W	0*	
2	O1.2	R/W	0*	
1	O1.1	R/W	0*	
0	O1.0	R/W	0*	



**7.6.13 Register 12 - Interrupt mask port 0 register**

All the bits of Interrupt mask port 0 register are set to logic 1 upon power-on or software reset, thus disabling interrupts. Interrupts may be enabled by setting corresponding mask bits to logic 0.

**Table 16. Register 12 - Interrupt mask port 0 register (address 0Ch) bit description**

Legend: \* default value.

Bit	Symbol	Access	Value	Description
7	M0.7	R/W	1*	enable or disable interrupts
6	M0.6	R/W	1*	0 = enable interrupt
5	M0.5	R/W	1*	1 = disable interrupt (default value)
4	M0.4	R/W	1*	
3	M0.3	R/W	1*	
2	M0.2	R/W	1*	
1	M0.1	R/W	1*	
0	M0.0	R/W	1*	

**7.6.14 Register 13 - Interrupt mask port 1 register**

All the bits of Interrupt mask port 1 register are set to logic 1 upon power-on or software reset, thus disabling interrupts. Interrupts may be enabled by setting corresponding mask bits to logic 0.

**Table 17. Register 13 - Interrupt mask port 1 register (address 0Dh) bit description**

Legend: \* default value.

Bit	Symbol	Access	Value	Description
7	M1.7	R/W	1*	enable or disable interrupts
6	M1.6	R/W	1*	0 = enable interrupt
5	M1.5	R/W	1*	1 = disable interrupt (default value)
4	M1.4	R/W	1*	
3	M1.3	R/W	1*	
2	M1.2	R/W	1*	
1	M1.1	R/W	1*	
0	M1.0	R/W	1*	

**7.6.15 Register 14 - Interrupt status port 0 register**

This register is read-only. It is used to identify the source of interrupt.

**Remark:** If the interrupts are masked, this register will return all zeros.

**Table 18. Register 14 - Interrupt status port 0 register (address 0Eh) bit description**

Legend: \* default value.

Bit	Symbol	Access	Value	Description
7	S0.7	read only	0*	identifies source of interrupt
6	S0.6	read only	0*	
5	S0.5	read only	0*	
4	S0.4	read only	0*	
3	S0.3	read only	0*	
2	S0.2	read only	0*	
1	S0.1	read only	0*	
0	S0.0	read only	0*	

**7.6.16 Register 15 - Interrupt status port 1 register**

This register is read-only. It is used to identify the source of interrupt.

**Remark:** If the interrupts are masked, this register will return all zeros.

**Table 19. Register 15 - Interrupt status port 1 register (address 0Fh) bit description**

Legend: \* default value.

Bit	Symbol	Access	Value	Description
7	S1.7	read only	0*	identifies source of interrupt
6	S1.6	read only	0*	
5	S1.5	read only	0*	
4	S1.4	read only	0*	
3	S1.3	read only	0*	
2	S1.2	read only	0*	
1	S1.1	read only	0*	
0	S1.0	read only	0*	

**7.7 Power-on reset**

When power is applied to V<sub>DD</sub>, an internal Power-On Reset (POR) holds the PCA9575 in a reset condition until V<sub>DD</sub> has reached V<sub>POR</sub>. At that point, the reset condition is released and the PCA9575 registers and state machine will initialize to their default states. The power-on reset typically completes the reset and enables the part by the time the power supply is above V<sub>POR</sub>. However, when it is required to reset the part by lowering the power supply, it is necessary to lower it below 0.2 V.

**7.8 RESET input**

A reset can be accomplished by holding the  $\overline{\text{RESET}}$  pin LOW for a minimum of t<sub>w(rst)</sub>. The PCA9575 registers and I<sup>2</sup>C-bus state machine will be held in their default state until the  $\overline{\text{RESET}}$  input is once again HIGH.

## 7.9 Software reset

The Software Reset Call allows all the devices in the I<sup>2</sup>C-bus to be reset to the power-up state value through a specific formatted I<sup>2</sup>C-bus command. To be performed correctly, it implies that the I<sup>2</sup>C-bus is functional and that there is no device hanging the bus.

The Software Reset sequence is defined as following:

1. A START command is sent by the I<sup>2</sup>C-bus master.
2. The reserved General Call I<sup>2</sup>C-bus address '0000 000' with the R/W bit set to 0 (write) is sent by the I<sup>2</sup>C-bus master.
3. The PCA9575 device(s) acknowledge(s) after seeing the General Call address '0000 0000' (00h) only. If the R/W bit is set to logic 1 (read), no acknowledge is returned to the I<sup>2</sup>C-bus master.
4. Once the General Call address has been sent and acknowledged, the master sends 1 byte. The value of the byte must be equal to 06h (1000 0011). The PCA9575 acknowledges this value only. If the byte is not equal to 06h, the PCA9575 does not acknowledge it. If more than 1 byte of data is sent, the PCA9575 does not acknowledge anymore.
5. Once the right byte has been sent and correctly acknowledged, the master sends a STOP command to end the Software Reset sequence: the PCA9575 then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time. If the master sends a Repeated START instead, no reset is performed. The I<sup>2</sup>C-bus master must interpret a non-acknowledge from the PCA9575 (at any time) as a 'Software Reset Abort'. The PCA9575 does not initiate a software reset.

## 7.10 Interrupt output ( $\overline{\text{INT}}$ )

The open-drain active LOW interrupt is activated when one of the port pins changes state and the port pin is configured as an input and the interrupt on it is not masked. The interrupt is deactivated when the port pin input returns to its previous state or the Input Port register is read. It is highly recommended to program the MSK register, and the CFG registers during the initialization sequence after power-up, since any change to them during Normal mode operation may cause undesirable interrupt events to happen.

**Remark:** Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register. Only a Read of the Input Port register that contains the bit(s) image of the input(s) that generated the interrupt clears the interrupt condition.

## 7.11 Standby

The PCA9575 goes into standby when the I<sup>2</sup>C-bus is idle. Standby supply current is lower than 2.0  $\mu\text{A}$  (typical).

## 8. Characteristics of the I<sup>2</sup>C-bus

The I<sup>2</sup>C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

### 8.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see [Figure 9](#)).

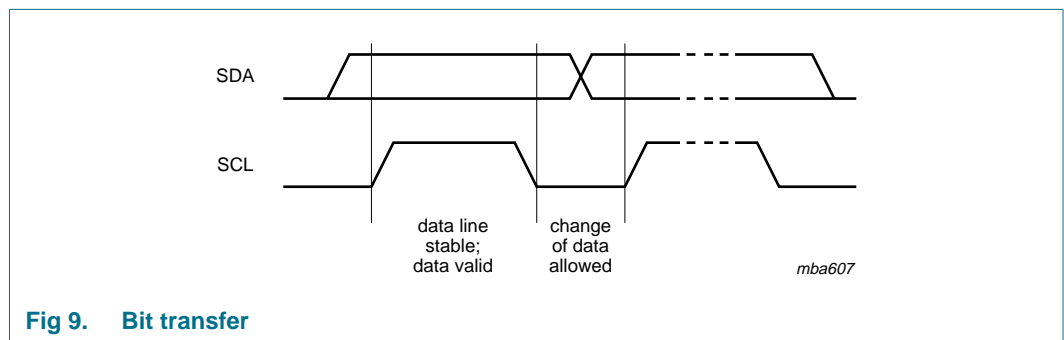


Fig 9. Bit transfer

#### 8.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see [Figure 10](#)).

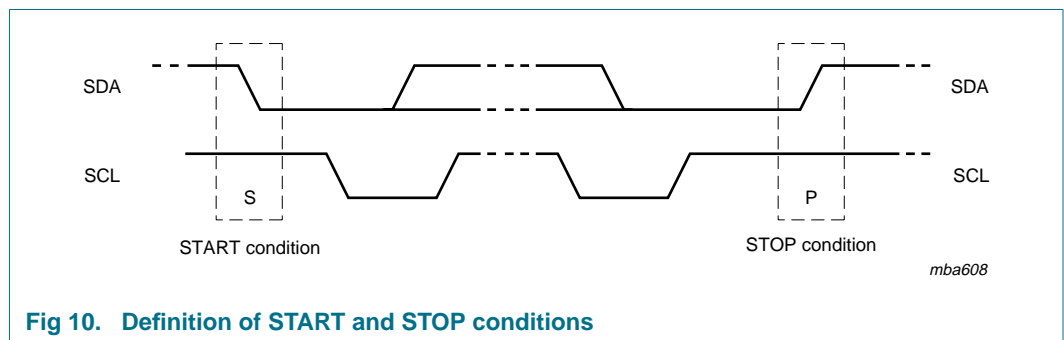
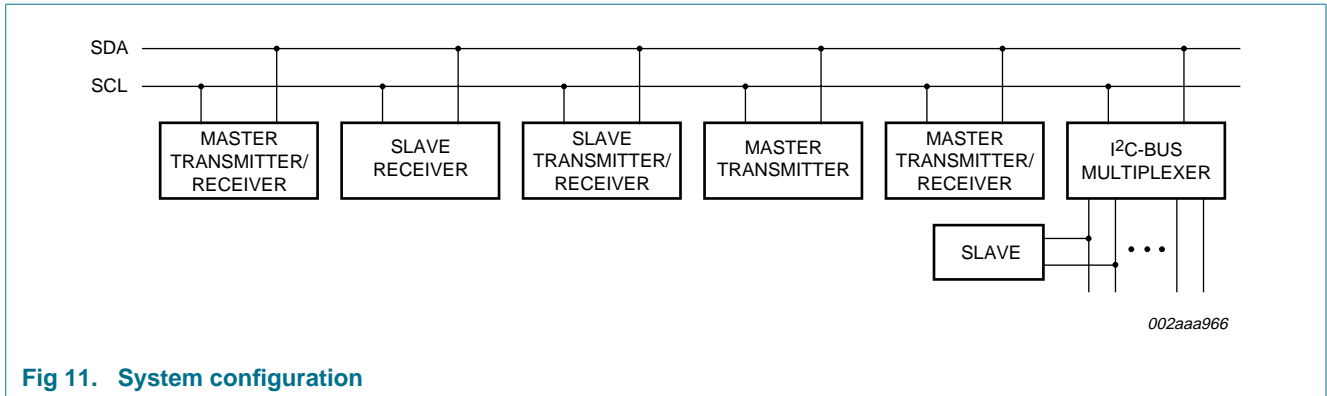


Fig 10. Definition of START and STOP conditions

### 8.2 System configuration

A device generating a message is a 'transmitter'; a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see [Figure 11](#)).

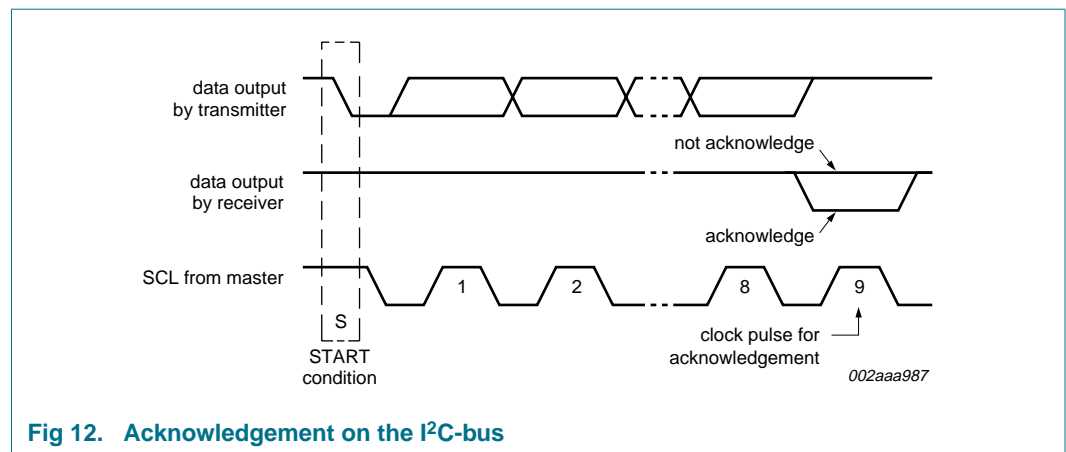


### 8.3 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up time and hold time must be taken into account.

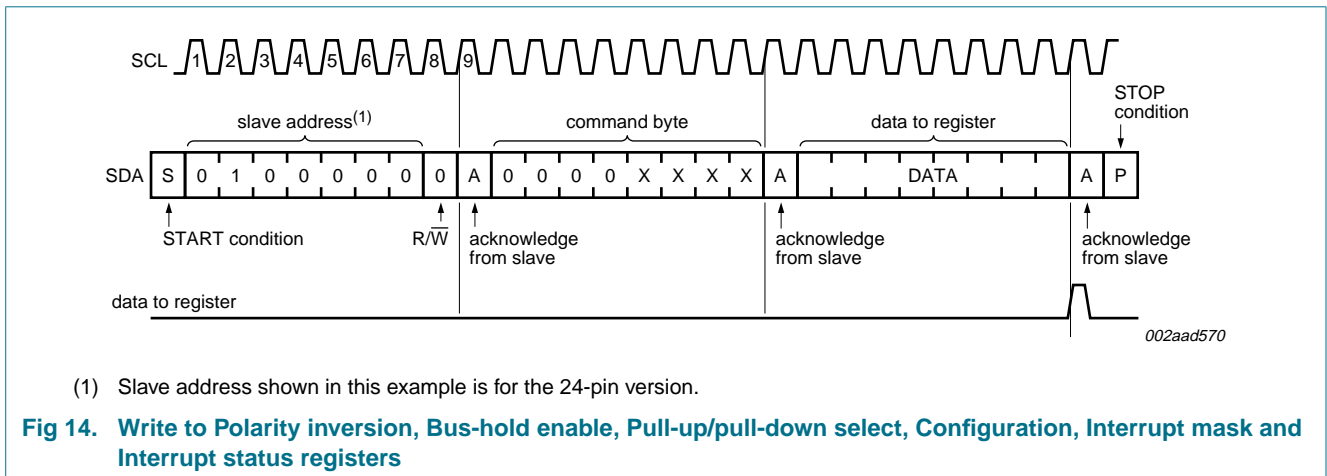
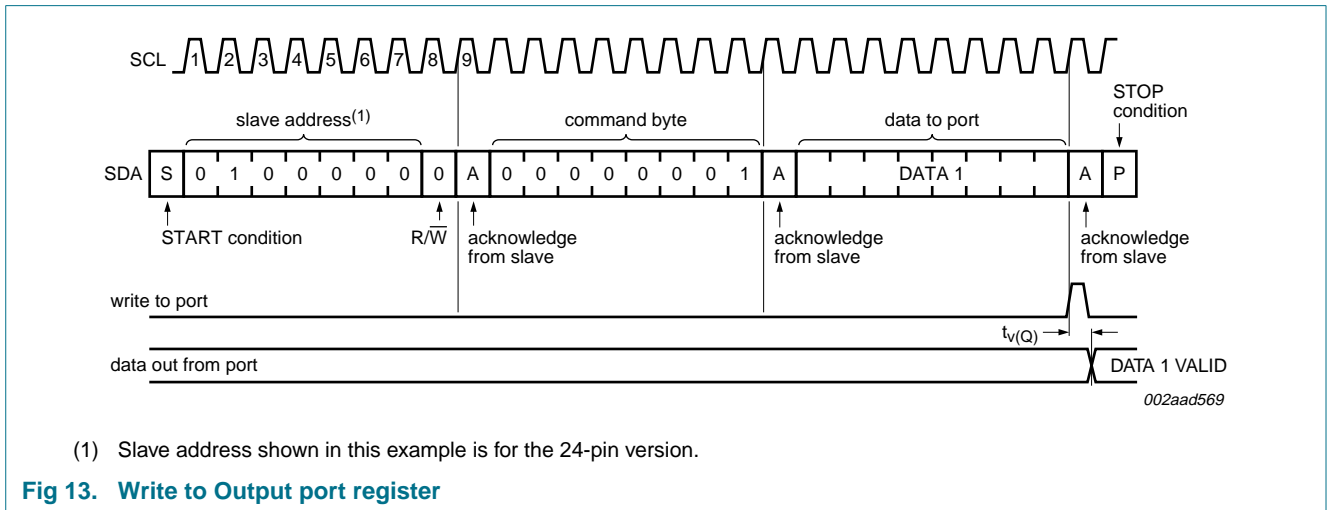
A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

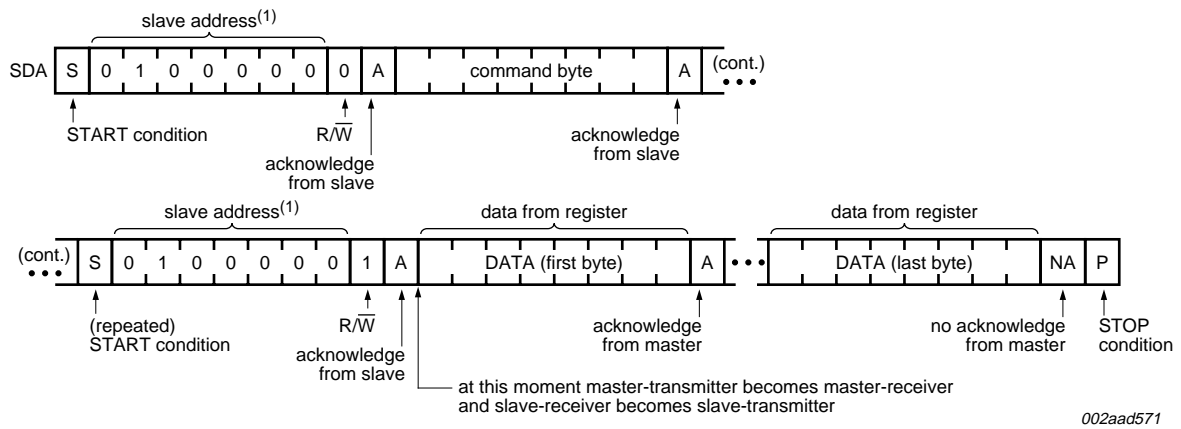


## 9. Bus transactions

Data is transmitted to the PCA9575 registers using 'Write Byte' transfers (see [Figure 13](#) and [Figure 14](#)).

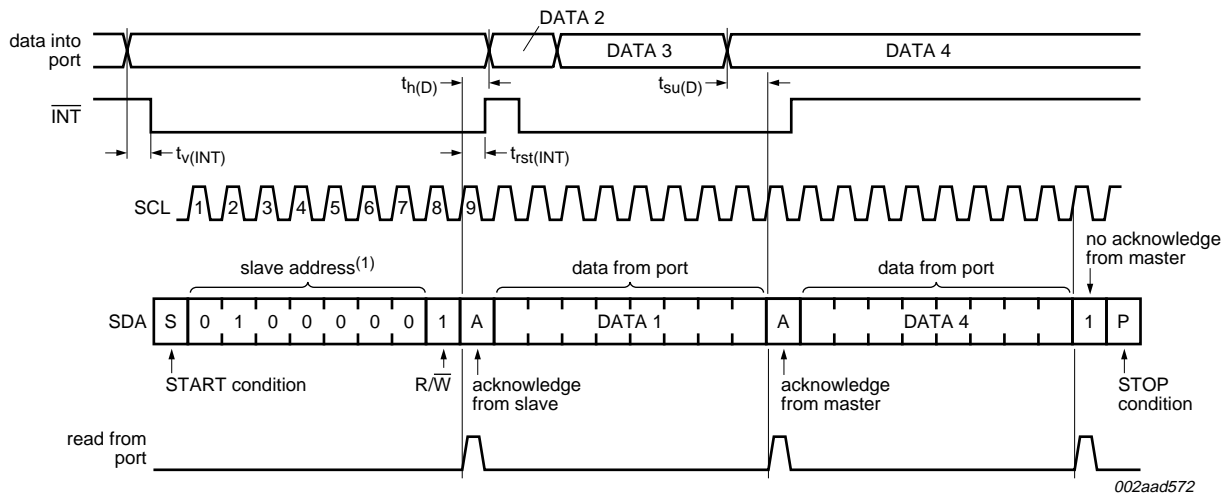
Data is read from the PCA9575 registers using 'Read Byte' transfers (see [Figure 15](#) and [Figure 16](#)).





(1) Slave address shown in this example is for the 24-pin version.

**Fig 15. Read from register**



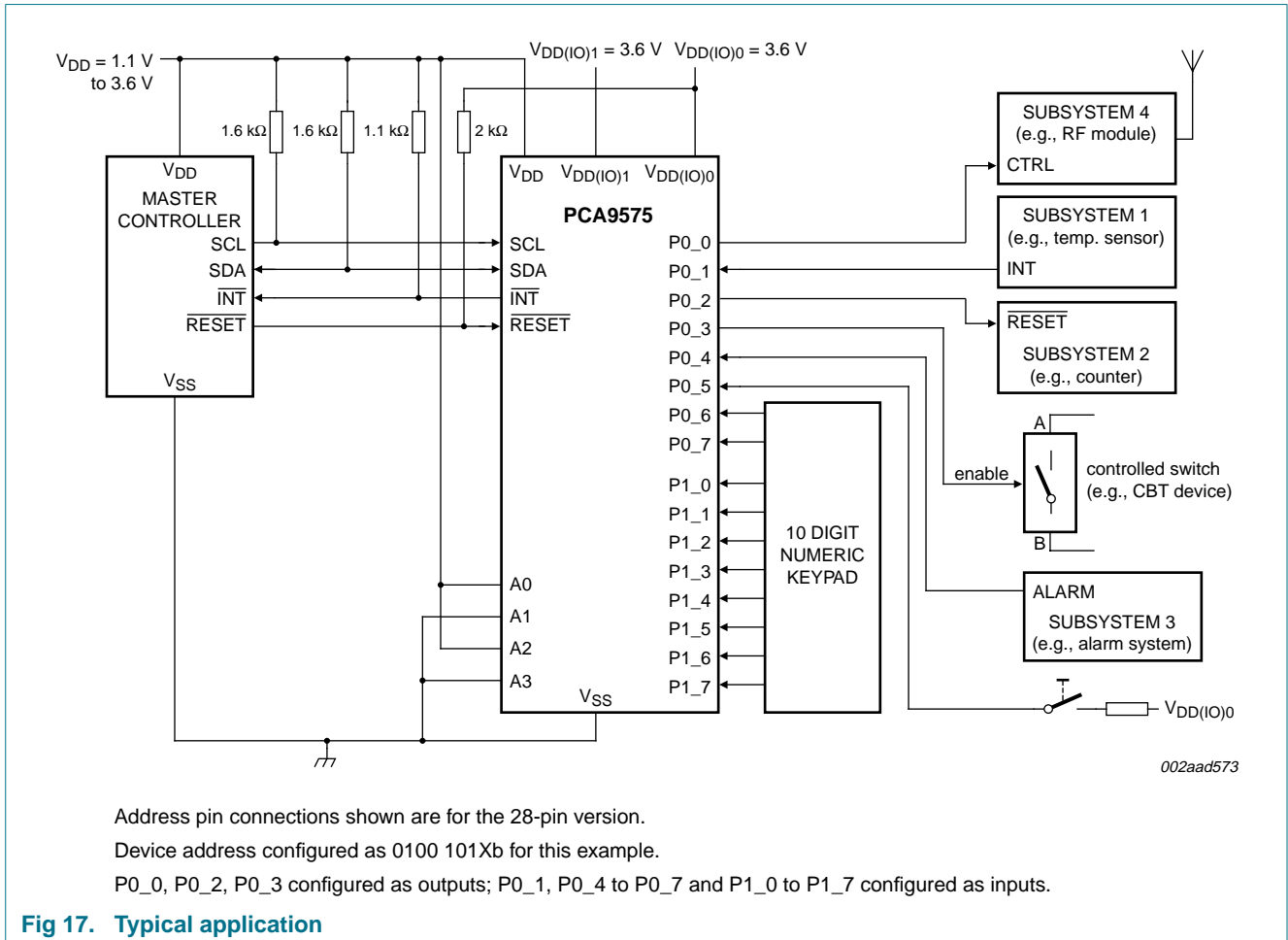
This figure assumes the command byte has previously been programmed with 00h.

Transfer of data can be stopped at any moment by a STOP condition.

(1) Slave address shown in this example is for the 24-pin version.

**Fig 16. Read Input port register**

### 10. Application design-in information



### 11. Limiting values

**Table 20. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DD</sub>	supply voltage		-0.5	+4.0	V
V <sub>DD(IO)0</sub>	input/output supply voltage 0		V <sub>SS</sub> - 0.5	+4.0	V
V <sub>DD(IO)1</sub>	input/output supply voltage 1		V <sub>SS</sub> - 0.5	+4.0	V
I <sub>I/O</sub>	input/output current		-	±5	mA
I <sub>I</sub>	input current		-	±20	mA
I <sub>DD</sub>	supply current		-	90	mA
I <sub>SS</sub>	ground supply current		-	90	mA
P <sub>tot</sub>	total power dissipation		-	75	mW
T <sub>stg</sub>	storage temperature		-65	+150	°C
T <sub>amb</sub>	ambient temperature		-40	+85	°C



## 12. Static characteristics

**Table 21. Static characteristics**

$V_{DD} = 1.1\text{ V to }3.6\text{ V}$ ;  $V_{DD(I/O)0} = 1.1\text{ V to }3.6\text{ V}$ ;  $V_{DD(I/O)1} = 1.1\text{ V to }3.6\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Supplies</b>						
$V_{DD}$	supply voltage		1.1	-	3.6	V
$V_{DD(I/O)0}$	input/output supply voltage 0		1.1	-	3.6	V
$V_{DD(I/O)1}$	input/output supply voltage 1		1.1	-	3.6	V
$I_{DD}$	supply current	operating mode; $V_{DD} = 3.6\text{ V}$ ; no load; $f_{SCL} = 100\text{ kHz}$ ; I/O = inputs	-	135	200	$\mu\text{A}$
$I_{stbL}$	LOW-level standby current	Standby mode; $V_{DD} = 3.6\text{ V}$ ; no load; $V_I = V_{SS}$ ; $f_{SCL} = 0\text{ kHz}$ ; I/O = inputs	-	0.25	2	$\mu\text{A}$
$I_{stbH}$	HIGH-level standby current	Standby mode; $V_{DD} = 3.6\text{ V}$ ; no load; $V_I = V_{DD(I/O)0} = V_{DD(I/O)1}$ ; $f_{SCL} = 0\text{ kHz}$ ; I/O = inputs	-	0.25	2	$\mu\text{A}$
$V_{POR}$	power-on reset voltage	no load; $V_I = V_{DD}$ or $V_{SS}$ (rising $V_{DD}$ )	-	0.7	1.0	V
<b>Input SCL; input/output SDA</b>						
$V_{IL}$	LOW-level input voltage		-0.5	-	+0.3 $V_{DD}$	V
$V_{IH}$	HIGH-level input voltage		0.7 $V_{DD}$	-	3.6	V
$I_{OL}$	LOW-level output current	$V_{OL} = 0.2\text{ V}$ ; $V_{DD} = 1.1\text{ V}$	1	-	-	mA
		$V_{OL} = 0.4\text{ V}$ ; $V_{DD} = 2.3\text{ V}$	3	-	-	mA
$I_L$	leakage current	$V_I = V_{DD}$ or $V_{SS}$	-1	-	+1	$\mu\text{A}$
$C_i$	input capacitance	$V_I = V_{SS}$	-	6	10	pF
<b>I/Os</b>						
$V_{IL}$	LOW-level input voltage		-0.5	-	+0.3 $V_{DD}$	V
$V_{IH}$	HIGH-level input voltage		0.3 $V_{DD}$	-	3.6	V
$I_{OL}$	LOW-level output current	$V_{OL} = 0.2\text{ V}$ ; $V_{DD(I/O)0} = 1.1\text{ V}$ ; $V_{DD(I/O)1} = 1.1\text{ V}$	1	-	-	mA
		$V_{OL} = 0.5\text{ V}$ ; $V_{DD(I/O)0} = 3.6\text{ V}$ ; $V_{DD(I/O)1} = 3.6\text{ V}$	2	3	-	mA
$V_{OH}$	HIGH-level output voltage	$I_{OH} = -1\text{ mA}$ ; $V_{DD(I/O)0} = 1.1\text{ V}$ ; $V_{DD(I/O)1} = 1.1\text{ V}$	0.8	-	-	V
$R_{pu(int)}$	internal pull-up resistance		50	100	150	k $\Omega$
$I_{LIH}$	HIGH-level input leakage current	$V_{DD(I/O)0} = 3.6\text{ V}$ ; $V_{DD(I/O)1} = 3.6\text{ V}$ ; $V_I = V_{DD(I/O)0}$ ; $V_I = V_{DD(I/O)1}$	-	-	1	$\mu\text{A}$
$I_H$	holding current	$V_I = 0.3\text{ V}$ ; $V_{DD(I/O)0} = 1.1\text{ V}$ ; $V_{DD(I/O)1} = 1.1\text{ V}$ ; $V_{DD} = 3.6\text{ V}$	10	-	-	$\mu\text{A}$
		$V_I = 0.8\text{ V}$ ; $V_{DD(I/O)0} = 1.1\text{ V}$ ; $V_{DD(I/O)1} = 1.1\text{ V}$ ; $V_{DD} = 3.6\text{ V}$	-10	-	-	$\mu\text{A}$
$I_{LIL}$	LOW-level input leakage current	$V_{DD(I/O)0} = 3.6\text{ V}$ ; $V_{DD(I/O)1} = 3.6\text{ V}$ ; $V_I = V_{SS}$	-	-	-1	$\mu\text{A}$
$C_i$	input capacitance		-	3.7	5	pF
$C_o$	output capacitance		-	3.7	5	pF

**Table 21. Static characteristics ...continued**

$V_{DD} = 1.1\text{ V to }3.6\text{ V}$ ;  $V_{DD(I/O)0} = 1.1\text{ V to }3.6\text{ V}$ ;  $V_{DD(I/O)1} = 1.1\text{ V to }3.6\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -40\text{ °C to }+85\text{ °C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Interrupt <math>\overline{\text{INT}}</math></b>						
$I_{OL}$	LOW-level output current	$V_{OL} = 0.4\text{ V}$ ; $V_{DD} = 1.1\text{ V}$	3	-	-	mA
<b>Select inputs (reset and address)</b>						
$V_{IL}$	LOW-level input voltage		-	-	+0.2	V
$V_{IH}$	HIGH-level input voltage		$V_{DD} - 0.2$	-	-	V
$I_{LI}$	input leakage current		-1	-	+1	$\mu\text{A}$
$C_i$	input capacitance		-	2	4	pF

### 13. Dynamic characteristics

**Table 22. Dynamic characteristics**

$V_{DD} = 1.1\text{ V to }3.6\text{ V}$ ;  $V_{DD(I/O)0} = 1.1\text{ V to }3.6\text{ V}$ ;  $V_{DD(I/O)1} = 1.1\text{ V to }3.6\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -40\text{ °C to }+85\text{ °C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Standard-mode I <sup>2</sup> C-bus		Fast-mode I <sup>2</sup> C-bus		Unit
			Min	Max	Min	Max	
$f_{SCL}$	SCL clock frequency		0	100	0	400	kHz
$t_{BUF}$	bus free time between a STOP and START condition		4.7	-	1.3	-	$\mu\text{s}$
$t_{HD;STA}$	hold time (repeated) START condition		4.0	-	0.6	-	$\mu\text{s}$
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	$\mu\text{s}$
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	$\mu\text{s}$
$t_{VD;ACK}$	data valid acknowledge time	[1]	0.3	3.45	0.1	0.9	$\mu\text{s}$
$t_{HD;DAT}$	data hold time		0	-	0	-	ns
$t_{VD;DAT}$	data valid time	[2]	300	-	50	-	ns
$t_{SU;DAT}$	data set-up time		250	-	100	-	ns
$t_{LOW}$	LOW period of the SCL clock		4.7	-	1.3	-	$\mu\text{s}$
$t_{HIGH}$	HIGH period of the SCL clock		4.0	-	0.6	-	$\mu\text{s}$
$t_f$	fall time of both SDA and SCL signals		-	300	$20 + 0.1C_b$ [3]	300	ns
$t_r$	rise time of both SDA and SCL signals		-	1000	$20 + 0.1C_b$ [3]	300	ns
$t_{SP}$	pulse width of spikes that must be suppressed by the input filter		-	50	-	50	ns

**Table 22. Dynamic characteristics ...continued**

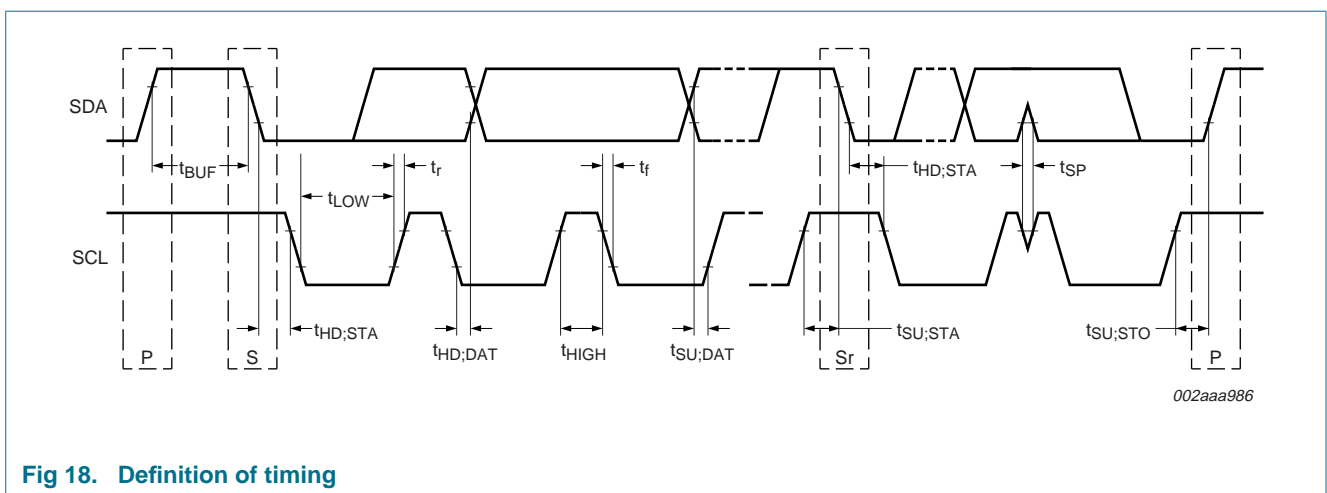
$V_{DD} = 1.1\text{ V to }3.6\text{ V}$ ;  $V_{DD(I/O)0} = 1.1\text{ V to }3.6\text{ V}$ ;  $V_{DD(I/O)1} = 1.1\text{ V to }3.6\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Standard-mode I <sup>2</sup> C-bus		Fast-mode I <sup>2</sup> C-bus		Unit
			Min	Max	Min	Max	
<b>Port timing</b>							
$t_{v(Q)}$	data output valid time	$V_{DD(I/O)0}, V_{DD(I/O)1} = V_{DD} = 1.1\text{ V}$	-	350	-	350	ns
		$V_{DD(I/O)0}, V_{DD(I/O)1} = V_{DD} = 2.3\text{ V to }3.6\text{ V}$	-	300	-	300	ns
$t_{su(D)}$	data input set-up time		150	-	150	-	ns
$t_{h(D)}$	data input hold time		1	-	1	-	$\mu\text{s}$
<b>Interrupt timing</b>							
$t_{v(INT)}$	valid time on pin $\overline{INT}$		-	4	-	4	$\mu\text{s}$
$t_{rst(INT)}$	reset time on pin $\overline{INT}$		-	4	-	4	$\mu\text{s}$
<b>Reset</b>							
$t_{w(rst)}$	reset pulse width	$V_{DD(I/O)0}, V_{DD(I/O)1} = V_{DD} = 1.1\text{ V}$	8	-	8	-	ns
		$V_{DD(I/O)0}, V_{DD(I/O)1} = V_{DD} = 2.3\text{ V to }3.6\text{ V}$	4	-	4	-	ns
$t_{rec(rst)}$	reset recovery time		0	-	0	-	ns
$t_{rst(SDA)}$	SDA reset time	<a href="#">Figure 19</a>	-	400	-	400	ns
$t_{rst(GPIO)}$	GPIO reset time	<a href="#">Figure 19</a>	-	400	-	400	ns

[1]  $t_{VD,ACK}$  = time for acknowledgement signal from SCL LOW to SDA (out) LOW.

[2]  $t_{VD,DAT}$  = minimum time for SDA data out to be valid following SCL LOW.

[3]  $C_b$  = total capacitance of one bus line in pF.



**Fig 18. Definition of timing**

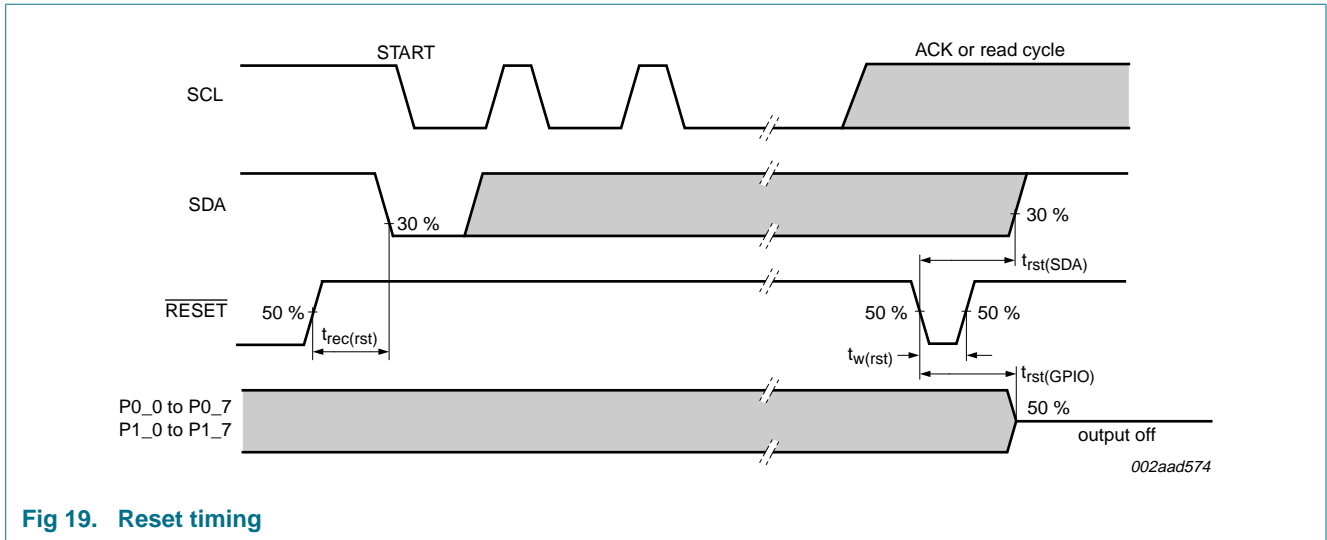
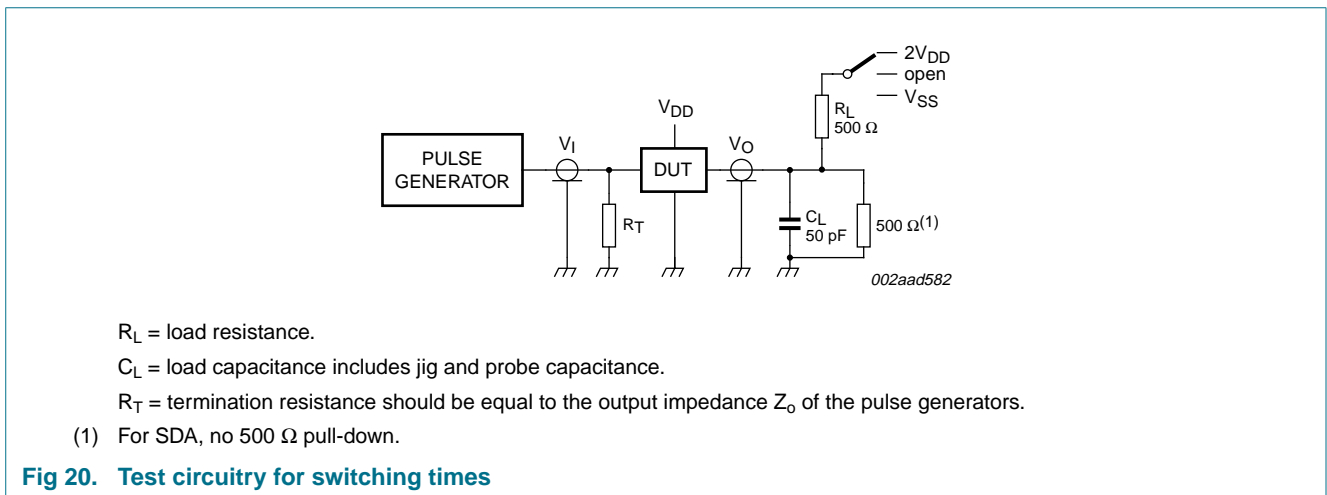


Fig 19. Reset timing

## 14. Test information



$R_L$  = load resistance.

$C_L$  = load capacitance includes jig and probe capacitance.

$R_T$  = termination resistance should be equal to the output impedance  $Z_o$  of the pulse generators.

(1) For SDA, no 500 Ω pull-down.

Fig 20. Test circuitry for switching times

15. Package outline

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

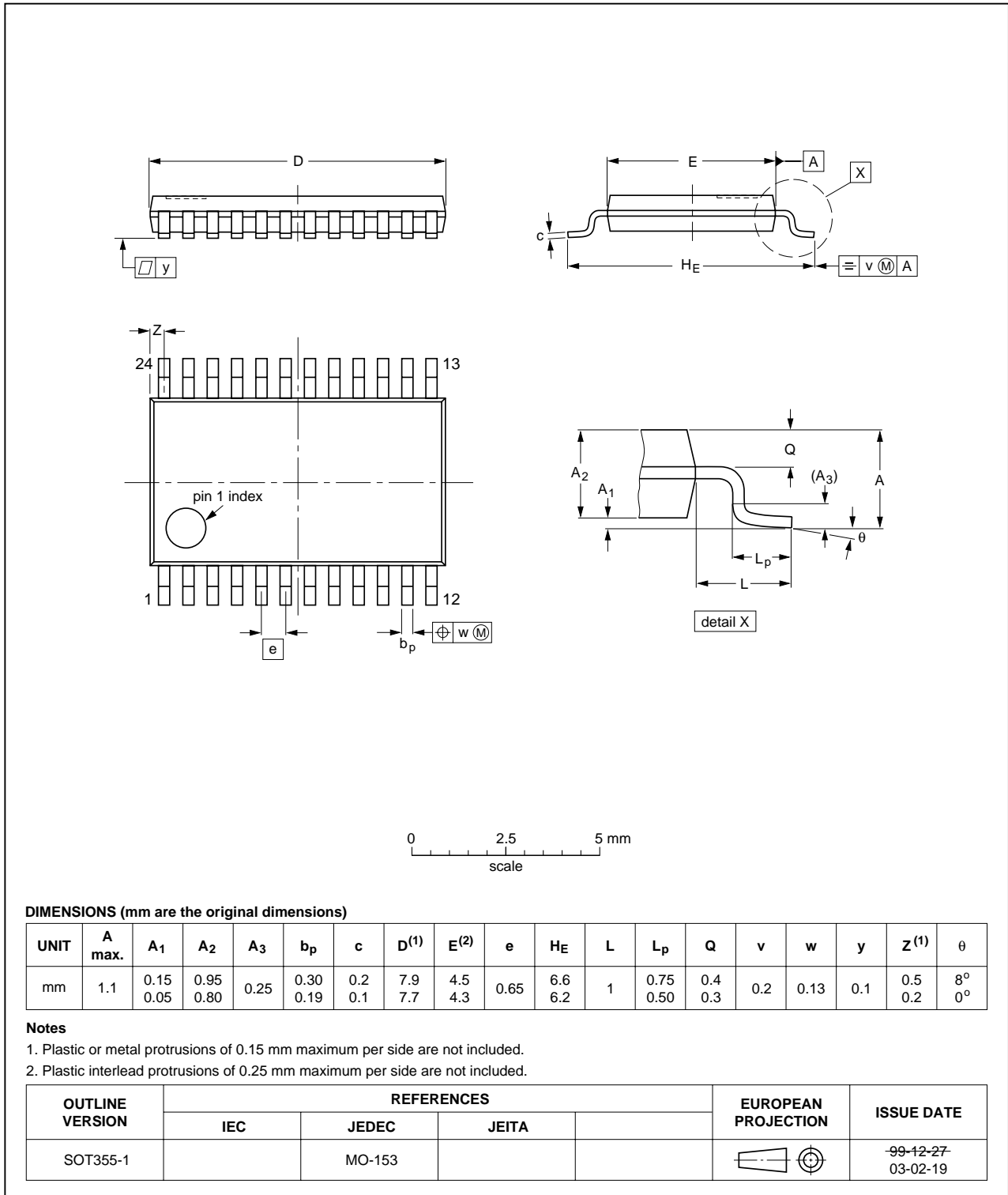


Fig 21. Package outline SOT355-1 (TSSOP24)

TSSOP28: plastic thin shrink small outline package; 28 leads; body width 4.4 mm

SOT361-1

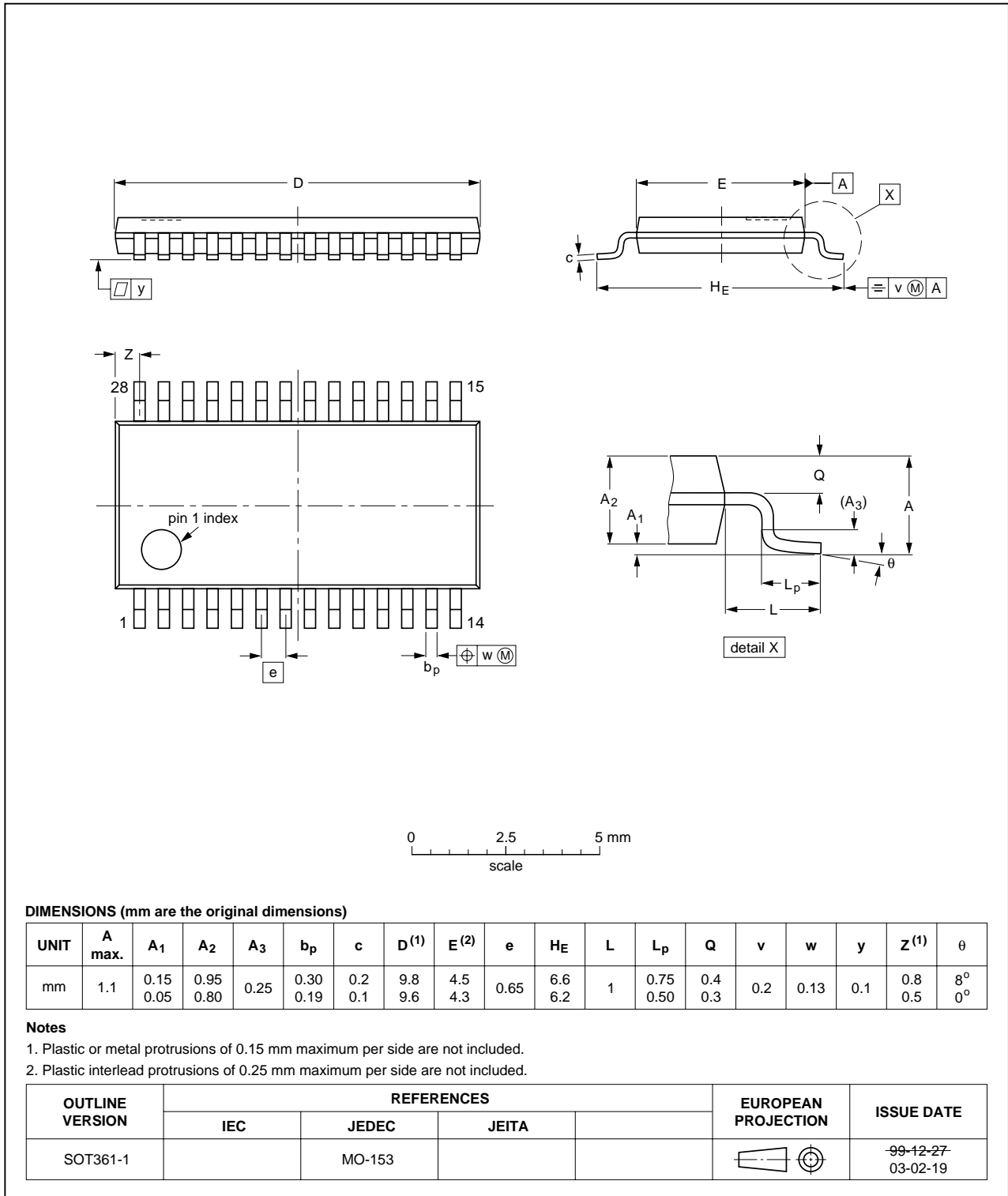


Fig 22. Package outline SOT361-1 (TSSOP28)

HWQFN24: plastic thermal enhanced very very thin quad flat package; no leads;  
24 terminals; body 4 x 4 x 0.75 mm

SOT994-1

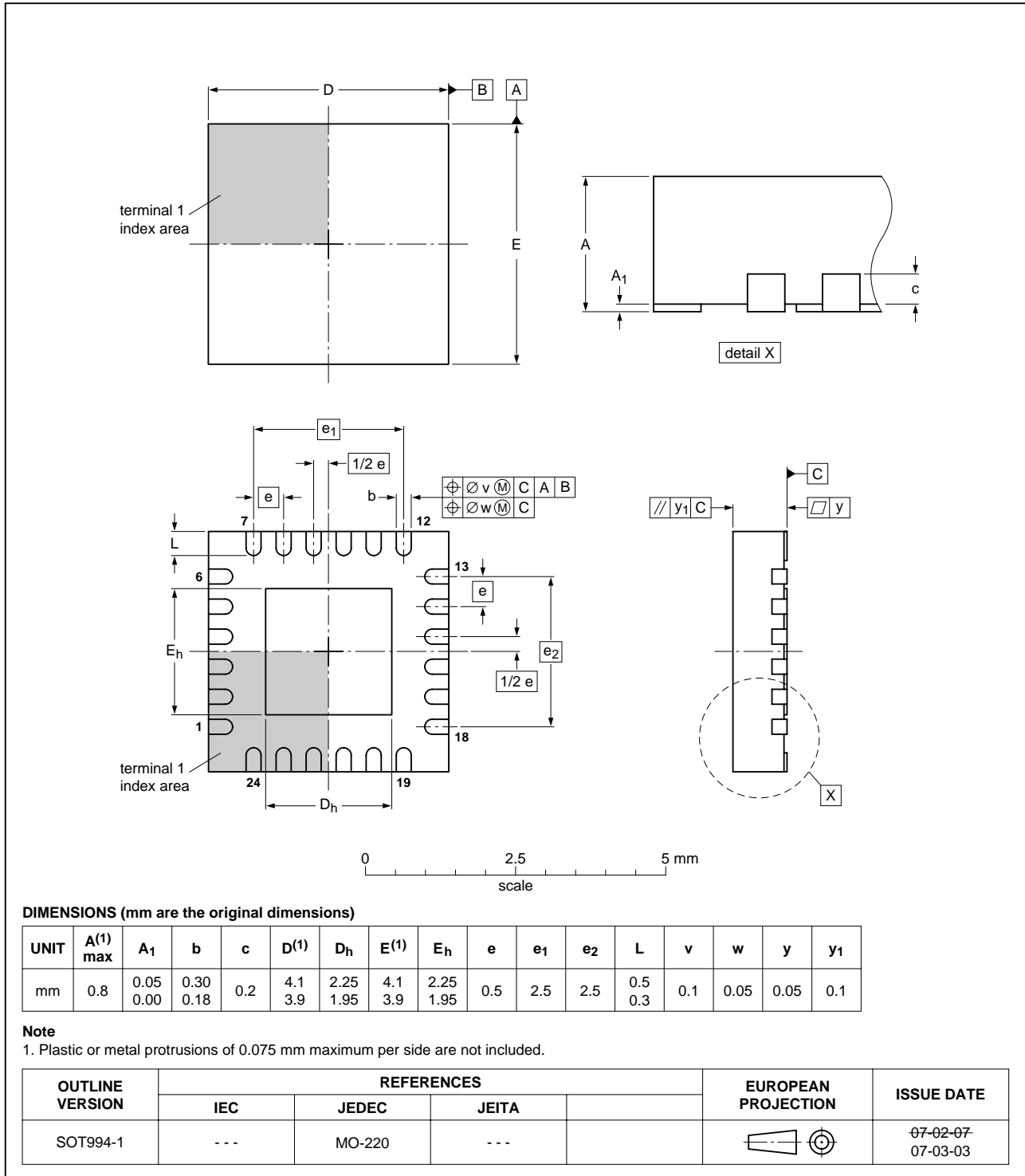


Fig 23. Package outline SOT994-1 (HWQFN24)

## 16. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe you must take normal precautions appropriate to handling integrated circuits.

## 17. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 17.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 17.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 17.3 Wave soldering

Key characteristics in wave soldering are:



- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

### 17.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 24](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 23](#) and [24](#)

**Table 23. SnPb eutectic process (from J-STD-020C)**

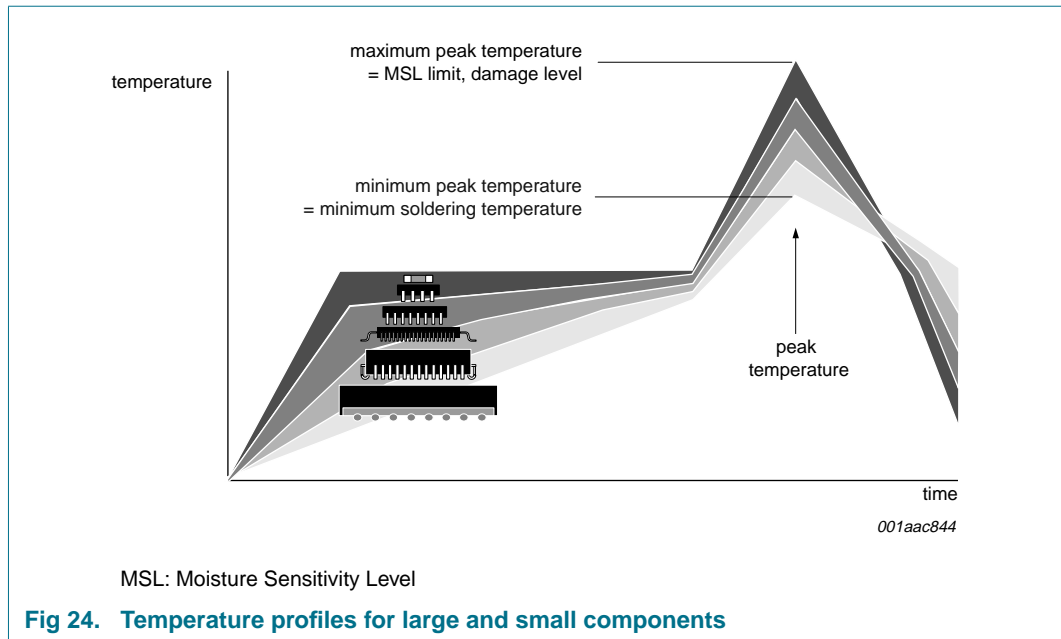
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

**Table 24. Lead-free process (from J-STD-020C)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 24](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

## 18. Abbreviations

**Table 25. Abbreviations**

Acronym	Description
CBT	Cross Bar Technology
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
GPIO	General Purpose Input/Output
HBM	Human Body Model
I/O	Input/Output
I <sup>2</sup> C-bus	Inter-Integrated Circuit bus
IC	Integrated Circuit
LED	Light Emitting Diode
LP	Low Pass
MM	Machine Model
PLC	Programmable Logic Controller
POR	Power-On Reset
RAID	Redundant Array of Independent Discs
RF	Radio Frequency
SMBus	System Management Bus

## 19. Revision history

Table 26. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9575_1	20081002	Product data sheet	-	-

## 20. Legal information

### 20.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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## 22. Contents

<b>1</b>	<b>General description</b> . . . . .	<b>1</b>	<b>10</b>	<b>Application design-in information</b> . . . . .	<b>24</b>
<b>2</b>	<b>Features</b> . . . . .	<b>2</b>	<b>11</b>	<b>Limiting values</b> . . . . .	<b>24</b>
<b>3</b>	<b>Applications</b> . . . . .	<b>3</b>	<b>12</b>	<b>Static characteristics</b> . . . . .	<b>25</b>
<b>4</b>	<b>Ordering information</b> . . . . .	<b>3</b>	<b>13</b>	<b>Dynamic characteristics</b> . . . . .	<b>26</b>
<b>5</b>	<b>Block diagram</b> . . . . .	<b>4</b>	<b>14</b>	<b>Test information</b> . . . . .	<b>28</b>
<b>6</b>	<b>Pinning information</b> . . . . .	<b>6</b>	<b>15</b>	<b>Package outline</b> . . . . .	<b>29</b>
6.1	Pinning . . . . .	6	<b>16</b>	<b>Handling information</b> . . . . .	<b>32</b>
6.2	Pin description . . . . .	7	<b>17</b>	<b>Soldering of SMD packages</b> . . . . .	<b>32</b>
<b>7</b>	<b>Functional description</b> . . . . .	<b>8</b>	17.1	Introduction to soldering . . . . .	32
7.1	I/O ports . . . . .	8	17.2	Wave and reflow soldering . . . . .	32
7.2	Device address . . . . .	8	17.3	Wave soldering . . . . .	32
7.3	Command register . . . . .	9	17.4	Reflow soldering . . . . .	33
7.4	Register definitions . . . . .	9	<b>18</b>	<b>Abbreviations</b> . . . . .	<b>34</b>
7.5	Writing to port registers . . . . .	9	<b>19</b>	<b>Revision history</b> . . . . .	<b>35</b>
7.6	Reading the port registers . . . . .	10	<b>20</b>	<b>Legal information</b> . . . . .	<b>36</b>
7.6.1	Register 0 - Input port 0 register . . . . .	10	20.1	Data sheet status . . . . .	36
7.6.2	Register 1 - Input port 1 register . . . . .	10	20.2	Definitions . . . . .	36
7.6.3	Register 2 - Polarity inversion port 0 register . . . . .	11	20.3	Disclaimers . . . . .	36
7.6.4	Register 3 - Polarity inversion port 1 register . . . . .	11	20.4	Trademarks . . . . .	36
7.6.5	Register 4 - Bus-hold/pull-up/pull-down enable 0 register . . . . .	12	<b>21</b>	<b>Contact information</b> . . . . .	<b>36</b>
7.6.6	Register 5 - Bus-hold/pull-up/pull-down enable 1 register . . . . .	13	<b>22</b>	<b>Contents</b> . . . . .	<b>37</b>
7.6.7	Register 6 - Pull-up/pull-down select port 0 register . . . . .	14			
7.6.8	Register 7 - Pull-up/pull-down select port 1 register . . . . .	14			
7.6.9	Register 8 - Configuration port 0 register . . . . .	15			
7.6.10	Register 9 - Configuration port 1 register . . . . .	15			
7.6.11	Register 10 - Output port 0 register . . . . .	16			
7.6.12	Register 11 - Output port 1 register . . . . .	16			
7.6.13	Register 12 - Interrupt mask port 0 register . . . . .	17			
7.6.14	Register 13 - Interrupt mask port 1 register . . . . .	17			
7.6.15	Register 14 - Interrupt status port 0 register . . . . .	18			
7.6.16	Register 15 - Interrupt status port 1 register . . . . .	18			
7.7	Power-on reset . . . . .	18			
7.8	RESET input . . . . .	18			
7.9	Software reset . . . . .	19			
7.10	Interrupt output (INT) . . . . .	19			
7.11	Standby . . . . .	19			
<b>8</b>	<b>Characteristics of the I<sup>2</sup>C-bus</b> . . . . .	<b>20</b>			
8.1	Bit transfer . . . . .	20			
8.1.1	START and STOP conditions . . . . .	20			
8.2	System configuration . . . . .	20			
8.3	Acknowledge . . . . .	21			
<b>9</b>	<b>Bus transactions</b> . . . . .	<b>22</b>			

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