DATA SHEET

PCA9500

8-bit I^2C and SMBus I/O port with 2-kbit EEPROM

Product data sheet
Supersedes data of 27 Jun 2003

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Philips Semiconductors

PHILIPS

8-bit I²C and SMBus I/O port with 2-kbit EEPROM PCA9500

FEATURES

- 8 general purpose input/output expander/collector
- Drop in replacement for PCF8574 with integrated 2-kbit EEPROM
- Internal 256 × 8 EEPROM
- Self timed write cycle
- 4 byte page write operation
- I²C and SMBus interface logic
- Internal power-on reset
- Noise filter on SCL/SDA inputs
- 3 address pins allowing up to 8 devices on the I²C/SMBus
- No glitch on power-up
- Supports hot insertion
- Power-up with all channels configured as inputs
- Low standby current
- Operating power supply voltage range of 2.5 V to 3.6 V
- 5 V tolerant inputs/outputs
- 0 kHz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JESDEC Standard JESD78 which exceeds 100 mA
- Package offerred: SO16, TSSOP16, HVQFN16

DESCRIPTION

The PCA9500 is an 8-bit I/O expander with an on-board 2-kbit EEPROM.

The I/O expander's eight quasi bidirectional data pins can be independently assigned as inputs or outputs to monitor board level status or activate indicator devices such as LEDs. The system master writes to the I/O configuation bits in the same way as for the PCF8574. The data for each Input or Output is kept in the corresponding Input or Output register. The system master can read all registers.

The EEPROM can be used to store error codes or board manufacturing data for read-back by application software for diagnostic purposes and is included in the I/O expander package.

The PCA9500 has three address pins with internal pull-up resistors allowing up to 8 devices to share the common two-wire I²C software protocol serial data bus. The fixed GPIO I²C address is the same as the PCF8574 and the fixed EEPROM I²C address is the same as the PCF8582C-2, so the PCA9500 appears as two separate devices to the bus master.

The PCA9500 supports hot insertion to facilitate usage in removable cards on backplane systems.

The PCA9501 is an alternative to the functionally similar PCA9500 for systems where a higher number of devices are required to share the same I²C-bus or an interrupt output is required.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DRAWING NUMBER
16-Pin Plastic SO (wide)	–40 °C to +85 °C	PCA9500D	PCA9500D	SOT162-1
16-Pin Plastic TSSOP	–40 °C to +85 °C	PCA9500PW	PCA9500	SOT403-1
16-Pin Plastic HVQFN	–40 °C to +85 °C	PCA9500BS	9500	SOT629-1

Standard packing quantities and other packaging data are available at www.standardproducts.philips.com/packaging.
SMBus as specified by the Smart Battery System Implementers Forum is a derivative of the Philips I²C patent.
I²C is a trademark of Philips Semiconductors Corporation.

PIN CONFIGURATION – SO, TSSOP

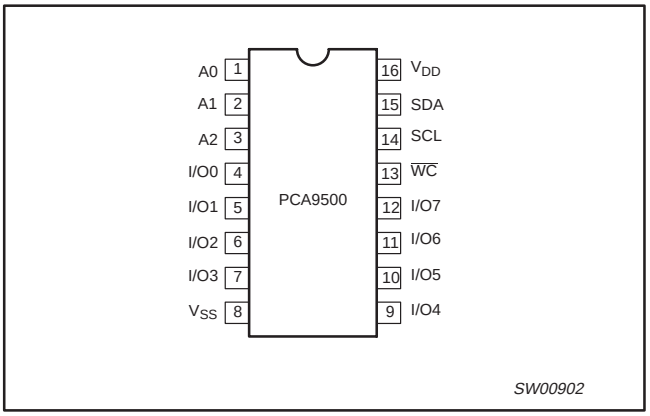


Figure 1. Pin configuration – SO, TSSOP

PIN CONFIGURATION – HVQFN

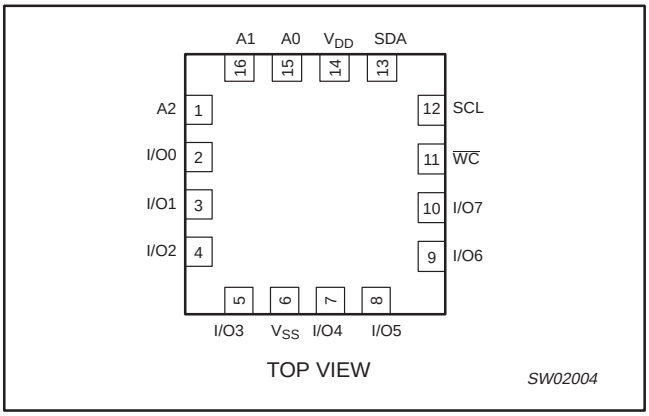


Figure 2. Pin configuration – HVQFN

PIN DESCRIPTION

SO, TSSOP PIN NUMBER	HVQFN PIN NUMBER	SYMBOL	NAME AND FUNCTION
1,2,3	15, 16, 1	A0–2	Address lines (internal pull-up)
4,5,6,7	2, 3, 4, 5	I/O0 to I/O3	Quasi-bidirectional I/O pins
8	6	V_{SS}	Supply ground
9,10,11,12	7, 8, 9, 10	I/O4 to I/O7	Quasi-bidirectional I/O pins
13	11	$\overline{WC}$	Active LOW write control pin
14	12	SCL	I^2C Serial Clock
15	13	SDA	I^2C Serial Data
16	14	V_{DD}	Supply Voltage

BLOCK DIAGRAM

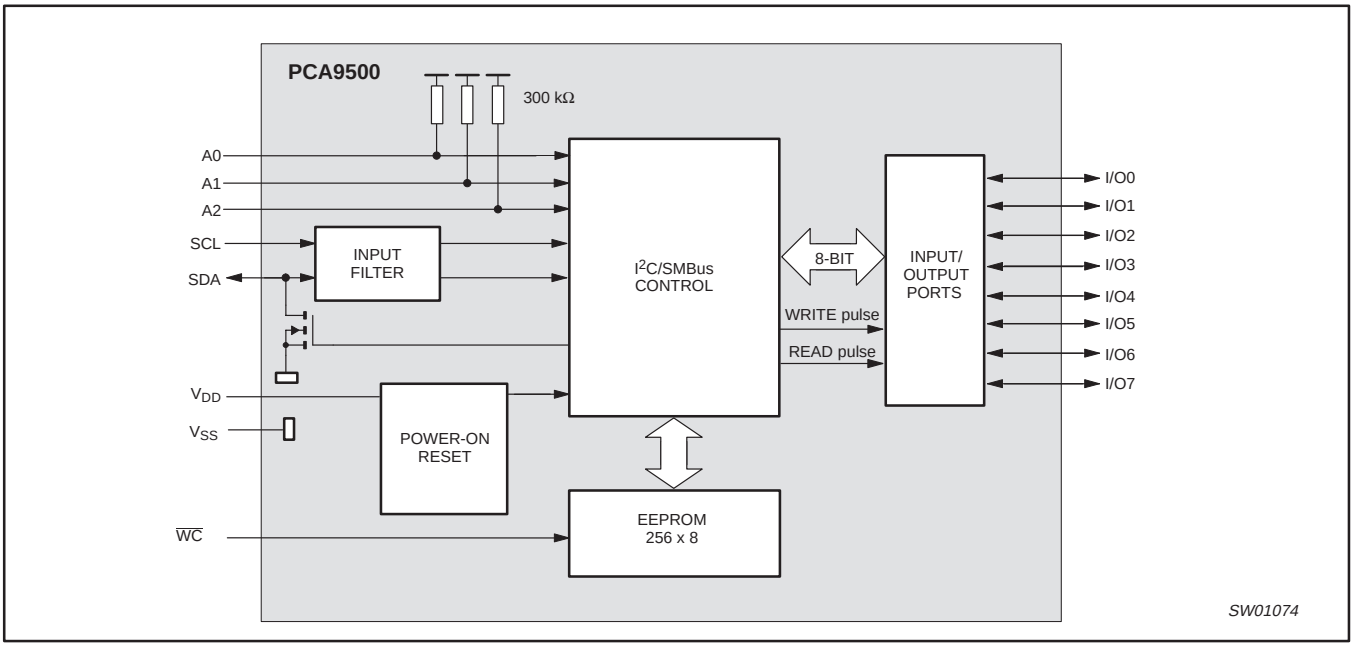


Figure 3. Block diagram

FUNCTIONAL DESCRIPTION

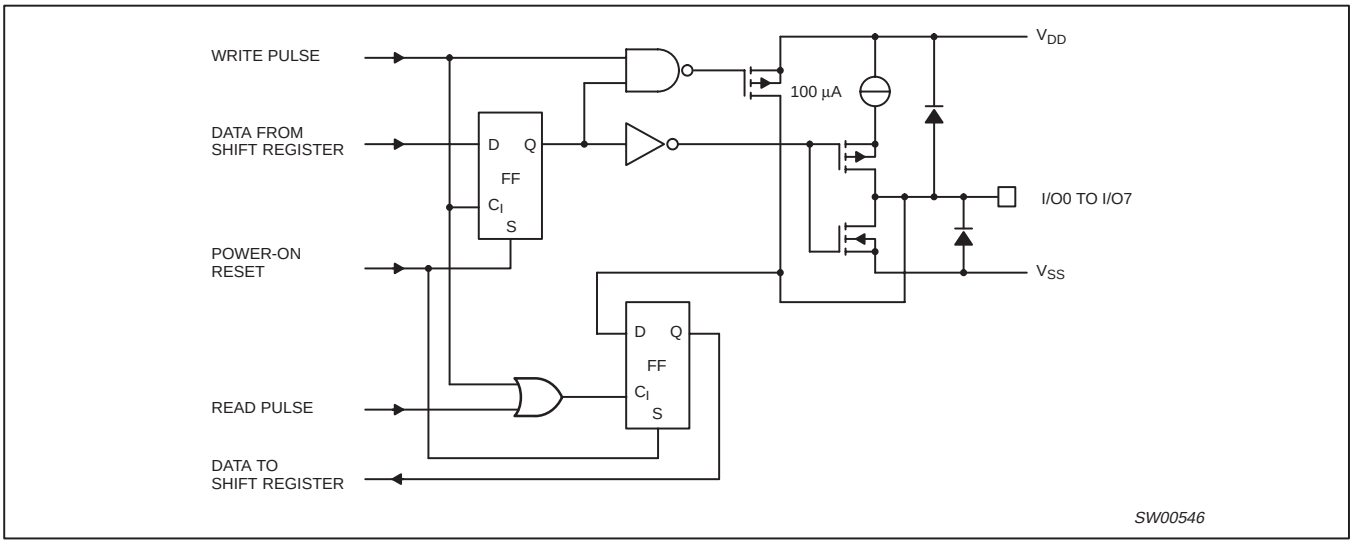


Figure 4. Simplified schematic diagram of each I/O

DEVICE ADDRESSING

Following a START condition the bus master must output the address of the slave it is accessing. The address of the PCA9500 is shown in Figure 5. Internal pullup resistors are incorporated on the hardware selectable address pins.

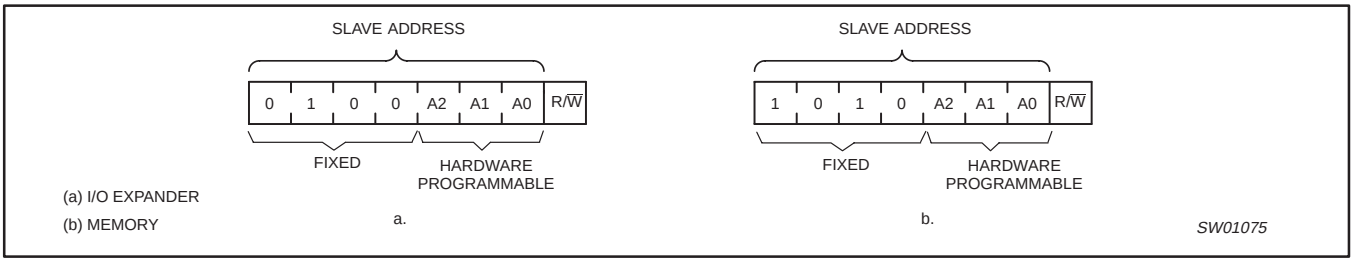


Figure 5. PCA9500 slave addresses

The last bit of the address byte defines the operation to be performed. When set to logic 1 a read is selected while a logic 0 selects a write operation.

CONTROL REGISTER

The PCA9500 contains a single 8-bit register called the Control Register, which can be written and read via the I2C-bus. This register is sent after a successful acknowledgment of the slave address.

It contains the I/O operation information.

I/O OPERATIONS (see also Figure 4)

Each of the PCA9500's eight I/Os can be independently used as an input or output. Output data is transmitted to the port by the I/O WRITE mode (see Figure 6). Input I/O data is transferred from the port to the microcontroller by the READ mode (See Figure 7).

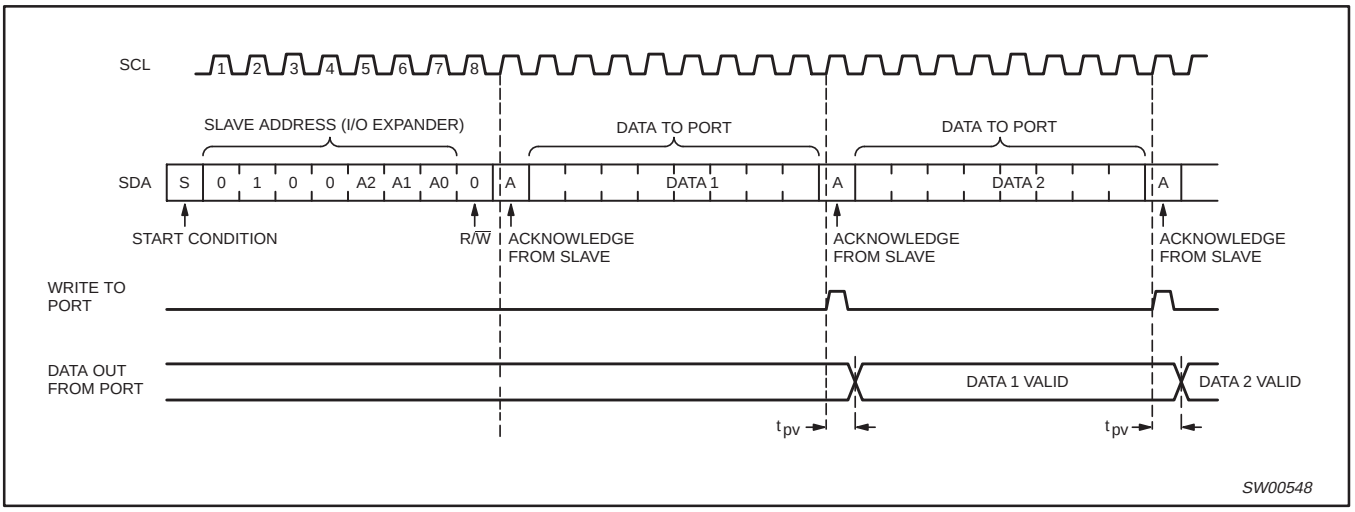


Figure 6. I/O WRITE mode (output)

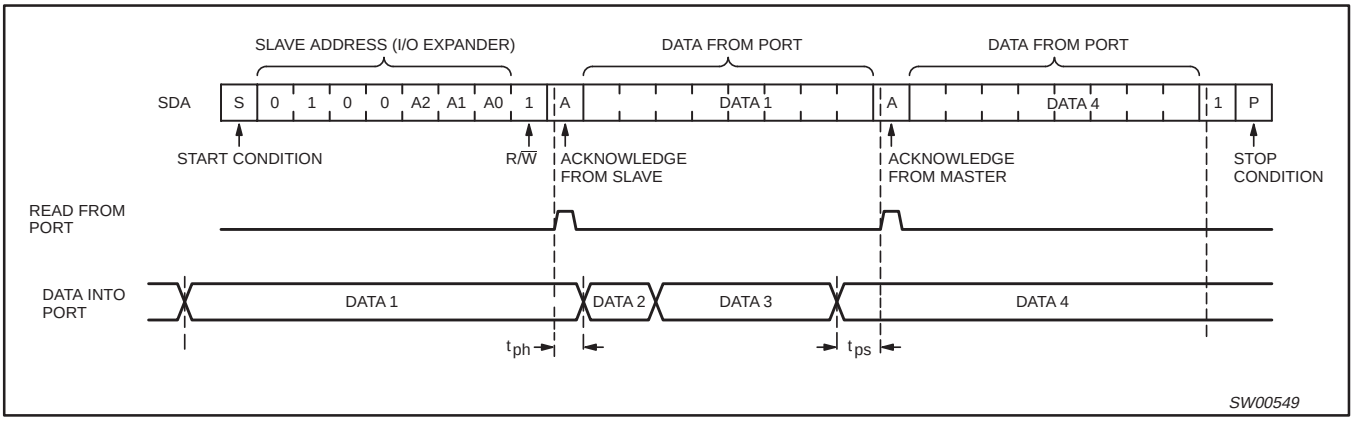


Figure 7. I/O READ mode (input)

Quasi-bidirectional I/Os (see Figure 8)

A quasi-bidirectional I/O can be used as an input or output without the use of a control signal for data direction. At power-on the I/Os are HIGH. In this mode, only a current source to V_{DD} is active. An additional strong pull-up to V_{DD} allows fast rising edges into heavily loaded outputs. These devices turn on when an output is written HIGH, and are switched off by the negative edge of SCL. The I/Os should be HIGH before being used as inputs.

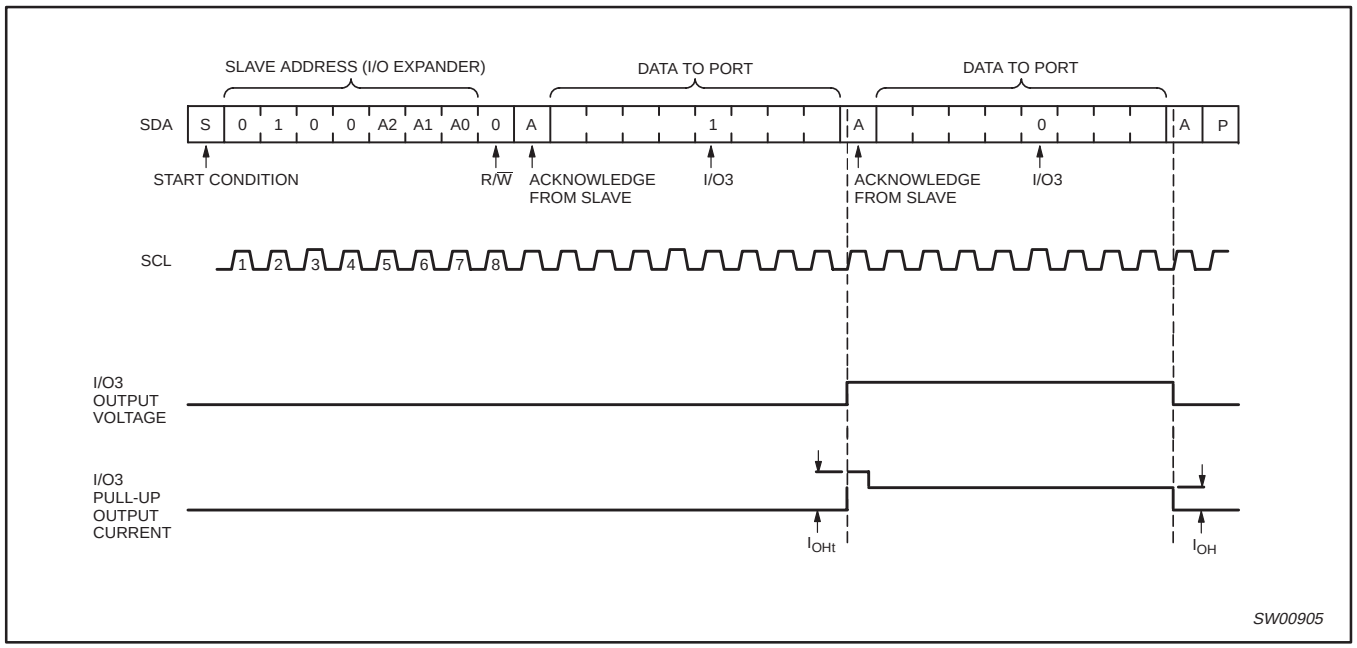


Figure 8. Transient pull-up current I_{OHt} while I/O3 changes from LOW-to-HIGH and back to LOW

MEMORY OPERATIONS

Write operations

Write operations require an additional address field to indicate the memory address location to be written. The address field is eight bits long, providing access to any one of the 256 words of memory. There are two types of write operations, byte write and page write.

Write operation is possible when $\overline{WC}$ control pin put at a low logic level (0). When this control signal is set at 1, write operation is not possible and data in the memory is protected.

Byte Write and Page Write explained below assume that Write Control pin ($\overline{WC}$) is set to 0.

Byte Write (see Figure 9)

To perform a byte write the start condition is followed by the memory slave address and the R/$\overline{W}$ bit set to 0. The PCA9500 will respond with an acknowledge and then consider the next eight bits sent as the word address and the eight bits after the word address as the data. The PCA9500 will issue an acknowledge after the receipt of both the word address and the data. To terminate the data transfer the master issues the stop condition, initiating the internal write cycle to the non-volatile memory. Only write and read operations to the Quasi-bidirectional I/O are allowed during the internal write cycle.

Page Write (see Figure 10)

A page write is initiated in the same way as the byte write. If after sending the first word of data, the stop condition is not received the PCA9500 considers subsequent words as data. After each data word the PCA9500 responds with an acknowledge and the two least significant bits of the memory address field are incremented. Should the master not send a stop condition after four data words the address counter will return to its initial value and overwrite the data previously written. After the receipt of the stop condition the inputs will behave as with the byte write during the internal write cycle.

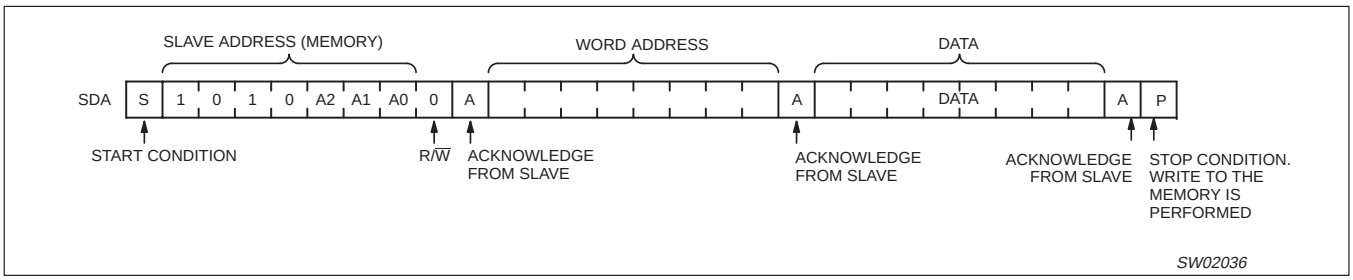


Figure 9. Byte write

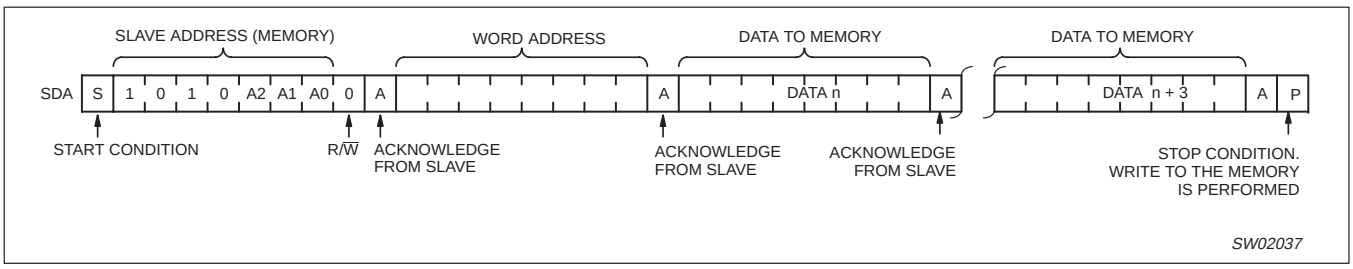


Figure 10. Page Write

Read operations

PCA9500 read operations are initiated in an identical manner to write operations with the exception that the memory slave address' R/$\overline{W}$ bit is set to a one. There are three types of read operations; current address, random and sequential.

Current Address Read (see Figure 11)

The PCA9500 contains an internal address counter that increments after each read or write access, as a result if the last word accessed was at address n then the address counter contains the address n+1.

When the PCA9500 receives its memory slave address with the R/$\overline{W}$ bit set to one it issues an acknowledge and uses the next eight clocks to transmit the data contained at the address stored in the address counter. The master ceases the transmission by issuing the stop condition after the eighth bit. There is no ninth clock cycle for the acknowledge.

Random Read (see Figure 12)

The PCA9500's random read mode allows the address to be read from to be specified by the master. This is done by performing a dummy write to set the address counter to the location to be read.

The master must perform a byte write to the address location to be read, but instead of transmitting the data after receiving the acknowledge from the PCA9500 the master reissues the start condition and memory slave address with the R/$\overline{W}$ bit set to one. The PCA9500 will then transmit an acknowledge and use the next eight clock cycles to transmit the data contained in the addressed location. The master ceases the transmission by issuing the stop condition after the eighth bit, omitting the ninth clock cycle acknowledge.

Sequential Read (see Figure 13)

The PCA9500 sequential read is an extension of either the current address read or random read. If the master doesn't issue a stop condition after it has received the eighth data bit, but instead issues an acknowledge, the PCA9500 will increment the address counter and use the next eight cycles to transmit the data from that location. The master can continue this process to read the contents of the entire memory. Upon reaching address 255 the counter will return to address 0 and continue transmitting data until a stop condition is received. The master ceases the transmission by issuing the stop condition after the eighth bit, omitting the ninth clock cycle acknowledge.

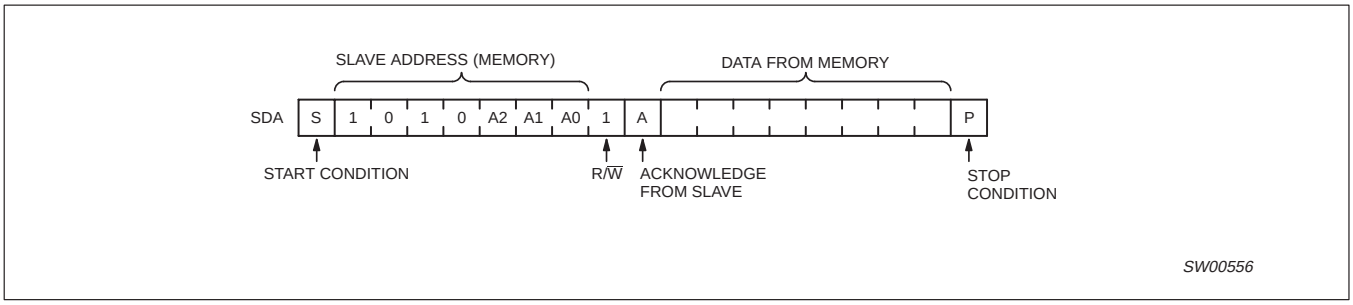


Figure 11. Current Address Read

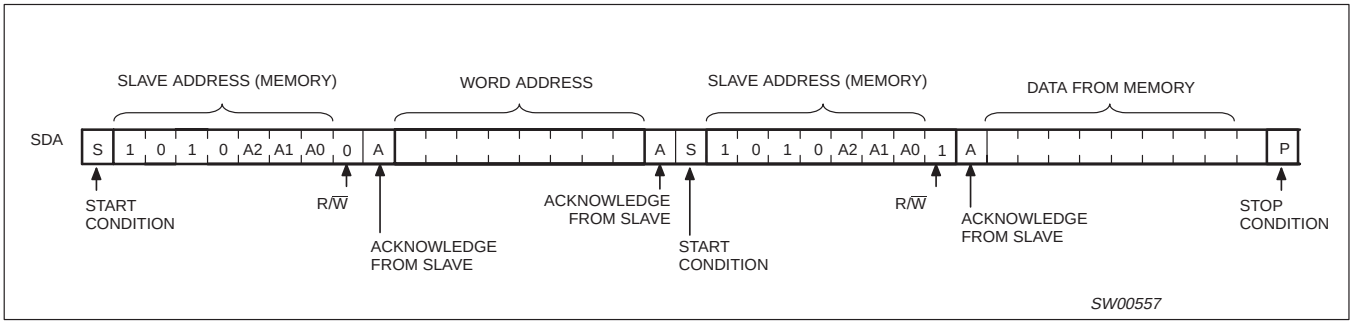


Figure 12. Random Read

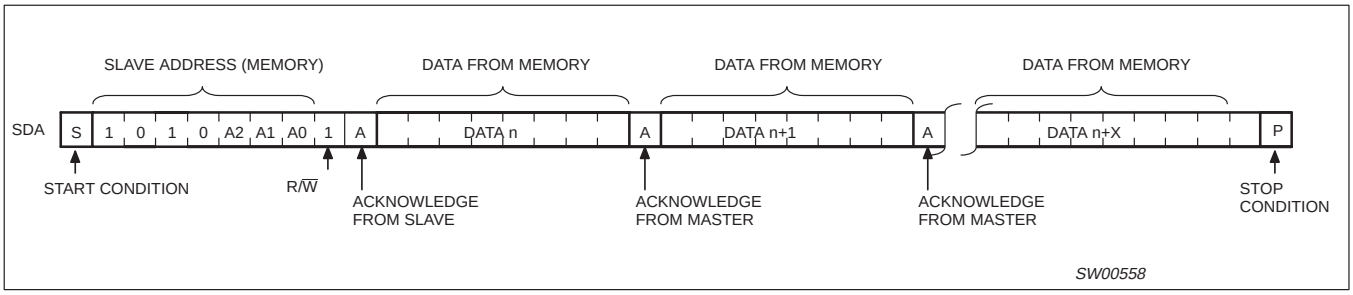


Figure 13. Sequential Read

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock phase. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (See Figure 14).

Start and Stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the Start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the Stop condition (P) (see Figure 15).

System configuration

A device generating a message is a “transmitter”, a device receiving is the “receiver”. The device that controls the message is the “master” and the devices which are controlled by the master are the “slaves” (see Figure 16).

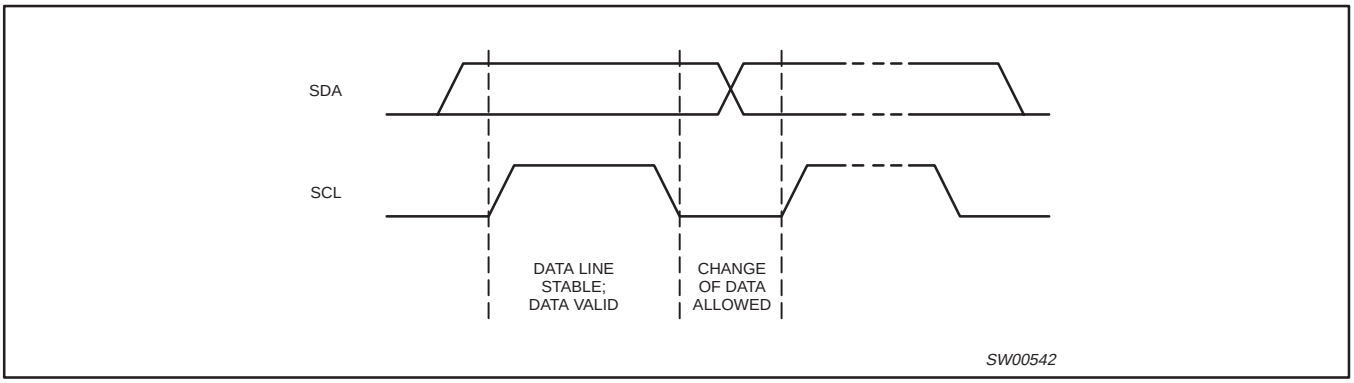


Figure 14. Bit transfer

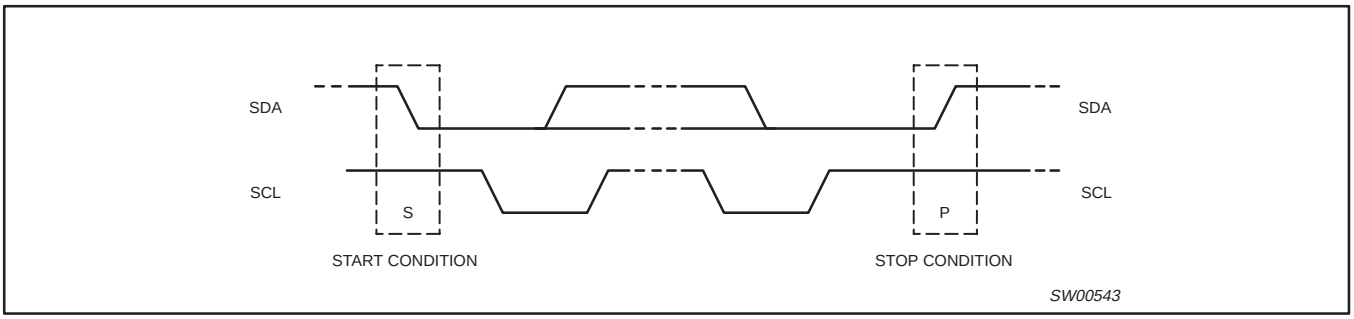


Figure 15. Definition of start and stop conditions

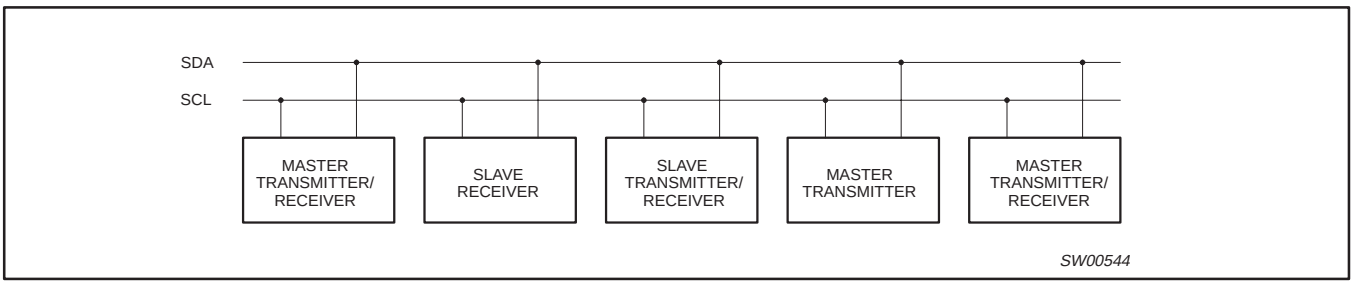


Figure 16. System configuration

Acknowledge (see Figure 17)

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

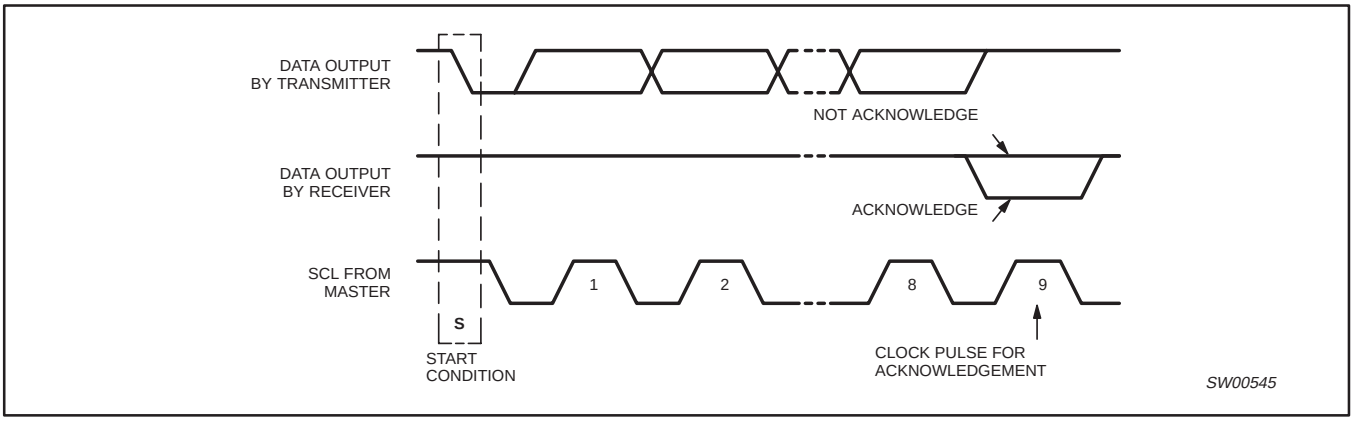


Figure 17. Acknowledgment on the I²C-bus

TYPICAL APPLICATION

Applications

- Board version tracking and configuration
- Board health monitoring and status reporting
- Multi-card systems in Telecom, Networking, and Base Station Infrastructure Equipment
- Field recall and troubleshooting functions for installed boards
- General-purpose integrated I/O with memory
- Drop in replacement for PCF8574 with integrated 2-kbit EEPROM
- Bus master sees GPIO and EEPROM as two separate devices
- Three hardware address pins allow up to 8 PCA9500s to be located in the same I²C/SMBus

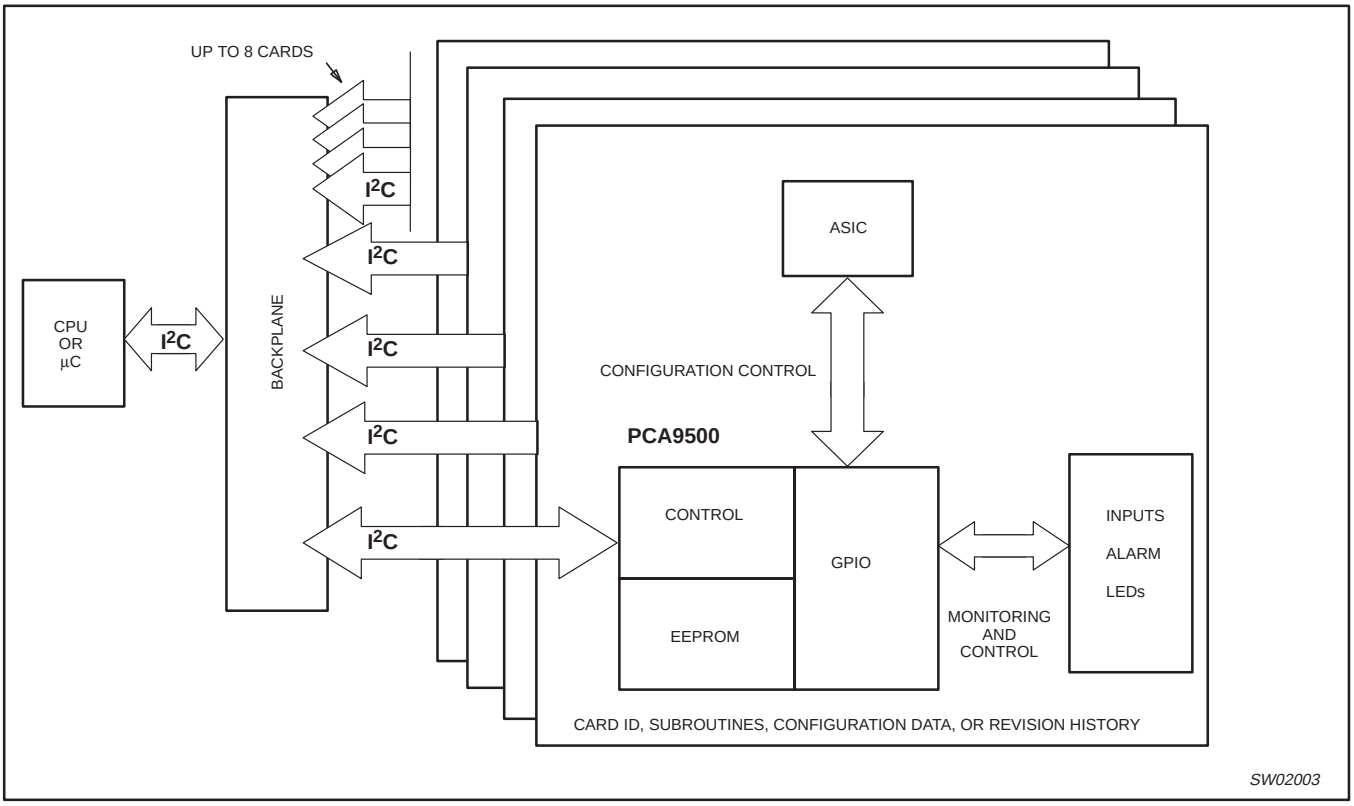
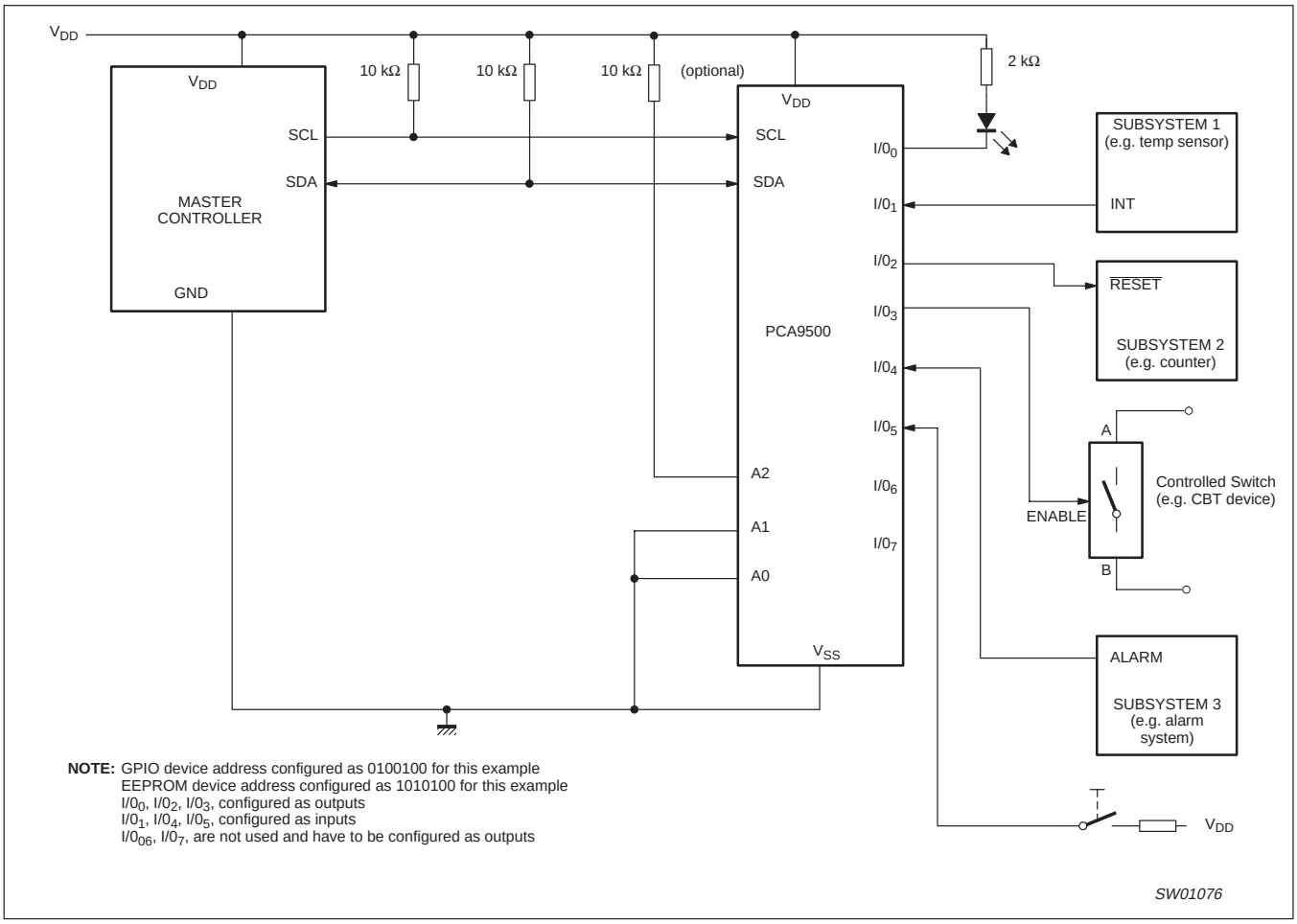


Figure 18. Typical application

A central processor/controller typically located on the system main board can use the 400 kHz I²C/SMBus to poll the PCA9500 devices located on the system cards for status or version control type of information. The PCA9500 may be programmed at manufacturing to store information regarding board build, firmware version, manufacturer identification, configuration option data… Alternately, these devices can be used as convenient interface for board configuration, thereby utilizing the I²C/SMBus as an intra-system communication bus.

TYPICAL APPLICATION



NOTE: GPIO device address configured as 0100100 for this example
EEPROM device address configured as 1010100 for this example
I/O_0, I/O_2, I/O_3, configured as outputs
I/O_1, I/O_4, I/O_5, configured as inputs
I/O_{06}, I/O_7, are not used and have to be configured as outputs

Figure 19. Typical application

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.5	4.0	V
V_I	Input voltage	V_{SS} – 0.5	5.5	V
I_I	DC input current	–20	20	mA
I_O	DC output current	–25	25	mA
I_{DD}	Supply current	–100	100	mA
I_{SS}	Supply current	–100	100	mA
P_{tot}	Total power dissipation	—	400	mW
P_O	Total power dissipation per output	—	100	mW
T_{stg}	Storage temperature	–65	+150	°C
T_{amb}	Operating temperature	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

T_{amb} = –40 to +85 °C unless otherwise specified; V_{CC} = 3.3 V

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supply						
V_{DD}	Supply voltage		2.5	3.3	3.6	V
I_{DDQ}	Standby current	A0, A1, A2, $\overline{WC}$ = HIGH	—	—	60	µA
I_{DD1}	Supply current read		—	—	1	mA
I_{DD2}	Supply current write		—	—	2	mA
V_{POR}	Power-on reset voltage		—	—	2.4	V
Input SCL; input, output SDA						
V_{IL}	LOW-level input voltage		–0.5	—	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	—	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3	—	—	mA
I_{LI}	Input leakage current	$V_I = V_{DD}$ or V_{SS}	–1	—	1	µA
C_I	Input capacitance	$V_I = V_{SS}$	—	—	7	pF
I/O Expander Port						
V_{IL}	LOW-level input voltage		–0.5	—	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	—	5.5	V
$I_{IHL(max)}$	Input current through protection diodes		–400	—	400	µA
I_{OL}	LOW-level output current	V_{OL} = 1 V	10	25	—	mA
I_{OH}	HIGH-level output current	$V_{OH} = V_{ss}$	30	100	300	µA
I_{OHt}	Transient pull-up current		—	2	—	mA
C_I	Input capacitance		—	—	10	pF
C_O	Output capacitance		—	—	10	pF
Address Inputs (A0, A1, A2), $\overline{WC}$ input						
V_{IL}	LOW-level input voltage		–0.5	—	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	—	5.5	V
I_{LI}	Input leakage current	$V_I = V_{DD}$	–1	—	1	µA
	Input leakage (pull-up) current	$V_I = V_{SS}$	10	25	100	µA

NOTES:

1. Each I/O must be externally limited to a maximum of 25 mA and the device must be limited to a maximum current of 100 mA.

NON-VOLATILE STORAGE SPECIFICATIONS

PARAMETER	SPECIFICATION
Memory cell data retention	10 years minimum
Number of memory cell write cycles	100,000 cycles minimum

I²C-BUS TIMING CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
I²C-bus timing (see Figure 20; Note 2)					
f_{SCL}	SCL clock frequency	—	—	400	kHz
t_{SW}	tolerable spike width on bus	—	—	50	ns
t_{BUF}	bus free time	1.3	—	—	µs
$t_{SU;STA}$	START condition set-up time	0.6	—	—	µs
$t_{HD;STA}$	START condition hold time	0.6	—	—	µs
t_r	SCL and SDA rise time	—	—	0.3	µs
t_f	SCL and SDA fall time	—	—	0.3	µs
$t_{SU;DAT}$	data set-up time	250	—	—	ns
$t_{HD;DAT}$	data hold time	0	—	—	ns
$t_{VD;DAT}$	SCL LOW to data out valid	—	—	1.0	µs
$t_{SU;STO}$	STOP condition set-up time	0.6	—	—	µs

NOTE:

2. All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

PORT TIMING CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
t_{pv}	Output data valid; $C_L \leq 100$ pF	—	—	4	µs
t_{ps}	Input data setup time; $C_L \leq 100$ pF	0	—	—	µs
t_{ph}	Input data hold time; $C_L \leq 100$ pF	4	—	—	µs

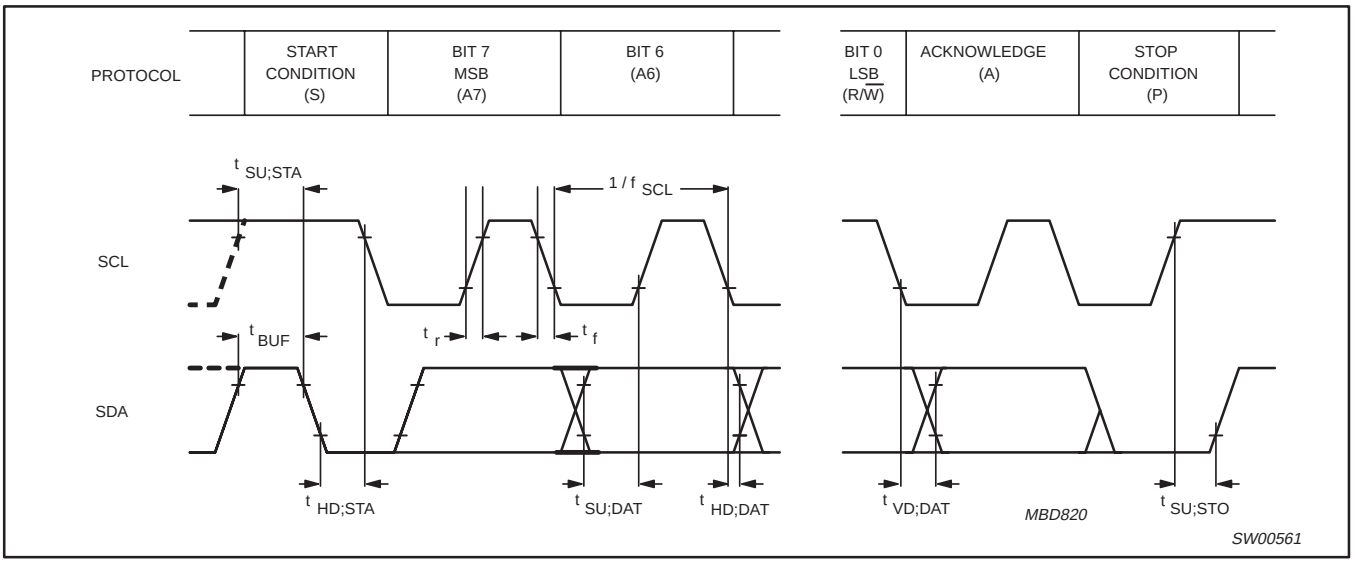


Figure 20.

POWER-UP TIMING

SYMBOL	PARAMETER	MAX.	UNIT
t_{PUR}[1]	Power-up to Read Operation	1	ms
t_{PUW}[1]	Power-up to Write Operation	5	ms

NOTE:
1. t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are guaranteed by design.

WRITE CYCLE LIMITS

SYMBOL	PARAMETER	MIN.	TYP. (5)	MAX.	UNIT
t_{WR}[1]	Write Cycle Time	—	5	10	ms

NOTE:
1. t_{WR} is the maximum time that the device requires to perform the internal write operation.

Write Cycle Timing

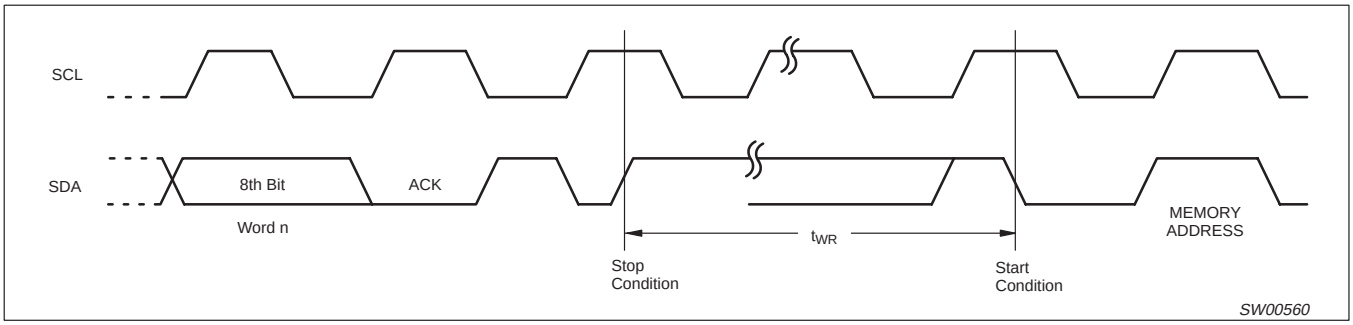


Figure 21.

TYPICAL PERFORMANCE CURVES

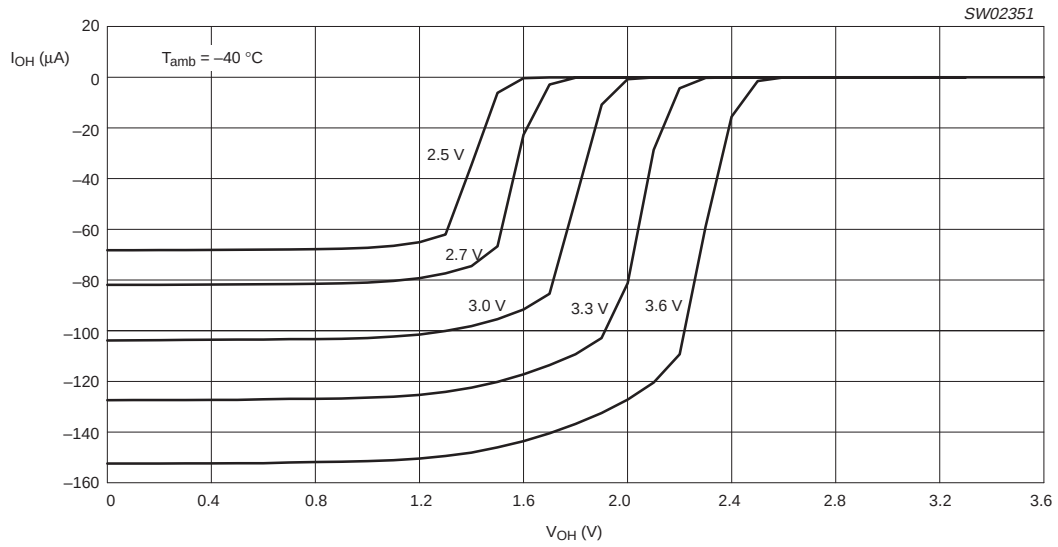


Figure 22. V_{OH} versus I_{OH} (T_{amb} = –40 °C)

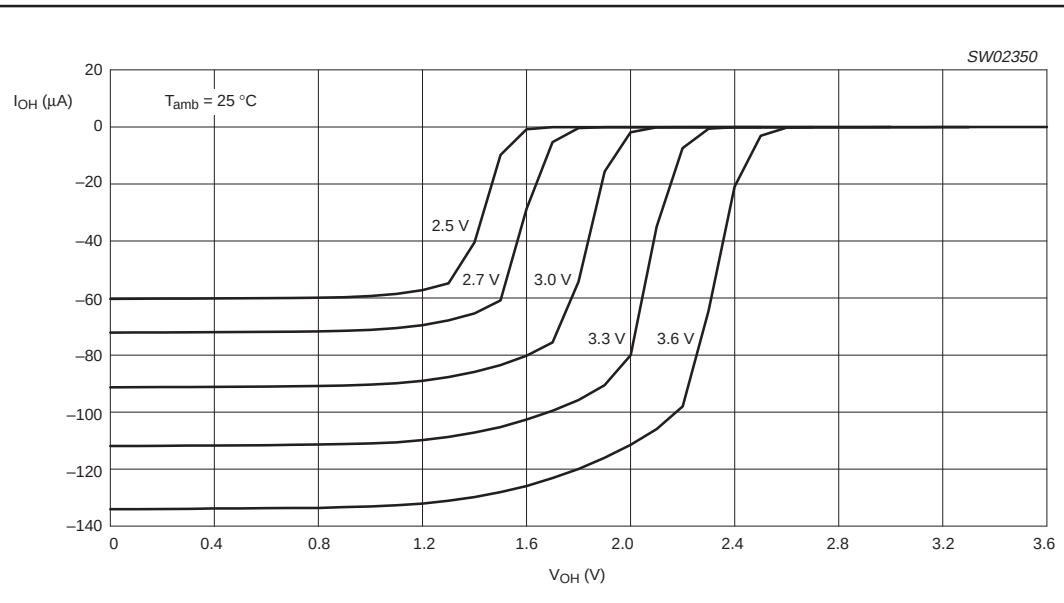


Figure 23. V_{OH} versus I_{OH} (T_{amb} = 25 °C)

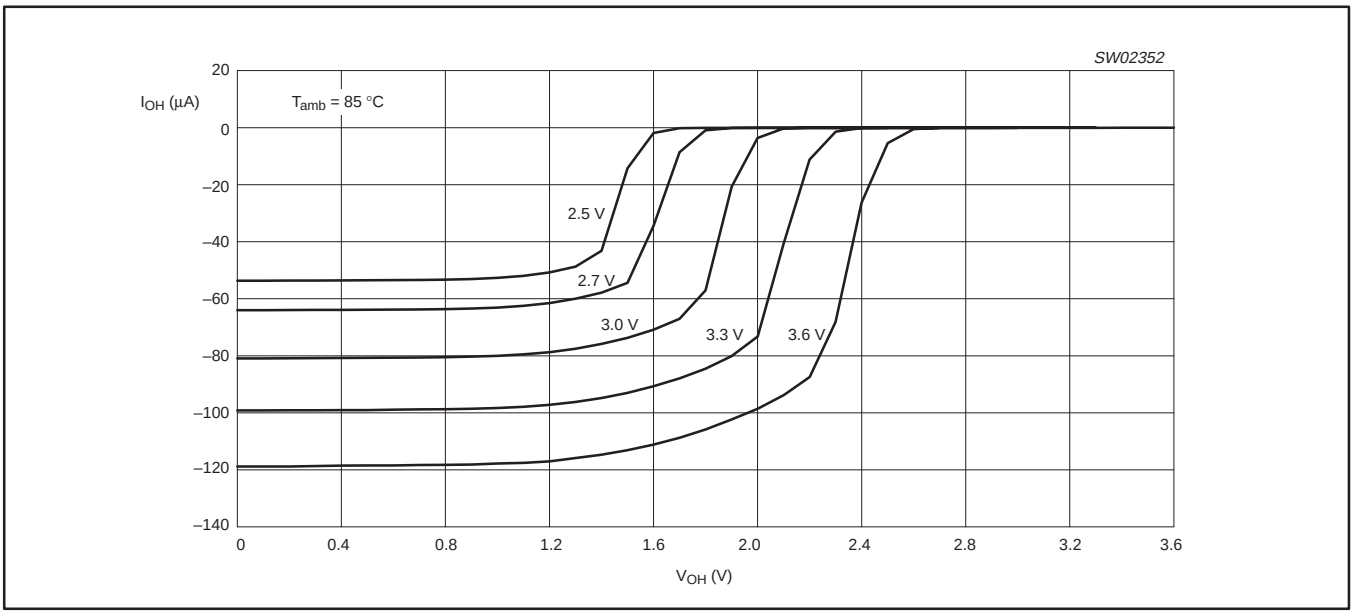


Figure 24. V_{OH} versus I_{OH} (T_{amb} = 85 °C)

NOTE:
Rapid fall off in V_{OH} at current inception is due to a diode that provides 5 V overvoltage protection for the GPIO I/O pins. When the GPIO I/O are being used as inputs, the internal current source V_{OH} should be evaluated to determine if external pull-up resistors are required to provide sufficient V_{IH} threshold noise margin.

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *IC Package Databook* (order code 9398 652 90011).

DIP

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature (T_{stg} max). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400°C, contact may be up to 5 seconds.

SO and SSOP

Reflow soldering

Reflow soldering techniques are suitable for all SO and SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is not recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.**

Even with these conditions, only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

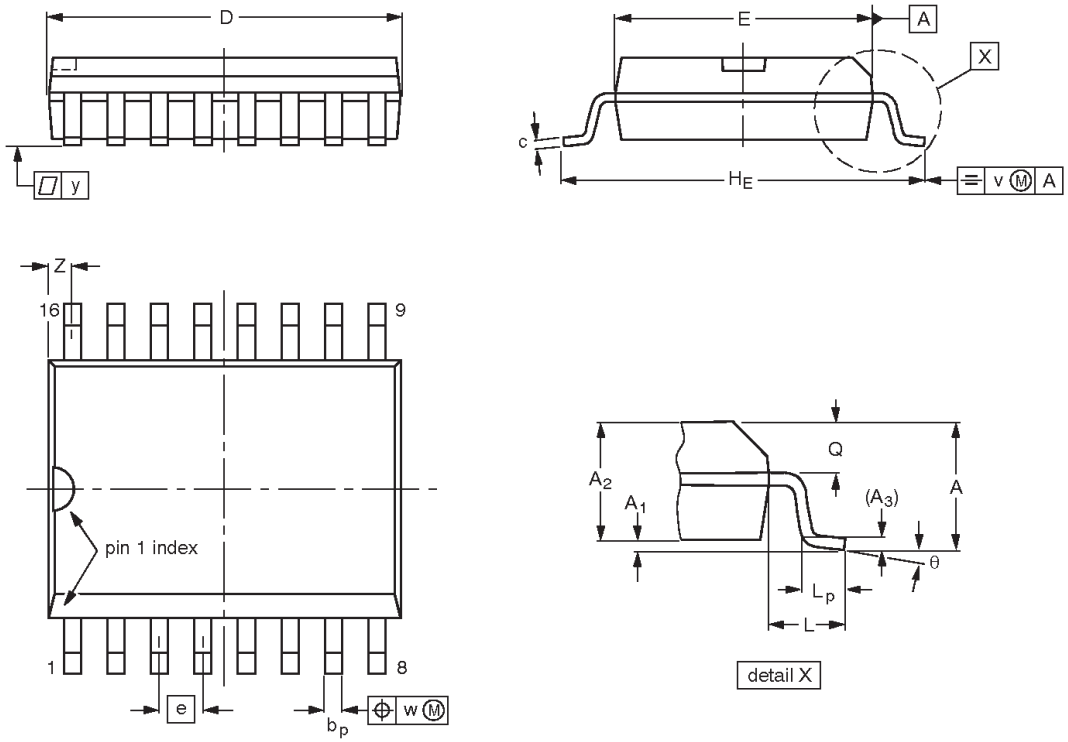
Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

SO16: plastic small outline package; 16 leads; body width 7.5 mm **SOT162-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

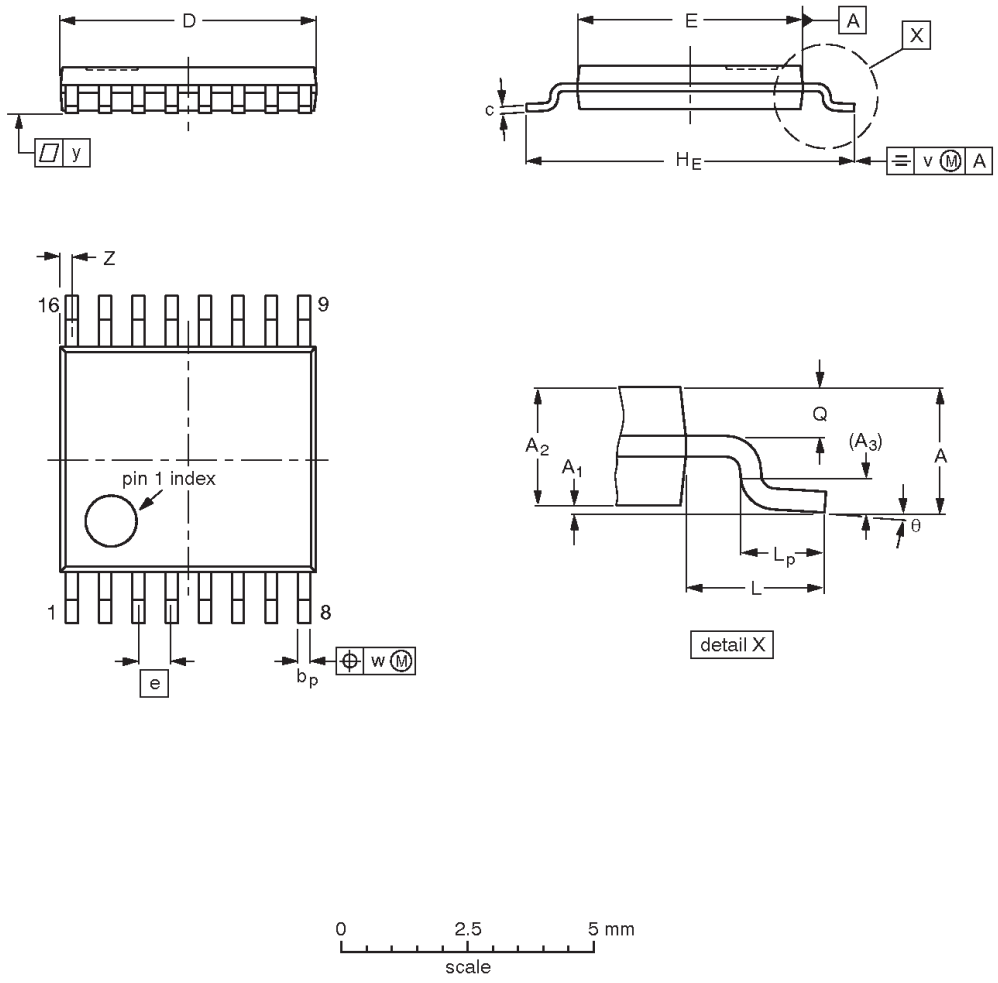
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT162-1	075E03	MS-013				~~99-12-27~~ 03-02-19

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

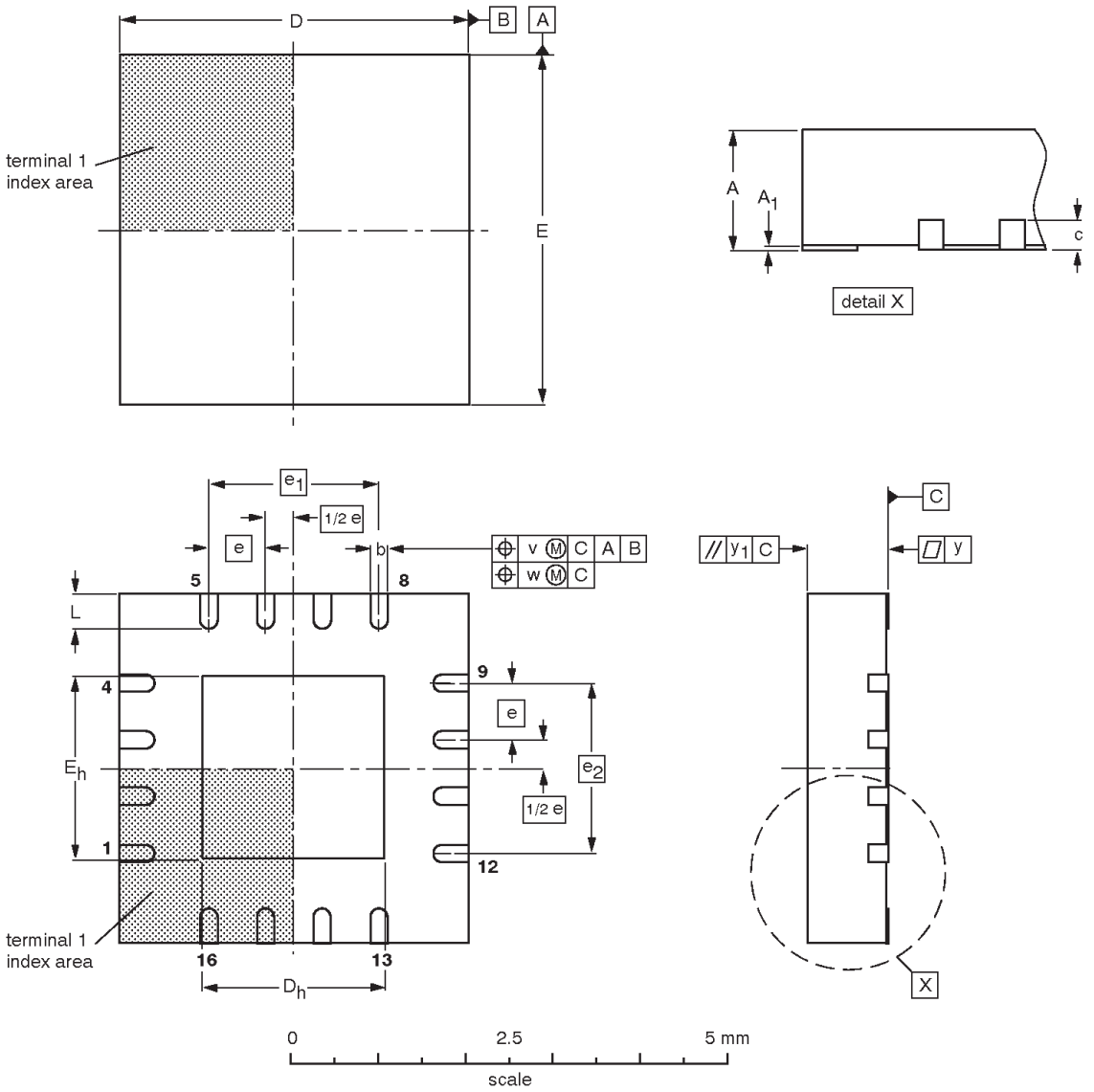
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

HVQFN16: plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 4 x 4 x 0.85 mm **SOT629-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A1	b	c	D(1)	Dh	E(1)	Eh	e	e1	e2	L	v	w	y	y1
mm	1	0.05 0.00	0.38 0.23	0.2	4.1 3.9	2.25 1.95	4.1 3.9	2.25 1.95	0.65	1.95	1.95	0.75 0.50	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT629-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

REVISION HISTORY

Rev	Date	Description
_3	20040930	**Product data sheet (9397 750 14134). Supersedes data of 2003 Jun 27 (9397 750 11682).** Modifications: ● Figure 19: resistor values changed to 10 kΩ ● “DC characteristics” table on page : add Table note 1. ● Added “Typical performance curves” section
_2	20030627	**Product data (9397 750 11682); ECN 853-2369 30018 dated 11 June 2003. Supersedes data of 2002 September 09 (9397 750 10326).**
_1	20020927	**Product data (9397 750 10326); ECN: 853–2369 28875 (2002 Sep 27)**

8-bit I²C and SMBus I/O port with 2-kbit EEPROM PCA9500

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

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Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data sheet	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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