



# PCA9511A

Hot swappable I<sup>2</sup>C-bus and SMBus bus buffer

Rev. 01 — 15 August 2005

Product data sheet

## 1. General description

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The PCA9511A is a hot swappable I<sup>2</sup>C-bus and SMBus buffer that allows I/O card insertion into a live backplane without corrupting the data and clock buses. Control circuitry prevents the backplane from being connected to the card until a stop command or bus idle occurs on the backplane without bus contention on the card. When the connection is made, the PCA9511A provides bidirectional buffering, keeping the backplane and card capacitances isolated.

The PCA9511A rise time accelerator circuitry allows the use of weaker DC pull-up currents while still meeting rise time requirements. The PCA9511A incorporates a digital ENABLE input pin, which enables the device when asserted HIGH and forces the device into a low current mode when asserted LOW, and an open-drain READY output pin, which indicates that the backplane and card sides are connected together (HIGH) or not (LOW).

During insertion, the PCA9511A SDA and SCL lines are precharged to 1 V to minimize the current required to charge the parasitic capacitance of the chip.

## 2. Features

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- Bidirectional buffer for SDA and SCL lines increases fan out and prevents SDA and SCL corruption during live board insertion and removal from multi-point backplane systems
- Compatible with I<sup>2</sup>C-bus standard mode, I<sup>2</sup>C-bus fast mode, and SMBus standards
- Built-in  $\Delta V/\Delta t$  rise time accelerators on all SDA and SCL lines (0.6 V threshold)
- Active HIGH ENABLE input
- Active HIGH READY open-drain output
- High-impedance SDA and SCL pins for  $V_{CC} = 0$  V
- 1 V precharge on all SDA and SCL lines
- Supporting clock stretching and multiple master arbitration/synchronization
- Operating power supply voltage range: 2.7 V to 5.5 V
- 0 kHz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO8, TSSOP8 (MSOP8)

## 3. Applications

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- cPCI, VME, AdvancedTCA cards and other multi-point backplane cards that are required to be inserted or removed from an operating system

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## 4. Feature selection

**Table 1: Feature selection chart**

Feature	PCA9510A	PCA9511A	PCA9512A	PCA9513A	PCA9514A
idle detect	yes	yes	yes	yes	yes
high-impedance SDA, SCL pins for $V_{CC} = 0\text{ V}$	yes	yes	yes	yes	yes
rise time accelerator circuitry on SDA <sub>n</sub> and SCL <sub>n</sub> lines	-	yes	yes	yes	yes
rise time accelerator circuitry hardware disable pin for lightly loaded systems	-	-	yes	-	-
rise time accelerator threshold 0.8 V versus 0.6 V improves noise margin	-	-	-	yes	yes
ready open-drain output	yes	yes	-	yes	yes
two $V_{CC}$ pins to support 5 V to 3.3 V level translation with improved noise margins	-	-	yes	-	-
1 V precharge on all SDA and SCL lines	in only	yes	yes	-	-
92 $\mu\text{A}$ current source on SCLIN and SDAIN for PICMG applications	-	-	-	yes	-

## 5. Ordering information

**Table 2: Ordering information**

$T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$

Type number	Topside mark	Package		
		Name	Description	Version
PCA9511AD	PA9511A	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
PCA9511ADP	9511A	TSSOP8 <sup>[1]</sup>	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1

[1] Also known as 'MSOP8'.

Standard packing quantities and other packaging data are available at [www.standardics.philips.com/packaging/](http://www.standardics.philips.com/packaging/).

6. Block diagram

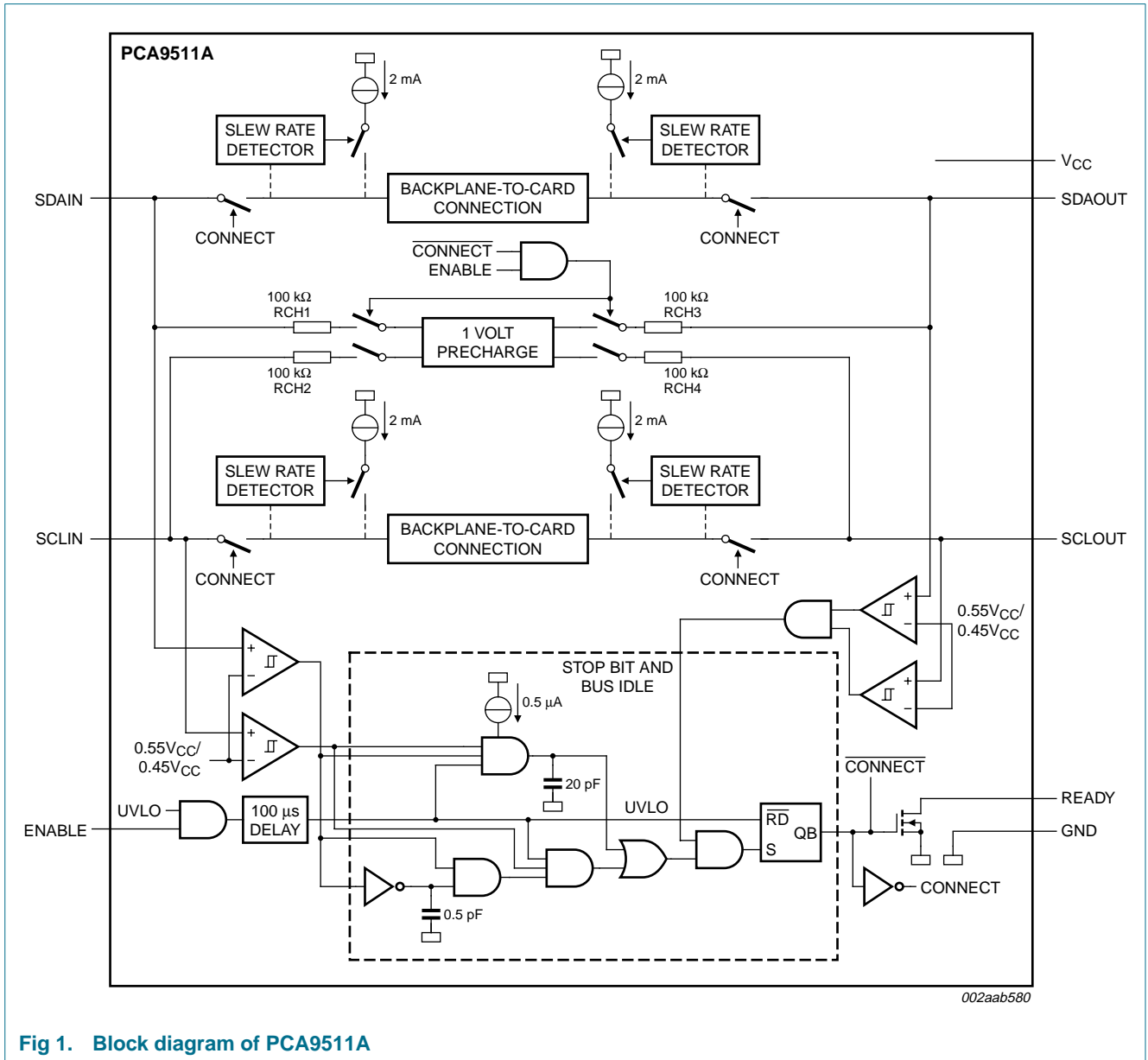


Fig 1. Block diagram of PCA9511A

## 7. Pinning information

### 7.1 Pinning

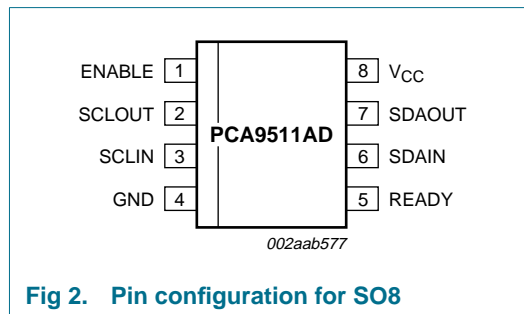


Fig 2. Pin configuration for SO8

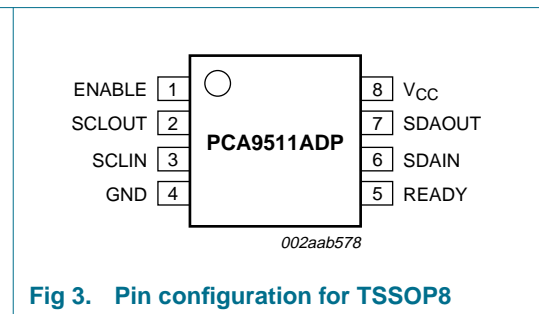


Fig 3. Pin configuration for TSSOP8

### 7.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
ENABLE	1	Chip enable. Grounding this input puts the part in a low current ( $< 1 \mu\text{A}$ ) mode. It also disables the rise time accelerators, isolates SDAIN from SDAOUT and isolates SCLIN from SCLOUT.
SCLOUT	2	serial clock output to and from the SCL bus on the card
SCLIN	3	serial clock input to and from the SCL bus on the backplane
GND	4	Ground. Connect this pin to a ground plane for best results.
READY	5	open-drain output which pulls LOW when SDAIN and SCLIN are disconnected from SDAOUT and SCLOUT, and goes HIGH when the two sides are connected
SDAIN	6	serial data input to and from the SDA bus on the backplane
SDAOUT	7	serial data output to and from the SDA bus on the card
V <sub>CC</sub>	8	power supply

## 8. Functional description

Refer to [Figure 1 "Block diagram of PCA9511A"](#).

### 8.1 Start-up

An undervoltage/initialization circuit holds the parts in a disconnected state which presents high-impedance to all SDA and SCL pins during power-up. A LOW on the ENABLE pin also forces the parts into the low current disconnected state when the  $I_{CC}$  is essentially zero. As the power supply is brought up and the ENABLE is HIGH or the part is powered and the ENABLE is taken from LOW to HIGH it enters an initialization state where the internal references are stabilized and the precharge circuit is enabled. At the end of the initialization state the 'Stop Bit And Bus Idle' detect circuit is enabled. With the ENABLE pin HIGH long enough to complete the initialization state ( $t_{en}$ ) and remaining HIGH when all the SDA and SCL pins have been HIGH for the bus idle time or when all pins are HIGH and a STOP condition is seen on the SDAIN and SCLIN pins, SDAIN is connected to SDAOUT and SCLIN is connected to SCLOUT. The 1 V precharge circuitry

is activated during the initialization and is deactivated when the connection is made. The precharge circuitry pulls up the SDA and SCL pins to 1 V through individual 100 k $\Omega$  nominal resistors. This precharges the pins to 1 V to minimize the worst case disturbances that result from inserting a card into the backplane where the backplane and the card are at opposite logic levels.

## 8.2 Connect circuitry

Once the connection circuitry is activated, the behavior of SDAIN and SDAOUT as well as SCLIN and SCLOUT become identical with each acting as a bidirectional buffer that isolates the input capacitance from the output bus capacitance while communicating the logic levels. A LOW forced on either SDAIN or SDAOUT will cause the other pin to be driven to a LOW by the part. The same is also true for the SCL pins. Noise between  $0.7V_{CC}$  and  $V_{CC}$  is generally ignored because a falling edge is only recognized when it falls below  $0.7V_{CC}$  with a slew rate of at least  $1.25\text{ V}/\mu\text{s}$ . When a falling edge is seen on one pin, the other pin in the pair turns on a pull-down driver that is referenced to a small voltage above the falling pin. The driver will pull the pin down at a slew rate determined by the driver and the load initially, because it does not start until the first falling pin is below  $0.7V_{CC}$ . The first falling pin may have a fast or slow slew rate, if it is faster than the pull down slew rate then the initial pull-down rate will continue. If the first falling pin has a slow slew rate then the second pin will be pulled down at its initial slew rate only until it is just above the first pin voltage then they will both continue down at the slew rate of the first.

Once both sides are LOW they will remain LOW until all the external drivers have stopped driving LOWs. If both sides are being driven LOW to the same value for instance, 10 mV by external drivers, which is the case for clock stretching and is typically the case for acknowledge, and one side external driver stops driving that pin will rise until the internal driver pulls it down to the offset voltage. When the last external driver stops driving a LOW, that pin will rise up and settle out just above the other pin as both rise together with a slew rate determined by the internal slew rate control and the RC time constant. As long as the slew rate is at least  $1.25\text{ V}/\mu\text{s}$ , when the pin voltage exceeds 0.6 V for the PCA9511A, the rise time accelerator's circuits are turned on and the pull-down driver is turned off.

## 8.3 Maximum number of devices in series

Each buffer adds about 0.1 V dynamic level offset at 25 °C with the offset larger at higher temperatures. Maximum offset ( $V_{\text{offset}}$ ) is 0.150 V with a 10 k $\Omega$  pull-up resistor. The LOW level at the signal origination end (master) is dependent upon the load and the only specification point is the I<sup>2</sup>C-bus specification of 3 mA will produce  $V_{OL} < 0.4\text{ V}$ , although if lightly loaded the  $V_{OL}$  may be  $-0.1\text{ V}$ . Assuming  $V_{OL} = 0.1\text{ V}$  and  $V_{\text{offset}} = 0.1\text{ V}$ , the level after four buffers would be 0.5 V, which is only about 0.1 V below the threshold of the rising edge accelerator (about 0.6 V). With great care a system with four buffers may work, but as the  $V_{OL}$  moves up from 0.1 V, noise or bounces on the line will result in firing the rising edge accelerator thus introducing false clock edges. Generally it is recommended to limit the number of buffers in series to two, and to keep the load light to minimize the offset.

The PCA9510A (rise time accelerator is permanently disabled) and the PCA9512A (rise time accelerator can be turned off) are a little different with the rise time accelerator turned off because the rise time accelerator will not pull the node up, but the same logic that turns

on the accelerator turns the pull-down off. If the  $V_{IL}$  is above  $\sim 0.6$  V and a rising edge is detected, the pull-down will turn off and will not turn back on until a falling edge is detected.

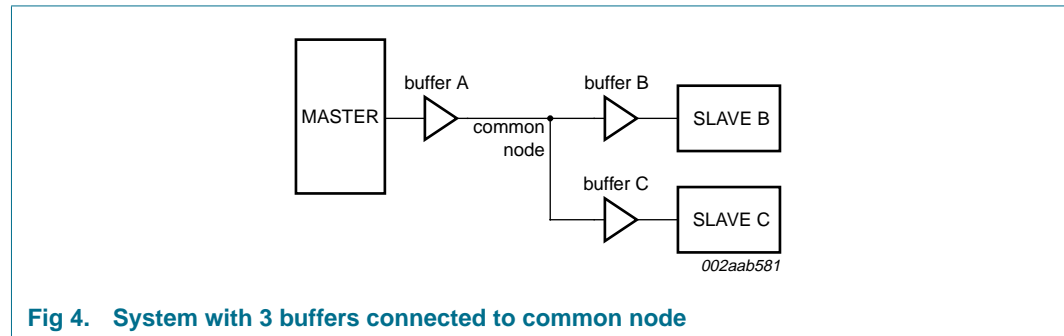


Fig 4. System with 3 buffers connected to common node

Consider a system with three buffers connected to a common node and communication between the Master and Slave B that are connected at either end of buffer A and buffer B in series as shown in Figure 4. Consider if the  $V_{OL}$  at the input of buffer A is 0.3 V and the  $V_{OL}$  of Slave B (when acknowledging) is 0.4 V with the direction changing from Master to Slave B and then from Slave B to Master. Before the direction change you would observe  $V_{IL}$  at the input of buffer A of 0.3 V and its output, the common node, is  $\sim 0.4$  V. The output of buffer B and buffer C would be  $\sim 0.5$  V, but Slave B is driving 0.4 V, so the voltage at Slave B is 0.4 V. The output of buffer C is  $\sim 0.5$  V. When the Master pull-down turns off, the input of buffer A rises and so does its output, the common node, because it is the only part driving the node. The common node will rise to 0.5 V before buffer B's output turns on, if the pull-up is strong the node may bounce. If the bounce goes above the threshold for the rising edge accelerator  $\sim 0.6$  V the accelerators on both buffer A and buffer C will fire contending with the output of buffer B. The node on the input of buffer A will go HIGH as will the input node of buffer C. After the common node voltage is stable for a while the rising edge accelerators will turn off and the common node will return to  $\sim 0.5$  V because the buffer B is still on. The voltage at both the Master and Slave C nodes would then fall to  $\sim 0.6$  V until Slave B turned off. This would not cause a failure on the data line as long as the return to 0.5 V on the common node ( $\sim 0.6$  V at the Master and Slave C) occurred before the data setup time. If this were the SCL line, the parts on buffer A and buffer C would see a false clock rather than a stretched clock, which would cause a system error.

## 8.4 Propagation delays

The delay for a rising edge is determined by the combined pull-up current from the bus resistors and the rise time accelerator current source and the effective capacitance on the lines. If the pull-up currents are the same, any difference in rise time is directly proportional to the difference in capacitance between the two sides. The  $t_{PLH}$  may be negative if the output capacitance is less than the input capacitance and would be positive if the output capacitance is larger than the input capacitance, when the currents are the same.

The  $t_{PHL}$  can never be negative because the output does not start to fall until the input is below  $0.7V_{CC}$ , and the output turn on has a non-zero delay, and the output has a limited maximum slew rate, and even if the input slew rate is slow enough that the output catches up it will still lag the falling voltage of the input by the offset voltage. The maximum  $t_{PHL}$  occurs when the input is driven LOW with zero delay and the output is still limited by its

turn-on delay and the falling edge slew rate. The output falling edge slew rate is a function of the internal maximum slew rate which is a function of temperature,  $V_{CC}$  and process, as well as the load current and the load capacitance.

### 8.5 Rise time accelerators

During positive bus transitions a 2 mA current source is switched on to quickly slew the SDA and SCL lines HIGH once the input level of 0.6 V for the PCA9511A is exceeded. The rising edge rate should be at least 1.25 V/ $\mu$ s to guarantee turn on of the accelerators.

### 8.6 READY digital output

This pin provides a digital flag which is LOW when either ENABLE is LOW or the start-up sequence described earlier in this section has not been completed. READY goes HIGH when ENABLE is HIGH and start-up is complete. The pin is driven by an open-drain pull-down capable of sinking 3 mA while holding 0.4 V on the pin. Connect a resistor of 10 k $\Omega$  to  $V_{CC}$  to provide the pull-up.

### 8.7 ENABLE low current disable

Grounding the ENABLE pin disconnects the backplane side from the card side, disables the rise-time accelerators, drives READY LOW, disables the bus precharge circuitry, and puts the part in a low current state. When the pin voltage is driven all the way to  $V_{CC}$ , the part waits for data transactions on both the backplane and card sides to be complete before reconnecting the two sides.

### 8.8 Resistor pull-up value selection

The system pull-up resistors must be strong enough to provide a positive slew rate of 1.25 V/ $\mu$ s on the SDA and SCL pins, in order to activate the boost pull-up currents during rising edges. Choose maximum resistor value using the formula:

$$R \leq 800 \times 10^3 \left( \frac{V_{CC(min)} - 0.6}{C} \right)$$

where R is the pull-up resistor value in  $\Omega$ ,  $V_{CC(min)}$  is the minimum  $V_{CC}$  voltage in volts, and C is the equivalent bus capacitance in picofarads (pF).

In addition, regardless of the bus capacitance, always choose  $R \leq 16$  k $\Omega$  for  $V_{CC} = 5.5$  V maximum,  $R \leq 24$  k $\Omega$  for  $V_{CC} = 3.6$  V maximum. The start-up circuitry requires logic HIGH voltages on SDAOUT and SCLOUT to connect the backplane to the card, and these pull-up values are needed to overcome the precharge voltage. See the curves in [Figure 5](#) and [Figure 6](#) for guidance in resistor pull-up selection.

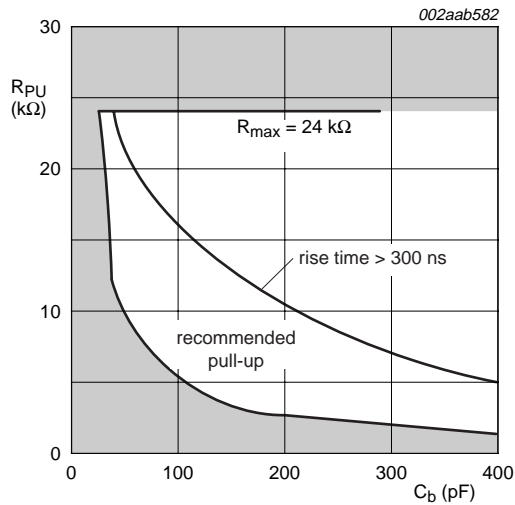


Fig 5. Bus requirements for 3.3 V systems

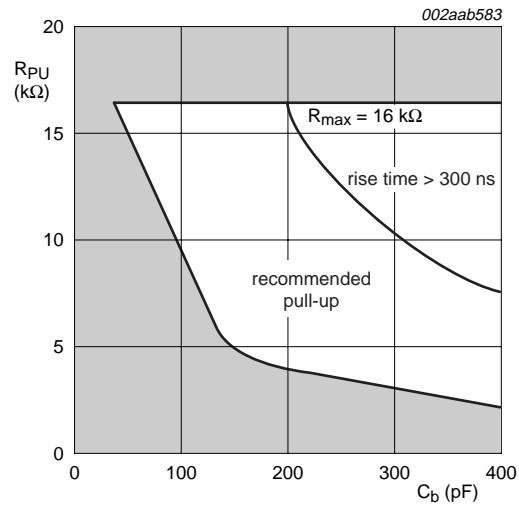


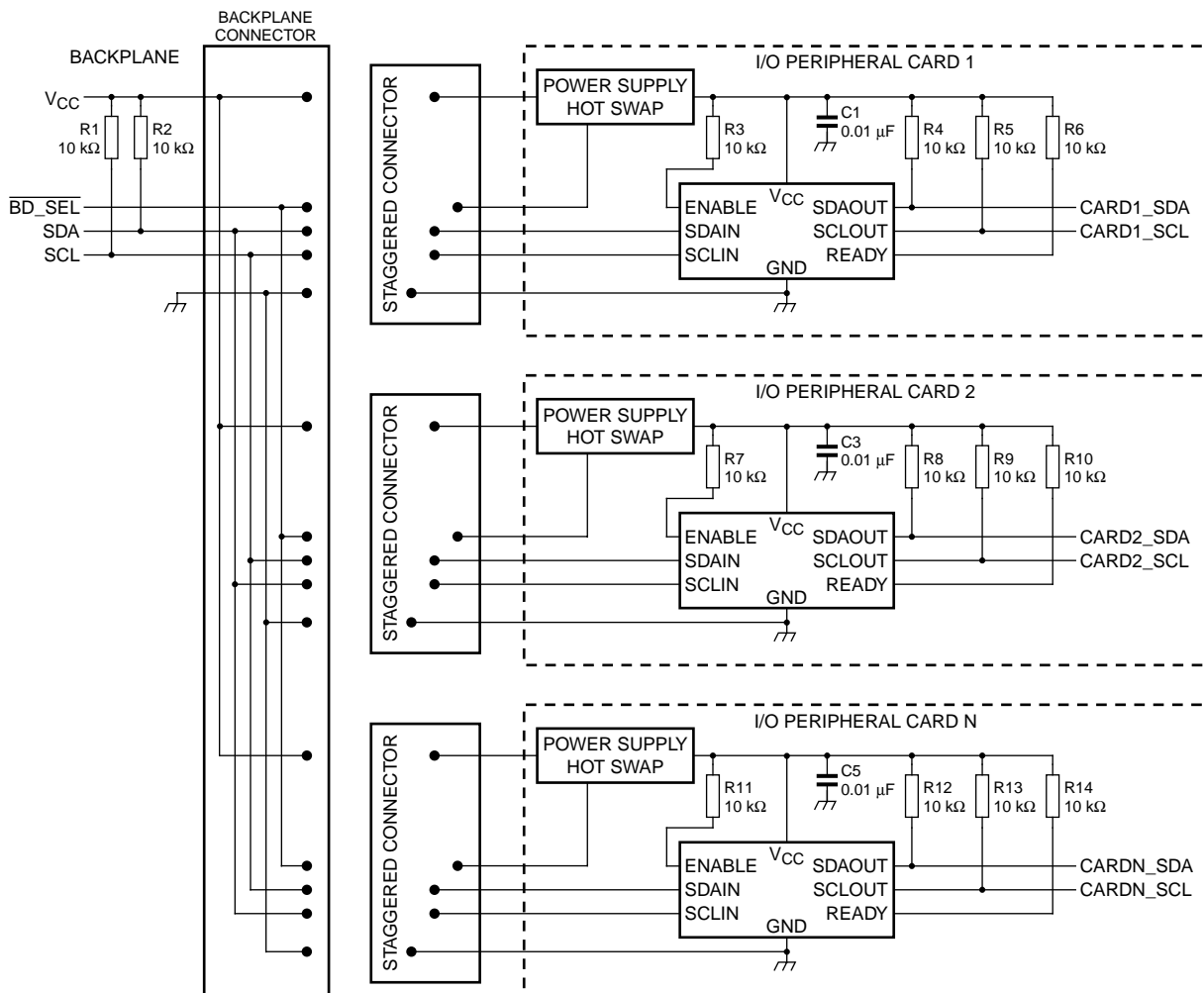
Fig 6. Bus requirements for 5 V systems

### 8.9 Hot swapping and capacitance buffering application

Figure 7 through Figure 10 illustrate the usage of the PCA9511A in applications that take advantage of both its hot swapping and capacitance buffering features. In all of these applications, note that if the I/O cards were plugged directly into the backplane, all of the backplane and card capacitances would add directly together, making rise time and fall time requirements difficult to meet. Placing a bus buffer on the edge of each card, however, isolates the card capacitance from the backplane. For a given I/O card, the PCA9511A drives the capacitance of everything on the card and the backplane must drive only the capacitance of the bus buffer, which is less than 10 pF, the connector, trace, and all additional cards on the backplane.

See Application Note AN10160, 'Hot Swap Bus Buffer' for more information on applications and technical assistance.





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**Remark:** The PCA9511A can be used in any combination depending on the number of rise time accelerators that are needed by the system. Normally only one PCA9511A would be required per bus.

**Fig 7. Hot swapping multiple I/O cards into a backplane using the PCA9511A in a cPCI, VME, and AdvancedTCA system**

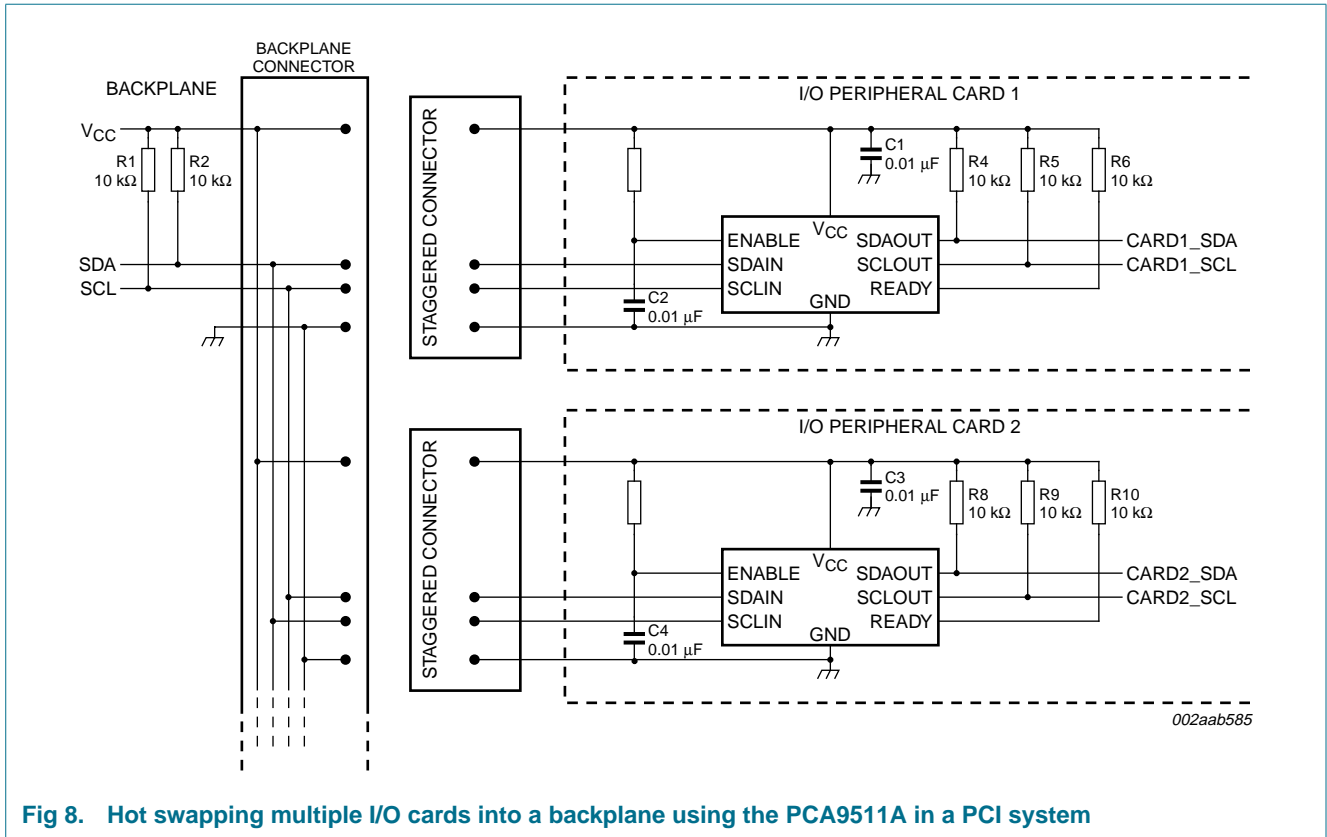
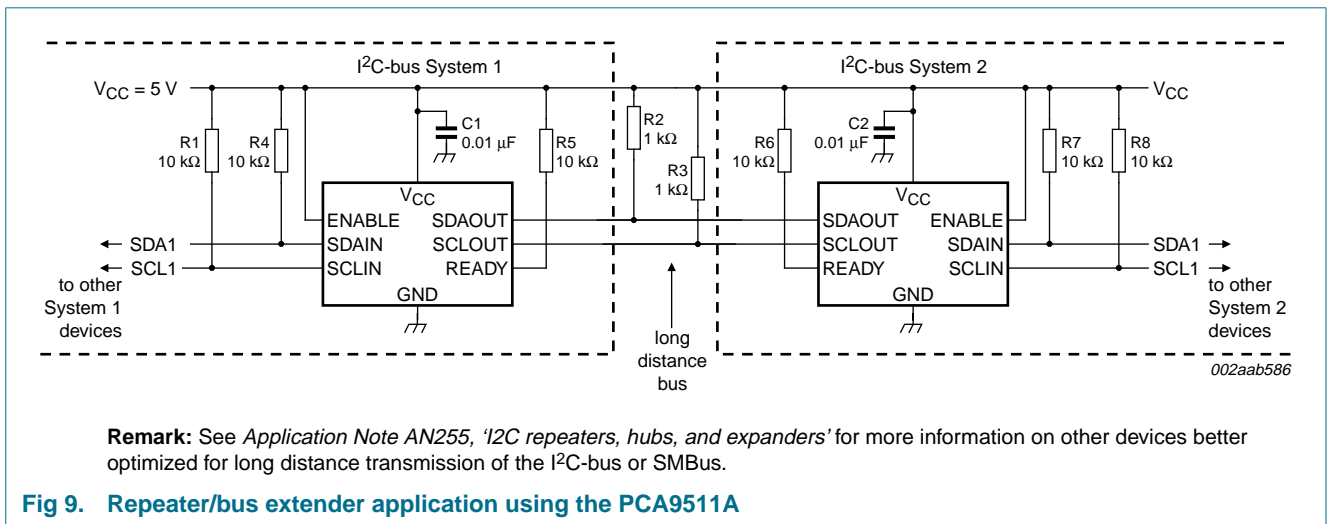
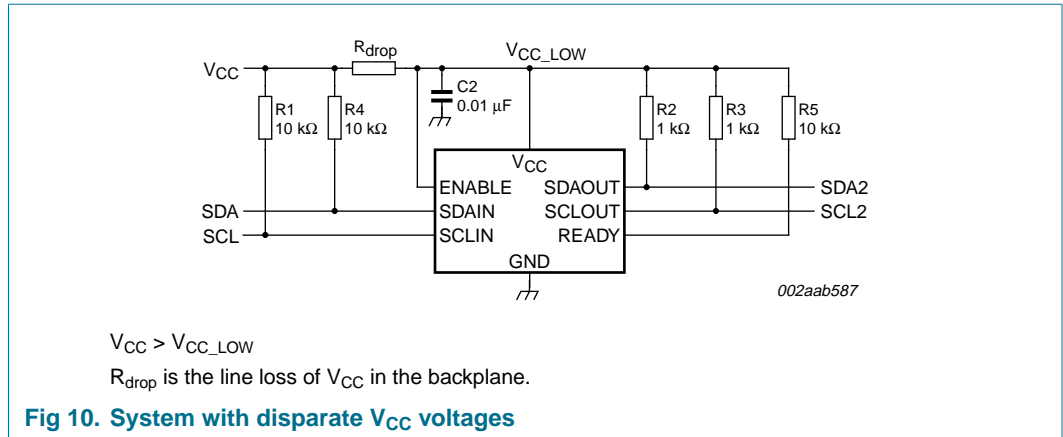


Fig 8. Hot swapping multiple I/O cards into a backplane using the PCA9511A in a PCI system

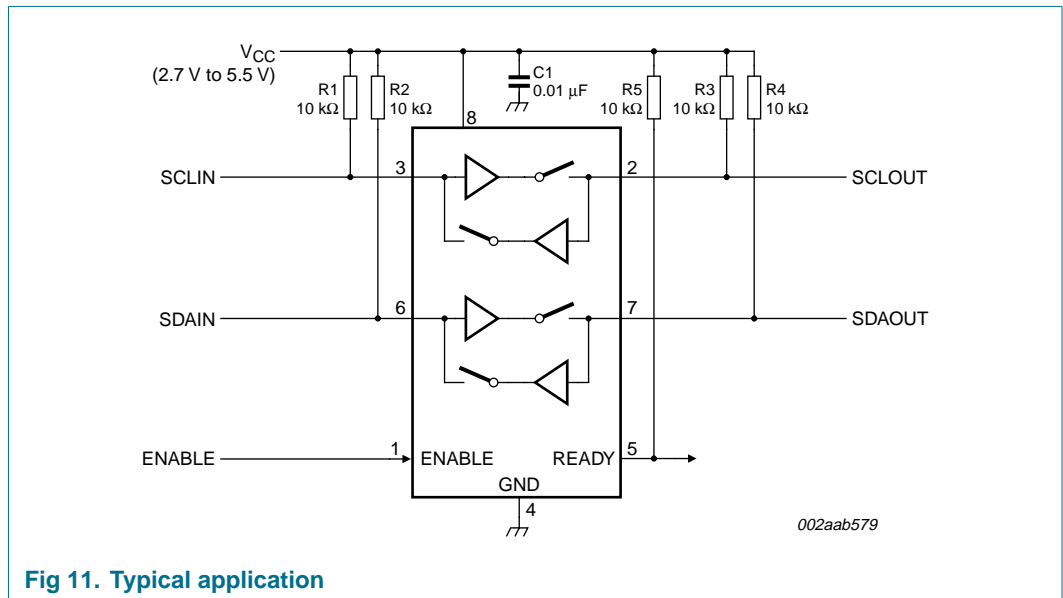


**Remark:** See Application Note AN255, 'I<sup>2</sup>C repeaters, hubs, and expanders' for more information on other devices better optimized for long distance transmission of the I<sup>2</sup>C-bus or SMBus.

Fig 9. Repeater/bus extender application using the PCA9511A



### 9. Application design-in information



### 10. Limiting values

**Table 4: Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		[1] -0.5	+7	V
$V_n$	voltage on SDAIN, SCLIN, SDAOUT, SCLOUT, READY, ENABLE		[1] -0.5	+7	V
$T_{oper}$	operating temperature		-40	+85	°C
$T_{stg}$	storage temperature		-65	+150	°C
$T_{sp}$	solder point temperature	10 s max.	-	+300	°C
$T_{j(max)}$	maximum junction temperature		-	+125	°C

[1] Voltages with respect to pin GND.

## 11. Characteristics

**Table 5: Characteristics**
 $V_{CC} = 2.7\text{ V to }5.5\text{ V}; T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C};$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Power supply</b>						
$V_{CC}$	supply voltage		[1] 2.7	-	5.5	V
$I_{CC}$	supply current	$V_{CC} = 5.5\text{ V};$ $V_{SDAIN} = V_{SCLIN} = 0\text{ V}$	[1] -	3.5	6	mA
$I_{CC(sd)}$	Shut-down mode supply current	$V_{ENABLE} = 0\text{ V};$ all other pins at $V_{CC}$ or GND	-	0.1	-	$\mu\text{A}$
<b>Start-up circuitry</b>						
$V_{pch}$	precharge voltage	SDA, SCL floating	[1] 0.8	1.1	1.2	V
$V_{IH(ENABLE)}$	HIGH-state input voltage on pin ENABLE		-	$0.5 \times V_{CC}$	$0.7 \times V_{CC}$	V
$V_{IL(ENABLE)}$	LOW-state input voltage on pin ENABLE		$0.3 \times V_{CC}$	$0.5 \times V_{CC}$	-	V
$I_{I(ENABLE)}$	input current on pin ENABLE	$V_{ENABLE} = 0\text{ V to }V_{CC}$	-	$\pm 0.1$	$\pm 1$	$\mu\text{A}$
$t_{en}$	enable time		[2] -	110	-	$\mu\text{s}$
$t_{idle(READY)}$	bus idle time to READY active		[1] 50	105	200	$\mu\text{s}$
$t_{dis(EN-RDY)}$	disable time (ENABLE to READY)		-	30	-	ns
$t_{stp(READY)}$	SDAIN to READY delay after STOP		[3] -	1.2	-	$\mu\text{s}$
$t_{READY}$	SCLOUT/SDAOUT to READY		[3] -	0.8	-	$\mu\text{s}$
$I_{LZ(READY)}$	off-state leakage current on pin READY	$V_{ENABLE} = V_{CC}$	-	$\pm 0.3$	-	$\mu\text{A}$
$C_{i(ENABLE)}$	input capacitance on pin ENABLE	$V_I = V_{CC}$ or GND	[4] -	1.9	4.0	pF
$C_{o(READY)}$	output capacitance on pin READY	$V_I = V_{CC}$ or GND	[4] -	2.5	4.0	pF
$V_{OL(READY)}$	LOW-state output voltage on pin READY	$I_{pu} = 3\text{ mA}; V_{ENABLE} = V_{CC}$	[1] -	-	0.4	V
<b>Rise time accelerators</b>						
$I_{trt(pu)}$	transient boosted pull-up current	positive transition on SDA, SCL; $V_{CC} = 2.7\text{ V};$ slew rate = $1.25\text{ V}/\mu\text{s}$	[5] 1	2	-	mA

**Table 5: Characteristics ...continued** $V_{CC} = 2.7\text{ V to }5.5\text{ V}$ ;  $T_{amb} = -40\text{ °C to }+85\text{ V}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Input-output connection</b>						
$V_{\text{offset}}$	offset voltage	10 k $\Omega$ to $V_{CC}$ on SDA, SCL; $V_{CC} = 3.3\text{ V}$	[1] [6] [8] 0	110	175	mV
$t_{\text{PLH}}$	LOW-to-HIGH propagation delay (SCL to SCL and SDA to SDA)	10 k $\Omega$ to $V_{CC}$ ; $C_L = 100\text{ pF}$ each side	-	0	-	ns
$t_{\text{PHL}}$	HIGH-to-LOW propagation delay (SCL to SCL and SDA to SDA)	10 k $\Omega$ to $V_{CC}$ ; $C_L = 100\text{ pF}$ each side	-	70	-	ns
$C_{i(\text{SCL/SDA})}$	SCL and SDA input capacitance		[4] -	5	7	pF
$V_{\text{OL}}$	LOW-state output voltage	$V_I = 0\text{ V}$ ; SDAn, SCLn pins; $I_{\text{sink}} = 3\text{ mA}$ ; $V_{CC} = 2.7\text{ V}$	[1] 0	-	0.4	V
$I_{\text{LI}}$	input leakage current	SDAn, SCLn pins; $V_{CC} = 5.5\text{ V}$	-1	-	+1	$\mu\text{A}$
<b>System characteristics</b>						
$f_{\text{SCL}}$	SCL clock frequency		[4] 0	-	400	kHz
$t_{\text{BUF}}$	bus free time between STOP and START condition		[4] 1.3	-	-	$\mu\text{s}$
$t_{\text{HD;STA}}$	START condition hold time		[4] 0.6	-	-	$\mu\text{s}$
$t_{\text{SU;STA}}$	START condition set-up time		[4] 0.6	-	-	$\mu\text{s}$
$t_{\text{SU;STO}}$	STOP condition set-up time		[4] 0.6	-	-	$\mu\text{s}$
$t_{\text{HD;DAT}}$	data hold time		[4] 300	-	-	ns
$t_{\text{SU;DAT}}$	data setup time		[4] 100	-	-	ns
$t_{\text{LOW}}$	SCL LOW time		[4] 1.3	-	-	$\mu\text{s}$
$t_{\text{HIGH}}$	SCL HIGH time		[4] 0.6	-	-	$\mu\text{s}$
$t_f$	fall time SDA and SCL		[4] [7] $20 + 0.1 \times C_b$	-	300	ns
$t_r$	rise time SDA and SCL		[4] [7] $20 + 0.1 \times C_b$	-	300	ns

[1] This specification applies over the full operating temperature range.

[2] The enable time can slow considerably for some parts when temperature is  $< -20\text{ °C}$ .

[3] Delays that can occur after ENABLE and/or idle times have passed.

[4] Guaranteed by design, not production tested.

[5]  $I_{\text{trt(pu)}}$  varies with temperature and  $V_{CC}$  voltage, as shown in [Section 11.1 "Typical performance characteristics"](#).

[6] The connection circuitry always regulates its output to a higher voltage than its input. The magnitude of this offset voltage as a function of the pull-up resistor and  $V_{CC}$  voltage is shown in [Section 11.1 "Typical performance characteristics"](#).

[7]  $C_b$  = total capacitance of one bus line in pF.

[8] Force  $V_{\text{SDAIN}} = V_{\text{SCLIN}} = 0.1\text{ V}$ , tie SDAOUT and SCLOUT through 10 k $\Omega$  resistor to  $V_{CC}$  and measure the SDAOUT and SCLOUT output.

11.1 Typical performance characteristics

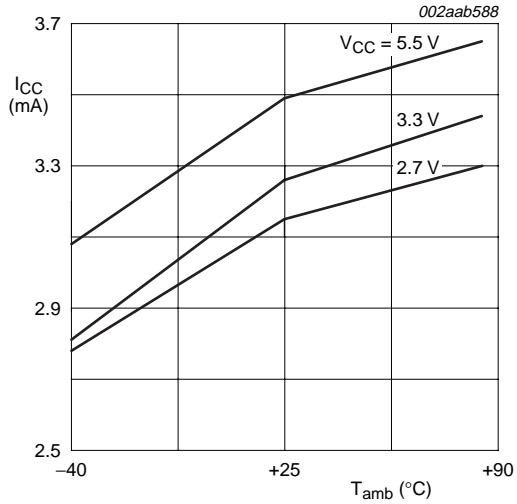


Fig 12. I<sub>CC</sub> versus temperature

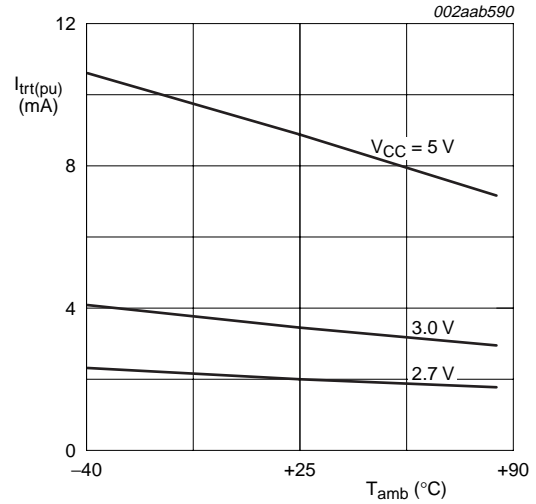
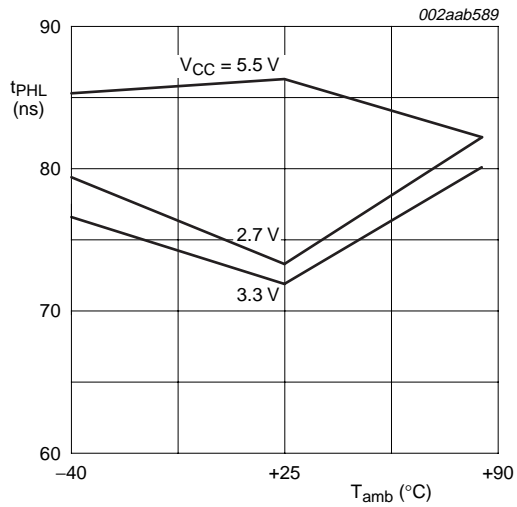


Fig 13. I<sub>trt(pu)</sub> versus temperature



C<sub>i</sub> = C<sub>o</sub> > 100 pF; R<sub>PU(in)</sub> = R<sub>PU(out)</sub> = 10 kΩ

Fig 14. Input/output t<sub>PHL</sub> versus temperature

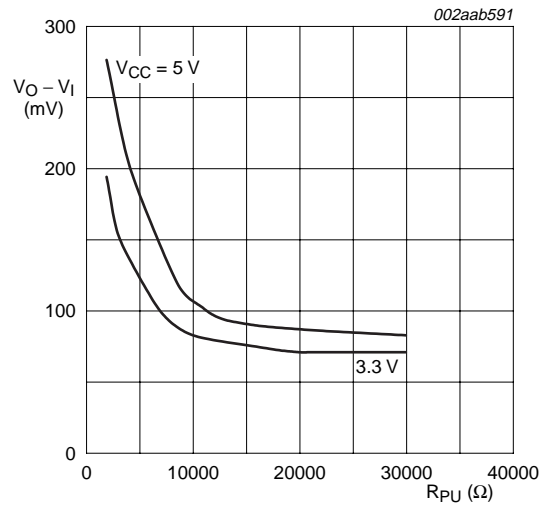
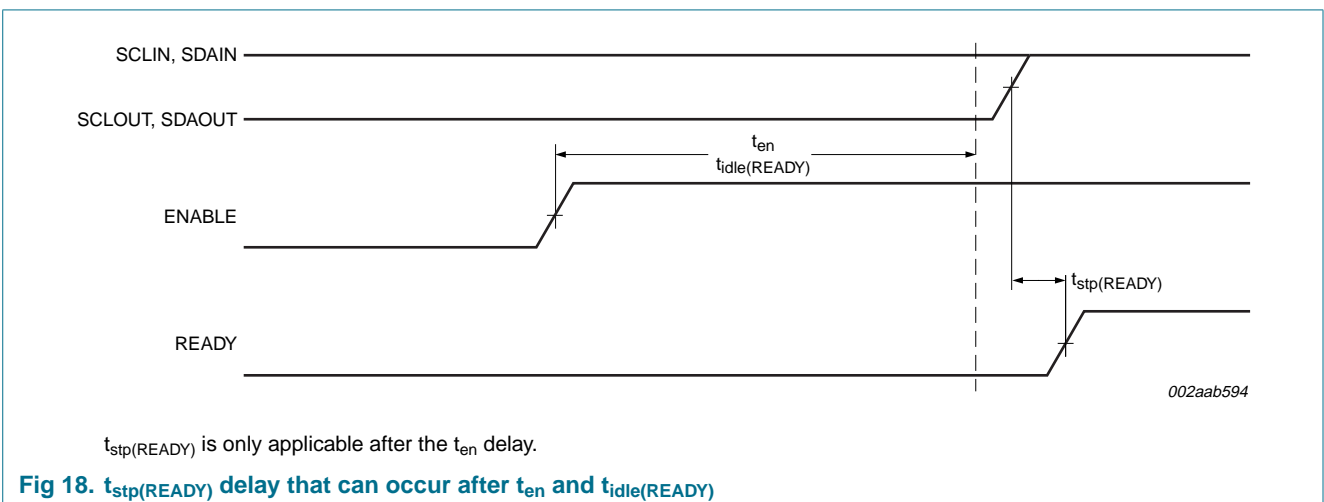
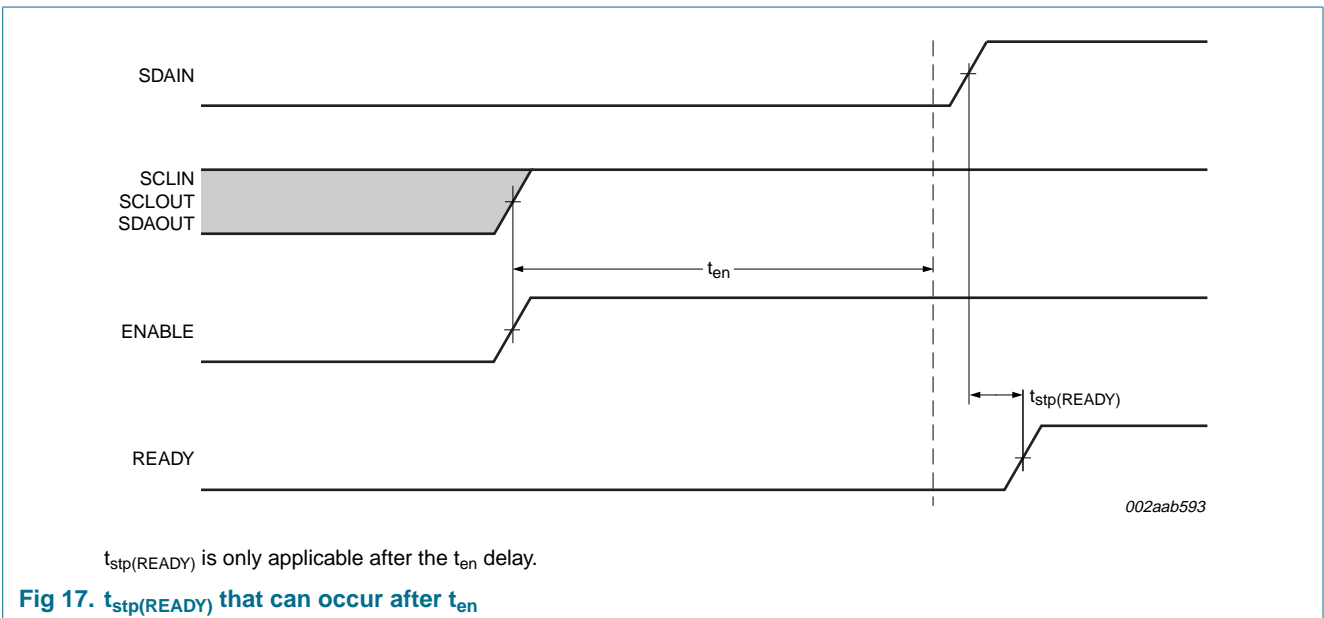
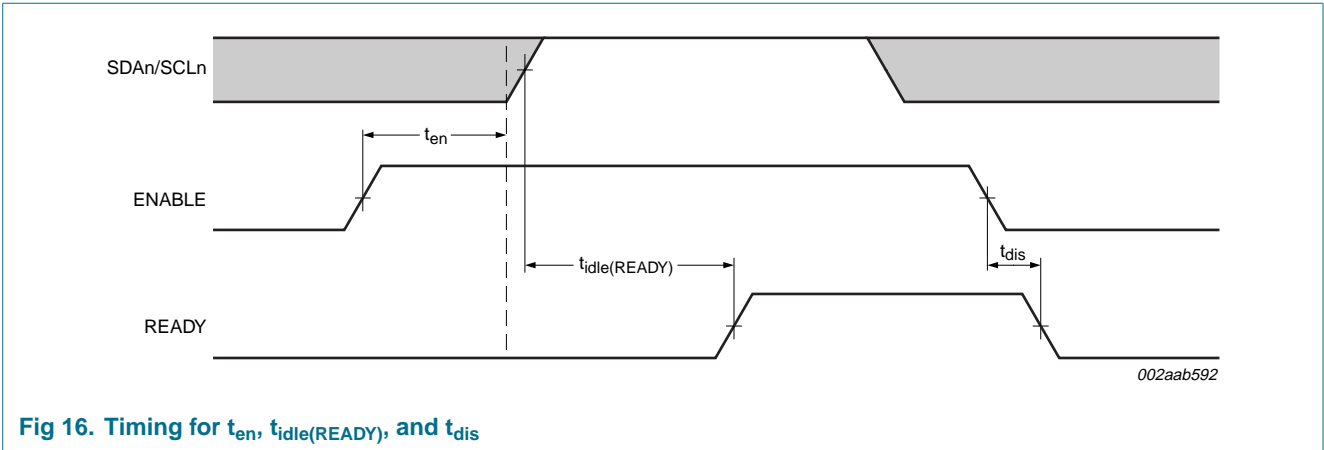
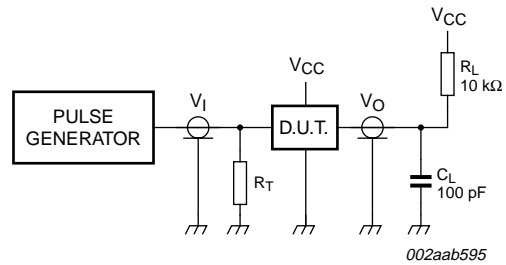


Fig 15. Connection circuitry V<sub>O</sub> - V<sub>I</sub>

11.2 Timing diagrams



## 12. Test information



$R_L$  = load resistor

$C_L$  = load capacitance includes jig and probe capacitance

$R_T$  = termination resistance should be equal to the output impedance  $Z_0$  of the pulse generators.

**Fig 19. Test circuitry for switching times**



13. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

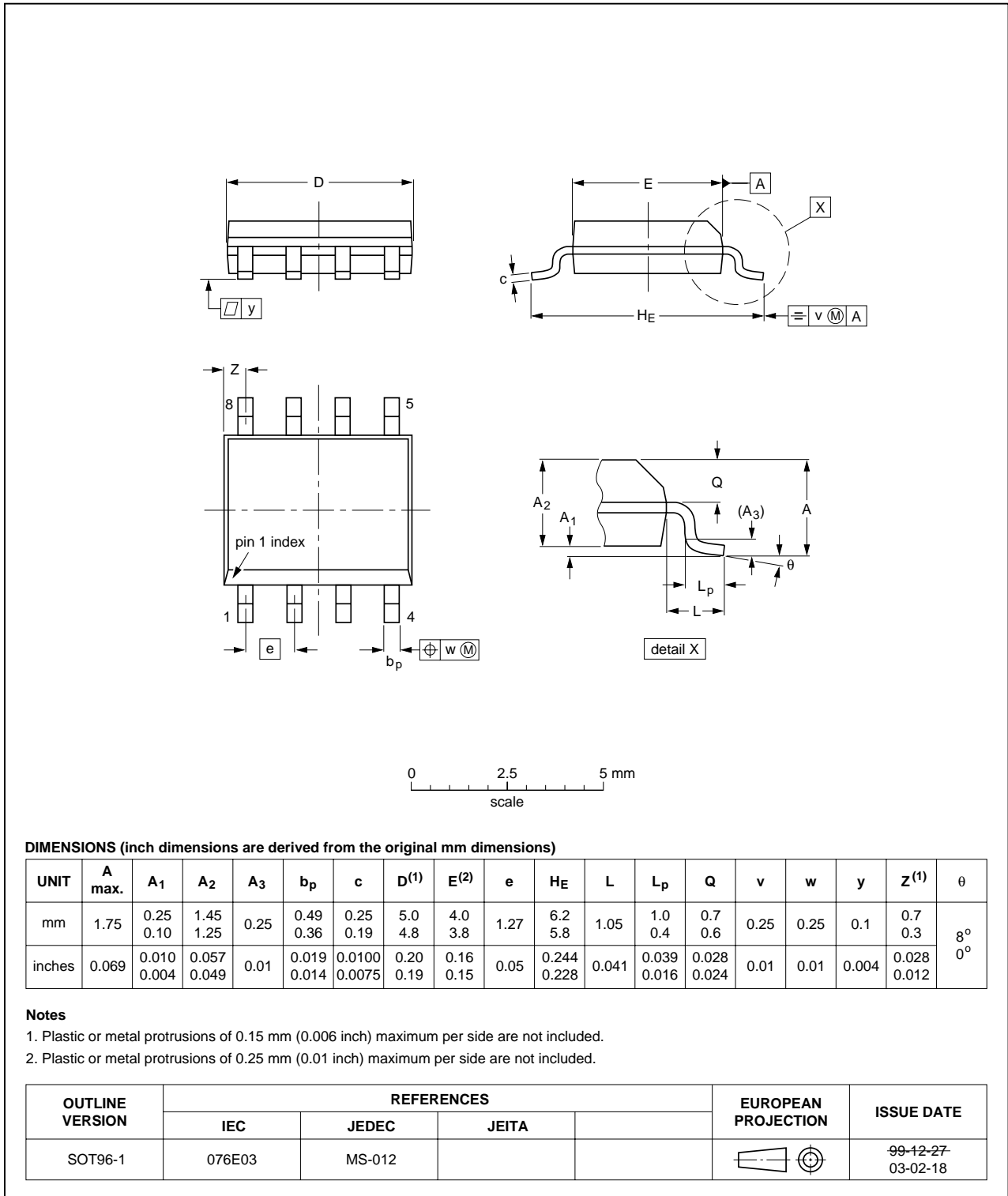


Fig 20. Package outline SOT96-1 (SO8)

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm

SOT505-1

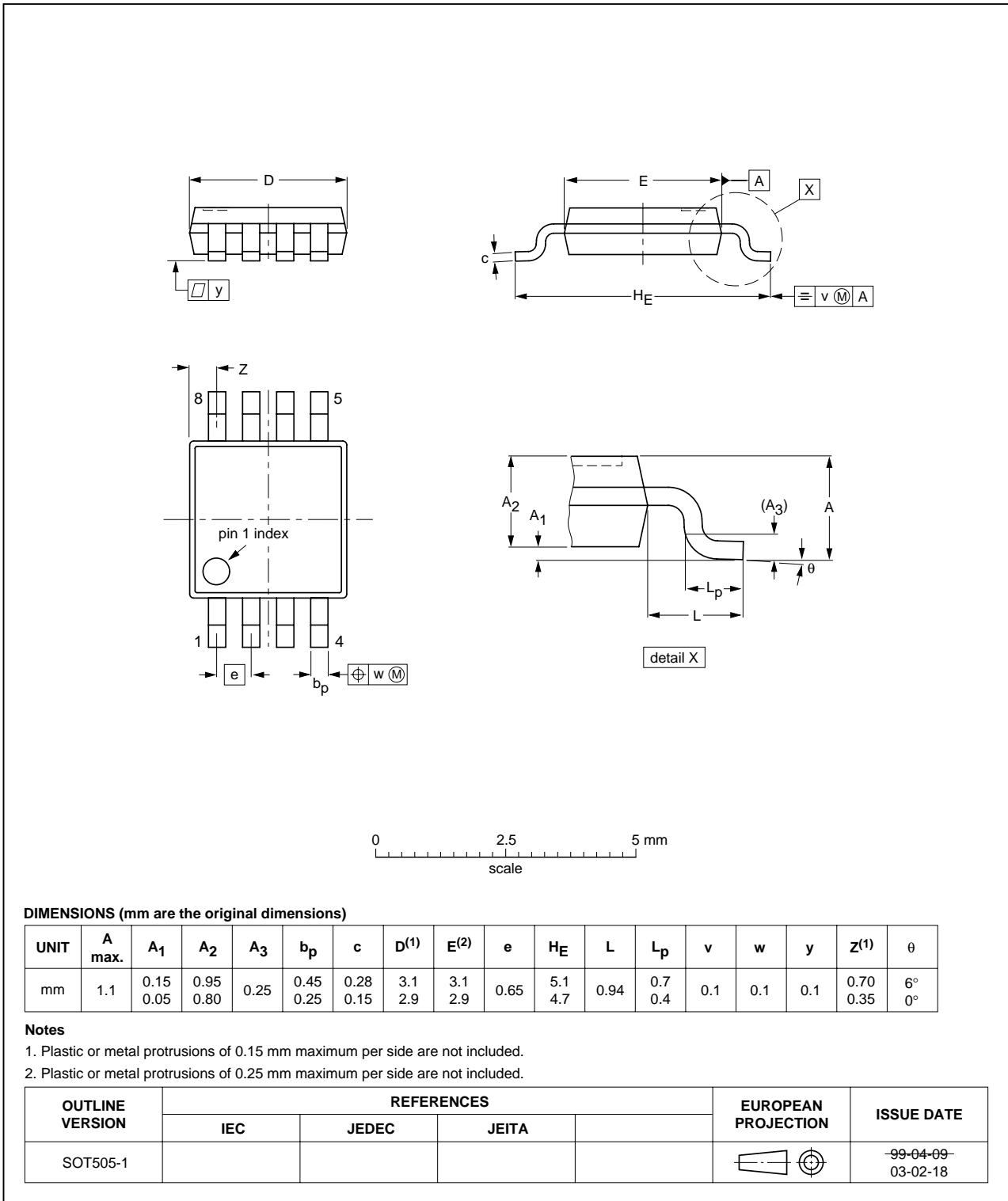


Fig 21. Package outline SOT505-1 (TSSOP8)

## 14. Soldering

### 14.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

### 14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness  $\geq 2.5$  mm
  - for packages with a thickness  $< 2.5$  mm and a volume  $\geq 350$  mm<sup>3</sup> so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness  $< 2.5$  mm and a volume  $< 350$  mm<sup>3</sup> so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

### 14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

- smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### 14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

#### 14.5 Package related soldering information

Table 6: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	Soldering method	
	Wave	Reflow [2]
BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
CWQCCN..L [8], PMFP [9], WQCCN..L [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the (LF)BGA Application Note (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

- [4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
- [5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- [6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- [7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
- [8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.
- [9] Hot bar soldering or manual soldering is suitable for PMFP packages.

## 15. Abbreviations

**Table 7: Abbreviations**

Acronym	Description
AdvancedTCA	Advanced Telecommunications Computing Architecture
CDM	Charged Device Model
cPCI	compact Peripheral Component Interface
ESD	Electrostatic Discharge
HBM	Human Body Model
I <sup>2</sup> C-bus	Inter IC bus
MM	Machine Model
PCI	Peripheral Component Interface
PICMG	PCI Industrial Computer Manufacturers Group
SMBus	System Management Bus
VME	VERSAModule Eurocard

## 16. Revision history

**Table 8: Revision history**

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PCA9511A_1	20050815	Product data sheet	-	9397 750 13269	-

## 17. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2] [3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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