

# DATA SHEET



## **PCA9537**

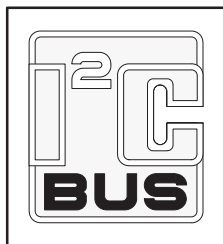
4-bit I<sup>2</sup>C-bus and SMBus low power  
I/O port with interrupt and reset

Product data sheet  
Supersedes data of 2004 Nov 29

2006 Sep 21

## 4-bit I<sup>2</sup>C-bus and SMBus low power I/O port with interrupt and reset

PCA9537



### FEATURES

- 4-bit I<sup>2</sup>C GPIO with interrupt and reset
- Operating power supply voltage range of 2.3 to 5.5 V
- 5 V tolerant I/Os
- Polarity inversion register
- Active LOW interrupt output
- Active LOW reset input
- Low stand-by current
- Noise filter on SCL/SDA inputs
- No glitch on power-up
- Internal power-on reset
- 4 I/O pins which default to 4 inputs
- 0 kHz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Offered in TSSOP10 package

### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DRAWING NUMBER
10-Pin Plastic TSSOP	-40 °C to +85 °C	PCA9537DP	9537	SOT552-1

Standard packing quantities and other packing data are available at [www.standardics.philips.com/packaging](http://www.standardics.philips.com/packaging). SMBus as specified by the Smart Battery System Implementers Forum is a derivative of the Philips I<sup>2</sup>C patent.

### DESCRIPTION

The PCA9537 is a 10-pin CMOS device that provide 4 bits of General Purpose parallel Input/Output (GPIO) expansion with interrupt and reset for I<sup>2</sup>C/SMBus applications and was developed to enhance the Philips family of I<sup>2</sup>C I/O expanders. I/O expanders provides a simple solution when additional I/O is needed for ACPI power switches, sensors, pushbuttons, LEDs, fans, etc.

The PCA9537 consists of a 4-bit Configuration register (Input or Output selection); 4-bit Input register, 4-bit Output register and a 4-bit Polarity inversion register (Active-HIGH or Active-LOW operation). The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each Input or Output is kept in the corresponding Input or Output register. The polarity of the input port register can be inverted with the Polarity Inversion Register. All registers can be read by the system master.

The PCA9537 open-drain interrupt output is activated when any input state differs from its corresponding input port register state and is used to indicate to the system master that an input state has changed. The power-on reset sets the registers to their default values and initializes the device state machine. The  $\overline{\text{RESET}}$  pin causes the same reset/initialization to occur without depowering the device.

The I<sup>2</sup>C address is fixed and allows only one device on the same I<sup>2</sup>C/SMBus.

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## PIN CONFIGURATION

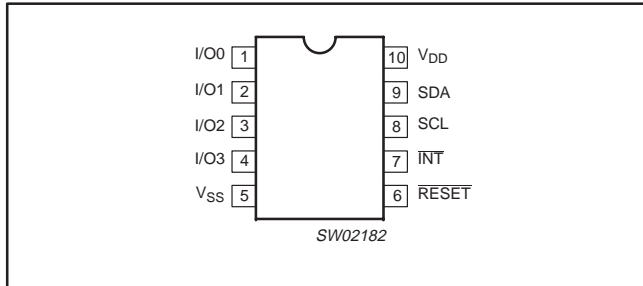


Figure 1. Pin configuration

## PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1–4	I/O0–3	I/O0 to I/O3
5	V <sub>SS</sub>	Supply ground
6	RESET	Active LOW reset input
7	INT	Interrupt output (open drain)
8	SCL	Serial clock line
9	SDA	Serial data line
10	V <sub>DD</sub>	Supply voltage

## BLOCK DIAGRAM

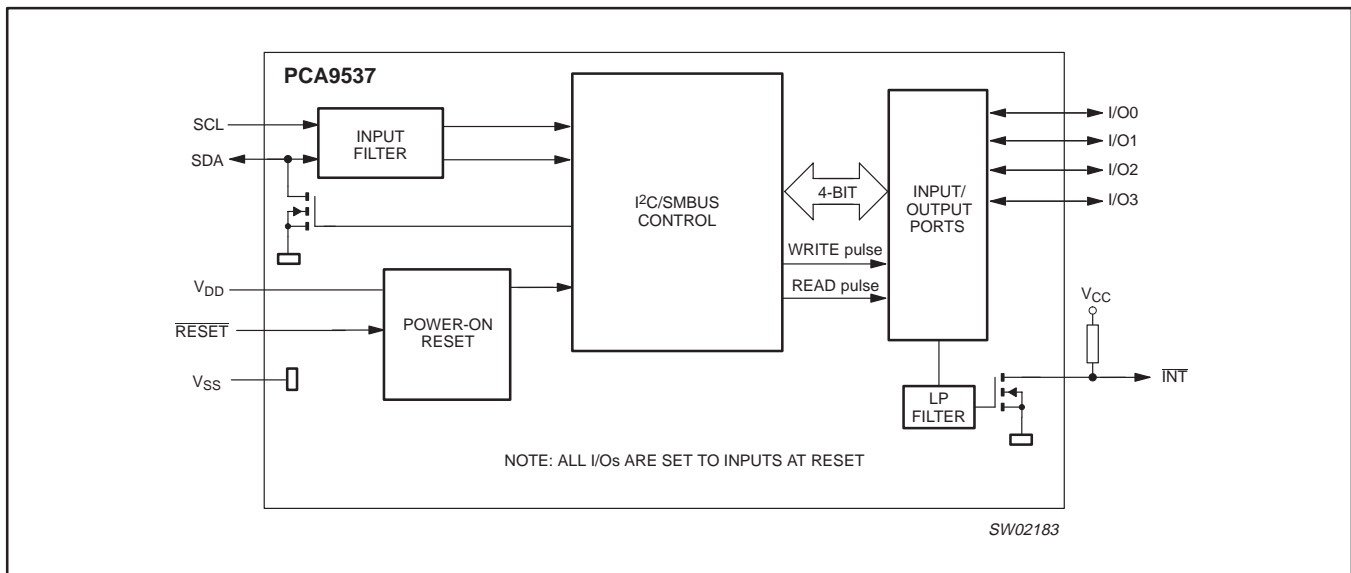


Figure 2. Block diagram

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## REGISTERS

### Command Byte

Command	Protocol	Function
0	Read byte	Input port register
1	Read/write byte	Output port register
2	Read/write byte	Polarity inversion register
3	Read/write byte	Configuration register

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

### Register 0 – Input Port Register

bit	I7	I6	I5	I4	I3	I2	I1	I0
	not used							
default	1	1	1	1	X	X	X	X

This register is a read only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writes to this register have no effect.

The default value 'X' is determined by the externally applied logic level.

### Register 1 – Output Port Register

bit	O7	O6	O5	O4	O3	O2	O1	O0
	not used							
default	1	1	1	1	1	1	1	1

This register reflects the outgoing logic levels of the pins defined as outputs by Register 3. Bit values in this register have no effect on pins defined as inputs. Reads from this register return the value that is in the flip-flop controlling the output selection, NOT the actual pin value.

### Register 2 – Polarity Inversion Register

bit	N7	N6	N5	N4	N3	N2	N1	N0
	not used							
default	0	0	0	0	0	0	0	0

This register allows the user to invert the polarity of the Input Port Register data. If a bit in this register is set (written with '1'), the corresponding Input Port data is inverted. If a bit in this register is cleared (written with a '0'), the Input Port data polarity is retained.

### Register 3 – Configuration Register

bit	C7	C6	C5	C4	C3	C2	C1	C0
	not used							
default	1	1	1	1	1	1	1	1

This register configures the directions of the I/O pins. If a bit in this register is set, the corresponding port pin is enabled as an input with high impedance output driver. If a bit in this register is cleared, the corresponding port pin is enabled as an output. At reset, the I/Os are configured as inputs.

### Power-on Reset

When power is applied to V<sub>DD</sub>, an internal power-on reset holds the PCA9537 in a reset condition until V<sub>DD</sub> has reached V<sub>POR</sub>. At that point, the reset condition is released and the PCA9537 registers and state machine will initialize to their default states. Thereafter, V<sub>DD</sub> must be lowered below 0.2 V to reset the device.

For a power reset cycle, V<sub>DD</sub> must be lowered below 0.2 V and then restored to the operating voltage.

### RESET Input

A reset can be accomplished by holding the RESET pin LOW for a minimum of t<sub>W</sub>. The PCA9537 registers and SMBus/I<sup>2</sup>C state machine will be held in their default state until the RESET input is once again HIGH. This input requires a pull-up resistor to V<sub>DD</sub> if no active connection is used.

### Interrupt Output

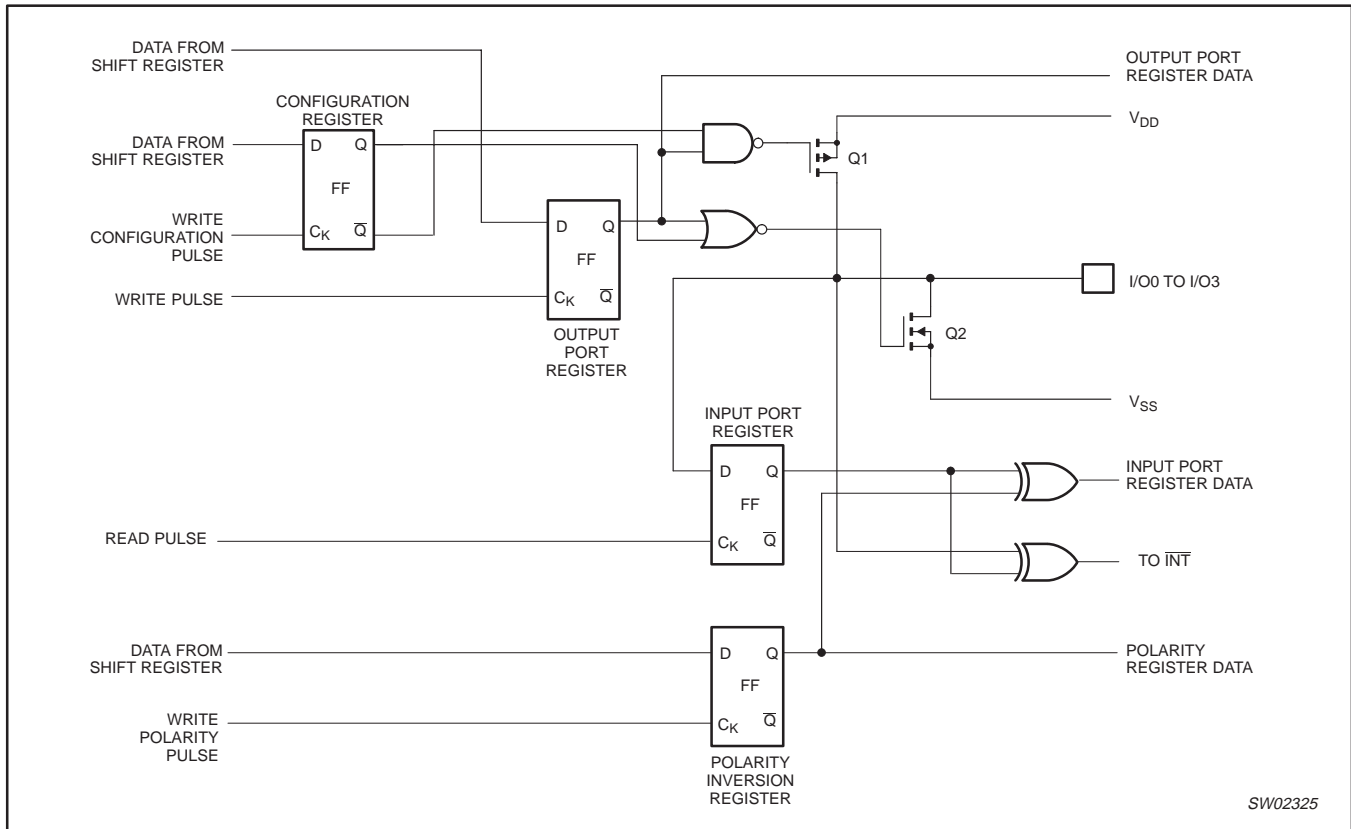
The open-drain interrupt output is activated when one of the port pins change state and the pin is configured as an input. The interrupt is deactivated when the input returns to its previous state or the input port register is read.

Note that changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the input port register.

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## SIMPLIFIED SCHEMATIC OF I/O0 TO I/O3



**NOTE:** At Power-on Reset, all registers return to default values.

**Figure 3. Simplified schematic of I/O0 to I/O3**

### I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input. The input voltage may be raised above V<sub>DD</sub> to a maximum of 5.5 V.

If the I/O is configured as an output, then either Q1 or Q2 is enabled, depending on the state of the output port register. Care should be exercised if an external voltage is applied to an I/O configured as an output because of the low-impedance paths that exist between the pin and either V<sub>DD</sub> or V<sub>SS</sub>.

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## Device address

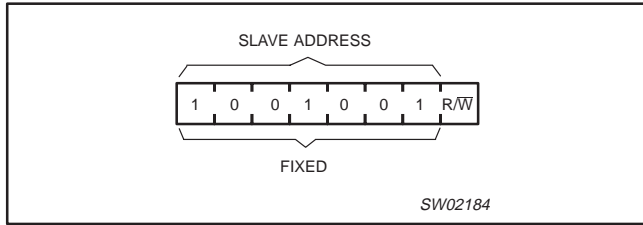


Figure 4. PCA9537 address

## Bus transactions

Data is transmitted to the PCA9537 registers using the write mode as shown in Figures 5 and 6. Data is read from the PCA9537 registers using the read mode as shown in Figures 7 and 8. These devices do not implement an auto-increment function so once a command byte has been sent, the register which was addressed will continue to be accessed by reads until a new command byte has been sent.

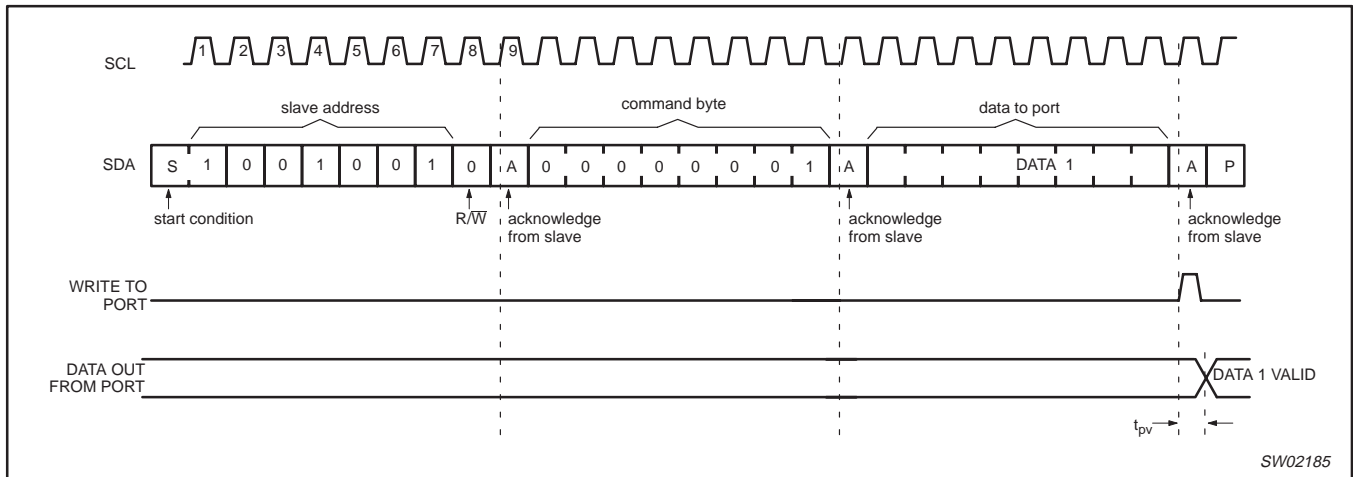


Figure 5. WRITE to output port register

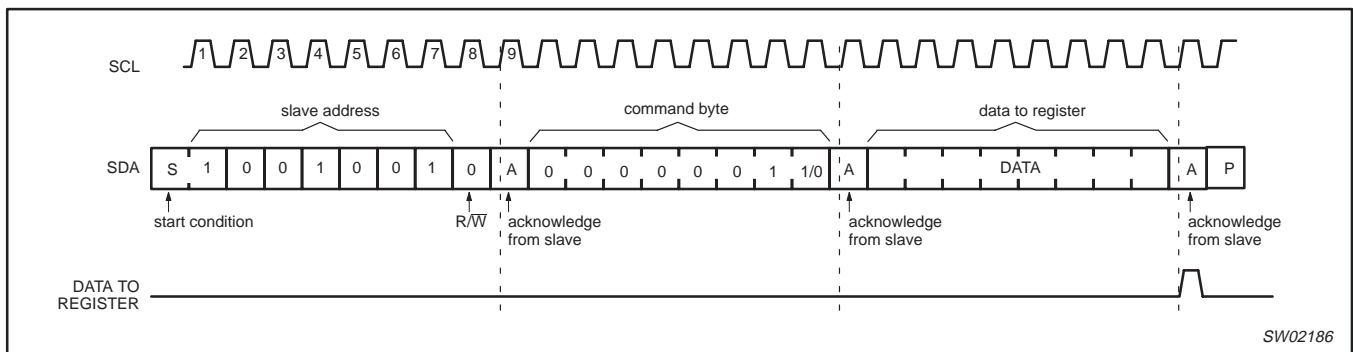


Figure 6. WRITE to configuration or polarity inversion registers

Expanded diagram found on page 13, Figure 16.

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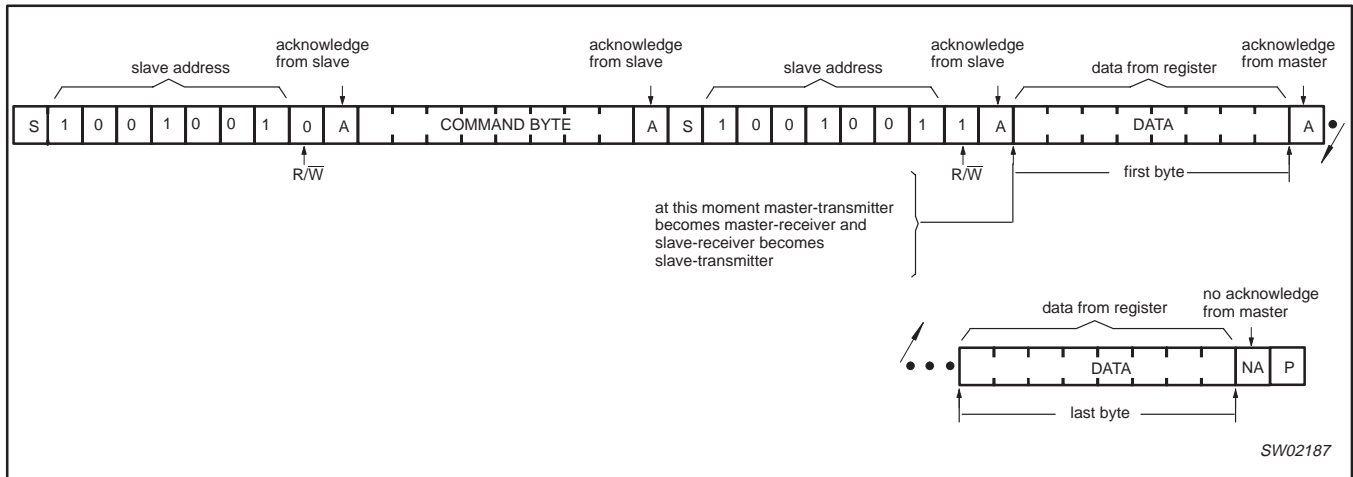
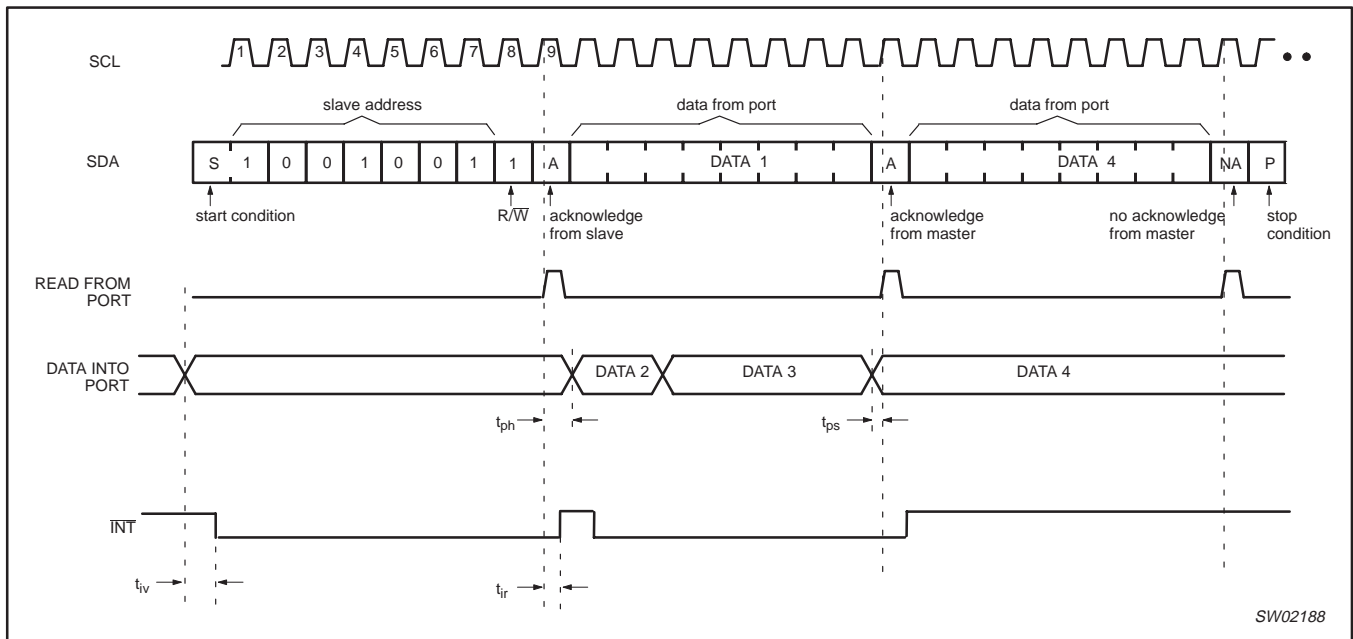


Figure 7. READ from register



**NOTES:**

1. This figure assumes the command byte has previously been programmed with 00h.
2. Transfer of data can be stopped at any moment by a stop condition.

Figure 8. READ input port register

Expanded diagram found on page 13, Figure 15.

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## TYPICAL APPLICATION

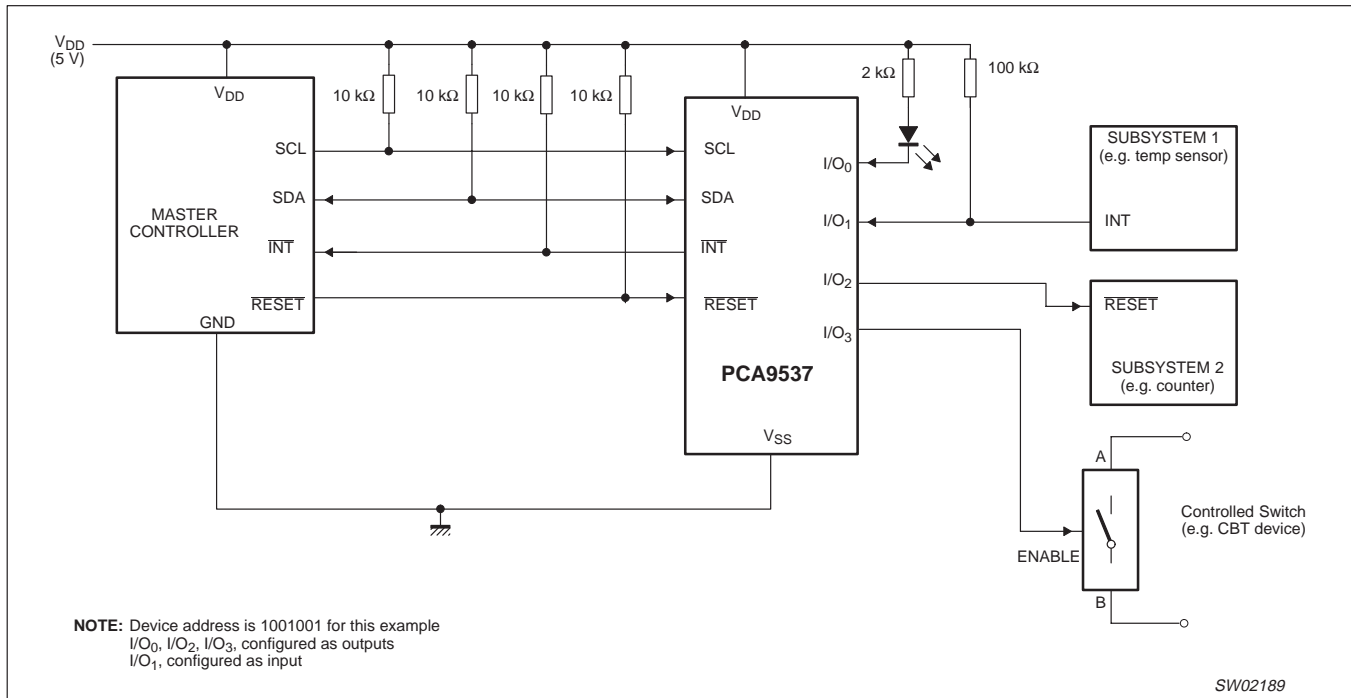


Figure 9. Typical application

### Minimizing I<sub>DD</sub> when the I/O is used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to V<sub>DD</sub> through a resistor as shown in Figure 9. Since the LED acts as a diode, when the LED is off the I/O V<sub>IN</sub> is about 1.2 V less than V<sub>DD</sub>. The supply current, I<sub>DD</sub>, increases as V<sub>IN</sub> becomes lower than V<sub>DD</sub> and is specified as ΔI<sub>DD</sub> in the DC characteristics table.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V<sub>DD</sub> when the LED is off. Figure 10 shows a high value resistor in parallel with the LED. Figure 11 shows V<sub>DD</sub> less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V<sub>IN</sub> at or above V<sub>DD</sub> and prevents additional supply current consumption when the LED is off.

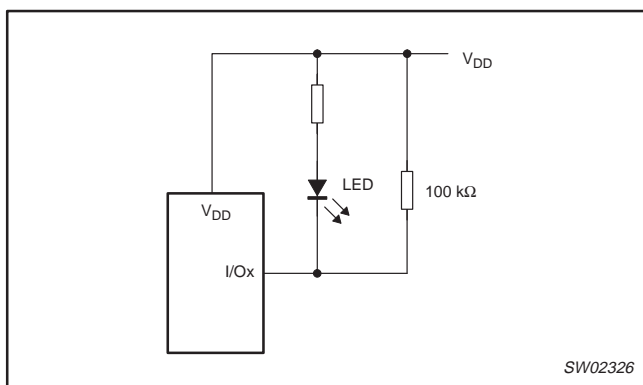


Figure 10. High value resistor in parallel with the LED

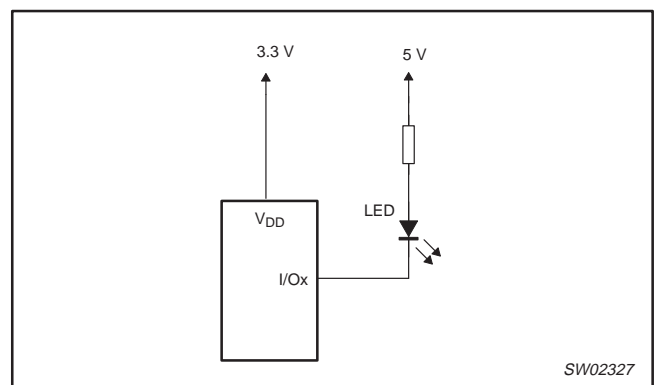


Figure 11. Device supplied by a lower voltage



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## ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V <sub>DD</sub>	Supply voltage		-0.5	6.0	V
I <sub>I</sub>	DC input current		—	±20	mA
V <sub>I/O</sub>	DC voltage on an I/O		V <sub>SS</sub> - 0.5	5.5	V
I <sub>I/O</sub>	DC output current on an I/O		—	±50	mA
I <sub>DD</sub>	Supply current		—	85	mA
I <sub>SS</sub>	Supply current		—	100	mA
P <sub>tot</sub>	Total power dissipation		—	200	mW
T <sub>stg</sub>	Storage temperature range		-65	+150	°C
T <sub>amb</sub>	Operating ambient temperature		-40	+85	°C
T <sub>J(MAX)</sub>	Maximum junction temperature		—	+125	°C

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## HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC24 under "Handling MOS devices".

## DC CHARACTERISTICS

$V_{DD} = 2.3$  to  $5.5$  V;  $V_{SS} = 0$  V;  $T_{amb} = -40$  °C to  $+85$  °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
<b>Supplies</b>						
$V_{DD}$	Supply voltage		2.3	—	5.5	V
$I_{DD}$	Supply current	Operating mode; $V_{DD} = 5.5$ V; no load; $f_{SCL} = 100$ kHz	—	104	175	$\mu$ A
$I_{stbl}$	Standby current	Standby mode; $V_{DD} = 5.5$ V; no load; $V_I = V_{SS}$ ; $f_{SCL} = 0$ kHz; I/O = inputs	—	0.25	1	$\mu$ A
$I_{stbh}$	Standby current	Standby mode; $V_{DD} = 5.5$ V; no load; $V_I = V_{DD}$ ; $f_{SCL} = 0$ kHz; I/O = inputs	—	0.25	1	$\mu$ A
$V_{POR}$	Power-on reset voltage (Note 1)	No load; $V_I = V_{DD}$ or $V_{SS}$	—	1.5	1.65	V
<b>Input SCL; input/output SDA</b>						
$V_{IL}$	LOW-level input voltage		-0.5	—	$0.3V_{DD}$	V
$V_{IH}$	HIGH-level input voltage		$0.7V_{DD}$	—	5.5	V
$I_{OL}$	LOW-level output current	$V_{OL} = 0.4$ V	3	7	—	mA
$I_L$	Leakage current	$V_I = V_{DD} = V_{SS}$	-1	—	+1	$\mu$ A
$C_I$	Input capacitance	$V_I = V_{SS}$	—	5	10	pF
<b>I/Os</b>						
$V_{IL}$	LOW-level input voltage		-0.5	—	0.8	V
$V_{IH}$	HIGH-level input voltage		2.0	—	5.5	V
$I_{OL}$	LOW-level output current	$V_{OL} = 0.5$ V; $V_{DD} = 2.3$ V; Note 2	8	10	—	mA
		$V_{OL} = 0.7$ V; $V_{DD} = 2.3$ V; Note 2	10	13	—	mA
		$V_{OL} = 0.5$ V; $V_{DD} = 4.5$ V; Note 2	8	17	—	mA
		$V_{OL} = 0.7$ V; $V_{DD} = 4.5$ V; Note 2	10	24	—	mA
		$V_{OL} = 0.5$ V; $V_{DD} = 3.0$ V; Note 2	8	14	—	mA
		$V_{OL} = 0.7$ V; $V_{DD} = 3.0$ V; Note 2	10	19	—	mA
$V_{OH}$	HIGH-level output voltage	$I_{OH} = -8$ mA; $V_{DD} = 2.3$ V; Note 3	1.8	—	—	V
		$I_{OH} = -10$ mA; $V_{DD} = 2.3$ V; Note 3	1.7	—	—	V
		$I_{OH} = -8$ mA; $V_{DD} = 3.0$ V; Note 3	2.6	—	—	V
		$I_{OH} = -10$ mA; $V_{DD} = 3.0$ V; Note 3	2.5	—	—	V
		$I_{OH} = -8$ mA; $V_{DD} = 4.5$ V; Note 3	4.1	—	—	V
		$I_{OH} = -10$ mA; $V_{DD} = 4.5$ V; Note 3	4.0	—	—	V
$I_L$	Leakage current	$V_I = V_{DD} = V_{SS}$	-1	—	1	$\mu$ A
$C_I$	Input capacitance		—	5	10	pF
<b>Interrupt INT</b>						
$I_{OL}$	LOW-level output current	$V_{OL} = 0.4$ V	3	13	—	mA
$I_{OH}$	HIGH-level output current	$V_{OL} = 0.4$ V	-1	—	+1	$\mu$ A
<b>Select Input RESET</b>						
$V_{IL}$	LOW-level input voltage		-0.5	—	0.8	V
$V_{IH}$	HIGH-level input voltage		2.0	—	5.5	V
$I_L$	Leakage current	$V_I = V_{DD} = V_{SS}$	-1	—	1	$\mu$ A

### NOTES:

- $V_{DD}$  must be lowered to 0.2 V in order to reset part.
- Each I/O must be externally limited to a maximum of 25 mA and the device must be limited to a maximum current of 100 mA.
- The total current sourced by all I/Os must be limited to 85 mA.

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## AC SPECIFICATIONS

SYMBOL	PARAMETER	STANDARD MODE I <sup>2</sup> C-bus		FAST MODE I <sup>2</sup> C-bus		UNITS
		MIN	MAX	MIN	MAX	
f <sub>SCL</sub>	Operating frequency	0	100	0	400	kHz
t <sub>BUF</sub>	Bus free time between STOP and START conditions	4.7	—	1.3	—	μs
t <sub>HD;STA</sub>	Hold time after (repeated) START condition	4.0	—	0.6	—	μs
t <sub>SU;STA</sub>	Repeated START condition setup time	4.7	—	0.6	—	μs
t <sub>SU;STO</sub>	Setup time for STOP condition	4.0	—	0.6	—	μs
t <sub>HD;DAT</sub>	Data in hold time	0	—	0	—	ns
t <sub>VD;ACK</sub>	Valid time for ACK condition <sup>2</sup>	0.3	3.45	0.1	0.9	μs
t <sub>VD;DAT</sub>	Data out valid time <sup>3</sup>	300	—	50	—	ns
t <sub>SU;DAT</sub>	Data setup time	250	—	100	—	ns
t <sub>LOW</sub>	Clock LOW period	4.7	—	1.3	—	μs
t <sub>HIGH</sub>	Clock HIGH period	4.0	—	0.6	—	μs
t <sub>F</sub>	Clock/Data fall time	—	300	20 + 0.1 C <sub>b</sub> <sup>1</sup>	300	ns
t <sub>R</sub>	Clock/Data rise time	—	1000	20 + 0.1 C <sub>b</sub> <sup>1</sup>	300	ns
t <sub>SP</sub>	Pulse width of spikes that must be suppressed by the input filters	—	50	—	50	ns
<b>Port Timing</b>						
t <sub>PV</sub>	Output data valid	—	200	—	200	ns
t <sub>PS</sub>	Input data setup time	100	—	100	—	ns
t <sub>PH</sub>	Input data hold time	1	—	1	—	μs
<b>Interrupt Timing</b>						
t <sub>IV</sub>	Interrupt valid	—	4	—	4	μs
t <sub>IR</sub>	Interrupt reset	—	4	—	4	μs
<b>RESET</b>						
t <sub>W</sub>	Reset pulse width	4	—	4	—	ns
t <sub>REC</sub>	Reset recovery time	0	—	0	—	ns
t <sub>RESET</sub>	Time to reset	400	—	400	—	ns

**NOTES:**

1. C<sub>b</sub> = total capacitance of one bus line in pF.
2. t<sub>VD;ACK</sub> = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.
3. t<sub>VD;DAT</sub> = minimum time for SDA data out to be valid following SCL LOW.

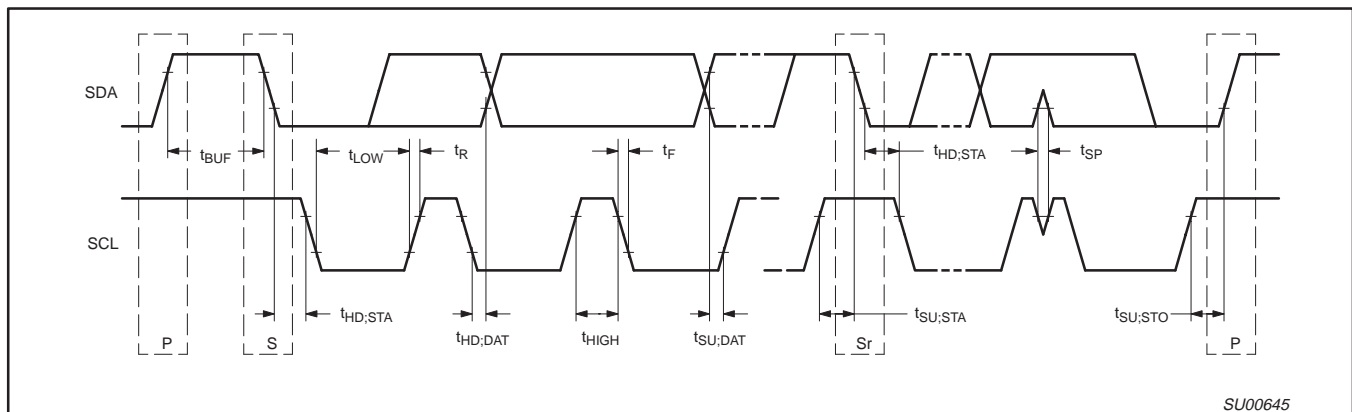


Figure 12. Definition of timing

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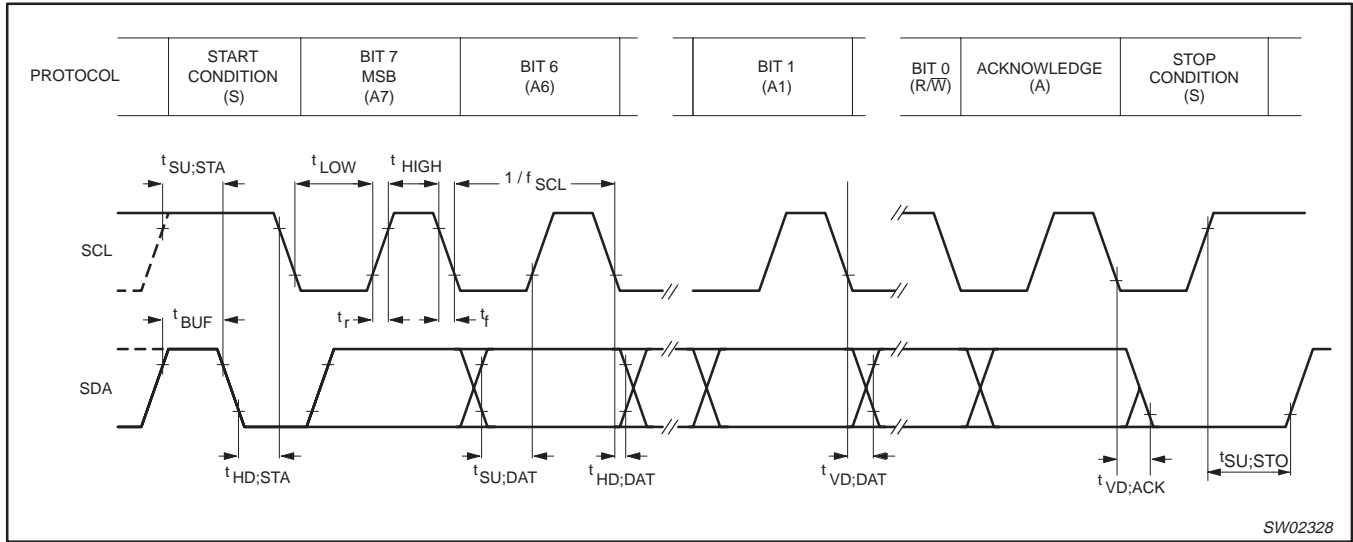


Figure 13. I<sup>2</sup>C-bus timing diagram; rise and fall times refer to  $V_{IL}$  and  $V_{IH}$

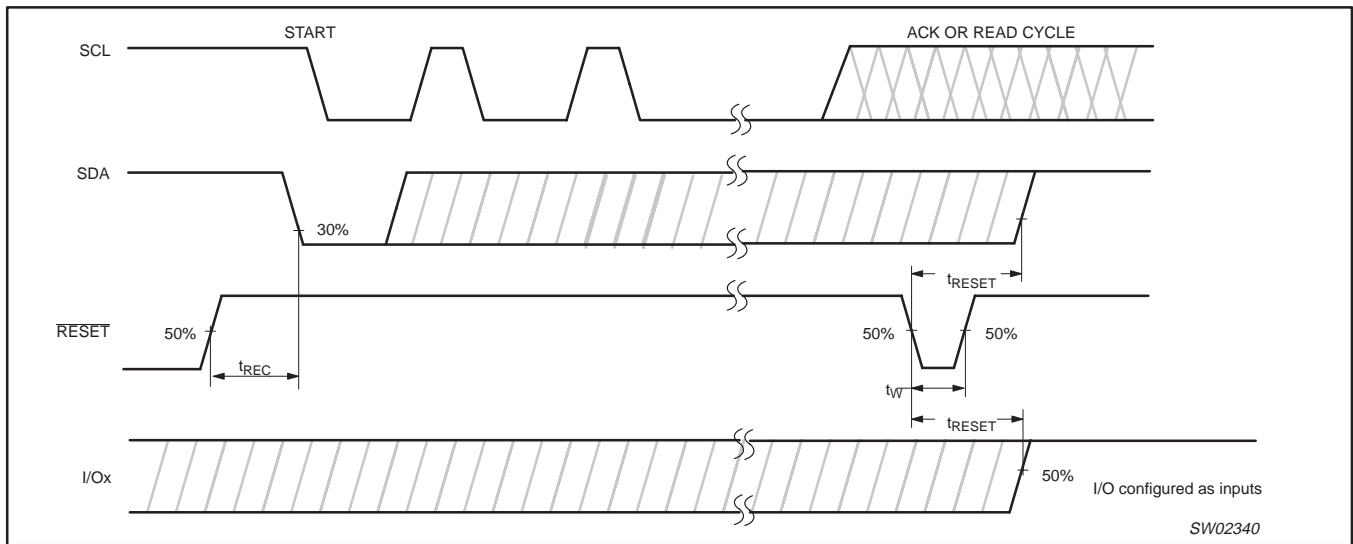


Figure 14. Definition of RESET timing

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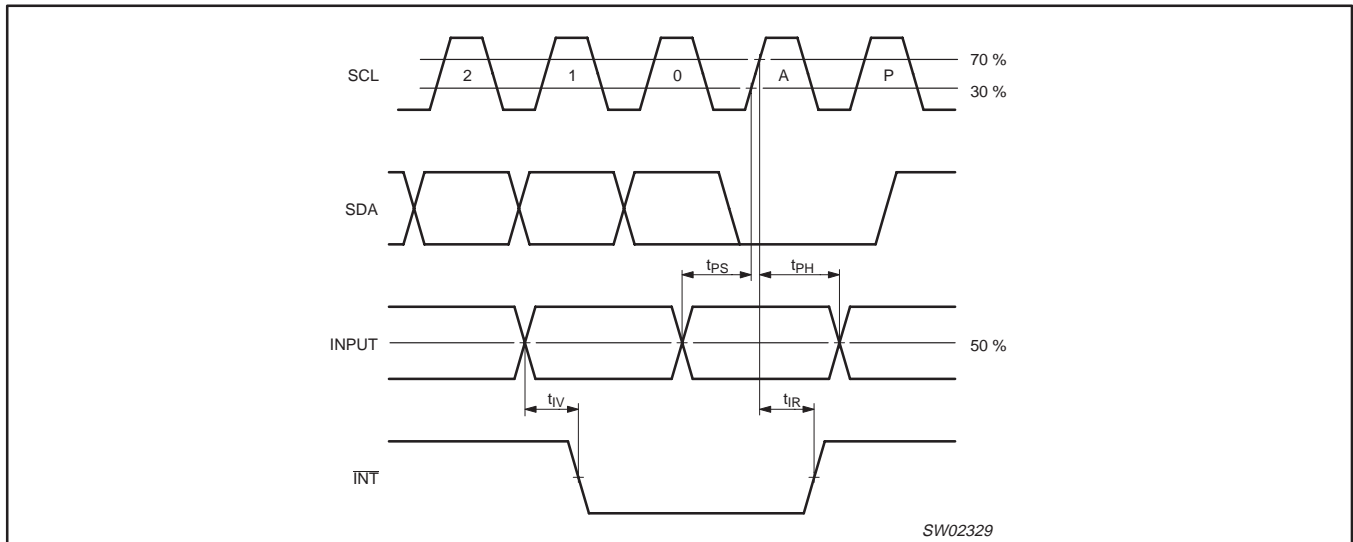


Figure 15. Expanded view of Read input port register

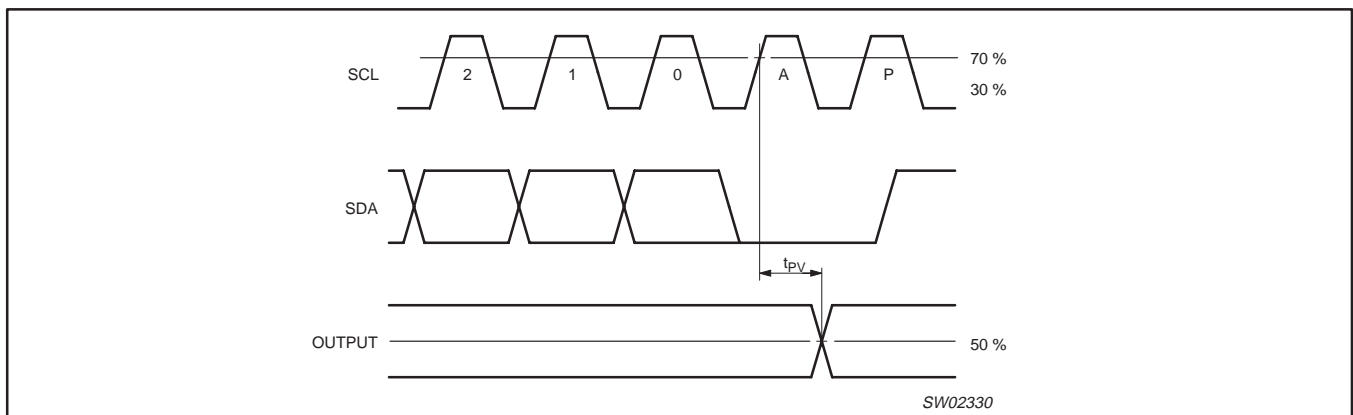


Figure 16. Expanded view of Write to output port register

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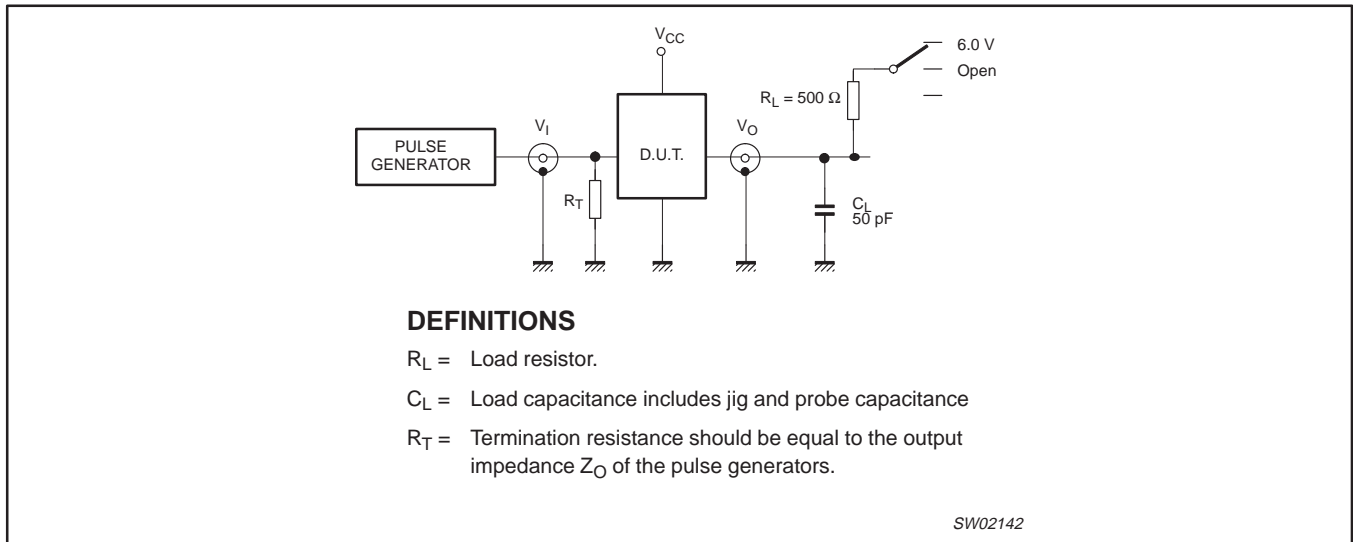


Figure 17. Test circuitry for switching times

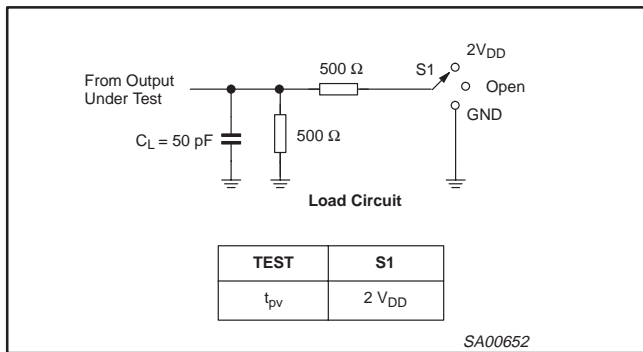


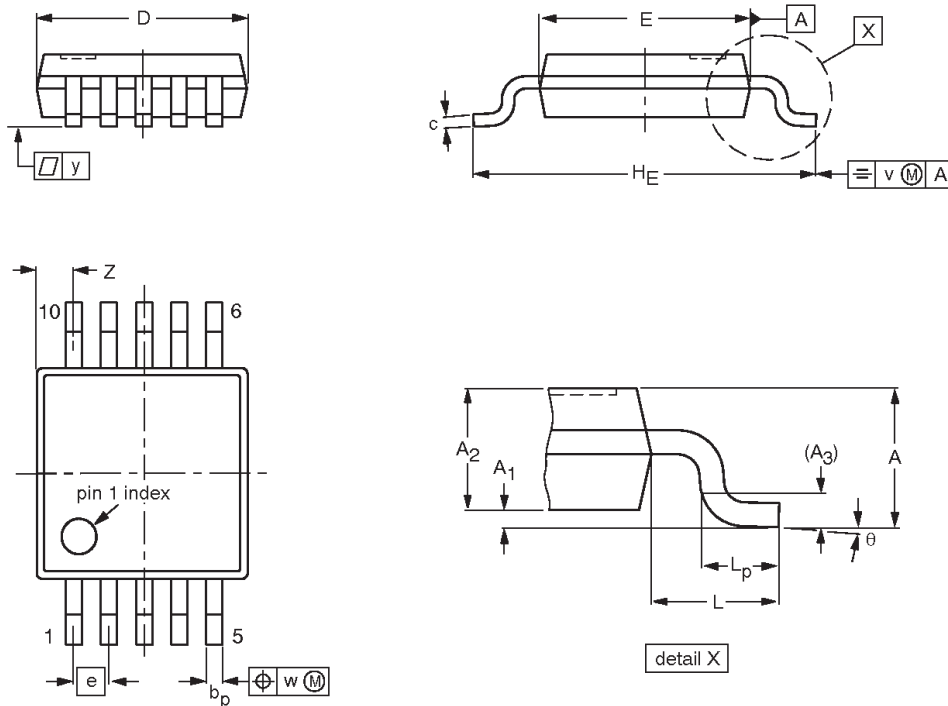
Figure 18. Test circuit

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**TSSOP10:** plastic thin shrink small outline package; 10 leads, body width 3 mm

**SOT552-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	v	w	y	Z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.15	0.23 0.15	3.1 2.9	3.1 2.9	0.5	5.0 4.8	0.95	0.7 0.4	0.1	0.1	0.1	0.67 0.34	6° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT552-1						-99-07-29- 03-02-18

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**4-bit I<sup>2</sup>C-bus and SMBus low power  
I/O port with interrupt and reset**

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**REVISION HISTORY**

Rev	Date	Description
_4	20060921	<b>Product data sheet. Supersedes data of 2004 Nov 29 (9397 750 14259).</b> Modifications: <ul style="list-style-type: none"><li>• Figure 3 on page 5: removed (2) ESD protection diodes</li></ul>
_3	20041129	<b>Product data sheet (9397 750 14259). Supersedes data of 2004 Sep 30 (9397 750 14052).</b>
_2	20040930	<b>Objective data sheet (9397 750 14052). Supersedes data of 2004 Aug 20 (9397 750 12894).</b>
_1	20040820	<b>Objective data sheet (9397 750 12894).</b>



# 4-bit I<sup>2</sup>C-bus and SMBus low power I/O port with interrupt and reset

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## Legal Information

### Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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