



PCA9549

Octal bus switch with individually I²C-bus controlled enables

Rev. 01 — 11 July 2006

Product data sheet

1. General description

The PCA9549 provides eight bits of high speed TTL-compatible bus switching controlled by the I²C-bus. The low ON-state resistance of the switch allows connections to be made with minimal propagation delay. Any individual A to B channel or combination of channels can be selected via the I²C-bus, determined by the contents of the programmable Control register. When the I²C-bus bit is HIGH (logic 1), the switch is on and data can flow from Port A to Port B, or vice versa. When the I²C-bus bit is LOW (logic 0), the switch is open, creating a high-impedance state between the two ports, which stops the data flow.

An active LOW reset input ($\overline{\text{RESET}}$) allows the PCA9549 to recover from a situation where the I²C-bus is stuck in a LOW state. Pulling the $\overline{\text{RESET}}$ pin LOW resets the I²C-bus state machine and causes all the bits to be open, as does the internal power-on reset function.

Three address pins allow up to eight devices on the same bus.

2. Features

- 8-bit bus switch (CBT)
- 5 Ω switch connection between two ports
- I²C-bus interface logic; compatible with SMBus standards
- Active LOW $\overline{\text{RESET}}$ input
- 3 address pins allowing up to 8 devices on the I²C-bus
- Bit selection via I²C-bus, in any combination
- Power-up with all bits deselected
- Low R_{on} switches
- No glitch on power-up
- Supports hot insertion
- Low standby current
- Operating power supply voltage range of 2.3 V to 5.5 V
- 5 V tolerant inputs
- 0 Hz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO24, TSSOP24, HVQFN24

PHILIPS

3. Ordering information

Table 1. Ordering information

| Type number | Package | | Version |
|-------------|---------|--|----------|
| | Name | Description | |
| PCA9549D | SO24 | plastic small outline package; 24 leads; body width 7.5 mm | SOT137-1 |
| PCA9549PW | TSSOP24 | plastic thin shrink small outline package; 24 leads; body width 4.4 mm | SOT355-1 |
| PCA9549BS | HVQFN24 | plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.85 mm | SOT616-1 |

3.1 Ordering options

Table 2. Ordering options

| Type number | Topside mark | Temperature range |
|-------------|--------------|-------------------|
| PCA9549D | PCA9549D | -40 °C to +85 °C |
| PCA9549PW | PCA9549 | -40 °C to +85 °C |
| PCA9549BS | 9549 | -40 °C to +85 °C |

4. Block diagram

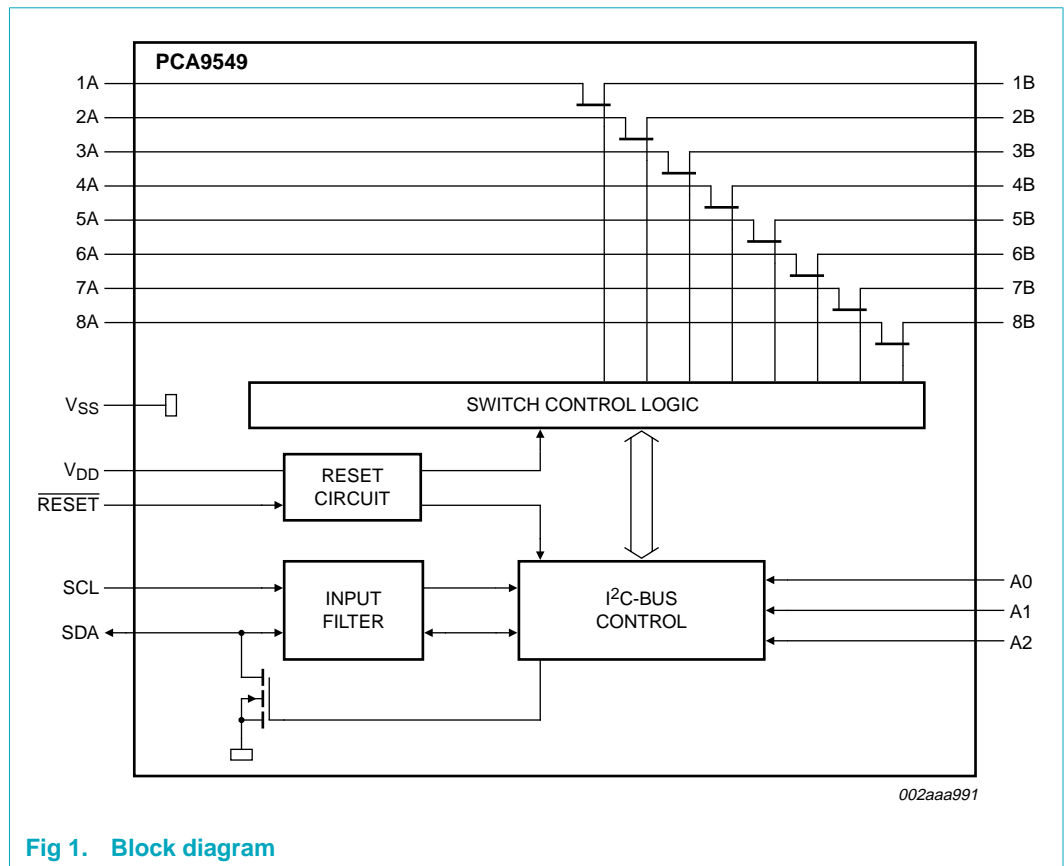
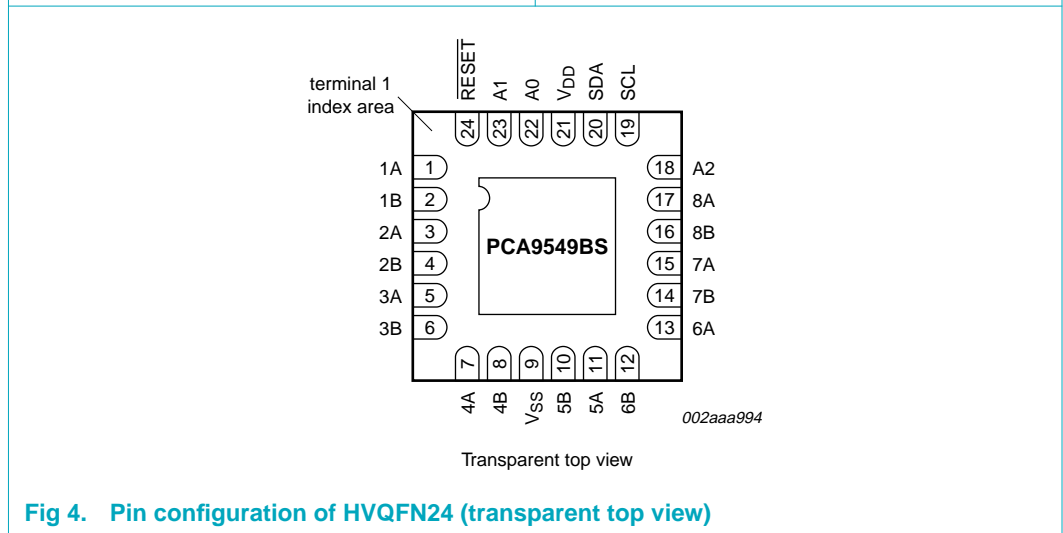
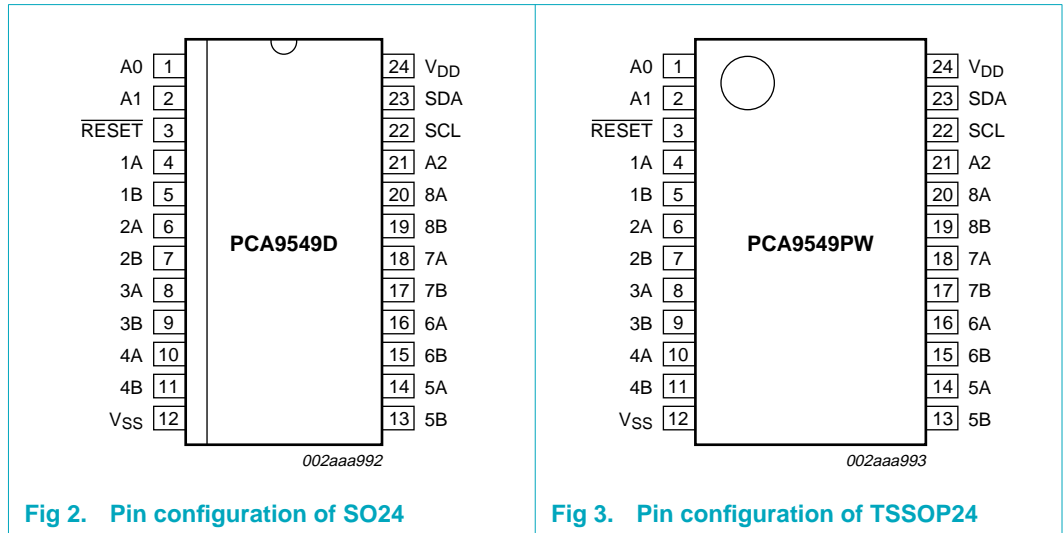


Fig 1. Block diagram

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 3. Pin description

| Symbol | Pin | | Description |
|---------------------------|-----------|------------------|------------------------|
| | SO, TSSOP | HVQFN | |
| A0 | 1 | 22 | address input 0 |
| A1 | 2 | 23 | address input 1 |
| $\overline{\text{RESET}}$ | 3 | 24 | active LOW reset input |
| 1A | 4 | 1 | input |
| 1B | 5 | 2 | output |
| 2A | 6 | 3 | input |
| 2B | 7 | 4 | output |
| 3A | 8 | 5 | input |
| 3B | 9 | 6 | output |
| 4A | 10 | 7 | input |
| 4B | 11 | 8 | output |
| V _{SS} | 12 | 9 ^[1] | supply ground |
| 5B | 13 | 10 | output |
| 5A | 14 | 11 | input |
| 6B | 15 | 12 | output |
| 6A | 16 | 13 | input |
| 7B | 17 | 14 | output |
| 7A | 18 | 15 | input |
| 8B | 19 | 16 | output |
| 8A | 20 | 17 | input |
| A2 | 21 | 18 | address input 2 |
| SCL | 22 | 19 | serial clock line |
| SDA | 23 | 20 | serial data line |
| V _{DD} | 24 | 21 | supply voltage |

[1] HVQFN package die supply ground is connected to both the V_{SS} pin and the exposed center pad. The V_{SS} pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board-level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board, and for proper heat conduction through the board thermal vias need to be incorporated in the PCB in the thermal pad region.

6. Functional description

6.1 Device addressing

Following a START condition, the bus master must output the address of the slave it is accessing. The address of the PCA9549 is shown in [Figure 5](#). To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.

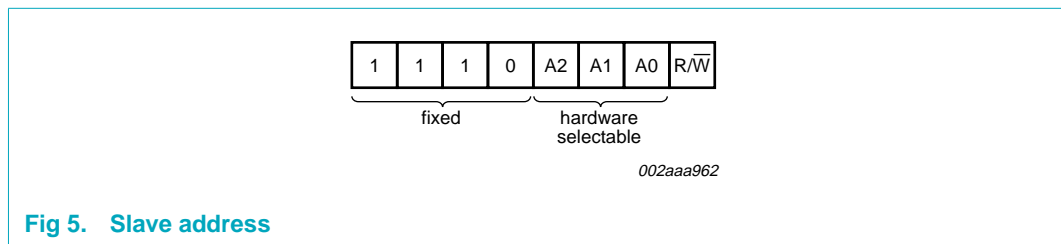


Fig 5. Slave address

The last bit of the slave address defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

6.2 Control register

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PCA9549, which will be stored in the Control register. If multiple bytes are received by the PCA9549, it will save the last byte received. This register can be written and read via the I²C-bus.

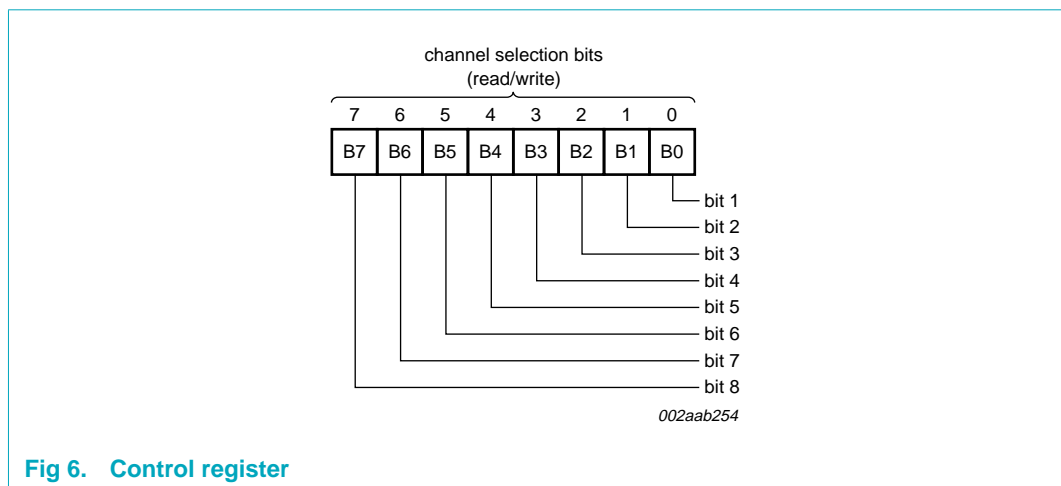


Fig 6. Control register

6.2.1 Control register definition

One or several bits are selected by the contents of the Control register. This register is written after the PCA9549 has been addressed. The entire control byte is used to determine which bit is to be selected. When a bit is selected to close, the bit will close after the Acknowledge has been placed on the I²C-bus.

Table 4. Control register

Write = channel selection; read = channel status.

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | Command |
|----|----|----|----|----|----|----|----|----------------|
| X | X | X | X | X | X | X | 0 | bit 1 disabled |
| X | X | X | X | X | X | X | 1 | bit 1 enabled |
| X | X | X | X | X | X | 0 | X | bit 2 disabled |
| X | X | X | X | X | X | 1 | X | bit 2 enabled |
| X | X | X | X | X | 0 | X | X | bit 3 disabled |
| X | X | X | X | X | 1 | X | X | bit 3 enabled |
| X | X | X | X | 0 | X | X | X | bit 4 disabled |
| X | X | X | X | 1 | X | X | X | bit 4 enabled |
| X | X | X | 0 | X | X | X | X | bit 5 disabled |
| X | X | X | 1 | X | X | X | X | bit 5 enabled |
| X | X | 0 | X | X | X | X | X | bit 6 disabled |
| X | X | 1 | X | X | X | X | X | bit 6 enabled |
| X | 0 | X | X | X | X | X | X | bit 7 disabled |
| X | 1 | X | X | X | X | X | X | bit 7 enabled |
| 0 | X | X | X | X | X | X | X | bit 8 disabled |
| 1 | X | X | X | X | X | X | X | bit 8 enabled |

[1] Several bits can be enabled at the same time. For example, B7 = 0, B6 = 1, B5 = 0, B4 = 0, B3 = 1, B2 = 1, B1 = 0, B0 = 0, means that bit 8, bit 6, bit 5, bit 2, and bit 1 are disabled and bit 7, bit 4, and bit 3 are enabled.

6.3 RESET input

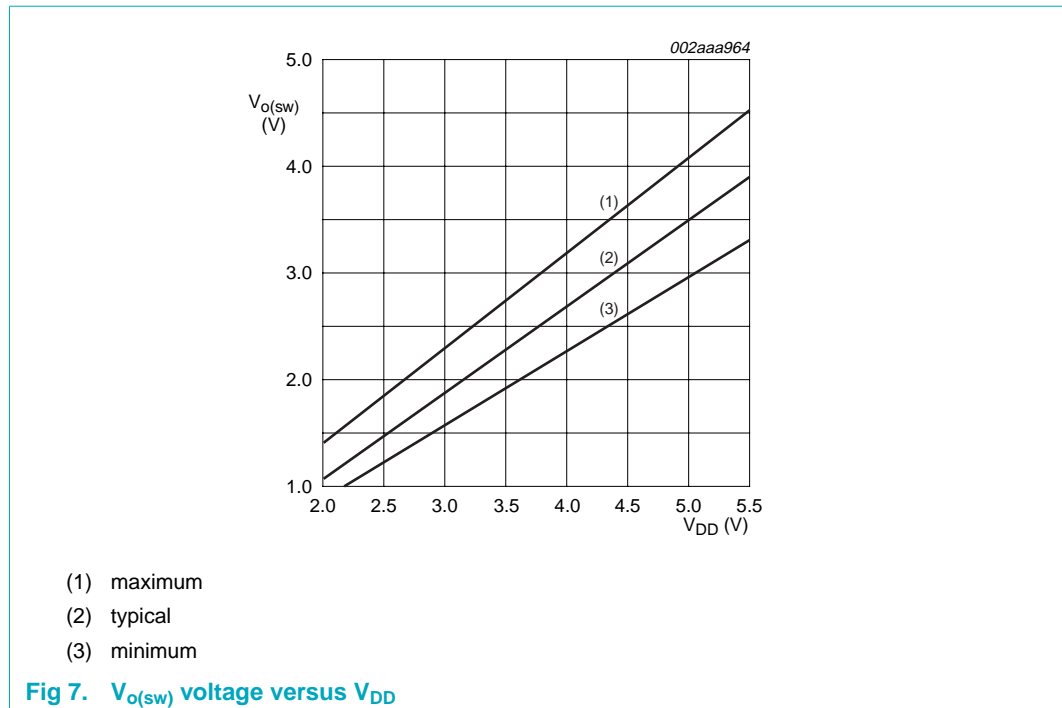
The $\overline{\text{RESET}}$ input is an active LOW signal which may be used to recover from a bus fault condition. By asserting this signal LOW for a minimum of $t_{w(\text{rst})L}$, the PCA9549 will reset its registers and I²C-bus state machine and will open all bits. The $\overline{\text{RESET}}$ input must be connected to V_{DD} through a pull-up resistor.

6.4 Power-on reset

When power is applied to V_{DD} , an internal Power-On Reset (POR) holds the PCA9549 in a reset state until V_{DD} has reached V_{POR} . At this point, the reset condition is released and the PCA9549 registers and I²C-bus state machine are initialized to their default states, all zeroes causing all the bits to be open (high-impedance state).

6.5 CBT characteristic over V_{DD} range

The bus switch is optimized at 5.0 V but can operate over the entire supply range with lower $V_{O(SW)}$ voltage and higher gate resistance.



[Figure 7](#) shows the voltage characteristics of the pass gate transistors (note that the PCA9549 is only tested at the points specified in [Section 9 “Static characteristics”](#)). In order for the PCA9549 to act as a voltage translator, the $V_{o(sw)}$ voltage should be equal to, or lower than the lowest bus voltage. For example, if the main bus was running at 5 V, and the downstream buses were 3.3 V and 2.7 V, then $V_{o(sw)}$ should be equal to or below 2.7 V to effectively clamp the downstream bus voltages. Looking at [Figure 7](#), we see that $V_{o(sw)}$ (maximum) will be at 2.7 V when the PCA9549 supply voltage is 3.5 V or lower so the PCA9549 supply voltage could be set to 3.3 V. Pull-up resistors can then be used to bring the bus voltages to their appropriate levels (see [Figure 16](#)).

7. Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

7.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see [Figure 8](#)).

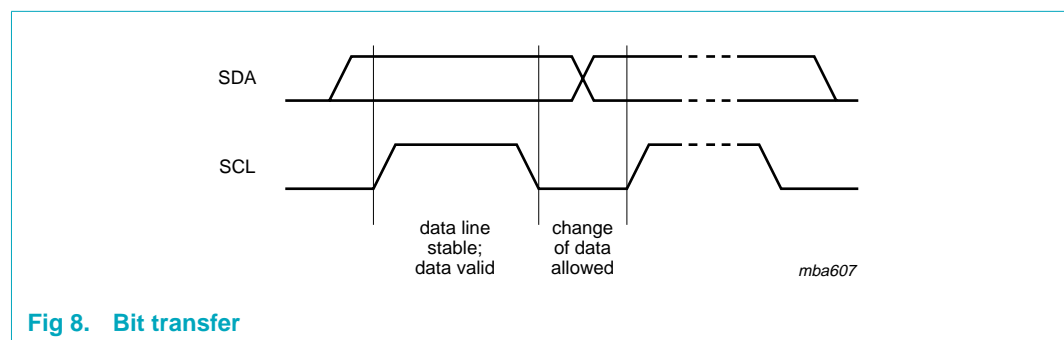


Fig 8. Bit transfer

7.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see [Figure 9](#)).

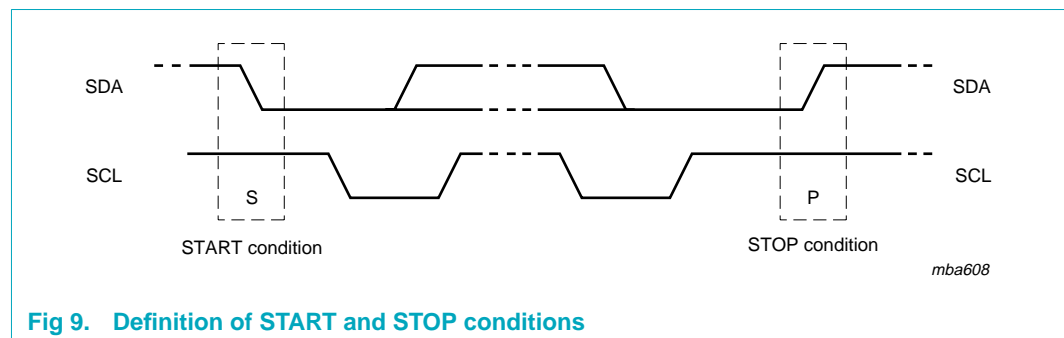
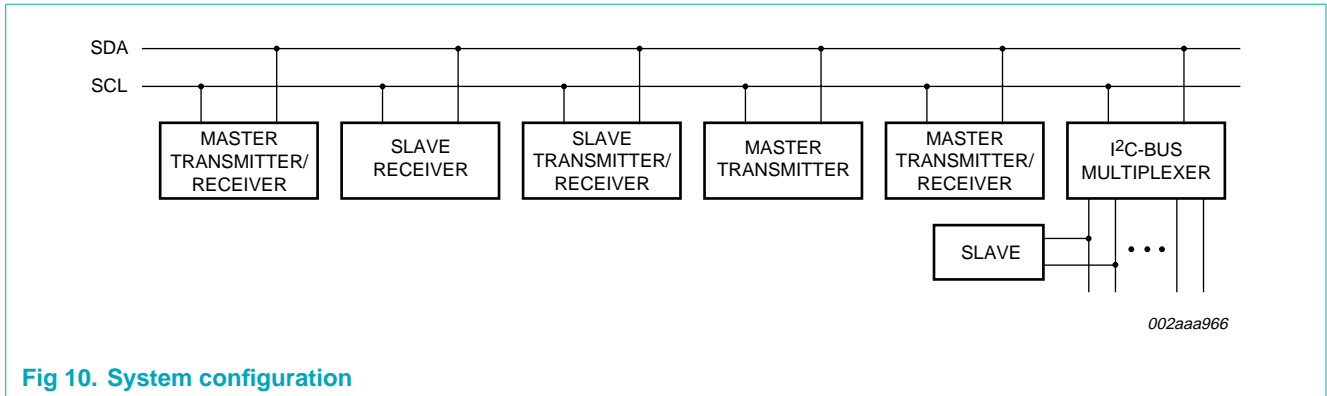


Fig 9. Definition of START and STOP conditions

7.2 System configuration

A device generating a message is a 'transmitter'; a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see [Figure 10](#)).

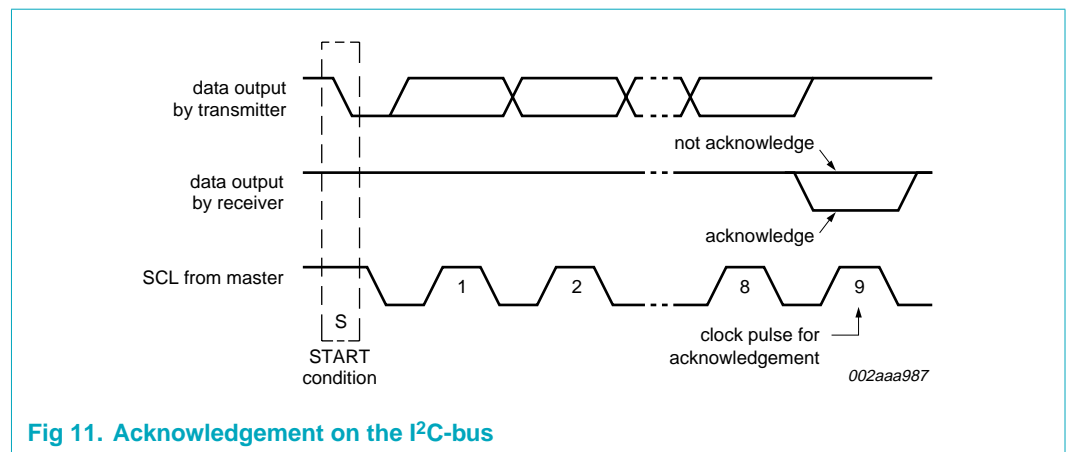


7.3 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

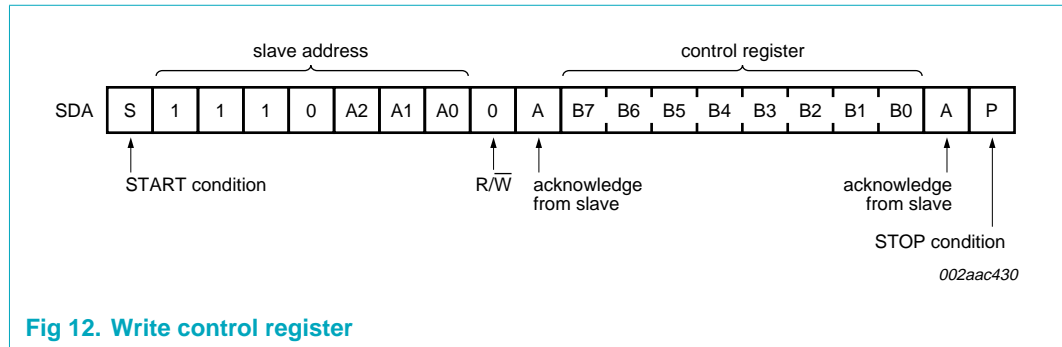
A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

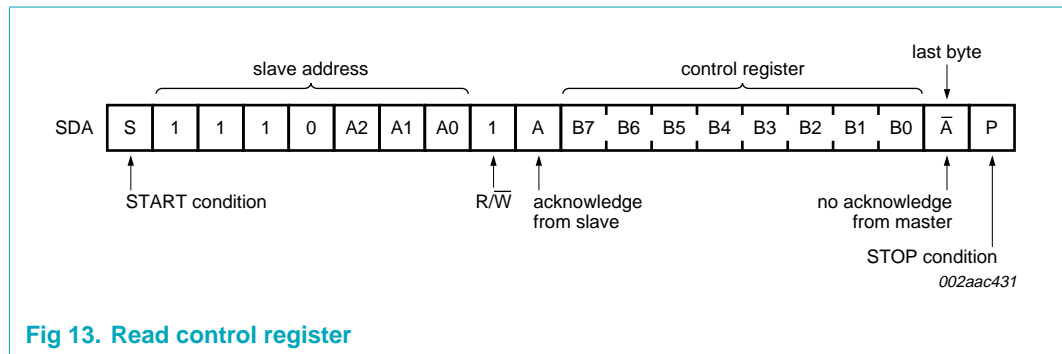


7.4 Bus transactions

Data is transmitted to the PCA9549 control register using the Write mode as shown in [Figure 12](#).



Data is read from the PCA9549 using the Read mode as shown in [Figure 13](#).



8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).^[1]

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------|------------|------|------|------|
| V _{DD} | supply voltage | | -0.5 | +7.0 | V |
| V _I | input voltage | | -0.5 | +7.0 | V |
| I _I | input current | | -20 | +20 | mA |
| I _O | output current | | -25 | +25 | mA |
| I _{DD} | supply current | | -100 | +100 | mA |
| I _{SS} | ground supply current | | -100 | +100 | mA |
| P _{tot} | total power dissipation | | - | 400 | mW |
| T _{stg} | storage temperature | | -60 | +150 | °C |
| T _{amb} | ambient temperature | operating | -40 | +85 | °C |

[1] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 125 °C.

9. Static characteristics

Table 6. Static characteristics

$V_{DD} = 2.3\text{ V to }3.6\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -40\text{ °C to }+85\text{ °C}$; unless otherwise specified.

See [Table 7 on page 12](#) for $V_{DD} = 4.5\text{ V to }5.5\text{ V}$ [1].

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------------|--------------------------|---|--------------|-----|----------------|---------------|
| Supply | | | | | | |
| V_{DD} | supply voltage | | 2.3 | - | 3.6 | V |
| I_{DD} | supply current | Operating mode; $V_{DD} = 3.6\text{ V}$; no load; $V_I = V_{DD}$ or V_{SS} ; $f_{SCL} = 100\text{ kHz}$ | - | 20 | 50 | μA |
| I_{stb} | standby current | Standby mode; $V_{DD} = 3.6\text{ V}$; no load; $V_I = V_{DD}$ or V_{SS} | - | 0.1 | 1 | μA |
| V_{POR} | power-on reset voltage | no load; $V_I = V_{DD}$ or V_{SS} | [2] - | 1.6 | 2.1 | V |
| Input SCL; input/output SDA | | | | | | |
| V_{IL} | LOW-level input voltage | | -0.5 | - | +0.3 V_{DD} | V |
| V_{IH} | HIGH-level input voltage | | 0.7 V_{DD} | - | 6 | V |
| I_{OL} | LOW-level output current | $V_{OL} = 0.4\text{ V}$ | 3 | - | - | mA |
| | | $V_{OL} = 0.6\text{ V}$ | 6 | - | - | mA |
| I_L | leakage current | $V_I = V_{DD}$ or V_{SS} | -1 | - | +1 | μA |
| C_i | input capacitance | $V_I = V_{SS}$ | - | 6 | 21 | pF |
| Select inputs A0 to A2, RESET | | | | | | |
| V_{IL} | LOW-level input voltage | | -0.5 | - | +0.3 V_{DD} | V |
| V_{IH} | HIGH-level input voltage | | 0.7 V_{DD} | - | $V_{DD} + 0.5$ | V |
| I_{LI} | input leakage current | pin at V_{DD} or V_{SS} | -1 | - | +1 | μA |
| C_i | input capacitance | $V_I = V_{SS}$ | - | 2 | 5 | pF |
| Pass gate | | | | | | |
| R_{on} | ON-state resistance | $V_{DD} = 3.0\text{ V to }3.6\text{ V}$; $V_O = 0.4\text{ V}$; $I_O = 15\text{ mA}$ | - | 7 | 12 | Ω |
| | | $V_{DD} = 2.3\text{ V to }2.7\text{ V}$; $V_O = 0.4\text{ V}$; $I_O = 10\text{ mA}$ | - | 8 | 15 | Ω |
| $V_{o(sw)}$ | switch output voltage | $V_{i(sw)} = V_{DD} = 3.3\text{ V}$; $I_{o(sw)} = -100\text{ }\mu\text{A}$ | - | 1.9 | - | V |
| | | $V_{i(sw)} = V_{DD} = 3.0\text{ V to }3.6\text{ V}$; $I_{o(sw)} = -100\text{ }\mu\text{A}$ | 1.6 | - | 2.8 | V |
| | | $V_{i(sw)} = V_{DD} = 2.5\text{ V}$; $I_{o(sw)} = -100\text{ }\mu\text{A}$ | - | 1.5 | - | V |
| | | $V_{i(sw)} = V_{DD} = 2.3\text{ V to }2.7\text{ V}$; $I_{o(sw)} = -100\text{ }\mu\text{A}$ | 1.0 | - | 2.0 | V |
| I_L | leakage current | $V_I = V_{DD}$ or V_{SS} | -1 | - | +1 | μA |
| C_{io} | input/output capacitance | $V_I = V_{SS}$ | - | 3 | 5 | pF |

[1] For operation between published voltage ranges, refer to the worst-case parameters in both ranges.

[2] V_{DD} must be lowered to 0.2 V in order to reset part.

Octal bus switch with individually I²C-bus controlled enables**Table 7. Static characteristics** $V_{DD} = 4.5\text{ V to }5.5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$; unless otherwise specified.See [Table 6 on page 11](#) for $V_{DD} = 2.3\text{ V to }3.6\text{ V}$ [1].

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------------------|--------------------------|--|--------------|-----|----------------|---------------|
| Supply | | | | | | |
| V_{DD} | supply voltage | | 4.5 | - | 5.5 | V |
| I_{DD} | supply current | Operating mode; $V_{DD} = 5.5\text{ V}$; no load; $V_I = V_{DD}$ or V_{SS} ; $f_{SCL} = 100\text{ kHz}$ | - | 65 | 100 | μA |
| I_{stb} | standby current | Standby mode; $V_{DD} = 5.5\text{ V}$; no load; $V_I = V_{DD}$ or V_{SS} | - | 0.6 | 2 | μA |
| V_{POR} | power-on reset voltage | no load; $V_I = V_{DD}$ or V_{SS} | [2] - | 1.7 | 2.1 | V |
| Input SCL; input/output SDA | | | | | | |
| V_{IL} | LOW-level input voltage | | -0.5 | - | +0.3 V_{DD} | V |
| V_{IH} | HIGH-level input voltage | | 0.7 V_{DD} | - | 6 | V |
| I_{OL} | LOW-level output current | $V_{OL} = 0.4\text{ V}$ | 3 | - | - | mA |
| | | $V_{OL} = 0.6\text{ V}$ | 6 | - | - | mA |
| I_{IL} | LOW-level input current | $V_I = V_{SS}$ | 1 | - | 1 | μA |
| I_{IH} | HIGH-level input current | $V_I = V_{SS}$ | 1 | - | 1 | μA |
| C_i | input capacitance | $V_I = V_{SS}$ | - | 6 | 21 | pF |
| Select inputs A[0:2]/RESET | | | | | | |
| V_{IL} | LOW-level input voltage | | -0.5 | - | +0.3 V_{DD} | V |
| V_{IH} | HIGH-level input voltage | | 0.7 V_{DD} | - | $V_{DD} + 0.5$ | V |
| I_{LI} | input leakage current | pin at V_{DD} or V_{SS} | -1 | - | +50 | μA |
| C_i | input capacitance | $V_I = V_{SS}$ | - | 2 | 5 | pF |
| Pass gate | | | | | | |
| R_{on} | ON-state resistance | $V_{DD} = 4.5\text{ V to }5.5\text{ V}$; $V_O = 0.4\text{ V}$; $I_O = 15\text{ mA}$ | - | 5 | 8 | Ω |
| $V_{O(sw)}$ | switch output voltage | $V_{i(sw)} = V_{DD} = 5.0\text{ V}$; $I_{o(sw)} = -100\text{ }\mu\text{A}$ | - | 3.6 | - | V |
| | | $V_{i(sw)} = V_{DD} = 4.5\text{ V to }5.5\text{ V}$; $I_{o(sw)} = -100\text{ }\mu\text{A}$ | 2.6 | - | 4.5 | V |
| I_L | leakage current | $V_I = V_{DD}$ or V_{SS} | -10 | - | +10 | μA |
| C_{io} | input/output capacitance | $V_I = V_{SS}$ | - | 3 | 5 | pF |

[1] For operation between published voltage ranges, refer to the worst-case parameters in both ranges.

[2] V_{DD} must be lowered to 0.2 V in order to reset part.

10. Dynamic characteristics

Table 8. Dynamic characteristics

| Symbol | Parameter | Conditions | Standard-mode I ² C-bus | | Fast-mode I ² C-bus | | Unit |
|----------------------|---|---|------------------------------------|---------------------|---------------------------------------|---------------------|------|
| | | | Min | Max | Min | Max | |
| t _{PD} | propagation delay | A to B; V _{DD} = 4.5 V to 5.5 V | - | 0.25 ^[1] | - | 0.25 ^[1] | ns |
| f _{SCL} | SCL clock frequency | | 0 | 100 | 0 | 400 | kHz |
| t _{BUF} | bus free time between a STOP and START condition | | 4.7 | - | 1.3 | - | μs |
| t _{HD;STA} | hold time (repeated) START condition | | 4.0 ^[2] | - | 0.6 | - | μs |
| t _{LOW} | LOW period of the SCL clock | | 4.7 | - | 1.3 | - | μs |
| t _{HIGH} | HIGH period of the SCL clock | | 4.0 | - | 0.6 | - | μs |
| t _{SU;STA} | set-up time for a repeated START condition | | 4.7 | - | 0.6 | - | μs |
| t _{SU;STO} | set-up time for STOP condition | | 4.0 | - | 0.6 | - | μs |
| t _{HD;DAT} | data hold time | | 0 ^[3] | 3.45 | 0 ^[3] | 0.9 | μs |
| t _{SU;DAT} | data set-up time | | 250 | - | 100 | - | ns |
| t _r | rise time of both SDA and SCL signals | | - | 1000 | 20 + 0.1C _b ^[4] | 300 | ns |
| t _f | fall time of both SDA and SCL signals | | - | 300 | 20 + 0.1C _b ^[4] | 300 | μs |
| C _b | capacitive load for each bus line | | - | 400 | - | 400 | μs |
| t _{SP} | pulse width of spikes that must be suppressed by the input filter | | - | 50 | - | 50 | ns |
| t _{VD;DAT} | data valid time | HIGH-to-LOW | - | 1 | - | 1 | μs |
| | | LOW-to-HIGH | - | 0.6 | - | 0.6 | μs |
| t _{VD;ACK} | data valid acknowledge time | | - | 1 | - | 1 | μs |
| RESET | | | | | | | |
| t _{w(rst)L} | LOW-level reset time | | 4 | - | 4 | - | ns |
| t _{rst} | reset time | SDA clear | 500 | - | 500 | - | ns |
| t _{REC;STA} | recovery time to START condition | | 0 | - | 0 | - | ns |

[1] Pass gate propagation delay is calculated from the 6 Ω typical R_{on} and the 50 pF load capacitance.

[2] After this period, the first clock pulse is generated.

[3] A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH(min)} of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

[4] C_b = total capacitance of one bus line in pF.

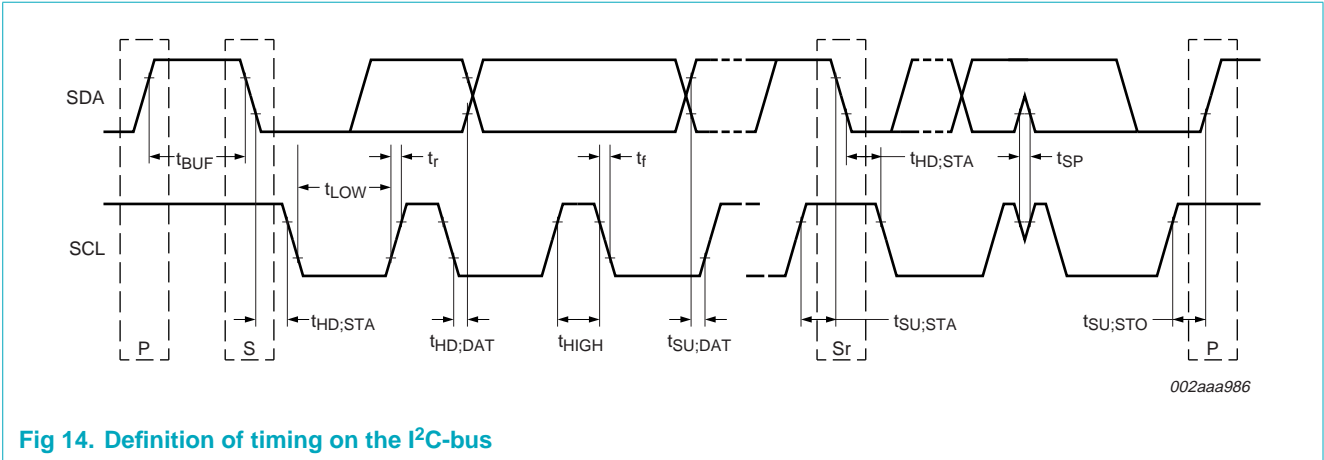


Fig 14. Definition of timing on the I²C-bus

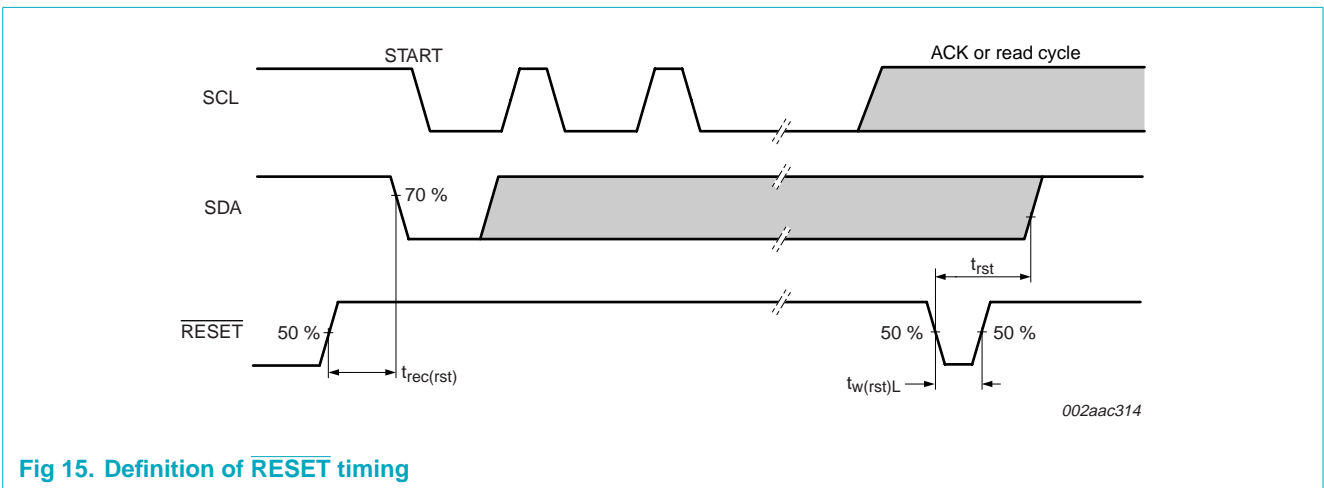
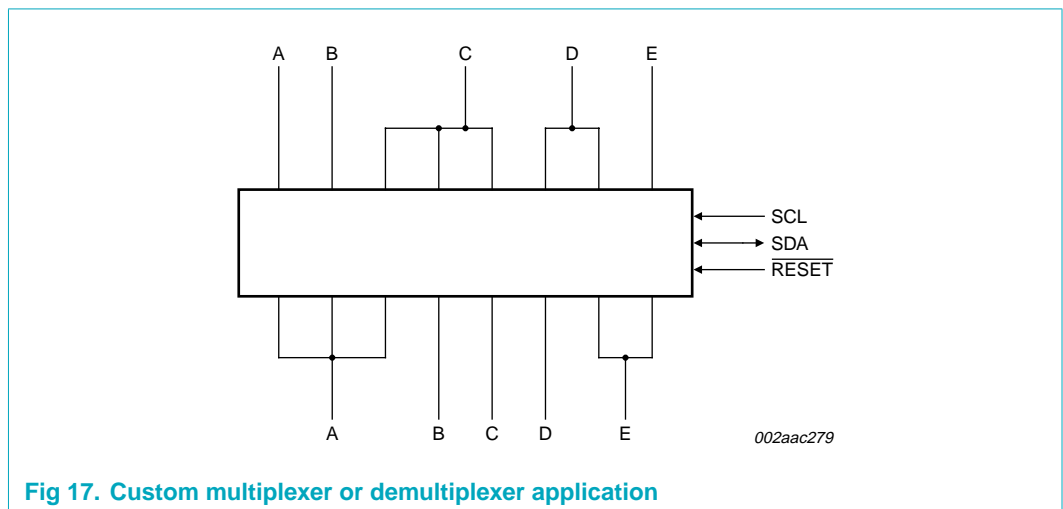
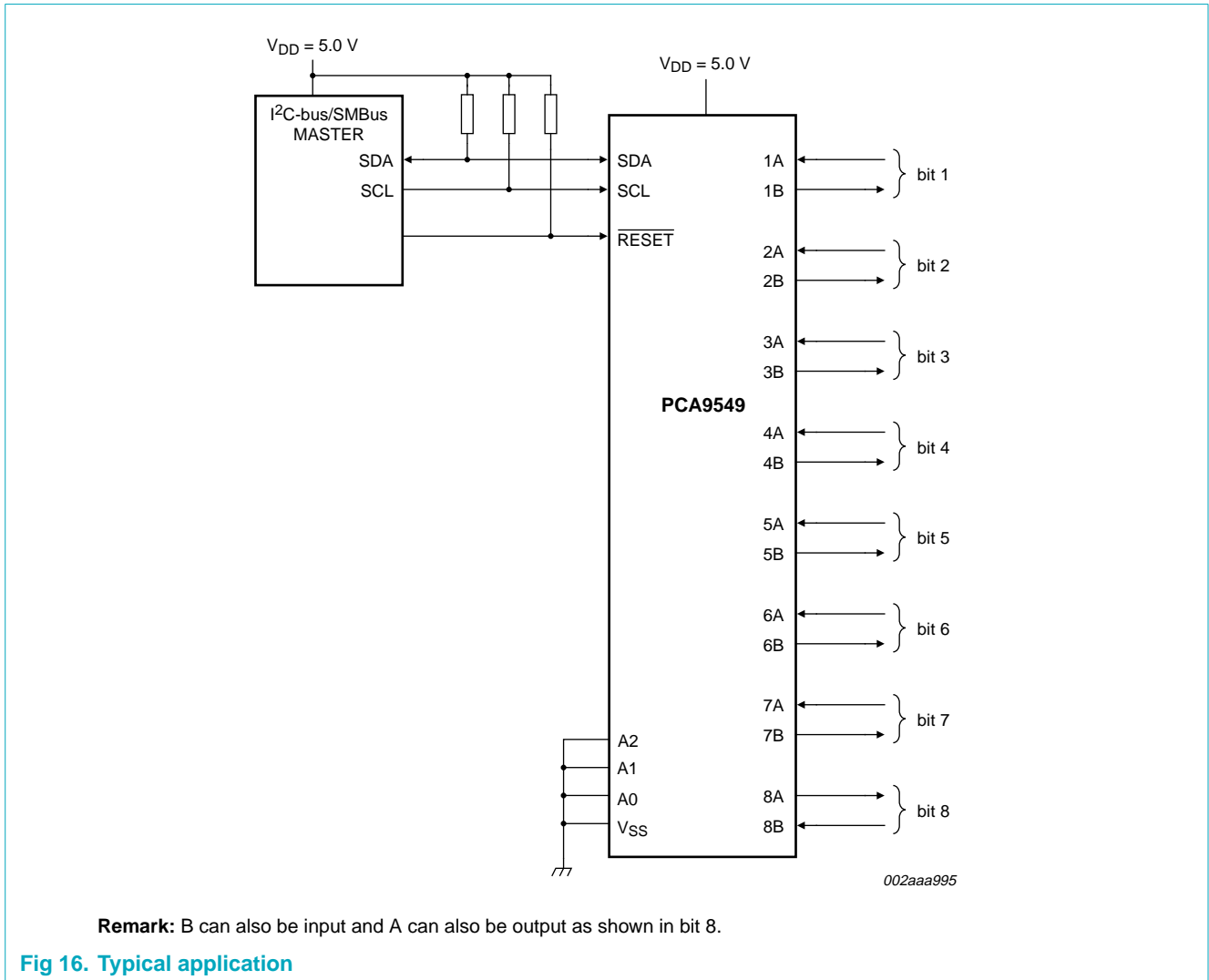
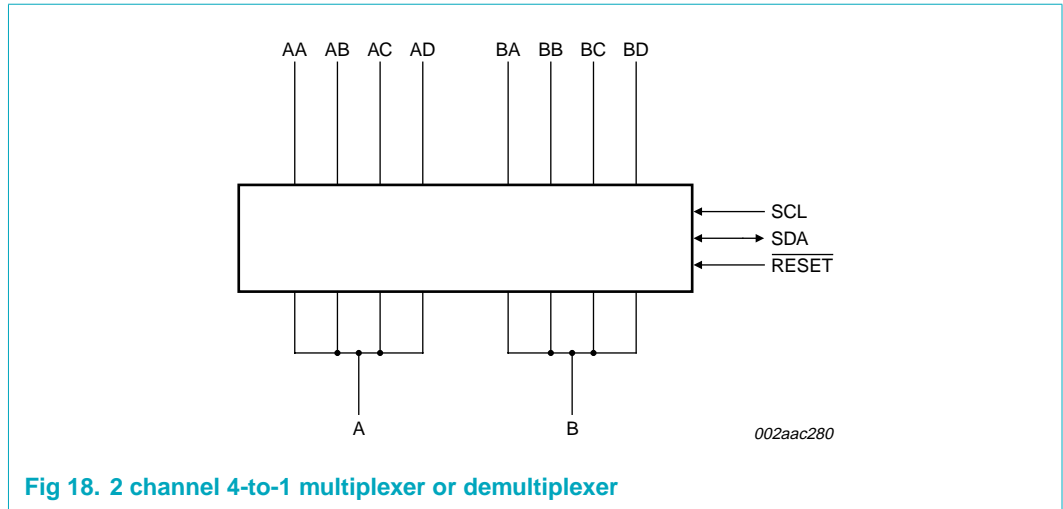


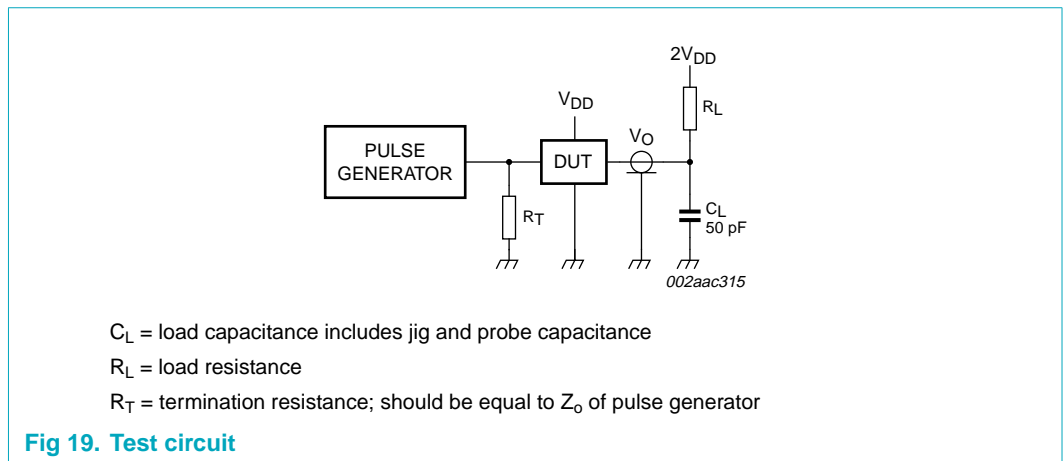
Fig 15. Definition of RESET timing

11. Application information





12. Test information



13. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

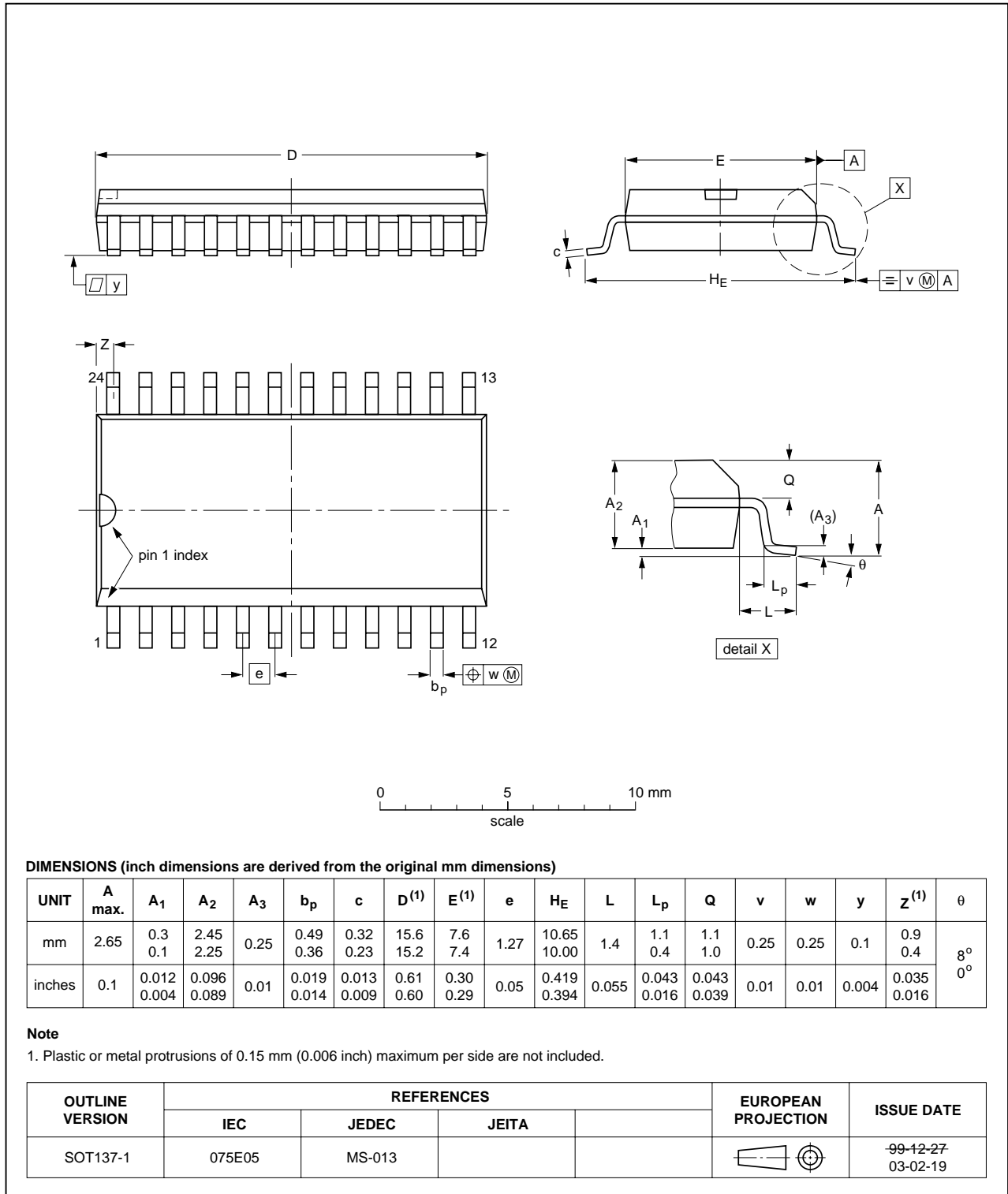


Fig 20. SO24 package outline (SOT137-1)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

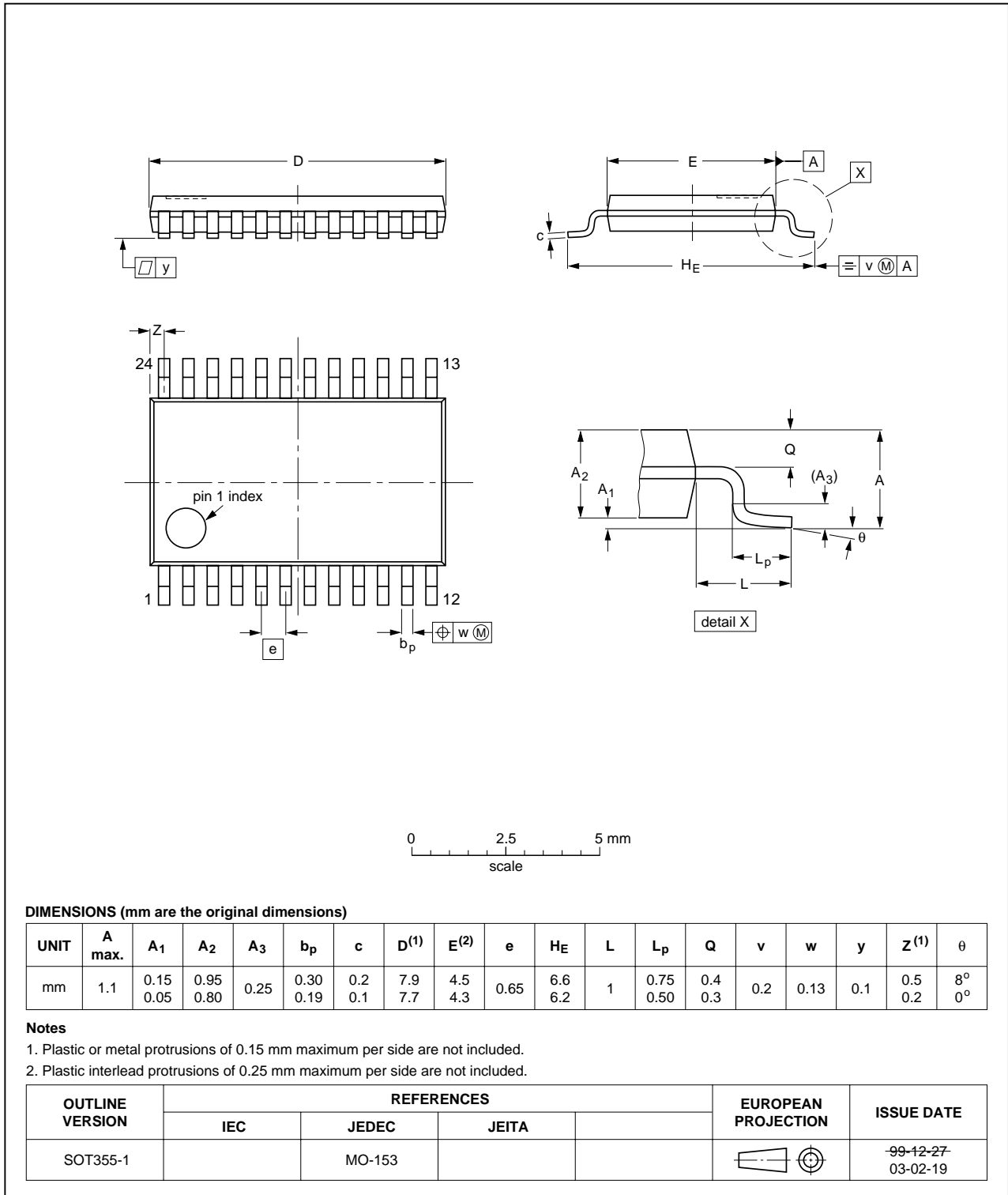


Fig 21. TSSOP24 package outline (SOT355-1)

HVQFN24: plastic thermal enhanced very thin quad flat package; no leads;
24 terminals; body 4 x 4 x 0.85 mm

SOT616-1

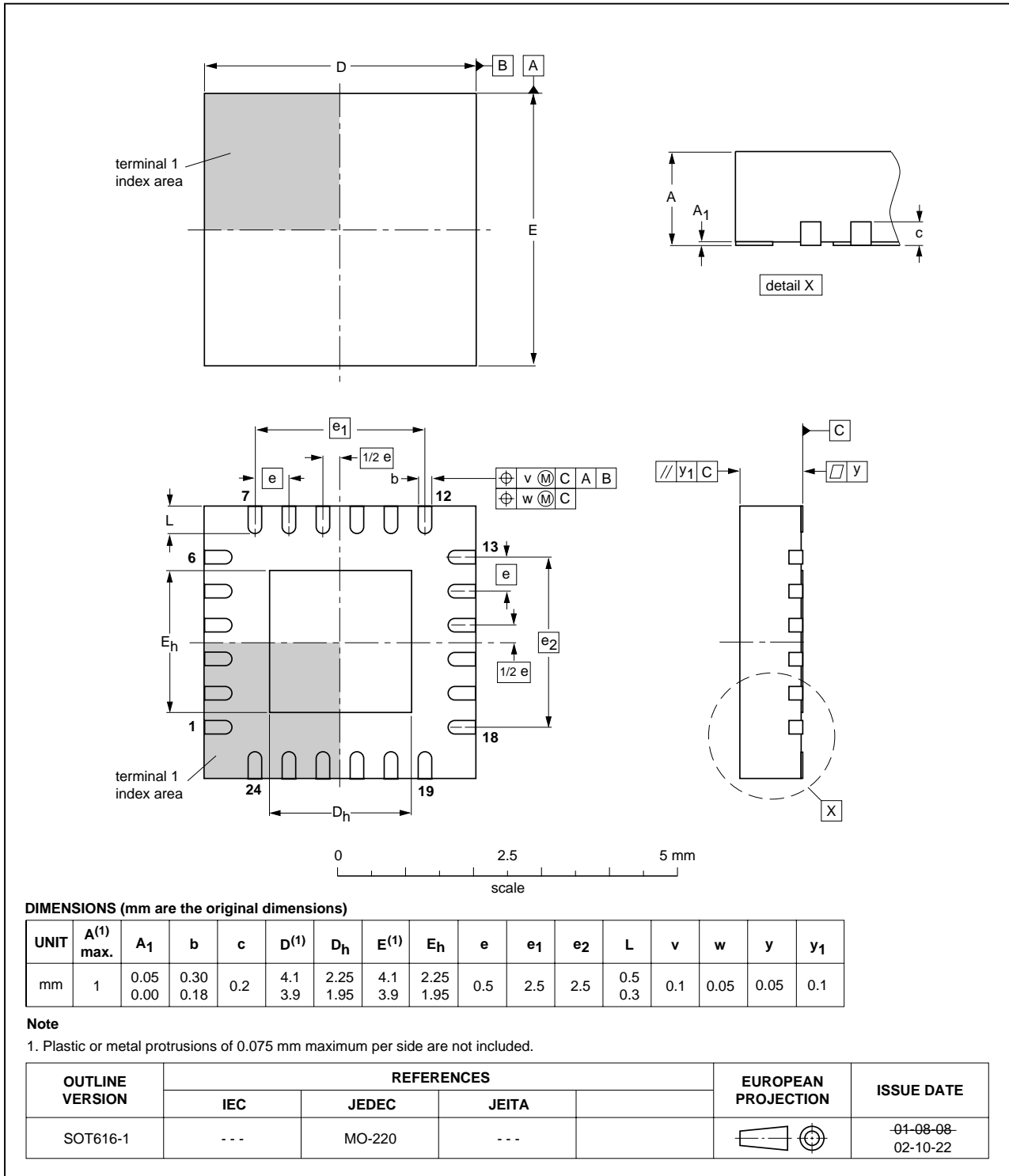


Fig 22. HVQFN24 package outline (SOT616-1)

14. Soldering

14.1 Introduction to soldering surface mount packages

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow temperatures range from 215 °C to 260 °C depending on solder paste material. The peak top-surface temperature of the packages should be kept below:

Table 9. SnPb eutectic process - package peak reflow temperatures (from J-STD-020C July 2004)

| Package thickness | Volume mm ³ < 350 | Volume mm ³ ≥ 350 |
|-------------------|------------------------------|------------------------------|
| < 2.5 mm | 240 °C + 0/-5 °C | 225 °C + 0/-5 °C |
| ≥ 2.5 mm | 225 °C + 0/-5 °C | 225 °C + 0/-5 °C |

Table 10. Pb-free process - package peak reflow temperatures (from J-STD-020C July 2004)

| Package thickness | Volume mm ³ < 350 | Volume mm ³ 350 to 2000 | Volume mm ³ > 2000 |
|-------------------|------------------------------|------------------------------------|-------------------------------|
| < 1.6 mm | 260 °C + 0 °C | 260 °C + 0 °C | 260 °C + 0 °C |
| 1.6 mm to 2.5 mm | 260 °C + 0 °C | 250 °C + 0 °C | 245 °C + 0 °C |
| ≥ 2.5 mm | 250 °C + 0 °C | 245 °C + 0 °C | 245 °C + 0 °C |

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):

Octal bus switch with individually I²C-bus controlled enables

- larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
- smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

14.5 Package related soldering information

Table 11. Suitability of surface mount IC packages for wave and reflow soldering methods

| Package ^[1] | Soldering method | |
|--|-----------------------------------|-----------------------|
| | Wave | Reflow ^[2] |
| BGA, HTSSON..T ^[3] , LBGA, LFBGA, SQFP, SSOP..T ^[3] , TFBGA, VFBGA, XSON | not suitable | suitable |
| DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS | not suitable ^[4] | suitable |
| PLCC ^[5] , SO, SOJ | suitable | suitable |
| LQFP, QFP, TQFP | not recommended ^{[5][6]} | suitable |
| SSOP, TSSOP, VSO, VSSOP | not recommended ^[7] | suitable |
| CWQCCN..L ^[8] , PMFP ^[9] , WQCCN..L ^[8] | not suitable | not suitable |

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

- [3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding $217\text{ °C} \pm 10\text{ °C}$ measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
- [4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
- [5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- [6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- [7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
- [8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.
- [9] Hot bar soldering or manual soldering is suitable for PMFP packages.

15. Abbreviations

Table 12. Abbreviations

| Acronym | Description |
|------------------|-----------------------------|
| CBT | Cross Bar Technology |
| CDM | Charged Device Model |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| I ² C | Inter Integrated Circuit |
| MM | Machine Model |
| PCB | Printed-Circuit Board |
| SMBus | System Management Bus |
| TTL | Transistor-Transistor Logic |

16. Revision history

Table 13. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-------------|--------------|--------------------|---------------|------------|
| PCA9549_1 | 20060711 | Product data sheet | - | - |

17. Legal information

17.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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