

# DATA SHEET



## **PCA9542**

### 2-channel I<sup>2</sup>C multiplexer and interrupt logic

Product data sheet  
Supersedes data of 2002 Mar 28

2004 Oct 01

2-channel I<sup>2</sup>C multiplexer and interrupt logic

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## FEATURES

- 1-of-2 bi-directional translating multiplexer
- I<sup>2</sup>C interface logic; compatible with SMBus
- 2 Active-LOW Interrupt Inputs
- Active-LOW Interrupt Output
- 3 address pins allowing up to 8 devices on the I<sup>2</sup>C-bus
- Channel selection via I<sup>2</sup>C-bus
- Power-up with all multiplexer channels deselected
- Low R<sub>dsON</sub> switches
- Allows voltage level translation between 1.8 V, 2.5 V, 3.3 V and 5 V buses
- No glitch on power-up
- Supports hot insertion
- Low stand-by current
- Operating power supply voltage range of 2.3 V to 5 V
- 5 V tolerant Inputs
- 0 kHz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 150 V MM per JESD22-A115 and 1000V per JESD22-C101
- Latchup testing is done to JESDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO14, TSSOP14

## DESCRIPTION

The PCA9542 is a 1-of-2 bi-directional translating multiplexer, controlled via the I<sup>2</sup>C-bus. The SCL/SDA upstream pair fans out to two SCx/SDx downstream pairs, or channels. Only one SCx/SDx channel is selected at a time, determined by the contents of the programmable control register. Two interrupt inputs, INT<sub>0</sub> and INT<sub>1</sub>, one for each of the SCx/SDx downstream pairs, are provided. One interrupt output, INT, which acts as an AND of the two interrupt inputs, is provided.

A power-on reset function puts the registers in their default state and initializes the I<sup>2</sup>C state machine with no channels selected.

## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
14-Pin Plastic SO	-40 °C to +85 °C	PCA9542D	SOT108-1
14-Pin Plastic TSSOP	-40 °C to +85 °C	PCA9542PW	SOT402-1

Standard packing quantities and other packaging data are available at [www.standardproducts.philips.com/packaging](http://www.standardproducts.philips.com/packaging).

The pass gates of the multiplexer are constructed such that the V<sub>DD</sub> pin can be used to limit the maximum high voltage which will be passed by the PCA9542. This allows the use of different bus voltages on each SCx/SDx pair, so that 1.8 V, 2.5 V, or 3.3 V parts can communicate with 5 V parts without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 5 V tolerant.

## PIN CONFIGURATION

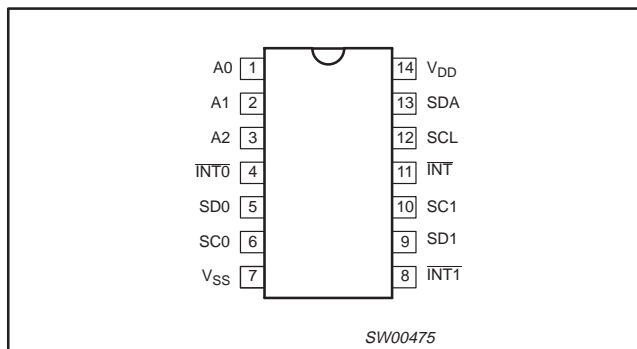


Figure 1. Pin configuration

## PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	A0	Address input 0
2	A1	Address input 1
3	A2	Address input 2
4	INT <sub>0</sub>	Active LOW interrupt input 0
5	SD0	Serial data 0
6	SC0	Serial clock 0
7	V <sub>SS</sub>	Supply ground
8	INT <sub>1</sub>	Active LOW interrupt input 1
9	SD1	Serial data 1
10	SC1	Serial clock 1
11	INT	Active LOW interrupt output
12	SCL	Serial clock line
13	SDA	Serial data line
14	V <sub>DD</sub>	Supply voltage

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## BLOCK DIAGRAM

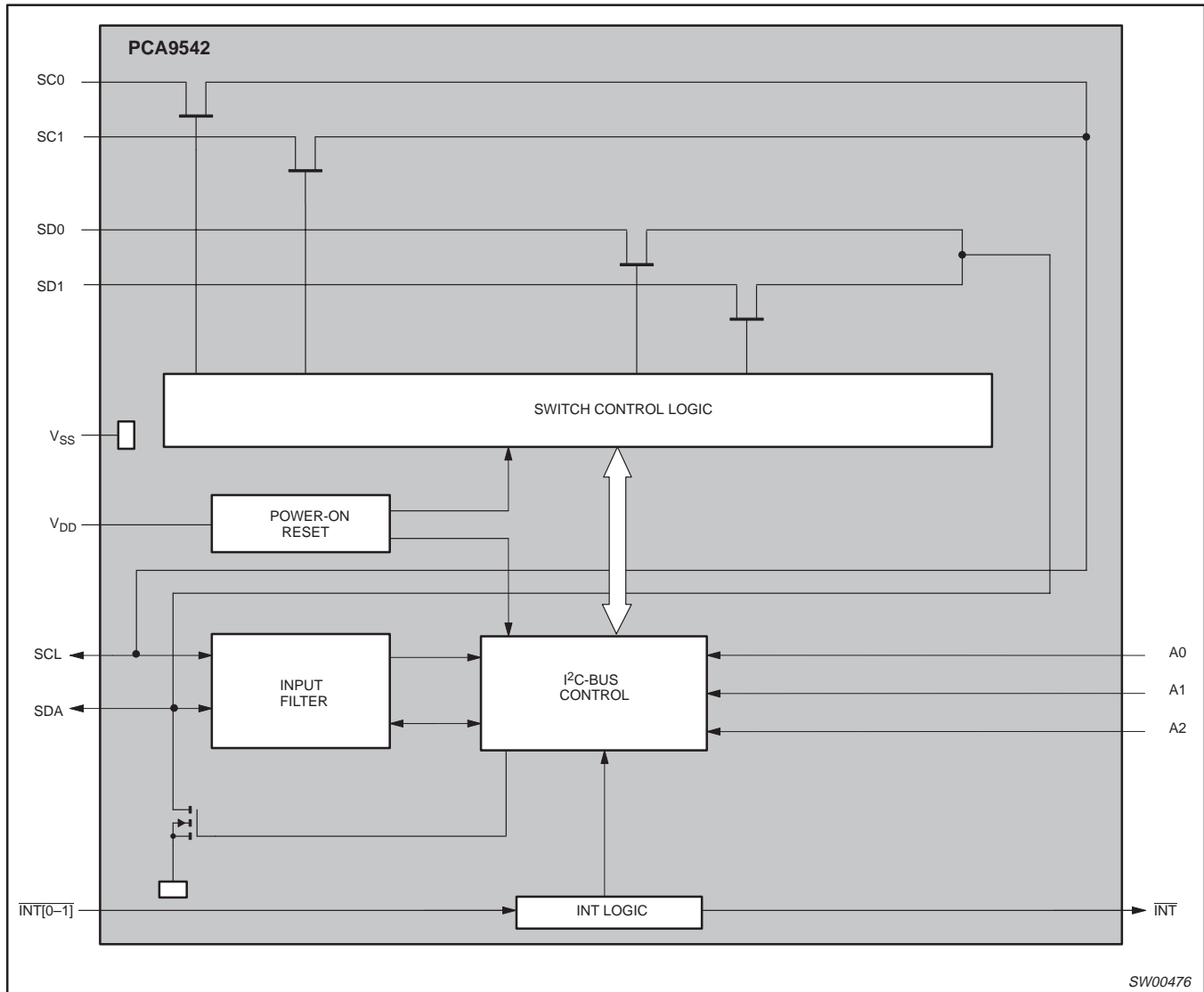


Figure 2. Block diagram

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## DEVICE ADDRESSING

Following a START condition the bus master must output the address of the slave it is accessing. The address of the PCA9542 is shown in Figure 3. To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.

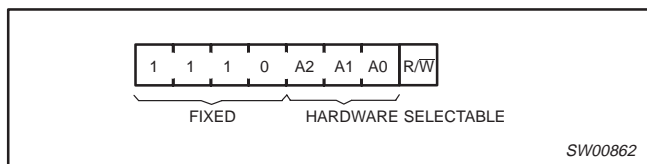


Figure 3. Slave address

The last bit of the slave address defines the operation to be performed. When set to logic 1, a read is selected while a logic 0 selects a write operation.

## CONTROL REGISTER

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PCA9542 which will be stored in the Control Register. If multiple bytes are received by the PCA9542, it will save the last byte received. This register can be written or read via the I<sup>2</sup>C-bus.

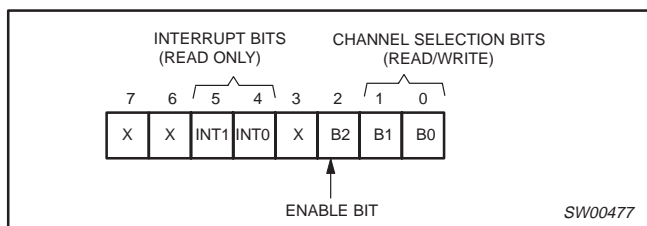


Figure 4. Control register

## CONTROL REGISTER DEFINITION

A SCx/SDx downstream pair, or channel, is selected by the contents of the control register. This register is written after the PCA9542 has been addressed. The 3 LSBs of the control byte are used to determine which channel is to be selected. When a channel is selected, it will become active after a Stop condition has been placed on the I<sup>2</sup>C-bus. This ensures that all SCx/SDx lines will be in a HIGH state when the channel is made active, so that no false conditions are generated at the time of connection.

Table 1. Control Register; Write — Channel Selection/  
Read — Channel Status

D7	D6	INT1	INT0	D3	B2	B1	B0	COMMAND
X	X	X	X	X	0	X	X	No channel selected
X	X	X	X	X	1	0	0	Channel 0 enabled
X	X	X	X	X	1	0	1	Channel 1 enabled
X	X	X	X	X	1	1	X	No channel selected
0	0	0	0	0	0	0	0	No channel selected; power-up default state

## POWER-ON RESET

When power is applied to V<sub>DD</sub>, an internal Power-On Reset holds the PCA9542 in a reset state until V<sub>DD</sub> has reached V<sub>POR</sub>. At this point, the reset condition is released and the PCA9542 registers and I<sup>2</sup>C state machine are initialized to their default states, all zeroes causing all the channels to be deselected.

## INTERRUPT HANDLING

The PCA9542 provides 2 interrupt inputs, one for each channel and one open drain interrupt output. When an interrupt is generated by any device, it will be detected by the PCA9542 and the interrupt output will be driven LOW. The channel need not be active for detection of the interrupt. A bit is also set in the control byte.

Bit 4 and Bit 5 of the control byte correspond to channel 0 and channel 1 of the PCA9542, respectively. Therefore, if an interrupt is generated by any device connected to channel 1, the state of the interrupt inputs is loaded into the control register when a read is accomplished. Likewise, an interrupt on any device connected to channel 0 would cause bit 4 of the control register to be set on the read. The master can then address the PCA9542 and read the contents of the control byte to determine which channel contains the device generating the interrupt. The master can then reconfigure the PCA9542 to select this channel, and locate the device generating the interrupt and clear it.

It should be noted that more than one device can be providing an interrupt on a channel, so it is up to the master to ensure that all devices on a channel are interrogated for an interrupt.

The interrupt inputs may be used as general purpose inputs if the interrupt function is not required.

If unused, interrupt input(s) must be connected to V<sub>DD</sub> through a pull-up resistor.

Table 2. Control Register; Read — Interrupt

D7	D6	INT1	INT0	D3	B2	B1	B0	COMMAND
0	0	X	0	X	X	X	X	No interrupt on channel 0
			1					Interrupt on channel 0
0	0	0	X	X	X	X	X	No interrupt on channel 1
								1

NOTE: The 2 interrupts can be active at the same time.

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**VOLTAGE TRANSLATION**

The pass gate transistors of the PCA9542 are constructed such that the  $V_{DD}$  voltage can be used to limit the maximum voltage that will be passed from one I<sup>2</sup>C-bus to another.

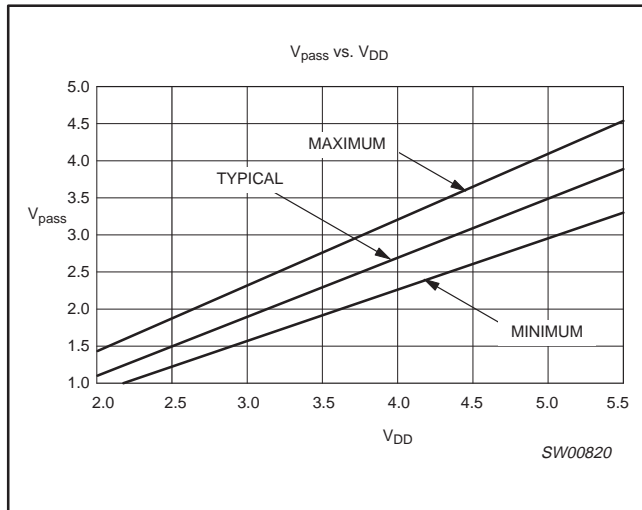


Figure 5.  $V_{pass}$  voltage

Figure 5 shows the voltage characteristics of the pass gate transistors (note that the graph was generated using the data specified in the DC Characteristics section of this datasheet). In order for the PCA9542 to act as a voltage translator, the  $V_{pass}$  voltage should be equal to, or lower than the lowest bus voltage. For example, if the main bus was running at 5 V, and the downstream buses were 3.3 V and 2.7 V, then  $V_{pass}$  should be equal to or below 2.7 V to effectively clamp the downstream bus voltages. Looking at Figure 5, we see that  $V_{pass}$  (max.) will be at 2.7 V when the PCA9542 supply voltage is 3.5 V or lower so the PCA9542 supply voltage could be set to 3.3 V. Pull-up resistors can then be used to bring the bus voltages to their appropriate levels (see Figure 12).

More Information can be found in Application Note AN262 *PCA954X family of I<sup>2</sup>C/SMBus multiplexers and switches*.

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## CHARACTERISTICS OF THE I<sup>2</sup>C-BUS

The I<sup>2</sup>C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

### Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 6).

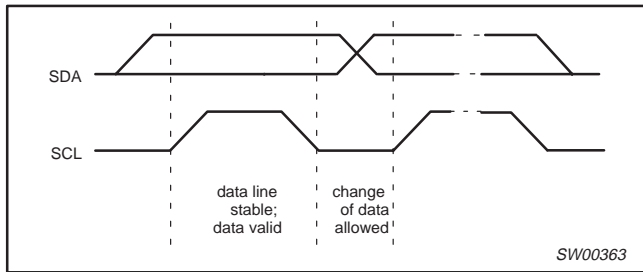


Figure 6. Bit transfer

## Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the Start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the Stop condition (P) (see Figure 7).

## System configuration

A device generating a message is a transmitter; a device receiving is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves (see Figure 8).

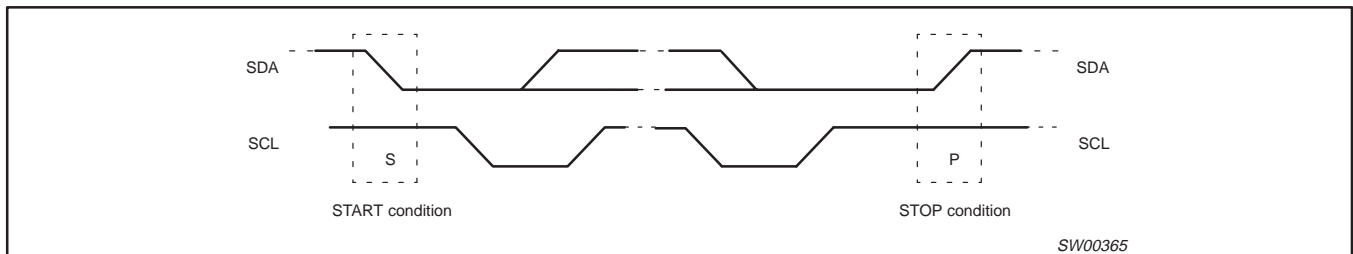


Figure 7. Definition of Start and Stop conditions

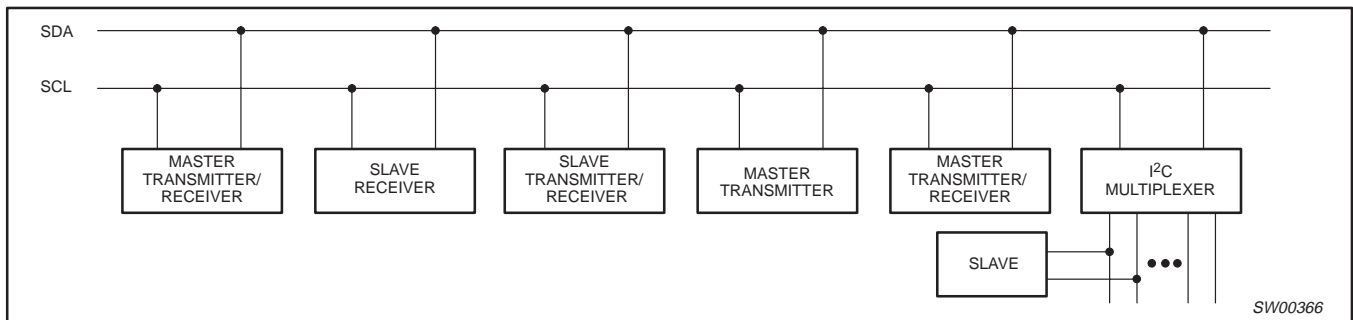


Figure 8. System configuration

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## Acknowledge

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

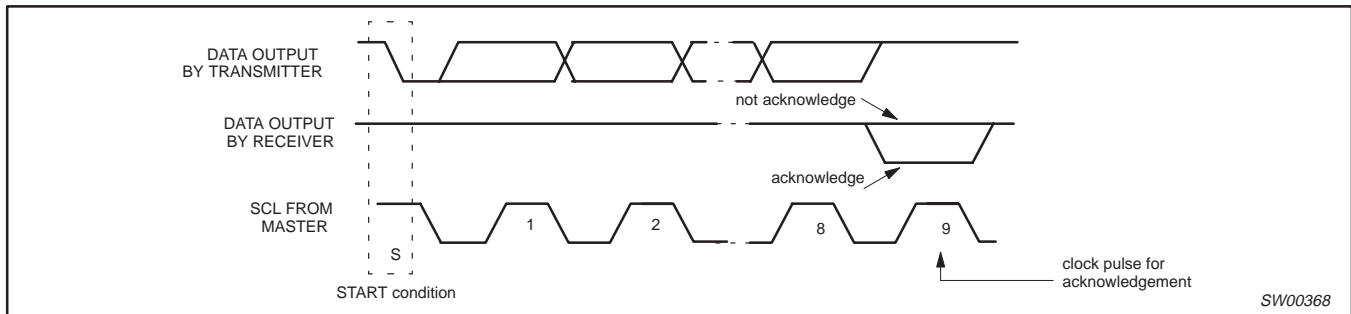


Figure 9. Acknowledgement on the I<sup>2</sup>C-bus

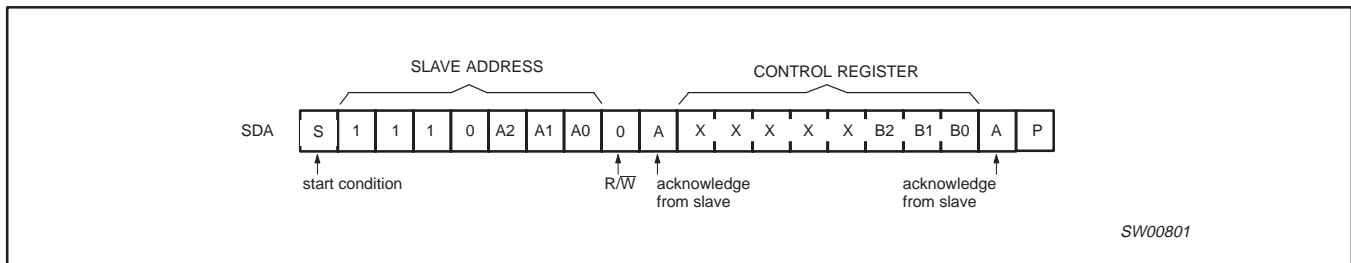


Figure 10. WRITE control register

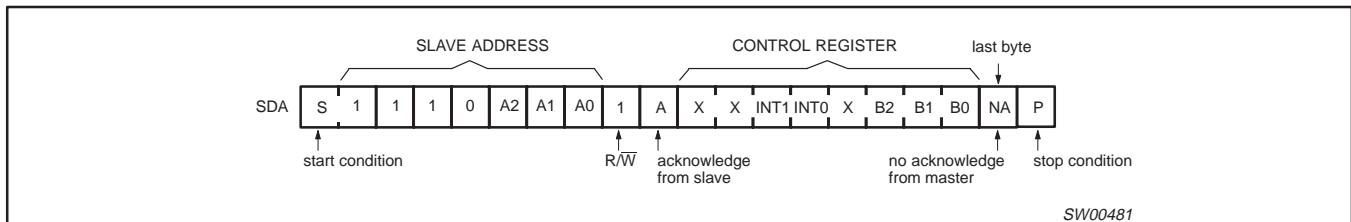


Figure 11. READ control register

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## TYPICAL APPLICATION

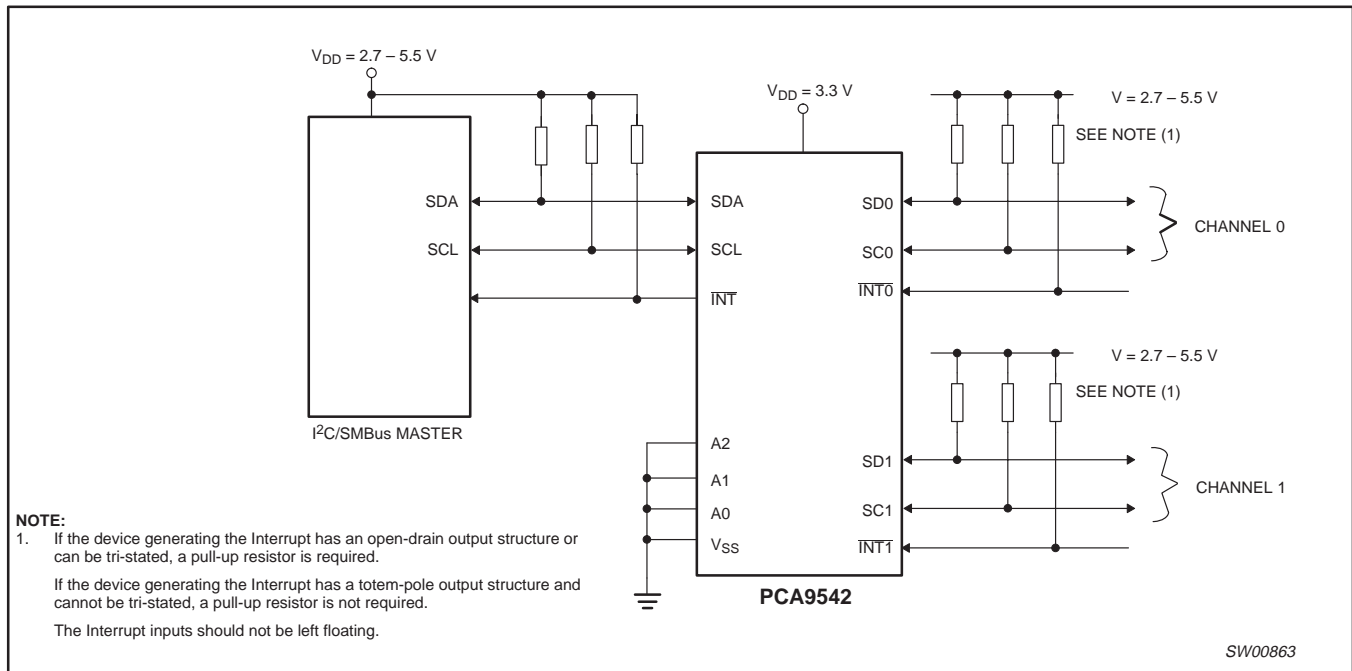


Figure 12. Typical Application



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**ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>**

In accordance with the Absolute Maximum Rating System (IEC 134). Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>DD</sub>	DC supply voltage		-0.5 to +7.0	V
V <sub>I</sub>	DC input voltage		-0.5 to +7.0	V
I <sub>I</sub>	DC input current		±20	mA
I <sub>O</sub>	DC output current		±25	mA
I <sub>DD</sub>	Supply current		±100	mA
I <sub>SS</sub>	Supply current		±100	mA
P <sub>tot</sub>	total power dissipation		400	mW
T <sub>stg</sub>	Storage temperature range		-60 to +150	°C
T <sub>amb</sub>	Operating ambient temperature		-40 to +85	°C

**NOTES:**

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

**DC CHARACTERISTICS**V<sub>DD</sub> = 2.3 V to 3.6 V; V<sub>SS</sub> = 0 V; T<sub>amb</sub> = -40 °C to +85 °C; unless otherwise specified. (See page 10 for V<sub>DD</sub> = 3.6 V to 5.5 V.)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
<b>Supply</b>						
V <sub>DD</sub>	Supply voltage		2.3		3.6	V
I <sub>DD</sub>	Supply current	Operating mode; V <sub>DD</sub> = 3.6 V; no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub> ; f <sub>SCL</sub> = 100 kHz	-	160	200	μA
I <sub>stb</sub>	Standby current	Standby mode; V <sub>DD</sub> = 3.6 V; no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub> ; f <sub>SCL</sub> = 0 KHz	-	25	100	μA
V <sub>POR</sub>	Power-on reset voltage	no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>	-	1.6	2.1	V
<b>Input SCL; input/output SDA</b>						
V <sub>IL</sub>	LOW-level input voltage		-0.5	-	0.3V <sub>DD</sub>	V
V <sub>IH</sub>	HIGH-level input voltage		0.7V <sub>DD</sub>	-	6	V
I <sub>OL</sub>	LOW-level output current	V <sub>OL</sub> = 0.4 V	3	-	-	mA
		V <sub>OL</sub> = 0.6 V	6	-	-	
I <sub>L</sub>	Leakage current	V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>	-1	-	+1	μA
C <sub>i</sub>	Input capacitance	V <sub>I</sub> = V <sub>SS</sub>	-	9	10	pF
<b>Select inputs A0, A1, A2, INT0, INT1</b>						
V <sub>IL</sub>	LOW-level input voltage		-0.5	-	+0.3V <sub>DD</sub>	V
V <sub>IH</sub>	HIGH-level input voltage		0.7V <sub>DD</sub>	-	V <sub>DD</sub> + 0.5	V
I <sub>LI</sub>	Input leakage current	V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>	-1	-	+1	μA
C <sub>i</sub>	Input capacitance	V <sub>I</sub> = V <sub>SS</sub>	-	1.6	3	pF
<b>Pass Gate</b>						
R <sub>ON</sub>	Switch resistance	V <sub>CC</sub> = 3.0 V to 3.6 V; V <sub>O</sub> = 0.4 V; I <sub>O</sub> = 15 mA	5	20	30	Ω
		V <sub>CC</sub> = 2.3 V to 2.7 V; V <sub>O</sub> = 0.4 V; I <sub>O</sub> = 10 mA	7	26	55	
V <sub>PASS</sub>	Switch output voltage	V <sub>swin</sub> = V <sub>DD</sub> = 3.3 V; I <sub>swout</sub> = -100 μA		2.2		V
		V <sub>swin</sub> = V <sub>DD</sub> = 3.0 V to 3.6 V; I <sub>swout</sub> = -100 μA	1.6		2.8	
		V <sub>swin</sub> = V <sub>DD</sub> = 2.5 V; I <sub>swout</sub> = -100 μA		1.5		
		V <sub>swin</sub> = V <sub>DD</sub> = 2.3 V to 2.7 V; I <sub>swout</sub> = -100 μA	1.1		2.0	
I <sub>L</sub>	Leakage current	V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>	-1	-	+1	μA
C <sub>io</sub>	Input/output capacitance	V <sub>I</sub> = V <sub>SS</sub>	-	3	5	pF
<b>INT Output</b>						
I <sub>OL</sub>	LOW-level output current	V <sub>OL</sub> = 0.4 V	3	-	-	mA
I <sub>OH</sub>	HIGH-level output current		-	-	+100	μA

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**DC CHARACTERISTICS**V<sub>DD</sub> = 3.6 V to 5.5 V; V<sub>SS</sub> = 0 V; T<sub>amb</sub> = -40 °C to +85 °C; unless otherwise specified. (See page 9 for V<sub>DD</sub> = 2.3 V to 3.6 V.)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
<b>Supply</b>						
V <sub>DD</sub>	Supply voltage		3.6		5.5	V
I <sub>DD</sub>	Supply current	Operating mode; V <sub>DD</sub> = 5.5 V; no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub> ; f <sub>SCL</sub> = 100 kHz	–	575	600	μA
I <sub>stb</sub>	Standby current	Standby mode; V <sub>DD</sub> = 5.5 V; no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub> ; f <sub>SCL</sub> = 0 kHz	–	80	200	μA
V <sub>POR</sub>	Power-on reset voltage	no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>	–	1.7	2.1	V
<b>Input SCL; input/output SDA</b>						
V <sub>IL</sub>	LOW level input voltage		–0.5	–	0.3V <sub>DD</sub>	V
V <sub>IH</sub>	HIGH level input voltage		0.7V <sub>DD</sub>	–	6	V
I <sub>OL</sub>	LOW level output current	V <sub>OL</sub> = 0.4 V	3	–	–	mA
		V <sub>OL</sub> = 0.6 V	6	–	–	mA
I <sub>IL</sub>	LOW level input current	V <sub>I</sub> = V <sub>SS</sub>	–10	–	10	μA
I <sub>IH</sub>	HIGH level input current	V <sub>I</sub> = V <sub>DD</sub>	–	–	100	μA
C <sub>i</sub>	Input capacitance	V <sub>I</sub> = V <sub>SS</sub>	–	9	10	pF
<b>Select inputs A0, A1, A2, INT0, INT1</b>						
V <sub>IL</sub>	LOW level input voltage		–0.5	–	+0.3V <sub>DD</sub>	V
V <sub>IH</sub>	HIGH level input voltage		0.7V <sub>DD</sub>	–	V <sub>DD</sub> + 0.5	V
I <sub>LI</sub>	Input leakage current	V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>	–1	–	+50	μA
C <sub>i</sub>	Input capacitance	V <sub>I</sub> = V <sub>SS</sub>	–	2	5	pF
<b>Pass Gate</b>						
R <sub>ON</sub>	Switch resistance	V <sub>CC</sub> = 4.5 V to 5.5 V; V <sub>O</sub> = 0.4 V; I <sub>O</sub> = 15 mA	4	11	24	Ω
V <sub>Pass</sub>	Switch output voltage	V <sub>swin</sub> = V <sub>DD</sub> = 5.0 V; I <sub>swout</sub> = –100 μA	–	3.5	–	V
		V <sub>swin</sub> = V <sub>DD</sub> = 4.5 V to 5.5 V; I <sub>swout</sub> = –100 μA	2.6	–	4.5	V
I <sub>L</sub>	Leakage current	V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>	–10	–	+100	μA
C <sub>io</sub>	Input/output capacitance	V <sub>I</sub> = V <sub>SS</sub>	–	3	5	pF
<b>INT Output</b>						
I <sub>OL</sub>	LOW level output current	V <sub>OL</sub> = 0.4 V	3	–	–	mA
I <sub>OH</sub>	HIGH level output current		–	–	+100	μA

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## AC CHARACTERISTICS

SYMBOL	PARAMETER	STANDARD-MODE I <sup>2</sup> C-BUS		FAST-MODE I <sup>2</sup> C-BUS		UNIT
		MIN	MAX	MIN	MAX	
t <sub>pd</sub>	Propagation delay from SDA to SD <sub>n</sub> or SCL to SC <sub>n</sub>	—	0.3 <sup>1</sup>	—	0.3 <sup>1</sup>	ns
f <sub>SCL</sub>	SCL clock frequency	0	100	0	400	kHz
t <sub>BUF</sub>	Bus free time between a STOP and START condition	4.7	—	1.3	—	μs
t <sub>HD;STA</sub>	Hold time (repeated) START condition After this period, the first clock pulse is generated	4.0	—	0.6	—	μs
t <sub>LOW</sub>	LOW period of the SCL clock	4.7	—	1.3	—	μs
t <sub>HIGH</sub>	HIGH period of the SCL clock	4.0	—	0.6	—	μs
t <sub>SU;STA</sub>	Set-up time for a repeated START condition	4.7	—	0.6	—	μs
t <sub>SU;STO</sub>	Set-up time for STOP condition	4.0	—	0.6	—	μs
t <sub>HD;DAT</sub>	Data hold time	0 <sup>2</sup>	3.45	0 <sup>2</sup>	0.9	μs
t <sub>SU;DAT</sub>	Data set-up time	250	—	100	—	ns
t <sub>R</sub>	Rise time of both SDA and SCL signals	—	1000	20 + 0.1C <sub>b</sub> <sup>3</sup>	300	ns
t <sub>F</sub>	Fall time of both SDA and SCL signals	—	300	20 + 0.1C <sub>b</sub> <sup>3</sup>	300	μs
C <sub>b</sub>	Capacitive load for each bus line	—	400	—	400	μs
t <sub>SP</sub>	Pulse width of spikes which must be suppressed by the input filter	—	50	—	50	ns
t <sub>VD;DATL</sub>	Data valid (HL)	—	1	—	1	μs
t <sub>VD;DATH</sub>	Data valid (LH)	—	0.6	—	0.6	μs
t <sub>VD;ACK</sub>	Data valid Acknowledge	—	1	—	1	μs
<b>INT</b>						
t <sub>iv</sub>	INT <sub>n</sub> to INT active valid time	—	4	—	4	μs
t <sub>ir</sub>	INT <sub>n</sub> to INT inactive delay time	—	2	—	2	μs
L <sub>pwr</sub>	LOW level pulse width rejection or INT <sub>n</sub> inputs	1	—	1	—	μs
H <sub>pwr</sub>	HIGH level pulse width rejection or INT <sub>n</sub> inputs	0.5	—	0.5	—	μs

**NOTES:**

1. Pass gate propagation delay is calculated from the 20 Ω typical R<sub>ON</sub> and and the 15 pF load capacitance.
2. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V<sub>IHmin</sub> of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
3. C<sub>b</sub> = total capacitance of one bus line in pF.

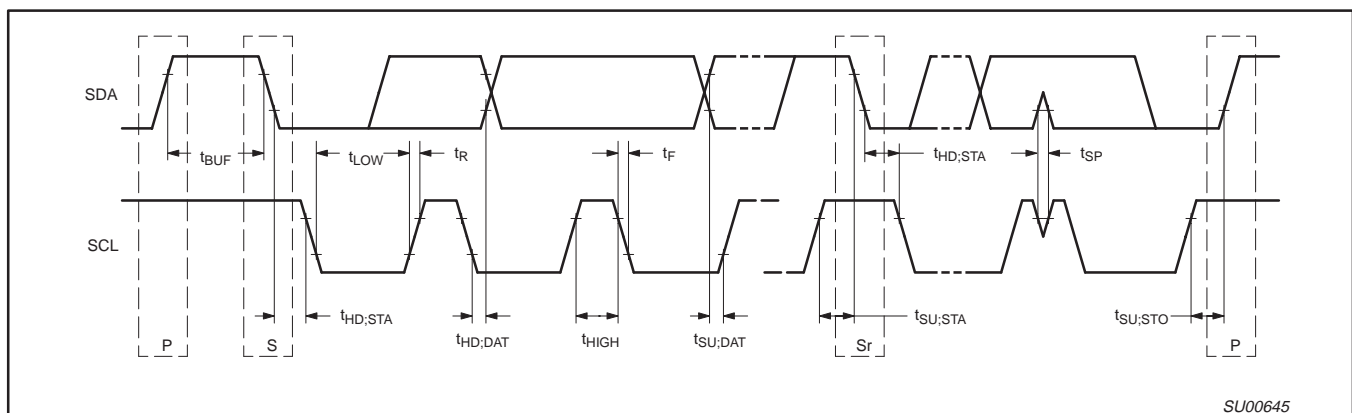


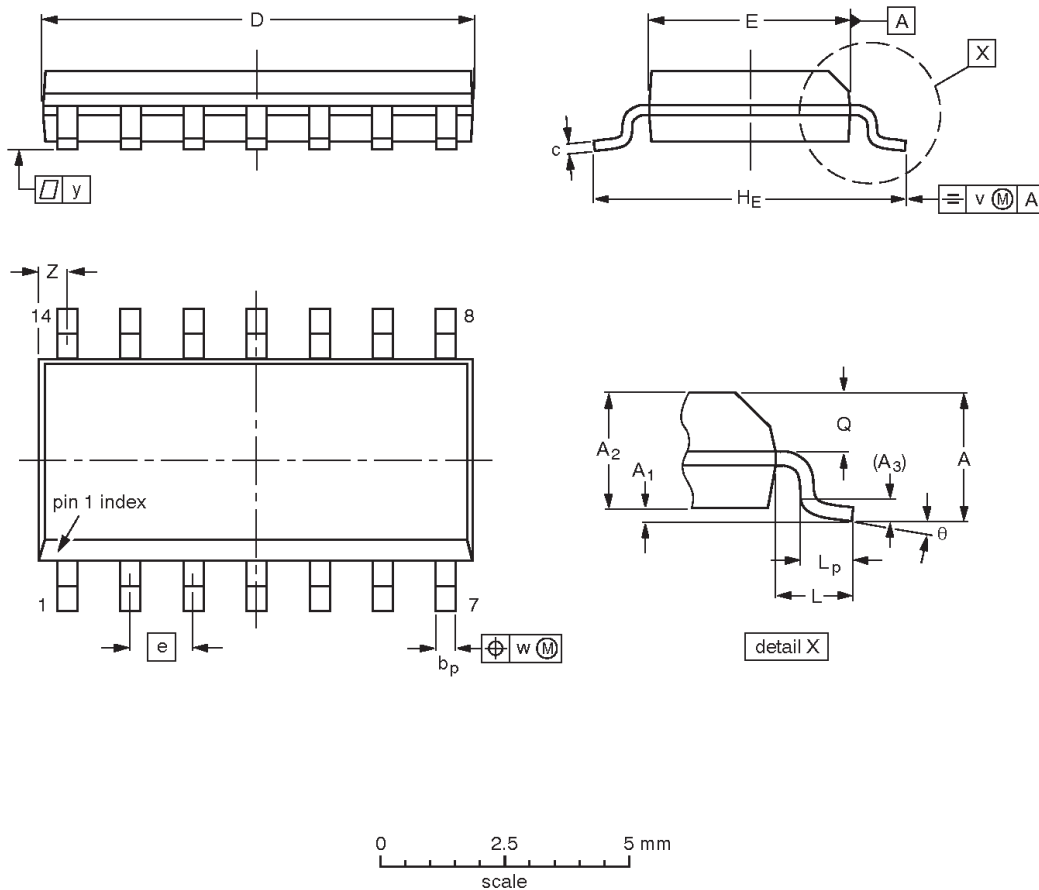
Figure 13. Definition of timing on the I<sup>2</sup>C-bus

# 2-channel I<sup>2</sup>C multiplexer and interrupt logic

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SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

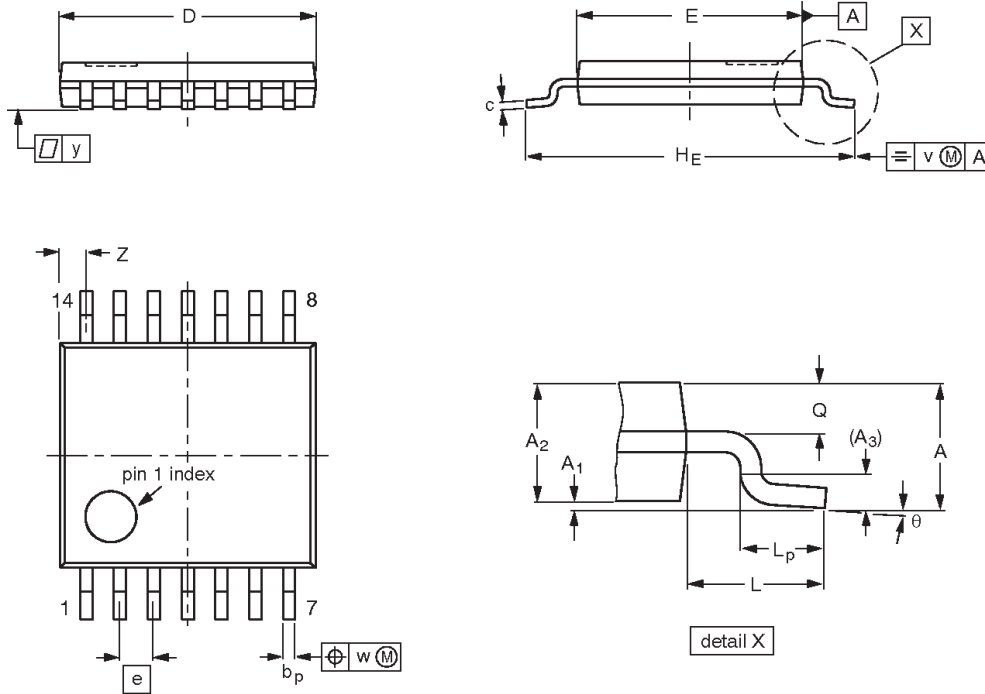
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				99-12-27 03-02-19

# 2-channel I<sup>2</sup>C multiplexer and interrupt logic

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**TSSOP14:** plastic thin shrink small outline package; 14 leads; body width 4.4 mm

**SOT402-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				-99-12-27 03-02-18

2-channel I<sup>2</sup>C multiplexer and interrupt logic

PCA9542

## REVISION HISTORY

Rev	Date	Description
_7	20041001	<b>Product data sheet (9397 750 14111). Supersedes data of 2002 Mar 28 (9397 750 09607).</b> Modifications: <ul style="list-style-type: none"><li>• Table 1 "Control Register; Write—Channel Selection / Read—Channel Selection" on page 4: add 'No channel selected; power-up default state' row to bottom of table.</li></ul>
_6	20020328	<b>Product data (9397 750 09607). ECN 853–2177 27939 of 28 March 2002.</b> <b>Supersedes data of 2001 May 07.</b>
_5	20010507	

2-channel I<sup>2</sup>C multiplexer and interrupt logic

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Purchase of Philips I<sup>2</sup>C components conveys a license under the Philips' I<sup>2</sup>C patent to use the components in the I<sup>2</sup>C system provided the system conforms to the I<sup>2</sup>C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

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Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2] [3]</sup>	Definitions
I	Objective data sheet	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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## Contact information

For additional information please visit  
<http://www.semiconductors.philips.com>. Fax: +31 40 27 24825

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For sales offices addresses send e-mail to:  
[sales.addresses@www.semiconductors.philips.com](mailto:sales.addresses@www.semiconductors.philips.com)

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