# Clock generator IC **BU2288FV**

The BU2288FV is an IC that generates plural clocks required for DVD system from a 2-channel PLL external crystal oscillator. The six kinds of signals for video and audio system are generated with low jitter.

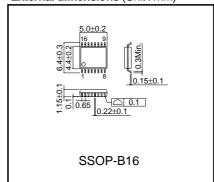
### Application

All DVD sets

#### Features

- 1) All clock signals needed for DVD can be generated by a single chip.
- 2) All output low jitter (No load 30psec)
- 3) No need for additional components. (BU2288FV has a PLL loop filter inside.)
- 4) 3.3V single power supply
- 5) Small SSOP-B16 package.

#### ●External dimensions (Unit: mm)



## ◆Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Applied voltage	VDD	-0.5 to +7.0	V
Input voltage	Vin	-0.5 to VDD+0.5	V
Storage temperature range	Tstg	-30 to +125	°C
Power dissipation	Pd	450	mW

- \* An operation is not guaranteed.

  \* In case it is used at Ta=25°C or more, 4.5mW is reduced at every1°C.

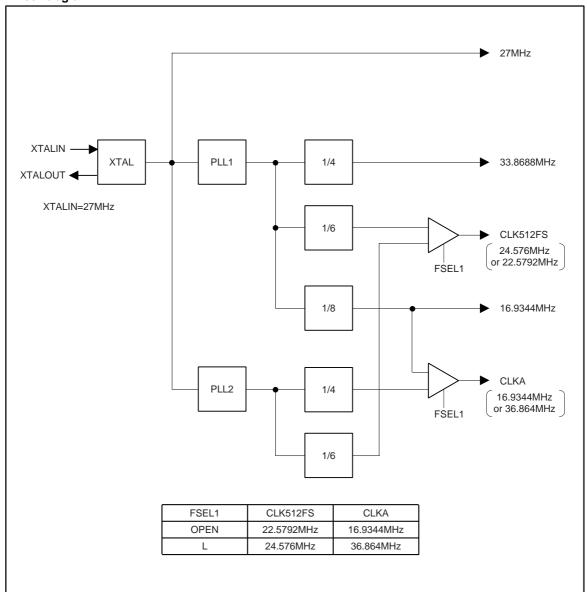
  \* Radiation resistance design is not used.

  \* Power dissipation is measured when BU2288FV is placed on the board.

# ●Recommended operating conditions (Ta=25°C)

Parameter	Symbol	Min.	Тур.	Max.	Unit
Supply voltage	Vdd	3.0	-	3.6	V
Input "H" voltage range	VIH	0.8Vpd	_	VDD	V
Input "L" voltage range	VIL	0	_	0.2Vdd	V
Operation temperature range	Topr	-5	-	70	°C
Output maximum load	CL	_	_	15	pF

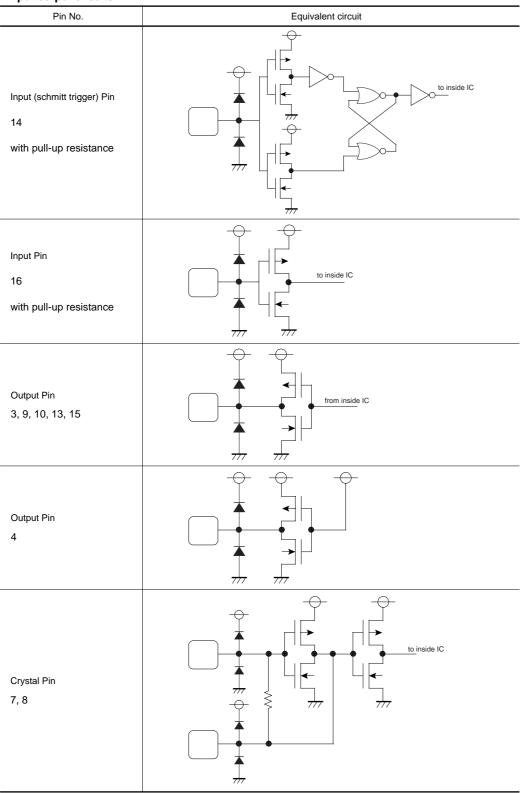
## Block diagram



# Pin descriptions

Pin No.	Pin name	Functions		
1	VDD2	Digital VDD for 27MHz clock output		
2	Vss2	Digital GND for 27MHz clock output		
3	CLK27M	27MHz clock output		
4	TEST	Output for test		
5	AVDD	Analog Vdd		
6	AVss	Analog GND		
7	XTALout	Standard crystal output		
8	XTALIN	Standard crystal input		
9	CLKA	Clock output (FSEL1=Open: 16.9344MHz, FSEL1=L: 36.864MHz)		
10	CLK512FS	Clock output (FSEL1=Open: 22.5792MHz, FSEL1=L: 24.576MHz)		
11	DVss	Digital GND		
12	DVDD	Digital VDD		
13	CLK16M	16.9344MHz clock output		
14	FSEL1	Output select : with pull-up Open : 16.9344MHz (Pin9), 22.5792MHz (Pin10) L : 36.864MHz (Pin9), 24.576Mhz (Pin10)		
15	CLK33M	33.8688MHz clock output		
16	OE	Output enable (open : enable, L : disable) : with pull-up		

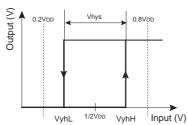
# ●Input output circuits



# ● Electrical characteristics (Unless specified otherwise Ta=25°C, VDD=3.3V, crystal frequency=27MHz)

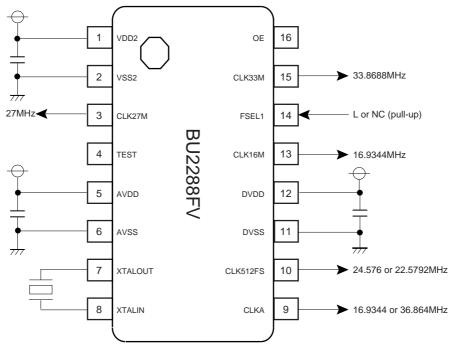
Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Output "H" voltage	Voн	2.4	_	-	V	IOH=-4.0mA
Output "L" voltage	Vol	_	_	0.4	V	IoL=4.0mA
FSEL Input VthL *3	VthL	0.2Vdd	_	-	V	*1
FSEL Input VthH *3	VthH	_	_	0.8Vpd	V	*1
Hysteresis width *3	Vhys	0.2	_	-	V	Vhys=VthH-VthL
Power supply current	IDD	_	27	40.5	mA	no load
CLK512FS	CLK512-A	_	22.5792	-	MHz	FSEL1=OPEN, XTAL *3136/625/6
	CLK512-B	_	24.576	-	MHz	FSEL1=L, XTAL *2048/375/6
CLK33M	CLK33M	_	33.8688	-	MHz	XTAL *3136/625/4
CLK16M	CLK16M	_	16.9344	-	MHz	XTAL *3136/625/8
CLK27M	CLK27M	_	27	_	MHz	XTAL output
CLK A	CLKA-A	_	16.9344	_	MHz	FSEL1=OPEN, XTAL *3136/625/8
	CLKA-B	_	36.864	_	MHz	FSEL1=L, XTAL *2048/375/4
Duty	Duty	45	50	55	%	1/2 VDD test
Jitter 1σ	JsSD	_	70	_	psec	Jitter 1sigma
Jitter MIN-MAX	JsABS	_	420	_	psec	MIN-MAX level
Rise time	tr	_	2.5	_	nsec	Time between 0.2VDD~0.8VDD
Fall time	tf	_	2.5	_	nsec	Time between 0.8Vpp~0.2Vpp
Output Lock time	tlock	_		1	msec	*2

Note: JITTER is mean value when using Time Interval Analyzer with 10,000 sampling \*1) graph



<sup>\*2)</sup> Time between voltage supply leads to 3.0V and output clock gats stable. Start up time of power supply sources satisfy this rated value at every time, case

## Application example



Note: The BU2288FV is basically placed on the board

Decoupling capacitance (0.1 $\mu$ F) need to be placed between Pin5 (AVDD) and Pin6 (AVSS).

Also Decoupling capacitance (0.1 $\mu$ F) need to be placed between Pin1 (VDD2) and Pin2 (VSS2), Pin11 (DVSS) and Pin12 (DVDD).

To obtain accurate frequency, capacitance (pF) need to be placed between Pin8 (XTALIN) and Pin6 (AVSS), Pin7 (XTALOUT) and Pin6 (AVSS).

Tantalum capacitance ( $10 \sim 100 \mu F$ ), ferrite beads may need to be placed to prevent power supply drop in certain boards case.

To reduce high frequency noise, selected bypass capacitors ( $\leq 1\Omega$  at problem high frequency) maybe used for power pin as close to BU2288FV as possible.

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