MC804256K32, MC804256K36

256Kx32, 256Kx36 Flow-Through Synchronous Burst SRAM

- **High performance, low power flow-through SRAM**
  - Ultra low power for high capacity applications
- **High performance**
  - 66, 83, 100 MHz Speed grades
  - 2-1-1-1 Burst Read
  - 1-1-1-1 Burst Write
  - 2-1-1-1-1-1-1-1... burst operation
- **Low power**
  - Low active power
  - Ultra low power ZZ standby mode
  - Single 3.3V supply (VDD)
  - Isolated 3.3V or 2.5V I/O supply (VDDQ)
- **Compatibility**
  - Individual Byte Write and Global Write masking
  - Interleave and burst address support
  - Two chip enables for easy expansion
  - Industry standard 100-Pin SRAM pinout
  - Industry standard SRAM specification
- **Applications**
  - Ideal for high speed, low power communications buffers
  - Power sensitive portable DSP applications

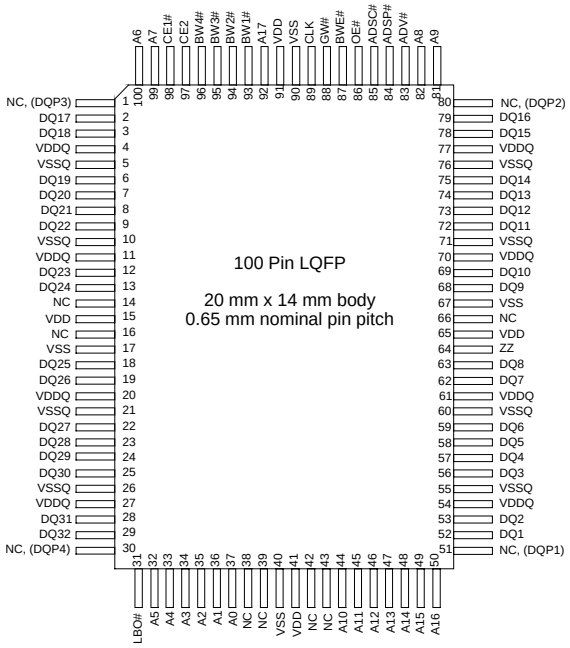


Figure 1. Pin Function

Overview

The MoSys MC804256K is a low power flow-through synchronous SRAM. Fabricated using an advanced low power, high performance CMOS process, the MoSys MC804256K is forward pin and function compatible with standard 32Kx32/36, 64Kx32/36 and 128Kx32/36 SRAM devices. These devices also include additional operating features like low power ZZ standby mode and linear burst order addressing. These additional operating features are defined so that, with proper implementation, designs can work transparently with 32Kx32/36, 64Kx32/36, 128Kx32/36 and 256Kx32/36 configurations. This allows the designer maximum configuration flexibility within a single footprint layout.

The MoSys MC804256K32/36 supports flow-through SRAM operating modes at maximum burst frequency including indefinite pipeline read or write (2-1-1-1-1-1-1...)

Parameter	Symbol	-15	-12	-10	Units
Cycle Time	tKC	15	12	10	ns
Access Time	tKQ	10	9	8.5	ns
Clock to High-Z	tKQHZ	8.6	7.5	5	ns

The MC804256K is packaged in a standard 100-pin LQFP.

Lowest Power

The MC804256K flow-through SRAM affords systems dramatic power savings due to the benefits of its proprietary MoSys technology. Peak operating power of a typical SRAM is 5x that of the MC804256K. This makes it ideal for portable applications as well as applications requiring a large amount of static RAM.

Part Number Designation

Example*: MC804256K32L-15 I*
Device Designation: *MC8*:, Series: *04*
Organization: *256K32, 256K36*
Package Type: *L*=LQFP
Speed: – 15 66 MHz
– 12 83 MHz
– 10 100 MHz
Temp: *I* = Industrial Temperature, optional

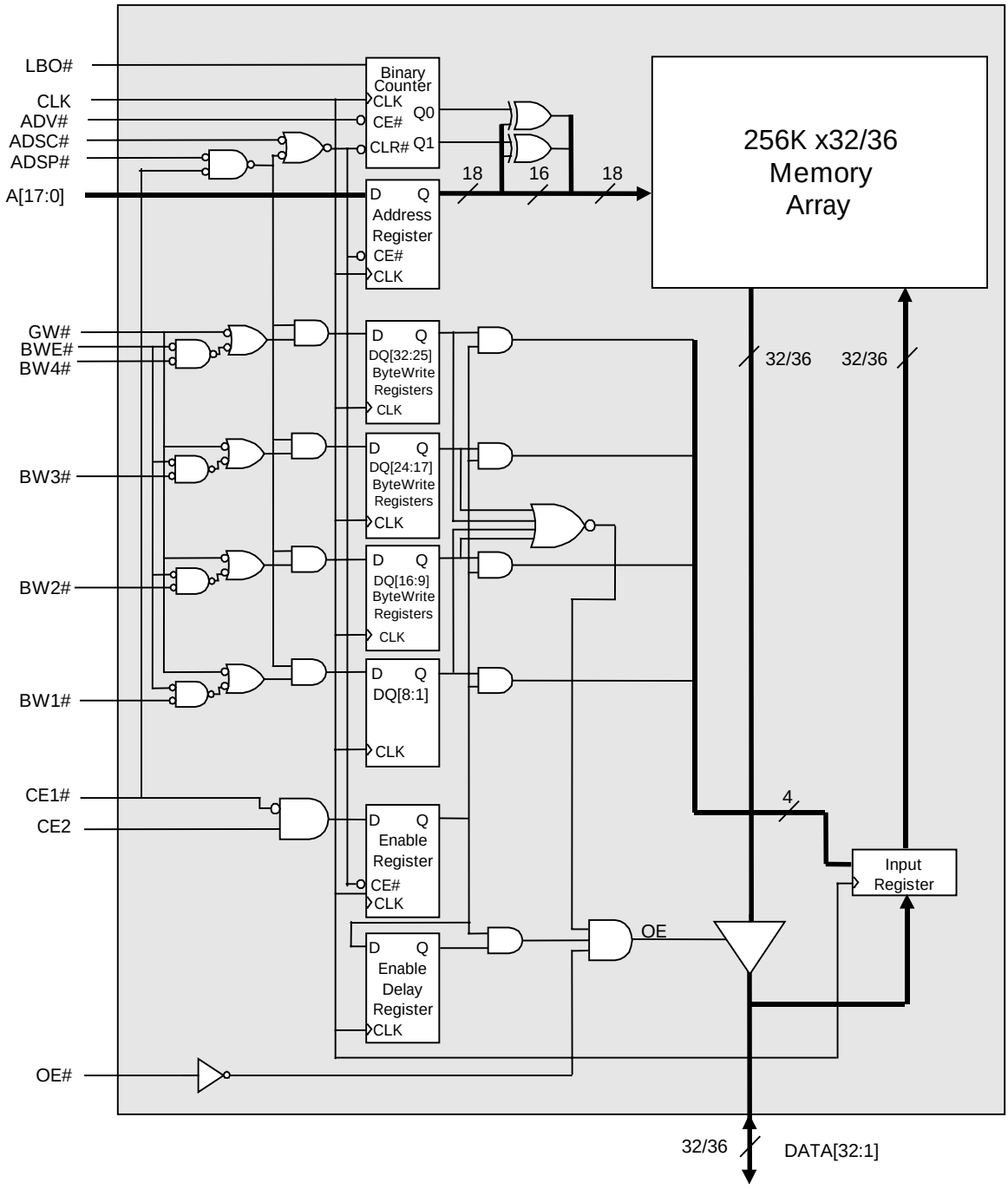


Figure 2 Functional Block Diagram

Table 1. Pin Description

Pin Number	Symbol	Type	Description
92, 50, 49, 48, 47, 46, 45, 44, 81, 82, 99, 100, 32, 33, 34, 35, 36, 37	A[17:0]	Input	Host Addresses
96, 95, 94, 93	BW[4:1]#	Input	Processor host bus byte enables.
88	GW#	Input	Global Write from cache controller
87	BWE#	Input	Byte Write Enable from controller
89	CLK	Input	Host bus clock
98	CE1#	Input	ADSP# mask and ADSC# chip enable
97	CE2	Input	Depth expansion chip enable
86	OE#	Input	Asynchronous output enable
83	ADV#	Input	Burst address counter advance
84	ADSP#	Input	ADS# of processor
85	ADSC#	Input	ADS# of controller
64	ZZ	Input	Low power sleep mode
31	LBO#	Input	Linear Burst Order
29, 28, 25, 24, 23, 22, 19, 18, 13, 12, 9, 8, 7, 6, 3, 2, 79, 78, 75, 74, 73, 72, 69, 68, 63, 62, 59, 58, 57, 56, 53, 52	DQ[32:1]	I/O	Data I/O pins
30, 1, 80, 51	NC/DQP[4:1]	I/O	Data parity I/O pins
14, 16, 38, 39, 42, 43, 66	NC	-	unused
15, 41, 65, 91	VDD	3.3 Volts	Power
17, 40, 67, 90	VSS	Ground	Ground
4, 11, 20, 27, 54, 61, 70, 77	VDDQ	I/O Supply	I/O Buffer Supply
5, 10, 21, 26, 55, 60, 71, 76	VSSQ	I/O Ground	I/O Buffer Ground

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{DD}	Core Supply Voltage		4.0	V
V_{DDQ}	I/O Supply Voltage		V_{DD}	V
V_{ih}	Input High Voltage		V_{DDQ} +0.5	V
V_{il}	Input Low Voltage	V_{SSQ} - 0.5		V
Ts	Storage Temperature	-65	150	°C

Notes: Max Vih is not to exceed maximum VDDQ

Table 3. Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Max	Units
V_{DD}	Supply Voltage	3.3V ±5%	3.135	3.465	V
V_{DDQ}	I/O Supply Voltage	2.5V +38%/-5%	2.375	3.465	V
V_{ih}	Input High Voltage		1.8	V_{DDQ} + 0.3	V
V_{il}	Input Low Voltage		-0.3	0.8	V
V_{oh}	Output High Voltage	I_{oh} = -5 mA	2.4		V
V_{ol}	Output Low Voltage	I_{ol} = 5 mA		0.4	V
T_{AC}	Commercial Operating Temp.		0	70	°C
T_{AI}	Industrial Operating Temp.		-40	85	°C

Table 4. Absolute Maximum AC Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{ih}	Input High Voltage	1.8	V_{DDQ}+1.0	V
V_{il}	Input Low Voltage	V_{SSQ} - 1.0	0.8	V
tOVR	Overshoot/Undershoot Voltage Duration		0.2*tCY	ns
tSET	Overshoot/Undershoot Settling Time		0.8*tCY	ns

Table 5. Maximum DC Current Requirements

Symbol	Condition	Current	Units
I_{DD}	Operating current, device selected; all inputs ≤ Vil or ≥ Vih; cycle time ≥ tKC min, V_{DD}= max, 0 pF load	50	mA
I_{DD1}	Idle current, device deselected; ADSP#, ADSC#, GW#, BW#s, ADV# and all other inputs except ZZ ≥ 2.8 volts; cycle time ≥ tKC min, V_{DD}= max, 0 pF load	10	mA
I_{DDZ}	Sleep mode, clock stopped, all inputs ≥ 2.8 v, V_{DD}= max	2	mA

Table 6. AC Timing Characteristics at Recommended Operating Conditions

		-10 (100 MHz)		-12 (83 MHz)		-15 (66 MHz)		
Sym	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
tAAH	ADV# hold	0.5		0.5		0.5		ns
tAAS	ADV# setup	2		2		2		ns
tADSH	ADSx# hold	0.5		0.5		0.5		ns
tADSS	ADSx# setup	2		2		2		ns
tAH	Address hold	0.5		0.5		0.5		ns
tAS	Address setup	2		2		2		ns
tCEH	Chip Enable hold	0.5		0.5		0.5		ns
tCES	Chip Enable setup	2		2		2		ns
tDH	Write Data hold	0.5		0.5		0.5		ns
tDS	Write Data setup	2		2		2		ns
tKC	Clock cycle	10		12		15		ns
tKH	Clock high	4.5		5.5		6.5		ns
tKL	Clock low	4.5		5.5		6.5		ns
tKQ	Clock to output valid		8.5		9		10	ns
tKQHZ	Clock to output high-Z	1.5	5.0	1.5	7.5	1.5	8.6	ns
tKQLZ	Clock to output low-Z	0		0		0		ns
tKQX	Clock to output invalid	1.5		1.5		1.5		ns
tOELZ	OE# to output low-Z	0		0		0		ns
tOEHZ	OE# to output high-Z		3.5		4.5		4.8	ns
tOEQ	OE# to output valid		3.5		4.5		4.8	ns
tOEQX	OE# to output invalid	0		0		0		ns
tWS	GW#, BWx# setup	2		2		2		ns
tWH	GW#, BWx# hold	0.5		0.5		0.5		ns
tZZs	ZZ standby		100		100		100	ns
tZZREC	ZZ recovery	100		100		100		

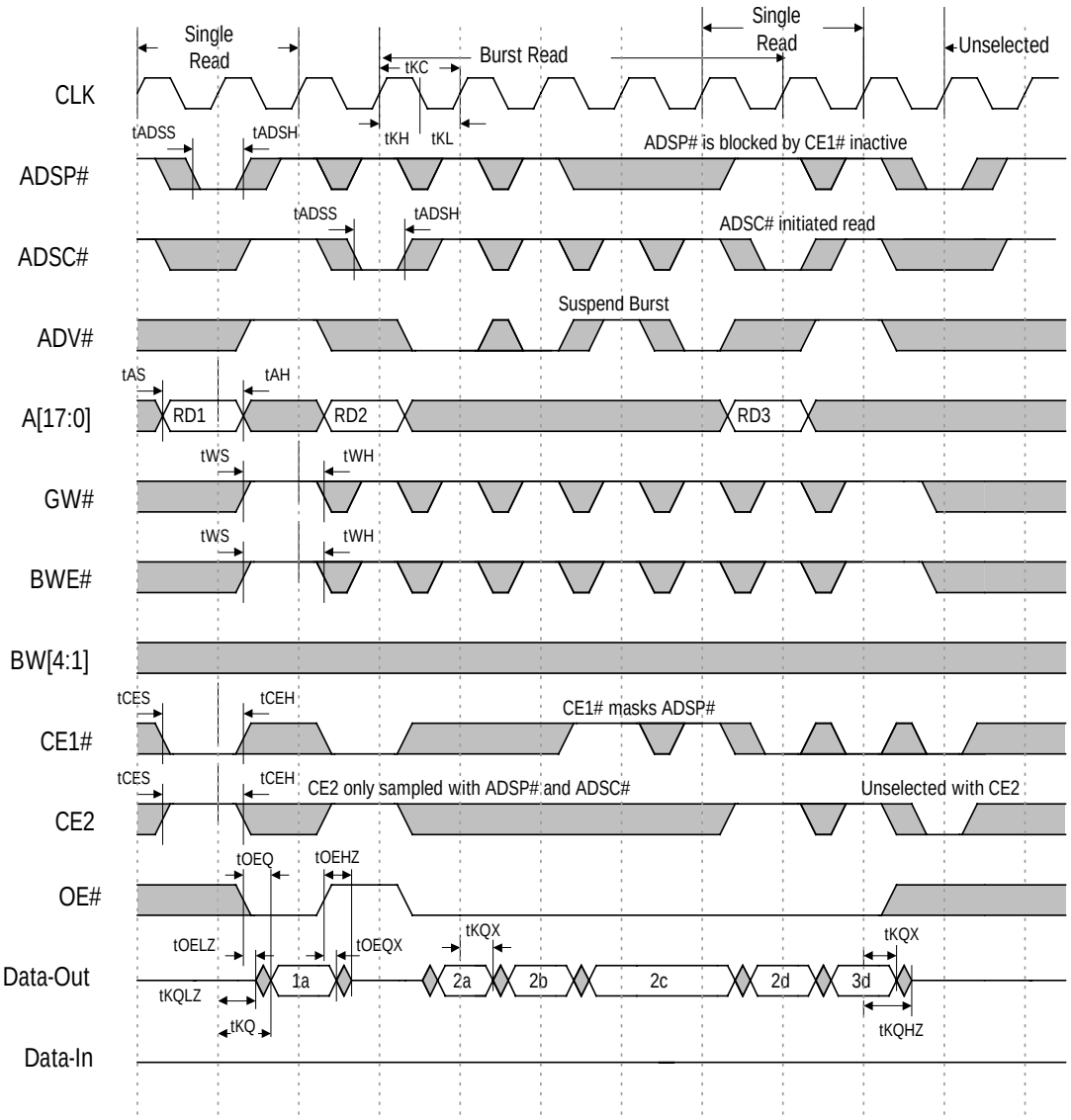


Figure 3 Read Cycle Timing

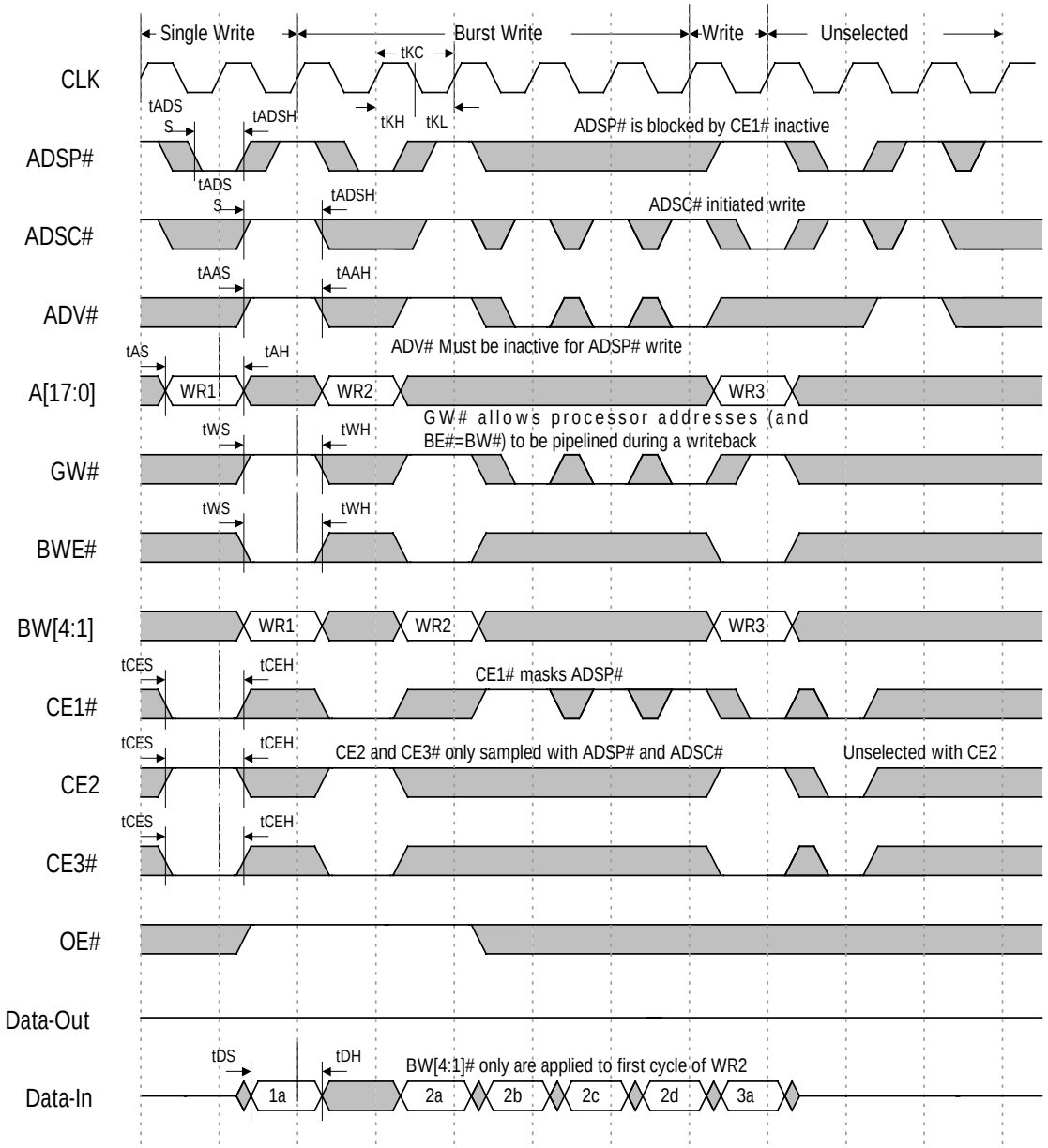


Figure 4 Write Cycle Timing

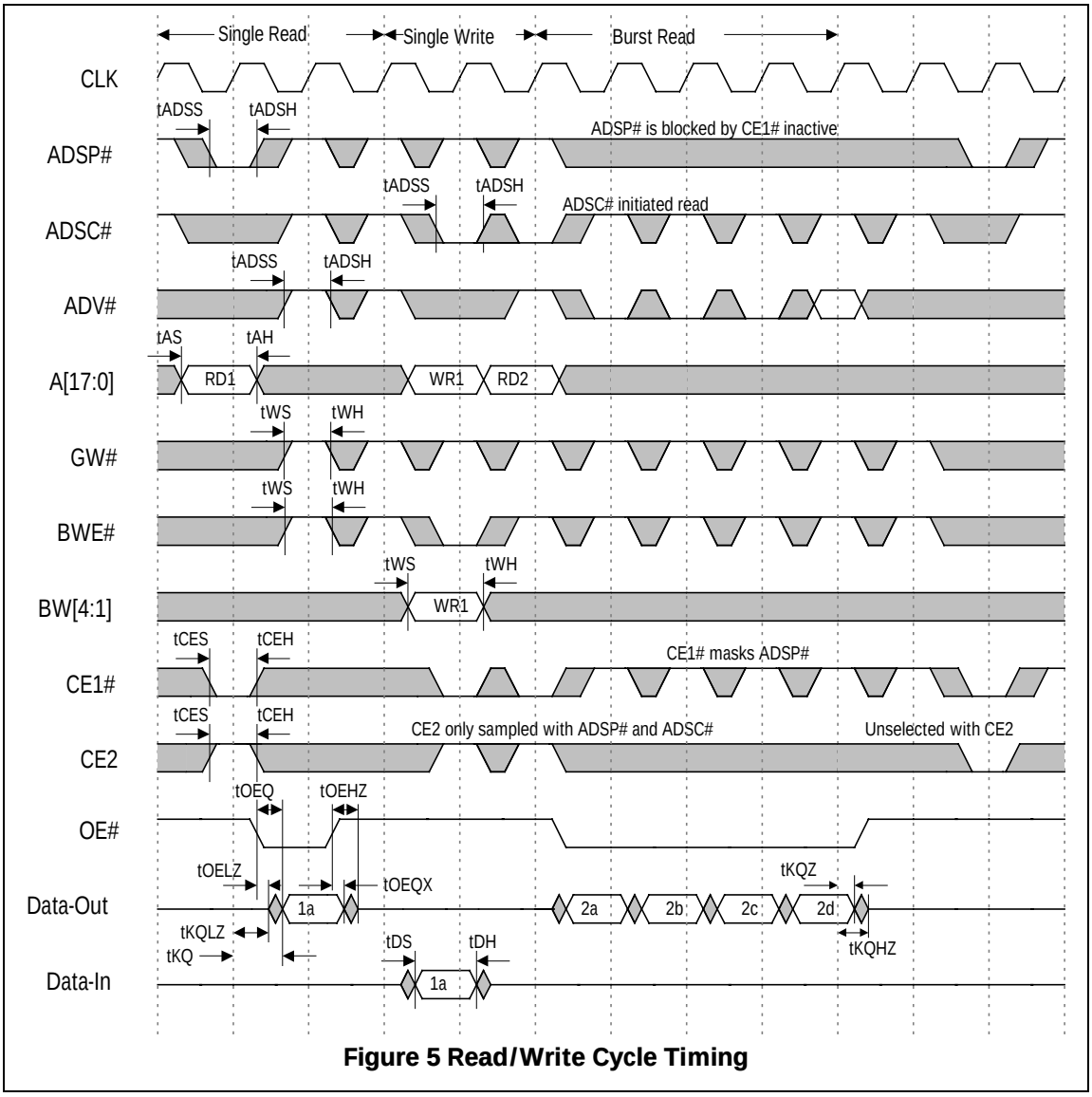


Figure 5 Read/Write Cycle Timing

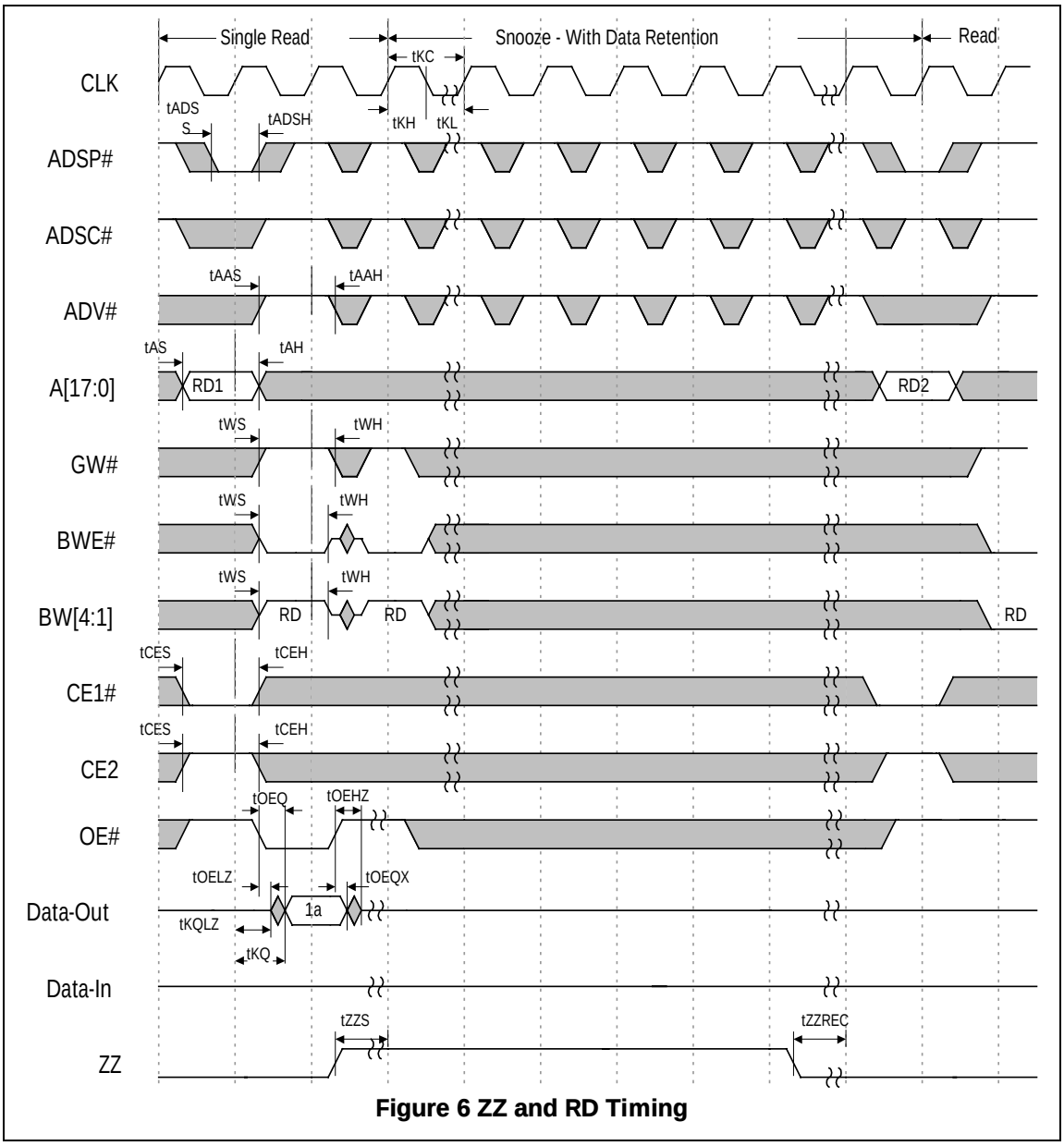
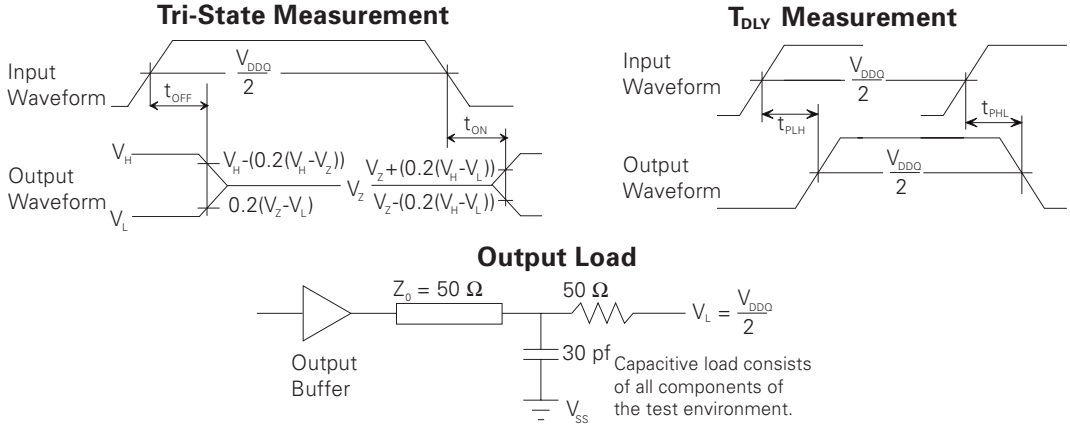


Figure 6 ZZ and RD Timing

Test and Measurement



Test Structure and Measurement Points

Notes

1 Valid Delay Measurement is made from the VDDQ / 2 on the input waveform to the VDDQ / 2 on the output waveform. Input waveform should have a slew rate of 1V/ns.

2 Tri-state t_{off} measurement is made from the VDDQ/2 on the input waveform to the output waveform moving 20% from its initial to final value VDDQ/2.

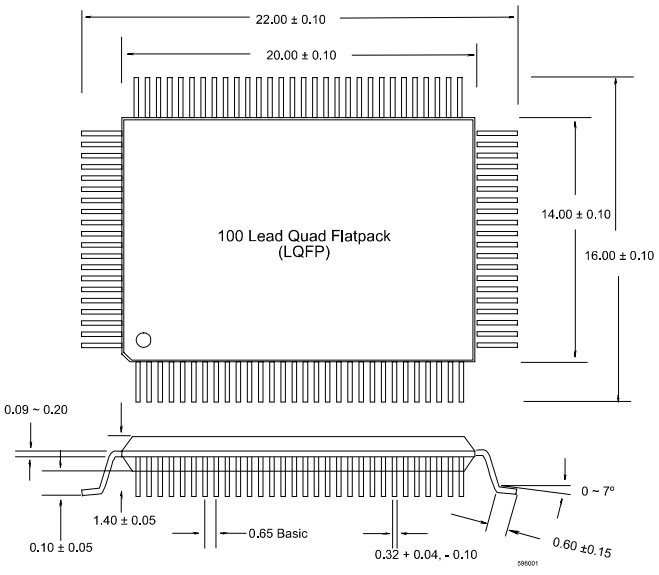


Figure 7. LQFP Mechanical Characteristics