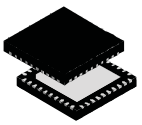
STMPE1218

12-channel capacitive touch key controller with 4-channel PWM controller

Preliminary data

Features

- 12 capacitive sensor inputs
- 12-bit general purpose input/output (GPIO)
- Configurable automatic impedance calibration
- Operating voltage 2.7 V –5.5 V
- 4-channel PWM controller with programmable blinking and fading
- 8 mA output on GPIO for LED driving
- I^2C interface (up to 400 kHz)
- 8 kV HBM ESD protection
- 50 fF sensitivity
- 128 steps capacitance measurement (6.0 pf dynamic range)
- Sleep mode for low power operation
- Advanced data filtering (AFS)
- Environment tracking calibration (ETC)
- Individually adjustable touch variance (TVR) setting for all channels
- Adjustable environmental variance (EVR) for optimal calibration



QFN40

Applications

- Portable media players
- Game consoles
- Mobile and smart phones

Description

The STMPE1218 is a GPIO 12-channel capacitive sensor able to interface a main digital ASIC via the two-line bidirectional bus (I^2C). It senses changes in capacitance using a fully digital architecture, giving fast and accurate results at very low power consumption. Environment tracking calibration ensures that changes in environment will never affect the correct operation of the capacitive touch keys.

Table 1. Device summary

Order code	Package	Packing
STMPE1218QTR	QFN40	Tape and reel

Contents

1 Pin configuration and function

Figure 1. STMPE1218 pin configuration

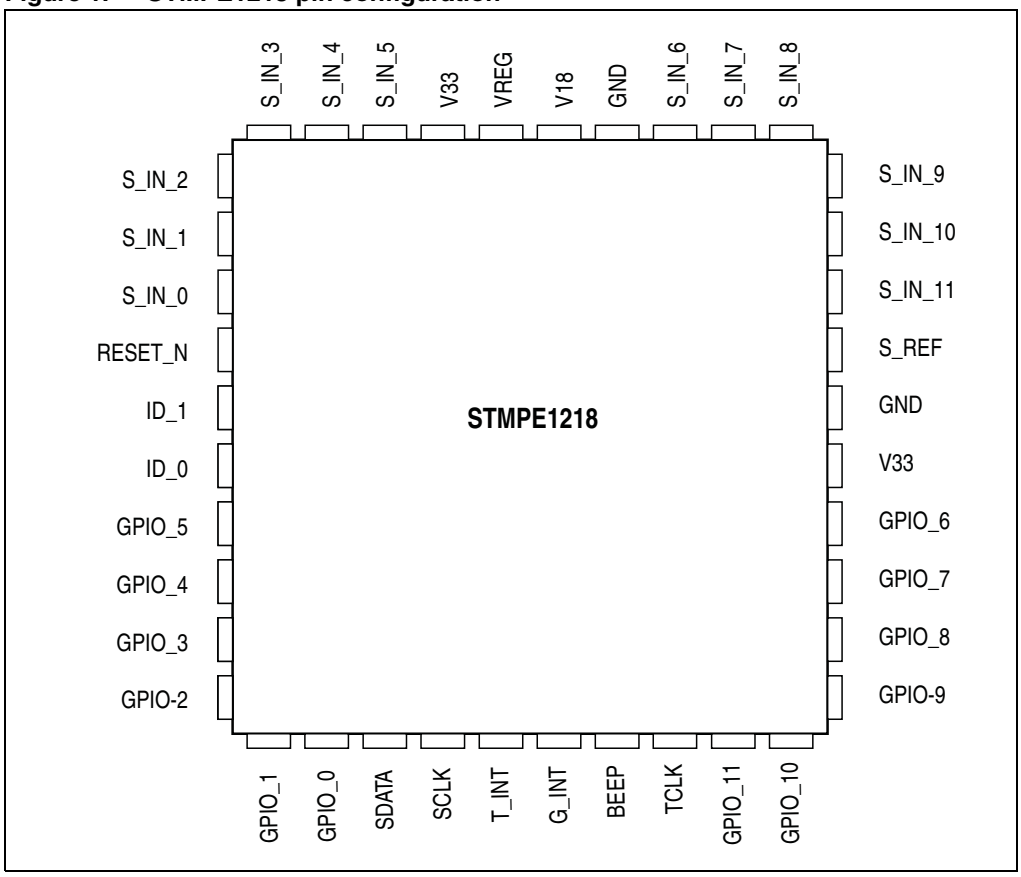


Table 2. Pin assignments and description

Pin number	Pin name	Description
1	GPIO_1	General purpose I/O
2	GPIO_0	General purpose I/O
3	SDATA	I^2C data
4	SCLK	I^2C clock
5	T_INT	Touch interrupt (open drain)
6	G_INT	General interrupt (open drain)
7	BEEP	Beep output
8	TCLK	Test pin (to be connected to GND)
9	GPIO_11	General purpose I/O
10	GPIO_10	General purpose I/O
11	GPIO_9	General purpose I/O

Table 2. Pin assignments and description (continued)

Pin number	Pin name	Description
12	GPIO_8	General purpose I/O
13	GPIO_7	General purpose I/O
14	GPIO_6	General purpose I/O
15	V33	2.7 V - 5.5 V supply
16	GND	Ground
17	S_REF	External reference capacitance
18	S_IN_11	Capacitance sensing input
19	S_IN_10	Capacitance sensing input
20	S_IN_9	Capacitance sensing input
21	S_IN_8	Capacitance sensing input
22	S_IN_7	Capacitance sensing input
23	S_IN_6	Capacitance sensing input
24	GND	Ground
25	V18	1.8 V supply
26	VREG	Internal 1.8 V regulator output
27	V33	2.7 V - 5.5 V supply
28	S_IN_5	Capacitance sensing input
29	S_IN_4	Capacitance sensing input
30	S_IN_3	Capacitance sensing input
31	S_IN_2	Capacitance sensing input
32	S_IN_1	Capacitance sensing input
33	S_IN_0	Capacitance sensing input
34	RESET_IN	Active low reset pin
35	ID_1	I^2C address
36	ID_0	I^2C address
37	GPIO_5	General purpose I/O
38	GPIO_4	General purpose I/O
39	GPIO_3	General purpose I/O
40	GPIO_2	General purpose I/O

Figure 2. STMPE1218 block diagram

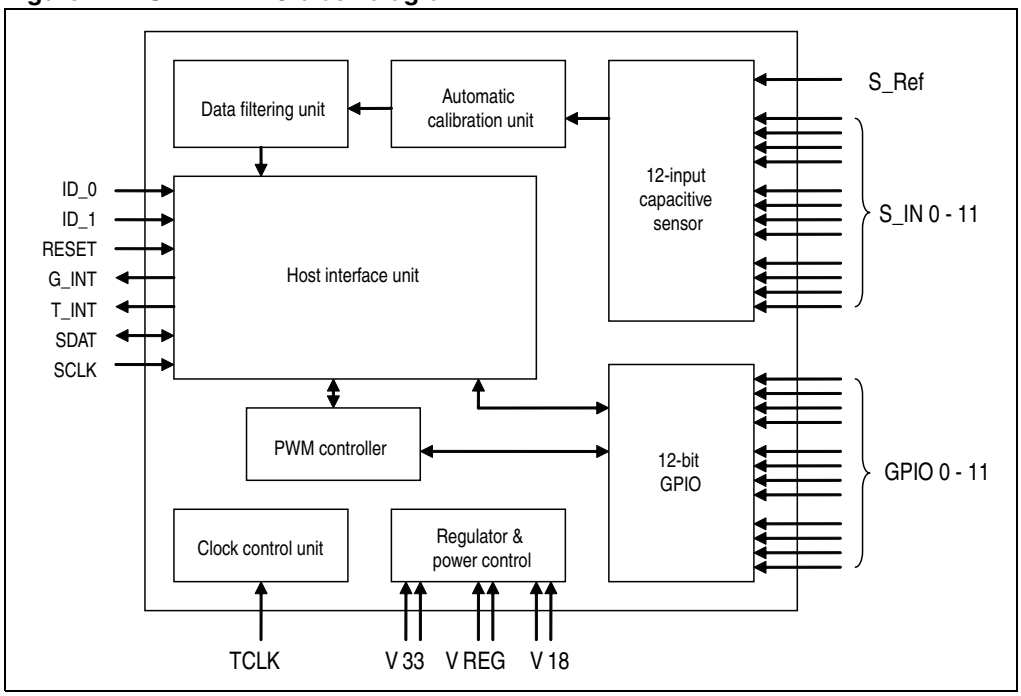
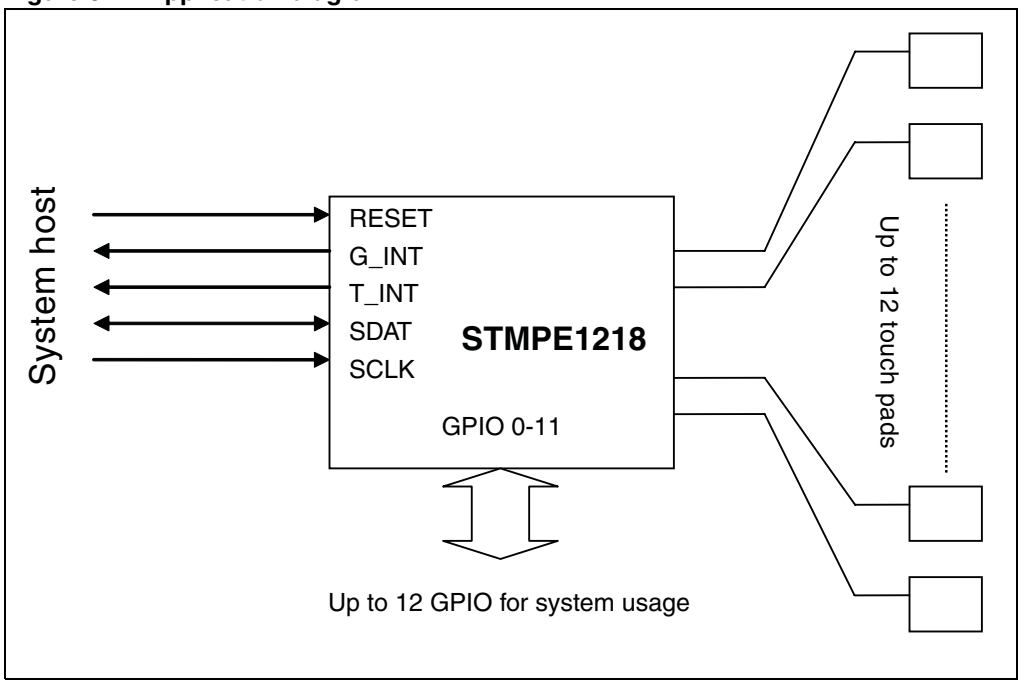


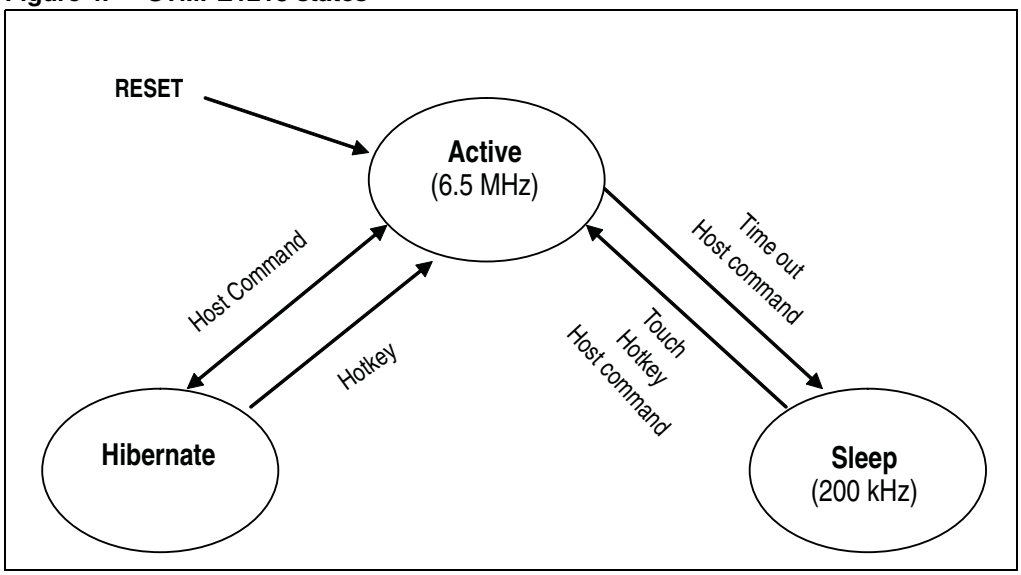
Figure 3. Application diagram



1.1 Power management

The STMPE1218 operates in 3 states.

Figure 4. STMPE1218 states



On reset, the STMPE1218 enters the active state immediately.

Sleep mode is entered by writing ‘1’ to sleep_en bit in the sys_ctrl register.

2 I²C interface

The features that are supported by the I²C interface are the following ones:

- I²C slave device
- Compliant to Philip I²C specification version 2.1
- Supports standard (up to 100 kbps) and fast (up to 400 kbps) modes.
- 7-bit and 10-bit device addressing modes
- General call
- Start/restart/stop

The address is selected by the state of 2 pins. The state of the pins is read upon reset and then the pins can be configured for normal operation. The pins have a pull-up or down to set the address. The I²C interface module allows the connected host system to access the registers in the STMPE1218.

Table 3. I²C addresses

ID_1	ID_0	7-bit address	7-bit address	
			Write LSD	Read LSD
0	0	0x58	0xB0	0xB1
0	1	0x59	0xB2	0xB3
1	0	0x5A	0xB4	0xB5
1	1	0x5B	0xB6	0xB7

2.1 Start condition

A Start condition is identified by a falling edge of SDATA while SCLK is stable at HIGH state. A Start condition must precede any data/command transfer. The device continuously monitors for a Start condition and will not respond to any transaction unless one is encountered.

2.2 Stop condition

A Stop condition is identified by a rising edge of SDATA while SCLK is stable at high state. A Stop condition terminates communication between the slave device and bus master. A read command that is followed by NoAck can be followed by a Stop condition to force the slave device into idle mode. When the slave device is in idle mode, it is ready to receive the next I²C transaction. A Stop condition at the end of a write command stops the write operation to registers.

2.3 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter releases the SDATA after sending eight bits of data. During the 9th bit the receiver pulls the SDATA LOW to acknowledge the receipt of the eight bits of data. The receiver may leave the SDATA in HIGH state if it would to not acknowledge the receipt of the data.

2.4 Data input

The device samples the data input on SDATA on the rising edge of the SCLK. The SDATA signal must be stable during the rising edge of SCLK and the SDATA signal must change only when SCLK is driven low.

2.5 Slave device address

The slave device address is a 7 or 10-bit address, where the least significant 3 bits are programmable. These 3 bit values will be loaded in once upon reset and after that, these 3 pins are no longer be needed except during General Call. Up to 4 STMPE1218 devices can be connected on a single I^2C bus.

2.6 Memory addressing

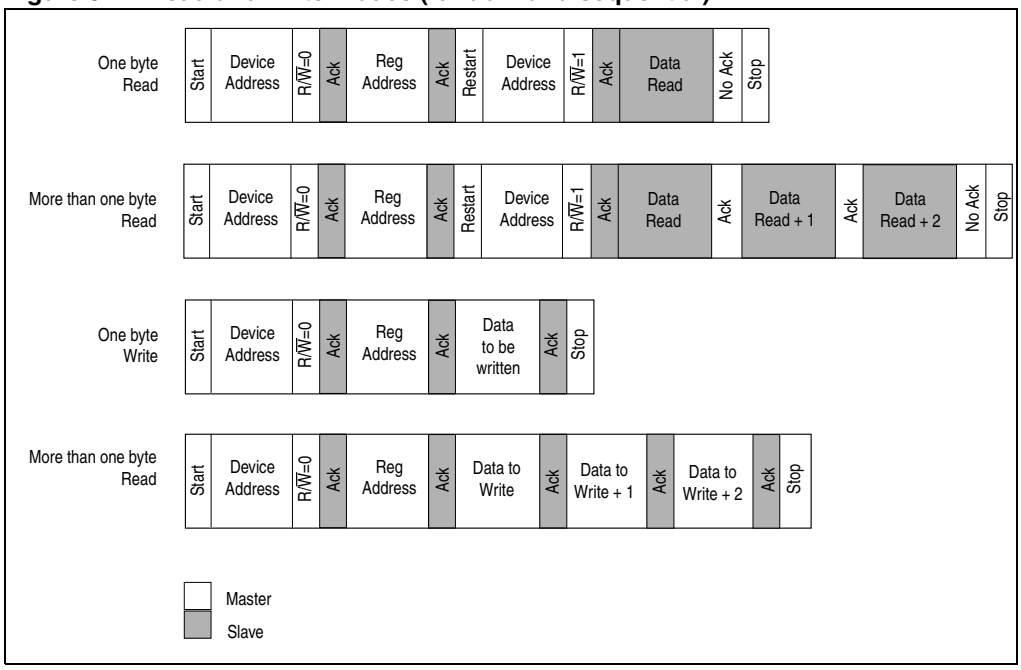
For the bus master to communicate to the slave device, the bus master must initiate a Start condition and be followed by the slave device address. Accompanying the slave device address, there is a Read/ Write bit (R/W). The bit is set to 1 for Read and 0 for Write operation.

If a match occurs on the slave device address, the corresponding device gives an acknowledgement on the SDA during the 9th bit time. If there is no match, it deselects itself from the bus by not responding to the transaction.

Table 4. Operation modes

Mode	Byte	Programming sequence
Read	≥1	Start, device address, R/$\overline{W}$ = 0, Register address to be read
		Restart, device address, R/$\overline{W}$ = 1, data read, STOP
		If no stop is issued, the data read can be continuously performed. If the register address falls within the range that allows an address auto-increment, then the register address auto-increments internally after every byte of data being read. For those register addresses that fall within a non-incremental address range, the address will be kept static throughout the entire write operations. Refer to the memory map table for the address ranges that are auto and non-increment.
Write	≥1	Start, device address, R/$\overline{W}$ = 0, register address to be written, data write, stop
		If no stop is issued, the data write can be continuously performed. If the register address falls within the range that allows address auto-increment, then the register address auto-increments internally after every byte of data being written in. For those register addresses that fall within a non-incremental address range, the address will be kept static throughout the entire write operations. Refer to the memory map table for the address ranges that are auto and non-increment. An example of a non-increment address is Data port for initializing the PWM commands.

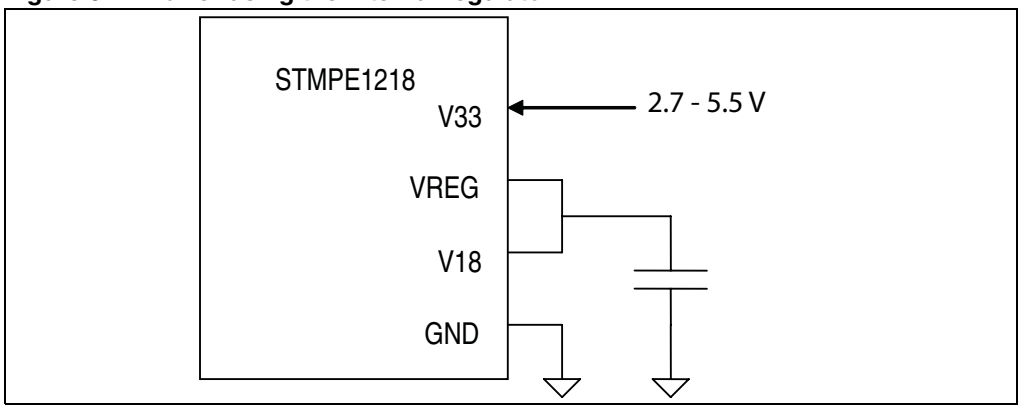
Figure 5. Read and write modes (random and sequential)



3 Power schemes

The STMPE1218 can be powered by a 2.7 V - 5.5 V supply through the internal voltage regulator. V33 powers all the GPIO directly, if LED driving is required on the GPIO, V33 should be at least 3.3 V.

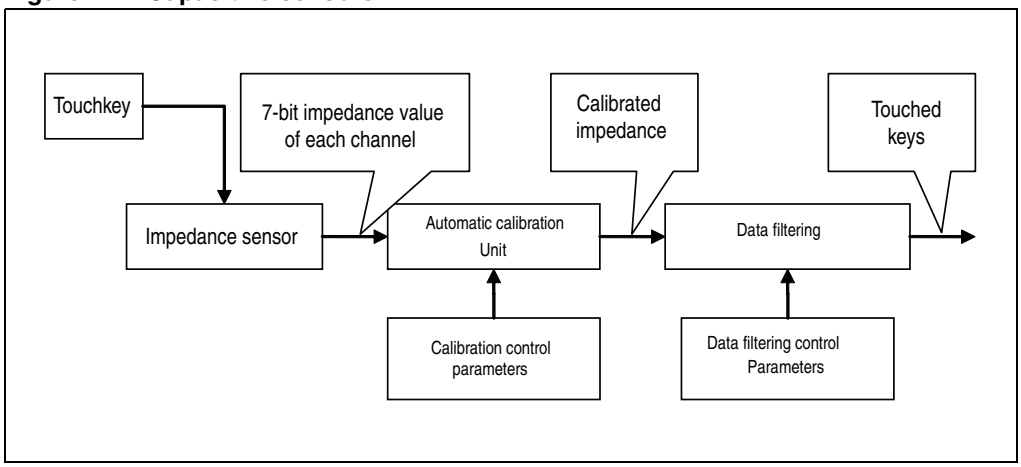
Figure 6. Power using the internal regulator



4 Capacitive sensors

The STMPE1218 capacitive sensor is based on fully digital, impedance change detection engine that is capable of detecting very small change in capacitance.

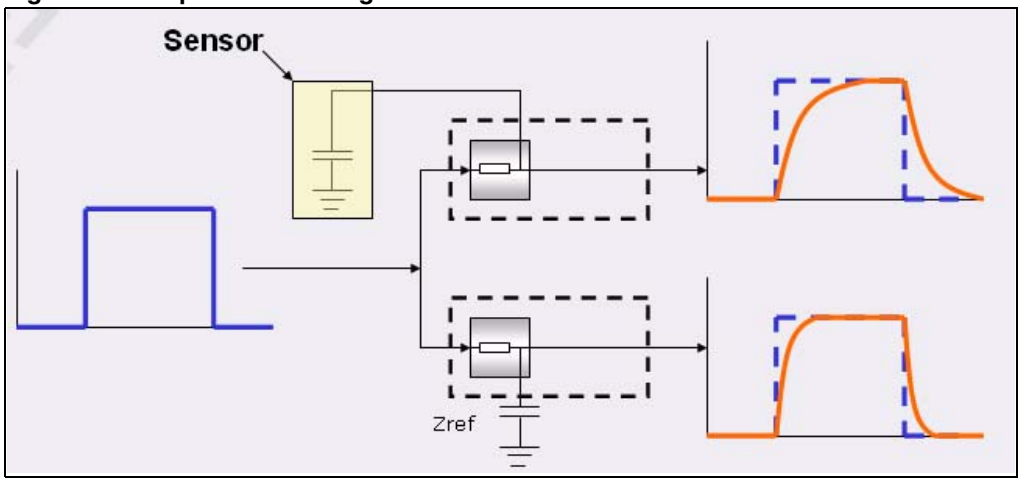
Figure 7. Capacitive sensors



4.1 Capacitive sensing

The STMPE1218 senses a human touch by the additional capacitance introduced to the pad (with respect to ground). This capacitance causes a delay in a clock signal on the sensing pad, and the delay in the sensing pad is compared with a reference clock and the difference is a direct representation of the additional capacitance introduced by the proximity/touch of finger.

Figure 8. Capacitive sensing

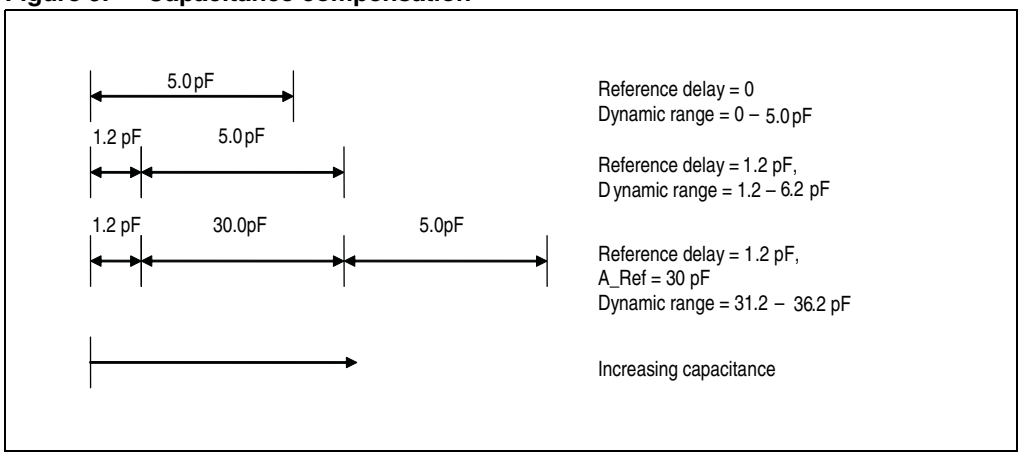


4.2 Capacitance compensation

The STMPE1218 is capable to measure up to 5.0 pF in capacitance difference between the reference point (Zref) and the individual channels. In the case where the PCB connection between the sensor pads and the device is too long, the Reference delay register is able to shift the reference by up to 5.0 pF, allowing the touch channels to measure added capacitance 5.0 pF with offset of 5.0 pF, as shown in following diagram.

In case this is still not enough to compensate for the capacitance on sensor lines (due to very long sensor traces), an external capacitor of up to 30 pF can be connected at the A_Ref pin. This allows to further shift up the dynamic range of the capacitance measurement.

Figure 9. Capacitance compensation



The sensed capacitance is accessible to host through the Impedance registers.

4.3 Calibration algorithm

The STMPE1218 maintains 2 parameters for each touch channels: TVR and calibrated impedance.

The calibrated impedance is an internal reference of which, if the currently measured touch.

If the impedance is more than the calibrated impedance, but the magnitude does not exceed calibrated impedance by TVR, it is not considered a touch. In this case, 2 scenarios are possible:

1. Environmental changes has caused the impedance to increase

2. The finger is near the sensing pad, but not near enough

In the first case, the change in impedance is expected to be small, as environmental changes are normally gradual. A value "EVR" is maintained to specify the maximum impedance change that is still considered an environmental change.

Table 5. Calibration action under different scenarios

Scenario	Touch sensing and calibration action
IMP>CALIBRATED IMP + TVR	touch, no calibration
IMP>CALIBRATED IMP + EVR	No touch, no calibration
IMP<CALIBRATED IMP + TVR IMP<CALIBRATED IMP + EVR	No touch, new calibrated IMP = previous
IMP>CALIBRATED IMP	calibrated IMP + change in IMP
IMP<CALIBRATED IMP	No touch, new calibrated IMP = new IMP

The ETC_WAIT register states a period of time of which, all touch inputs must remain "no touch" for the next calibration to be carried out.

The CAL_INTERVAL register states the period of time between successive calibrations when there are prolonged no touch conditions.

4.3.1 Noise filtering

When the STMPE1218 is operating in the vicinity of highly emissive circuits (DC-DC converter, PWM controller/drive etc.), the sensor inputs will be affected by high-frequency noise. In this situation, the time-integrating function can be used to distinguish between real touch or emission-related false touch.

The integration time and strength threshold registers are used to configure the STMPE1218‘s time integrating function.

4.3.2 Data filtering

The output from the calibration unit is an instantaneous "touch" or "no touch" status. This output is directed to the filtering stage where the touch is integrated across a programmable period of time. The output of the integration stage would be a strength (in the strength register) that indicates the number of times a "touch" is seen, across the integration period.

The strength is then compared with the value in the strength threshold register. If strength exceeds the strength threshold, this is considered a final, filtered touch status.

In data filtering stage, 3 modes of operation are supported:

Mode 1: only the touch channel with the highest strength is taken

Mode 2: the 2 touch channels with the highest strength are taken

Mode 3: all touch channels with strength > strength threshold are taken

These modes are selected using the feature selector register.

The final, filtered data is accessible through the “touch byte” register.

4.3.3 BEEP output

The STMPE1218 is able to drive an external piezo buzzer directly with the built-in beep generator.

5 Register map and function description

This section lists and describes the registers of the STMPE1218 device, starting with a register map and then detailed descriptions of register types.

Table 6. Register summary map table

Address	Module registers	Bit	Type	Reset value	Description
0x00	CHIP_ID_0	16	R	0x12	Device identification
0x01	CHIP_ID_1	16	R	0x18	Device identification
0x02	ID_VER	8	R/W	0x01	Revision number
0x03	SYS_CTRL_1	8	R/W	0x00	System control
0x04	SYS_CTRL_2	8	R/W	0x8F	System control
0x08	INT_CTRL	8	R/W	0x00	Interrupt control
0x09	INT_EN	8	R/W	0x00	Interrupt enable
0x0A	INT_STA	8	R	0x00	Interrupt status
0x0B	GPIO_INT_EN_lsb	8	R/W	0x00	GPIO interrupt enable
0x0C	GPIO_INT_EN__msb	8			
0x0D	GPIO_INT_STA_lsb	8	R/W	0x00	GPIO interrupt status
0x0E	GPIO_INT_STA_msb	8			
0x10	GPIO_MP_lsb	8	R/W	0x00	GPIO monitor pin state
0x11	GPIO_MP_msb	8		0x00	
0x12	GPIO_DATA_lsb	8	R/W	0x00	GPIO data register
0x13	GPIO_DATA_msb	8		0x00	
0x14	GPIO_DIR_lsb	8	R/W	0x00	GPIO set pin direction
0x15	GPIO_DIR_msb	8		0x00	
0x16	GPIO_AF_lsb	8	R/W	0x00	GPIO alternate function
0x17	GPIO_AF_msb	8		0x00	
0x20	FEAT_SEL	8	R/W	0x04	Feature select
0x21	ETC_WAIT	8	R/W	0x47	Wait time
0x22	CAL_INTERVAL	8	R/W	0x30	Calibration interval
0x23	INTEGRATION_ TIME	8	R/W	0x0F	Integration time
0x25	CTRL	8	R/W	0x00	Control
0x26	INT_MASK	8	R/W	0x08	Interrupt mask
0x27	INT_CLR	8	R/W	0x00	Interrupt clear
0x28	FILTER_PERIOD	8	W	0x00	Filter period
0x29	FILTER_THRESHOLD	8	R/W	0x00	Filter threshold
0x2A	REF_DLY	8	R/W	0x00	Reference delay

Table 6. Register summary map table (continued)

Address	Module registers	Bit	Type	Reset value	Description
0x30 - 0x3B	TVR	8	R/W	0x08	Touch variance setting
0x40	EVR	8	R/W	0x04	Enviromental variance
0x50 - 0x5B	STRENGTH_THRES	8	R/W	0x01	Strength threshold
0x60 - 0x6B	STRENGTH	8	R/W	0x00	Strength
0x70 - 0x7B	CAL_IMPEDANCE	8	R	0x00	Calibration impedance
0x80 - 0x8B	IMPEDANCE	8	R	0x00	Impedance
0x90	TOUCH_BYTE_L	8	R	0x00	Touch sensing data output
0x91	TOUCH_BYTE_H	8	R	0x00	Touch sensing data output
0x92	INT_PENDING	8	R/W	0x00	Interrupt pending
0xA0	PWM_OFF_STATE	8	R/W	0x00	PWM off state
0xA1	MASTER_EN	8	R/W	0x00	Master enable
0xB0	PWM_0_SET	8	R/W	0x00	PWM0 setup
0xB1	PWM_0_CTRL	8	R/W	0x00	PWM0 control
0xB2	RAMP_0_RATE	8	R/W	0x00	PWM0 ramp rate
0xB4	PWM_1_SET	8	R/W	0x00	PWM1 setup
0xB5	PWM_1_CTRL	8	R/W	0x00	PWM1 control
0xB6	RAMP_1_RATE	8	R/W	-	PWM1 ramp rate
0xB8	PWM_2_SET	8	R/W	0x00	PWM2 setup
0xB9	PWM_2_CTRL	8	R/W	0x00	PWM2 control
0xBA	RAMP_2_RATE	8	R/W	0x00	PWM2 ramp rate
0xBC	PWM_3_SET	8	R/W	0x00	PWM3 setup
0xBD	PWM_3_CTRL	8	R/W	0x00	PWM3 control
0xBE	PWM_3_RATE	8	R/W	0x00	PWM3 ramp rate
0xC0	BEEP_EN	8	R/W	0x00	BEEP enable
0xC2	BEEP_PER	8	R/W	0x00	BEEP period
0xC3	BEEP_FREQ	8	R/W	0x00	BEEP frequency

6 Clock and power manager module

Table 7. Clock and power manager registers map

Address	Register name	Bit	Type	Reset	Function
0x00	CHIP_ID_0	16	R	0x30	Device identification
0x01	CHIP_ID_1	16	R	0x03	Device identification
0x02	ID_VER	8	R/W	0x01	Revision number
0x03	SYS_CTRL_1	8	R/W	0x00	System control
0x04	SYS_CTRL_2	8	R/W	0x8F	System control

CHIP_ID_0 Device identification

Address: 0x00

Type: R

Reset: 0x12

Description: 16-bit device identification.

CHIP_ID_1 Device identification

Address: 0x01

Type: R

Reset: 0x18

Description: 16-bit device identification.

ID_VER Revision number

Address: 0x02

Type: R/W

Reset: 0x01

Description: 8-bit revision number

SYS_CTRL_1 System control register 1

7	6	5	4	3	2	1	0
RESERVED				SLEEP_EN	WARM_RESET	SOFT_RESET	HIBERNATE

Address: 0x03

Type: R/W

Reset: 0x00

Description: The reset control register enables the system's control functions.

[7:4] Reserved

[3] Sleep_en

[2] Warm_reset:
Write '1' to initiate a warm reset

[1] Soft_reset:
Write '1' to initiate a soft reset

[0] Hibernate:
Write '1' to enter hibernate mode

SYS_CTRL_2 System control register 2

7	6	5	4	3	2	1	0
SENSOR_CLOCK_2	SENSOR_CLOCK_ 1	SENSOR_CLOCK_0	CLOCK_SELECT	BEEP CLOCK DISABLE	GPIO CLOCK DISABLE	PWM_CLOCK_DISABLE	TOUCH_CLOCK_DISABLE

Address: 0x04

Type: R/W

Reset: 0x8F

Description: The reset control register allows to control clock and gating function.

[7:5] Sensor clock: See description in the table below.

[4] Clock_select:
0 for 6.5 MHz
1 for 200 KHz

[3] BEEP clock disable:
Write '1' to disable clock to BEEP unit

[2] GPIO clock disable:
Write '1' to disable clock to GPIO unit

[1] PWM clock disable:
Write '1' to disable clock to PWM unit

[0] Touch clock disable:
Write '1' to disable clock to TOUCH unit

Table 8. Sensor clock setting

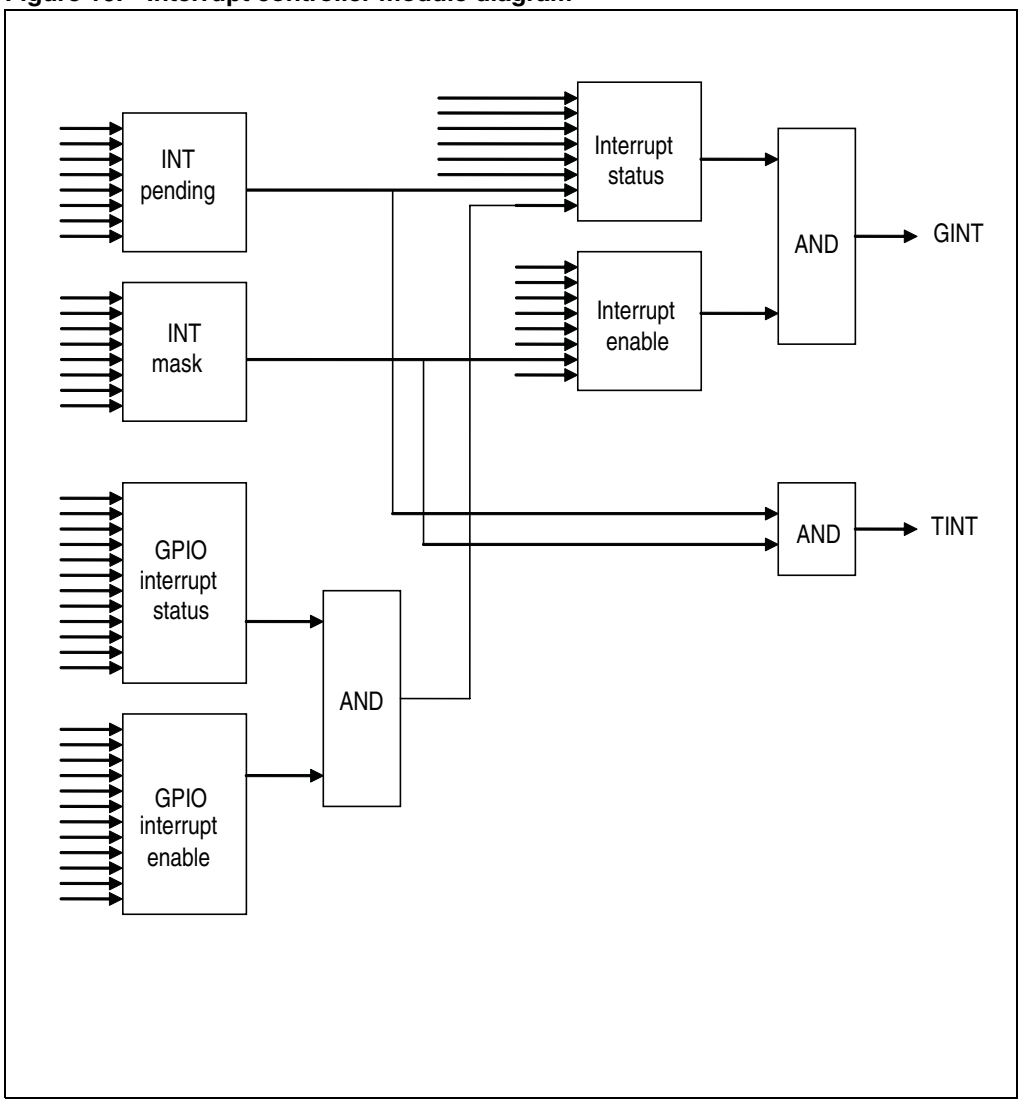
Mode	Divider	Sensor clock [2:0]	Active	Calibration	Idle
Operational (6.5 MHz)	1	000	12.8 KHz	100 KHz	400 Hz
	2	001	6.4 KHz	50 KHz	200 Hz
	4	010	3.2 KHz	25 KHz	100 Hz
	8	011	1.6 KHz	12.5 KHz	50 Hz
	16	1xx	800 Kz	6.25 KHz	25 Hz
Autosleep (200 KHz)	1	000	400 Hz	3.2 KHz	12.5 Hz
	2	001	200 Hz	1.6 KHz	6.2 Hz
	4	010	100 Hz	800 Hz	3.1 Hz
	8	011	50 Hz	400 Hz	1.5 Hz
	16	1xx	25 Hz	200 Hz	0.75 Hz

7 Interrupt controller module

Two interrupt pins are available in the STMPE1218 device. The G_INT is activated by a number of system events, and cleared by clearing the corresponding interrupt.

T_INT is activated by touch detection only and cleared by reading the touch byte.

Figure 10. Interrupt controller module diagram



INT_CTRL Interrupt control register

7	6	5	4	3	2	1	0
RESERVED					POLARITY	TYPE	INT_EN

Address: 0x08

Type: R/W

Reset: 0x00

Description: This register is used to enable control the polarity, edge/level and enabling of the interrupt system.

[7:3] Reserved

[2] Polarity:
0: active low
1: active high
This controls both GINT and TINT

[1] Type:
0: level trigger
1: edge trigger (pulse width is 200 µS)
This controls both GINT and TINT

[0] Int_en:
0: to disable all interrupt
1: to enable all interrupt

INT_EN Interrupt enable register

7	6	5	4	3	2	1	0
RESERVED		GPIO	PWM3	PWM2	PWM1	PWM0	TOUCH

Address: 0x09

Type: R/W

Reset: 0x00

Description: This register is used to enable the interruption from a system related interrupt source to the host.

[7:6] Reserved

[5] GPIO:
One or more level transition in enabled GPIOs

[4] PWM3:
Completion of PWM sequence

[3] PWM2:
Completion of PWM sequence

[2] PWM1:
Completion of PWM sequence

[1] PWM0:
Completion of PWM sequence

[0] Touch:
One or more touch is sensed

INT_STA Interrupt status register

7	6	5	4	3	2	1	0
RESERVED		GPIO	PWM3	PWM2	PWM1	PWM0	TOUCH

Address: 0x0A

Type: R

Reset: 0x00

Description: This register reflects the status of the interrupt events.
Writing ‘1’ clears the corresponding bit.
Writing ‘0’ has no effect.

[7:6] Reserved

[5] GPIO:
One or more level transition in enabled GPIOs

[4] PWM3:
Completion of PWM sequence

[3] PWM2:
Completion of PWM sequence

[2] PWM1:
Completion of PWM sequence

[1] PWM0:
Completion of PWM sequence

[0] Touch:
One or more touch is sensed

GPIO_INT_EN_lsb GPIO interrupt enable register LSB

7	6	5	4	3	2	1	0
IEG[x]							

Address: 0x0B

Type: R/W

Reset: 0x00

Description: The GPIO interrupt register (LSB) is used to enable the interruption from a particular interrupt source to the host. The IEG[x] bits are the interrupt enable mask bits corresponding to the GPIO[7:0] pins.

[7:0] IEG[x]:
Interrupt enable GPIO mask (where x = 7 to 0)
Writing a '1' to the IE[x] bit enables the interruption to the host.

GPIO_INT_EN_MSB GPIO interrupt enable register MSB

7	6	5	4	3	2	1	0
RESERVED				IEG[x			

Address: 0x0C

Type: R/W

Reset: 0x00

Description: The GPIO interrupt enable register (MSB) is used to enable the interruption from a particular GPIO interrupt source to the host. The IEG[11:8] bits are the interrupt enable mask bits corresponding to the GPIO[11:8] pins.

[7:4] Reserved

[3:0] IEG[x]:
Interrupt enable GPIO mMask (where x = 11 to 8)
Writing a '1' to the IE[x] bit will enable the interruption to the host.

GPIO_INT_STA_LSB GPIO interrupt status register LSB

7	6	5	4	3	2	1	0
ISG[x]							

Address: 0x0D

Type: R/W

Reset: 0x00

Description: The GPIO interrupt status register LSB monitors the status of the interruption from a particular GPIO pin interrupt source to the host. Regardless whether the IEGPIOR bits are enabled or not, the INT_STA_GPIO_LSB bits are still updated. The ISG[7:0] bits are the interrupt status bits correspond to the GPIO[7:0] pins.

[7:0] ISG[x]:
Interrupt status GPIO (where x = 7 to 0)
Read:
Interrupt status of the GPIO[x]. Reading the register will clear any bits that has been set to '1'
Write:
Writing to this register has no effects

GPI_INT_STA_MSB GPIO interrupt status register MSB

7	6	5	4	3	2	1	0
RESERVED				ISG[x]			

Address: 0x0E

Type: R/W

Reset: 0x00

Description: The GPIO interrupt status register MSB monitors the status of the interruption from a particular GPIO pin interrupt source to the host. Regardless whether the GPIO_INT_EN bits are enabled or not, the GPIO_INT_STA bits are still updated. The ISG[11:8] bits are the interrupt status bits corresponding to the GPIO[11:8] pins.

[7:4] Reserved

[3:0] ISG[x]:
Interrupt status GPIO (where x = 11 to 8)
Read:
Interrupt status of the GPIO[x]. Reading the register will clear any bits that has been set to '1'
Write:
Writing to this register has no effects.

8 GPIO controller

A total of 12 GPIOs are available in the STMPE1218. The GPIO controller contains the registers that allow the host system to configure each of the pins into either a GPIO, direct output of a TOUCH channel or a PWM output. Unused GPIOs should be configured as outputs to minimize the power consumption.

A group of registers are used to control the exact function of each of the 12 GPIO. The registers and their respective address is listed in the following table.

Table 9. GPIO controller registers summary map

Address	Register name	Description	Auto-increment
0x10	GPMR_LSB	GPIO monitor pin state register	YES
0x11	GPMR_MSB	GPIO monitor pin state register	YES
0x12	GPSR_LSB	GPIO set pin state register	YES
0x13	GPSR_MSB	GPIO set pin state register	YES
0x14	GPDR_LSB	GPIO set pin direction register	YES
0x15	GPDR_MSB	GPIO set pin direction register	YES
0x16	GPFR_LSB	GPIO function register	YES
0x17	GPFR_MSB	GPIO function register	YES

All GPIO registers are named as GPxx, where:

Xxx represents the functional group

For LSB registers:

7	6	5	4	3	2	1	0
IO-7	IO-6	IO-5	IO-4	IO-3	IO-2	IO-1	IO-0

For MSB registers:

7	6	5	4	3	2	1	0
				IO-11	IO-10	IO-9	IO-8

The function of each bit is shown in the following table:

Table 10. GPIO control bits function

Register name	Function
GPIO monitor pin state	Reading this bit yields the current state of the bit. Writing has no effect.
GPIO set pin state	Writing '1' to this bit causes the corresponding GPIO to go to '1' state Writing '0' to this bit causes the corresponding GPIO to go to '0' state
GPIO set pin direction	'0' sets the corresponding GPIO to input state, and '1' sets it to output state. All bits are '0' on reset.
GPIO function	'0' sets the corresponding GPIO to function as GPIO, and '1' sets it to Touch Key Direct Output mode. For GPIO 0-3, if GPIO Function is set to Touch Key Direct Output mode and AF bits in the PWM Master Enable Register is enabled, the corresponding GPIO will function as PWM output.

9 Capacitive touch module registers

FEATURE_SELECT Feature select

7	6	5	4	3	2	1	0
RESERVED					AFS[1:0]		Filter EN

Address: 0x20

Type: R/W

Reset: 0x04

Description: Controls AFS (advanced filtering system and second level filtering feature

[7:3] Reserved

[2:1] AFS[1:0]:
‘11’: AFS mode 1 (only 1 key)
‘10’: AFS mode 2 (all keys)
11: AFS mode 3 (2 keys)

[1] AFS1:
Write '1' to enable AFS mode 1 (only 1 key with strongest touch)

[0] Filter EN:
Write '1' to enable filter

ETC_WAIT Wait time setting

7	6	5	4	3	2	1	0
ETC_WAIT[7:0]							

Address: 0x21

Type: R/W

Reset: 0x47

Description: Sets the wait time between the calibration and the last button touch

[7:0] ETC_WAIT[7:0]:
ETC wait time = ETC_Wait[7:0] *64 + sensor clock period
A "non-touch" condition must persist for this wait time, before an ETC operation is carried out.
Range: 800mS - 12.8S

CAL_INTERVAL Calibration interval

7	6	5	4	3	2	1	0
CAL_INTERVAL							

Address: 0x22

Type: R/W

Reset: 0x30

Description: Calibration interval.

[7:0] Calibration interval:
Interval between calibration = calibration Interval [7:0] * sensor clock period * 50
Range: 625 mS - 10 S

INTEGRATION TIME Integration time

7	6	5	4	3	2	1	0
INTEGRATION_TIME[7:0]							

Address: 0x23

Type: R/W

Reset: 0x0F

Description: Integration time.

[7:0] Integration time in AFS mode
Total period of integration = sensor clock period * Integration Time [7:0]
Range: 50 µs - 100 mS

CTRL Control

7	6	5	4	3	2	1	0
RESERVED				SENSOR_ACTIVE	HDC_U	HDC_C	HOLD

Address: 0x25

Type: R/W

Reset: 0x00

Description: Control.

[7:4] Reserved

[3] SENSOR-ACTIVE:
This bit must be written ‘1’ for the correct operation of the capacitive sensor.

[2] HDC_U:
Write '1' to perform unconditional host driven calibration.
Cleared to '0' when calibration is completed
Only applicable HOLD is '1'

[1] HDC_C:
Write '1' to perform conditional host driven calibration.
Calibration is performed if and only if no touch is detected.
Cleared to '0' when calibration is completed
Only applicable HOLD is '1'

[0] HOLD:
'0' to enable ETC
'1' to disable ETC

INT_MASK Interrupt mask

7	6	5	4	3	2	1	0
RESERVED				EOC	RESERVED	RESERVED	TOUCH

Address: 0x26

Type: R/W

Reset: 0x08

Description: Writing '1' to this register disables the corresponding interrupt source.

[7:4] Reserved

[3] EOC:
End of calibration
This interrupt occurs on both automatic and forced calibration

[2] Reserved:
Must be set to ‘1’

[1] Reserved:
Must be set to ‘1’

[0] Touch:
Touch module activity

INT_CLR Interrupt clear

7	6	5	4	3	2	1	0
RESERVED				EOC	RESERVED	RESERVED	TOUCH

Address: 0x27

Type: R/W

Reset: 0x00

Description: Writing '1' to this register clears the corresponding interrupt source in INT PENDING register.

[7:4] Reserved

[3] EOC:
End of calibration. This interrupt occurs on both automatic and forced calibration

[2] Reserved

[1] Reserved

[0] Touch:
Touch module activity

FILTER_PERIOD Filter period

7	6	5	4	3	2	1	0
FILTER_COUNT							

Address: 0X28

Type: R/W

Reset: 0x00

Description: Filter period.

[7:0] Filter_count:

Additional filter to stabilize touch output in AFS mode.

AFS touch output is monitored for Filter Count [7:0] times every integration time. For each time a "touch status" is detected, an internal "Filter Counter" is incremented once. This counter value is then compared with Filter Threshold (register 0x3E)

FILTER_THRESHOLD Filter threshold

7	6	5	4	3	2	1	0
FILTER_THRESHOLD							

Address: 0x29

Type: R/W

Reset: 0x00

Description: Filter threshold.

[7:0] FILTER_THRESHOLD:

An internal "Filter Counter" is compared with Filter Threshold [7:0] to determine if a valid touch has occurred.

REFERENCE_DELAY Reference delay

7	6	5	4	3	2	1	0
RESERVED	REFERENCE_DELAY						

Address: 0x2A

Type: R/W

Reset: 0x00

Description: Shifting of capacitive sensor dynamic range. The capacitance value set into this register is in effect, equivalent to capacitor connected to the S_Ref pin.

[7] Reserved

[6:0] Reference_delay:

Valid range = 0-127

Each step represents capacitance value of 0.06 pF

Warm reset is required after this value is updated

TVR

Touch variance setting

7	6	5	4	3	2	1	0
RESERVED	TVR						

Address: 0x30 - 0x3B

Type: R/W

Reset: 0x08

Description: Touch variance setting.

[7] Reserved

[6:0] TVR:
Setting TVR between 0-99.
A high TVR value decreases sensitivity of the sensor, but increasing its tolerance to ambient noise.
A small TVR value increases the sensitivity.

EVR Enviromental variance

7	6	5	4	3	2	1	0
RESERVED	TVR						

Address: 0x40

Type: R/W

Reset: 0x04

Description: Enviromental variance setting.

[7] Reserved

[6] EVR:
EVR is used to detect "Non-Touch" condition

STRENGTH_THRESHOLD Strength threshold

7	6	5	4	3	2	1	0
STRENGTH_THRESHOLD							

Address: 0x50 - 0x5B

Type: R/W

Reset: 0x01

Description: Strength threshold.

[7:0] Strength_threshold:
Setting threshold to be used in AFS mode to determine valid touch

STRENGTH Strength

7	6	5	4	3	2	1	0
STRENGTH							

Address: 0x60 - 0x6B

Type: R

Reset: 0x00

Description: The number of times where a sense capacitance exceeds the calibrated reference impedance

[7:0] Strength:
Read-only field
Counts the number of times a sensed impedance exceeds calibrated reference impedance over and integration time. Maximum strength equals Integration Time [7:0]

CALIBRATED_IMPEDANCE Calibrated impedance

7	6	5	4	3	2	1	0
CAL_IMPEDANCE							

Address: 0x70 - 0x7B

Type: R

Reset: 0x00

Description: Calibrated impedance is an integral reference value maintained by the device.

[7:0] CALIBRATED IMPEDANCE:
Calibrated reference impedance

IMPEDANCE Impedance

7	6	5	4	3	2	1	0
IMPEDANCE							

Address: 0x80 - 0x8B

Type: R

Reset: 0x00

Description: Impedance is the instantaneous impedance value seen at the input pin of each cap. sensing pin.

[7:0] IMPEDANCE:
Currently sensed impedance

TOUCH_BYTE_L Touch sensing data output

7	6	5	4	3	2	1	0
TOUCH							

Address: 0x90

Type: R

Reset: 0x00

Description: Touch sensing data output.

[7:0] Touch:
Reads '1' if the corresponding capacitance sensing channel reads a valid TOUCH

TOUCH_BYTE_H Touch sensing data output

7	6	5	4	3	2	1	0
RESERVED				TOUCH			

Address: 0x91

Type: R

Reset: 0x00

Description: Touch sensing data output.

[7:4] Reserved

[3:0] Touch:
Reads '1' if the corresponding capacitance sensing channel reads a valid TOUCH

INT_PENDING Interrupt pending

7	6	5	4	3	2	1	0
RESERVED				EOC	I2A	A21	TOUCH

Address: 0x92

Type: R/W

Reset: 0x00

Description: Reflects the status of each interrupt source

[7:4] Reserved

[3] EOC:
End of calibration

[2] I2A:
SLEEP to active transition

[1] A21:
Active to SLEEP transition

[0] Touch:
Touch detect

10 BEEP generation module registers

BEEP_EN Beep enable generation

7	6	5	4	3	2	1	0
RESERVED							BEEP_EN

Address: 0xC0

Type: R/W

Reset: 0x00

Description: Beep enable generation

[7:1] Reserved

[0] BEEP_EN:
0: to disable beep generation on TOUCH
1: to enable beep generation on TOUCH

BEEP_PERIOD Beep period

7	6	5	4	3	2	1	0
BEEP_PERIOD [7:0]							

Address: 0xC1

Type: R/W

Reset: 0x00

Description: Beep period

[7:0] Beep_period:
Period = Beep - Period [7:0] * System clock 2^{16}
System clock = 6.5 MHz (typ)
Min period = 0.154 uS * 2^{16} = 10 mS
Max period = 0.154 uS * 2^{16} *255 = 2.55 S

BEEP_FREQUENCY — Beep frequency

7	6	5	4	3	2	1	0
BEEP_FREQUENCY							

Address: 0xC2

Type: R/W

Reset: 0x00

Description: Beep frequency

[7:0] Beep_frequency:
Frequency of beep = System Clock / (Beep Frequency [7:0] * 64)

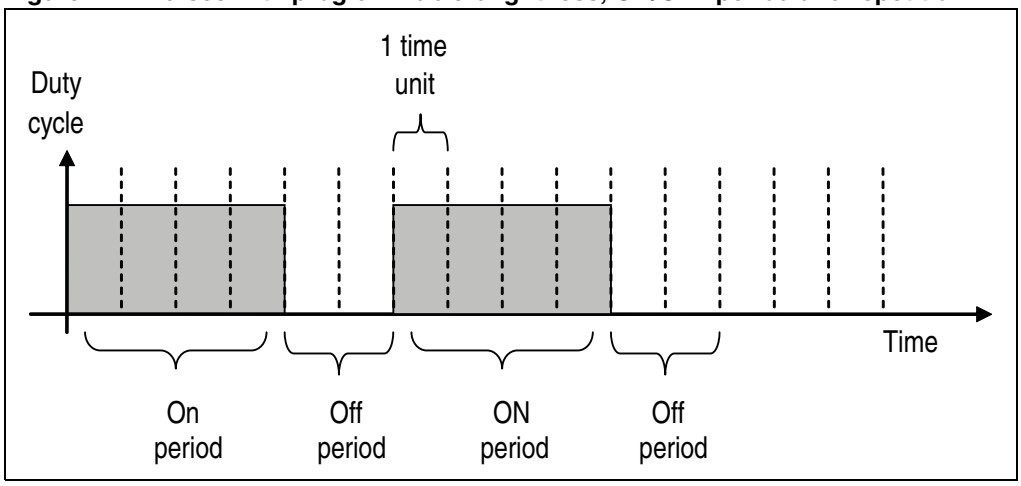
Min Freq = 6.5 MHz/(255*64) = 398 Hz
Max Freq = 102 kHz

11 Basic PWM controller

The basic PWM controller allows simpler brightness control and basic blinking patterns. The STMPE1218 is fitted with a 4-channel basic PWM controller.

The PWM controllers outputs are connected to the GPIO 0-3. In order to activate the PWM channels, the alternate function bits in the master enable register must be set to '1'. The PWM controllers are capable of generating the following brightness patterns:

Figure 11. Pulses with programmable brightness, ON/OFF period and repetition



On period = period 0[1:0] * time unit [3:0]

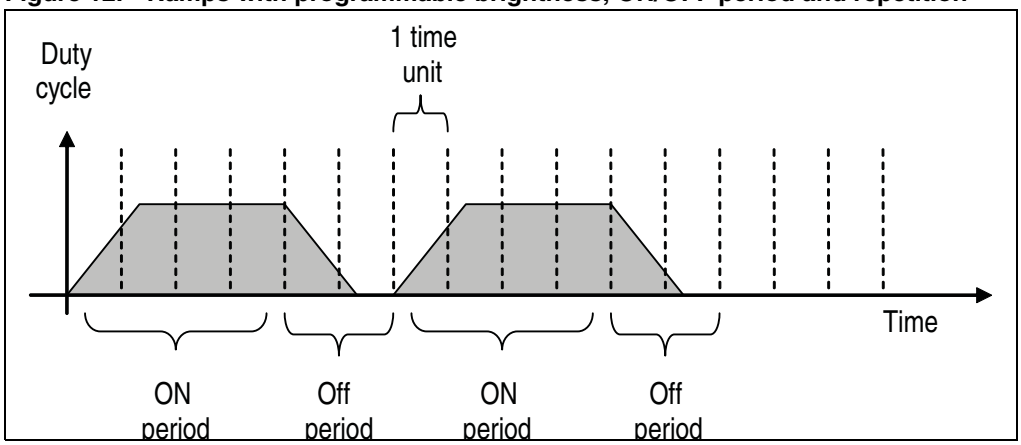
Off period = period 1[1:0] * time unit [3:0]

Duty cycle during “on period” = brightness [7:4]

Number of cycles = repetition [2:0]

Ramp mode is disabled.

Figure 12. Ramps with programmable brightness, ON/OFF period and repetition



“On” period = period 0[1:0] * time unit [2:0]

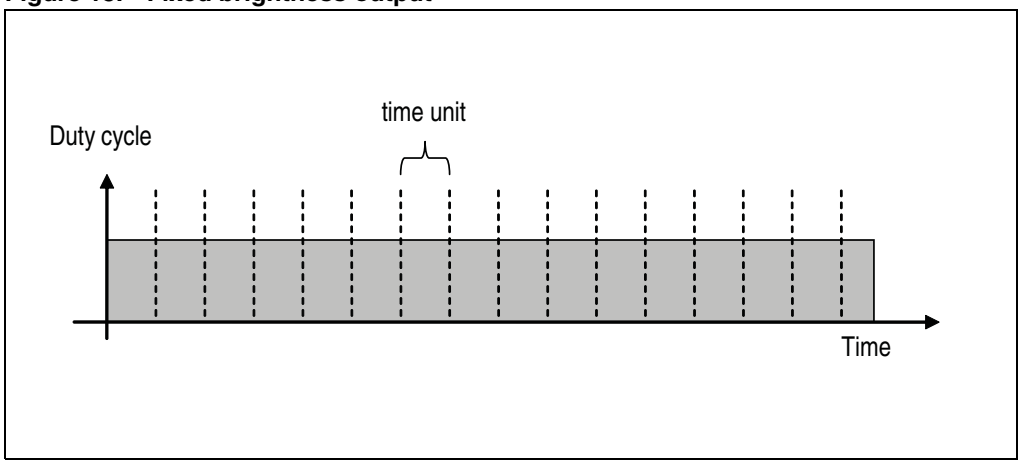
“Off” period = period 1[1:0] * time unit [2:0]

Duty cycle during “on” period = brightness [7:4]

Number of cycles = repetition [2:0]

Ramp up rate is programmable.

Figure 13. Fixed brightness output



“On” period = period 0[1:0] * time unit [3:0]

Off period = 0

Duty cycle during “on” period = brightness [7:4]

Number of cycles = repetition [2:0] = 0 (means infinite repetition)

11.1 PWM function register map

Table 11. PWM function register map summary table

Register name	Description	Auto-increment (during sequential R/W)
PWM_OFF_STATE	Sets the output level when PWM is disabled	Yes
MASTER_EN	Enables/disables individual basic PWM channels	Yes
PWM_0_SET	PWM_0 setup	Yes
PWM_0_CTRL	PWM_0 control	Yes
RAMP_0_RATE	PWM_0 ramp rate	Yes
PWM_1_SET	PWM_1 setup	Yes
PWM_1_CTRL	PWM_1 control	Yes
RAMP_1_RATE	PWM_1 ramp rate	Yes
PWM_2_SET	PWM_2 setup	Yes
PWM_2_CTRL	PWM_2 control	Yes
RAMP_2_RATE	PWM_2 ramp rate	Yes
PWM_3_SET	PWM_3 setup	Yes
PWM_3_CTRL	PWM_3 control	Yes
PWM_3_RATE	PWM_3 ramp rate	Yes

PWM_OFF_STATE PWM OFF state

7	6	5	4	3	2	1	0
RESERVED				OUT3	OUT2	OUT1	OUT0

Address: 0xA0

Type: R/W

Reset: 0x00

Description: The PWM group control register determines the output state for the GPIO that is configured as PWM, when the PWM channels are in OFF state.

[7:4] Reserved

[3:0] OUT3:0:
Default is '0'
'1' - PWM channel outputs '1' when disabled
'0' - PWM channel outputs '0' when disabled

MASTER_EN Master enable

7	6	5	4	3	2	1	0
AF3	AF2	AF1	AF0	EN3	EN2	EN1	EN0

Address: 0xA1

Type: R/W

Reset: 0x00

Description: The Master enable register provides the control to enable/disable the individual PWM controller.

[7:4] AF[3:0]
Alternate function
Default is “0”

[3:0] PWM channel enable
Default is “0”
Software writes ‘1’ to start the PWM channel
Hardware writes ‘0’ when the PWM blinking is completed

RAMP_RATE_n Ramp rate register n=0-3

7	6	5	4	3	2	1	0
RESERVED	RAMP_DOWN				RAMP_UP		

Address: 0xB2, 0xB6, 0xBA, 0xBE

Type: R/W

Reset: 0x00

Description: The Ramp rate register sets the rate of ramp up/down of the PWM controller.

[7] RESERVED

[6:3] RAMP_DOWN:
‘000’ = 1/4 of time unit per brightness level change
‘001’ = 1/8 of time unit per brightness level change
‘010’ = 1/16 of time unit per brightness level change
‘011’ = 1/32 of time unit per brightness level change
‘100’ = 1/64 of time unit per brightness level change
’101’ = 1/128 of time unit per brightness level change
‘110’ = reserved
‘111’ = reserved

[2:0] RAMP_UP:
‘000’ = 1/4 of time unit per brightness level change
‘001’ = 1/8 of time unit per brightness level change
‘010’ = 1/16 of time unit per brightness level change
‘011’ = 1/32 of time unit per brightness level change
‘100’ = 1/64 of time unit per brightness level change
’101’ = 1/128 of time unit per brightness level change
‘110’ = reserved
‘111’ = reserved

PWM_n_SET PWM_n setup registers n=0-3

7	6	5	4	3	2	1	0
BRIGHTNESS				TIMING			RAMP_EN

Address: 0xB0, 0xB4, 0xB8, 0xBC

Type: R/W

Reset: 0x00

Description: The PWM setup registers sets up the brigtheness and period of the PWM controller.

[7:4] Brightness:
This defines the duty cycle during the ON period of the PWM channel output which in turn determines the brightness level of the LED that the PWM output drives.
0000: duty cycle ratio 1:15 (6.25%, minimum brightness)
0001: duty cycle ratio 2:14 (12.50%)
0010: duty cycle ratio 3:13 (18.75%)
0011: duty cycle ratio 4:12 (25.00%)
0100: duty cycle ratio 5:11 (31.25%)
0101: duty cycle ratio 6:10 (37.50%)
0110: duty cycle ratio 7: 9 (43.75%)
0111: duty cycle ratio 8: 8 (50.00%)
1000: duty cycle ratio 9: 7 (56.25%)
1001: duty cycle ratio 10: 6 (62.50%)
1010: duty cycle ratio 11: 5 (68.75%)
1011: duty cycle ratio 12: 4 (75.00%)
1100: duty cycle ratio 13: 3 (81.25%)
1101: duty cycle ratio 14: 2 (87.50%)
1110: duty cycle ratio 15: 1 (93.75%)
1111: duty cycle ratio 16: 0 (100.00%, maximum brightness)

[3:1] TIMING:
TIMING is the time unit from which the duration of the ON period and OFF period is defined in:
“000” = 20 mS
“001” = 40 mS
“010” = 80 mS
“011” = 160 mS
“100” = 320 mS
“101” = 640 mS
“110” = 1280 mS
“111” = 2560 mS

[0] RAMP_EN:
‘0’ to disable ramp mode
‘1’ to enable ramp mode

PWM_n_CTRL — PWM_n control registers n=0-3

7	6	5	4	3	2	1	0
PERIOD_0		PERIOD_1		REPETITION			FRAME ORDER

Address: 0xB1, 0xB5, 0xB9, 0xBD

Type: R/W

Reset: 0x00

Description: The PWM setup registers defines the period in blinking mode.

[7:6] PERIOD 0:
This defines the ON period time which is when the PWM channel output is toggling. The time unit is as defined in the TIMING bits of the respective TIMING_SETUP registers:
00: 1 time unit
01: 2 time unit
10: 3 time unit
11: 4 time unit

[5:4] PERIOD 1:
This defines the OFF period time which is when the PWM channel output is low, that is, not toggling. The time unit is as defined in the TIMING bits of the respective TIMING_SETUP registers:
00: 0 time unit. This means that there is no OFF period but only ON period, that is, the PWM channel output will always be toggling.
01: 1 time unit
10: 2 time unit
11: 3 time unit

[3:1] REPETITION:
This defines the number of repetition of pairs of PERIOD 0 and PERIOD 1.
000: Infinite repetition.
001: Execute only one pair.
010: Execute 2 pairs.
011: Execute 3 pairs.
100: Execute 4 pairs.
101: Execute 5 pairs.
110: Execute 6 pairs.
111: Execute 7 pairs.

[0] FRAME ORDER:
For PWM mode, this defines which frame, PERIOD0 or PERIOD1 comes first.
0: PERIOD 0 is outputted first then PERIOD 1.
1: PERIOD 1 is outputted first then PERIOD 0.

11.2 Interrupt on basic PWM controller

The basic PWM controller can be programmed to generate interrupts on completion of the blinking sequence. However, there are some limitations:

a) Each basic PWM controller has its own bit in interrupt the enable/status registers.

b) If enabled, the completion in any of the PWM controllers triggers interrupts. No interrupt is generated if infinite repetition is set.

12 Maximum rating

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 12. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
V18	Power supply	–	–	2.5	V
V33	Power supply	–	–	6.0	V
V_{IN}	Digital input	-0.3	–	V18 +0.3	V
T_J	Operating temperature	-40	–	85	C
T_S	Storage temperature	-55	–	125	C
ESD	HBM on all pins	–	8	–	kV

12.1 Recommended operating conditions

Table 13. Recommended operating conditions

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
V18	Power supply	1.65	1.8	1.95	V
V33	Power supply	2.7	–	5.5	V
V_{IN}	Digital input	–	–	–	V
T_J	Operating temperature	-45	25	85	C

13 Electrical specifications

Table 14. DC electrical characteristics (GPIO, reset, ADDR, I²C)

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
V_{IL}	Input voltage low state (reset/I²C)	V_{CC} = 1.8	-0.3 V	–	0.35 V_{CC}	V
V_{IH}	Input voltage high state (reset/I²C)	V_{CC} = 1.8	0.65 V_{CC}	–	V_{IO}+0.3	V
V_{IL}	Input voltage low state (GPIO)	V_{33} = 2.7 - 5.0	-0.3	–	0.35 V_{33}	V
V_{IH}	Input voltage high state (GPIO)	V_{33} = 2.7 - 5.0	0.65 V_{33}	–	V_{33}+0.3	V
V_{OL}	Output voltage low state (GPIO)	V_{33} = 3.3 –5.0 V, I_{OL} = 8 mA	-0.3 V	–	0.25 V_{IO}	V
V_{OH}	Output voltage high state (GPIO)	V_{33} = 3.3 –5.0 V, I_{OL} = 8 mA	0.75 V_{33}	–	V_{33}+0.3	V
$I_{LEAKAGE}$	Input leakage current	V_{IN} = 5.5 V, V_{33} = 5.5 V All GPIOs	–	0.05	0.5	µA

Table 15. Power consumption (-40 °C - 85 °C)

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
Iactive1	ACTIVE current 100% touch activity	Internal REG	–	1.0	1.4	mA
Iactive2	ACTIVE current 5% touch activity	Internal REG	–	75	110	µA
Isleep	SLEEP current	Internal REG	–	25	40	µA
Ihibernate	HIBERNATE current	Internal REG	–	5	10	µA

13.1 Capacitive sensing characteristics

Table 16. Capacitive sensing characteristics

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
Res	Capacitive measurement resolution	Aref = not connected	-	50	-	fF
DR	Dynamic range	Aref = not connected	-	6	-	pF
L	Linearity of sensor	Aref = not connected Maximum deviation calculated from full scale capacitance measurement data	-	10	-	%

14 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 14. Package outline for QFN40 (5 x 5 mm) - pitch 0.4 mm

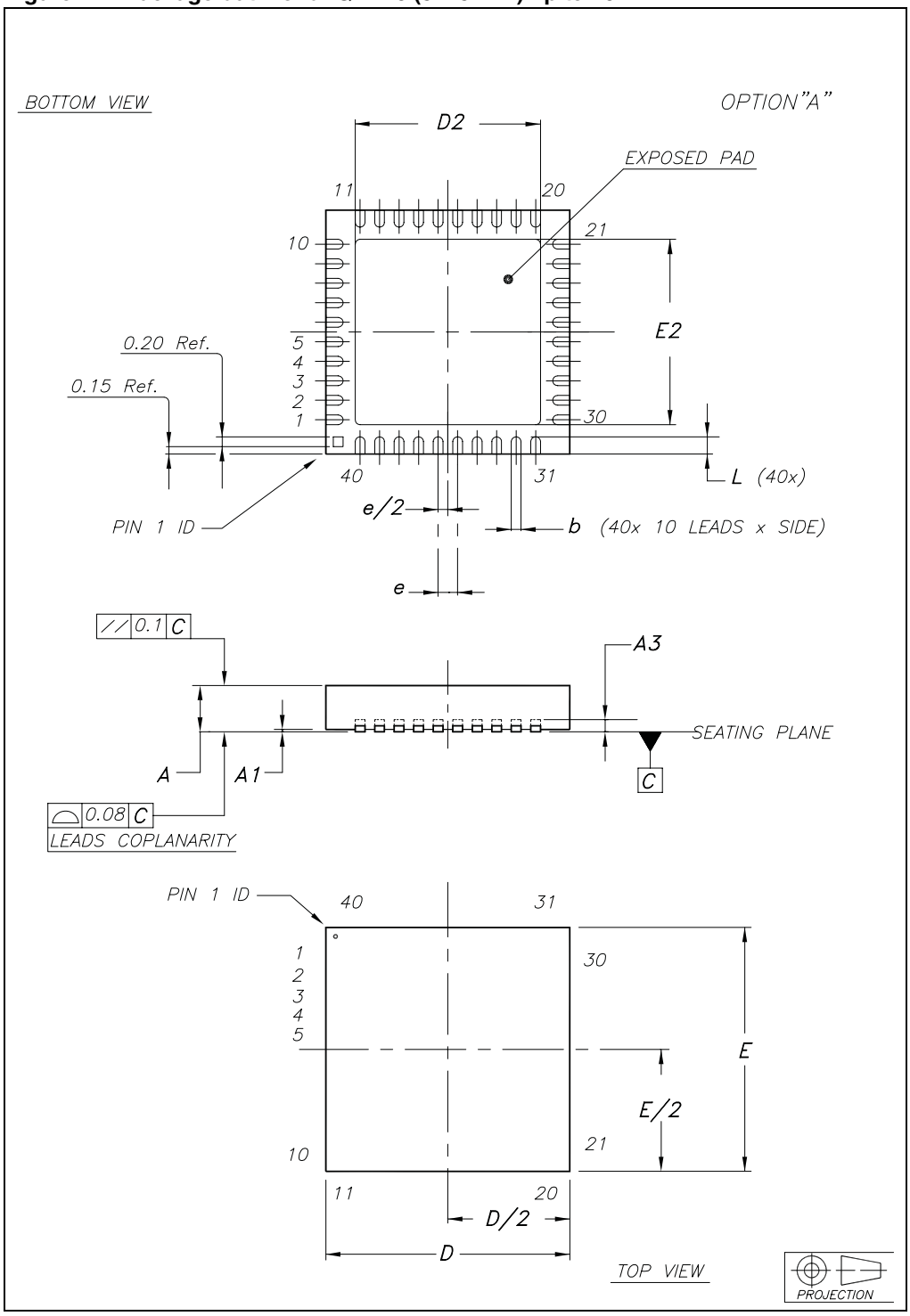


Figure 15. QFN40 recommended footprint without ground pad VIA

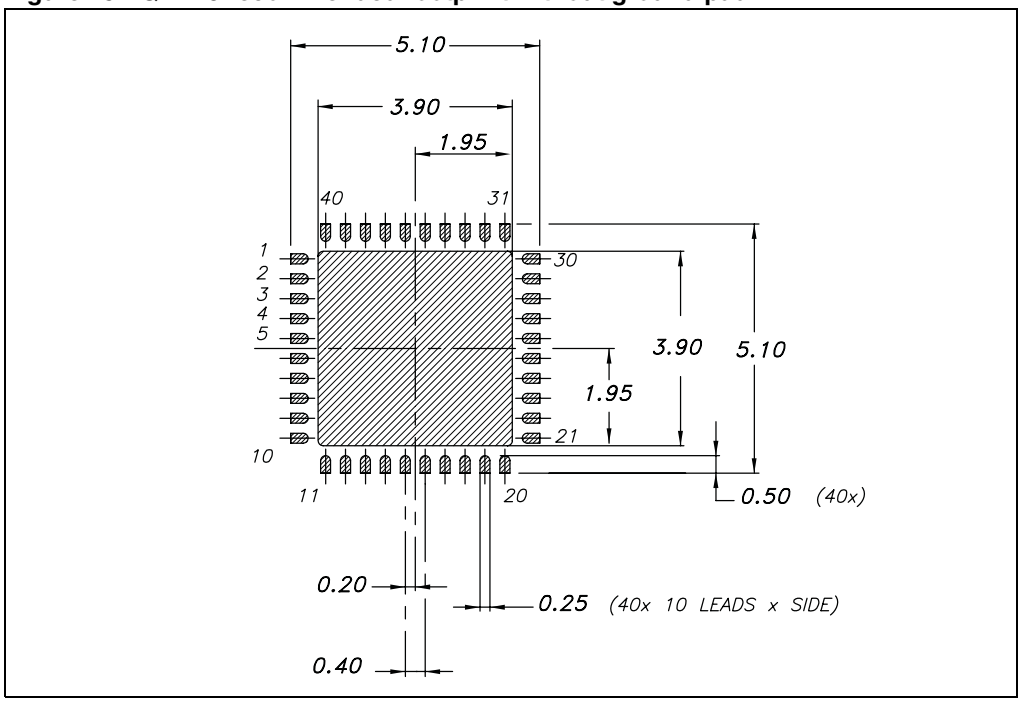


Figure 16. QFN40 recommended footprint with ground pad VIA

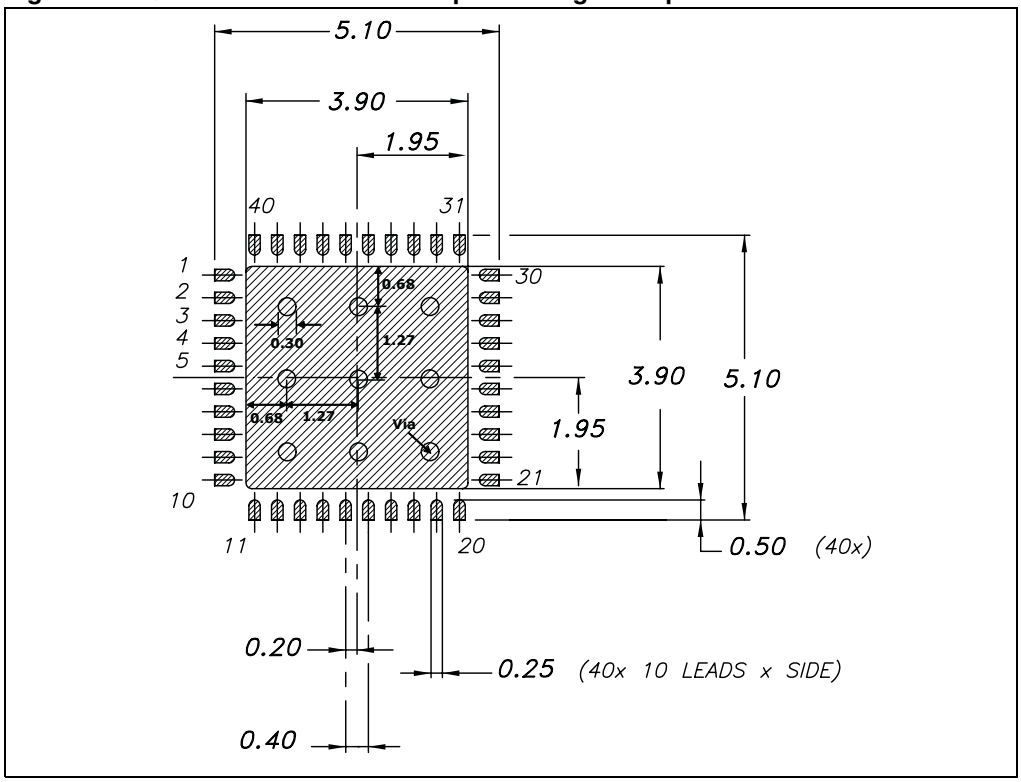


Figure 17. Tape information for QFN40 (5 x 5 mm) - pitch 0.4 mm

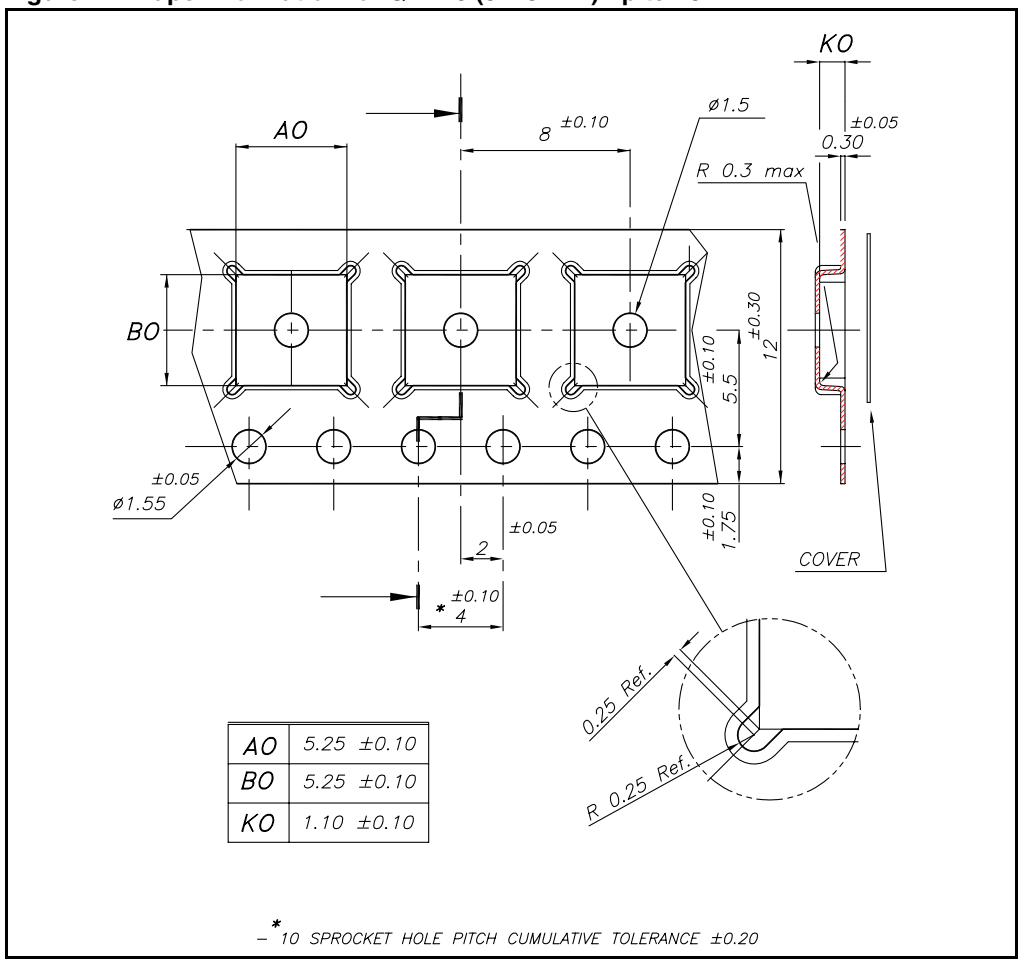
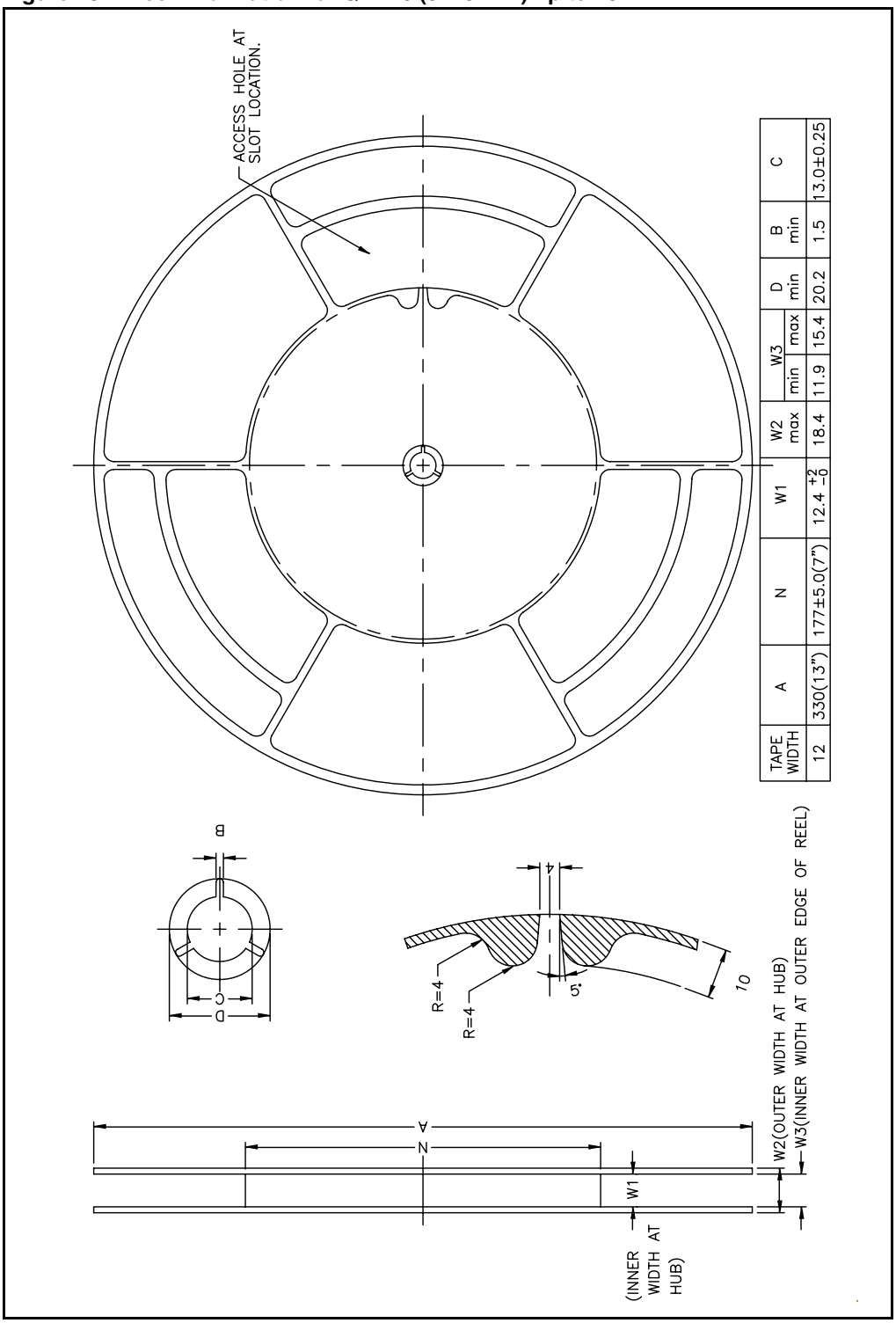


Figure 18. Reel information for QFN40 (5 x 5 mm) - pitch 0.4 mm



TAPE WIDTH	A	N	W1	W2 max	W3 min	W3 max	D min	B min	C
12	330(13")	177±5.0(7")	12.4 $^{+2}_{0}$	18.4	11.9	15.4	20.2	1.5	13.0±0.25

15 Revision history

Table 17. Document revision history

Date	Revision	Changes
27-May-2009	1	Initial release.
29-May-2009	2	Minor text changes in the Features section.

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