SEMTECH

SX8650

World's Lowest Power & Smallest Footprint 4-wire Resistive Touchscreen Controller with 15kV ESD

ADVANCED COMMUNICATIONS & SENSING DATASHEET

GENERAL DESCRIPTION

The SX8650 is an ultra low power 4-wire resistive touchscreen controller optimized for portable equipment where power and board-space are at a premium.

It incorporates a highly accurate 12-bit ADC for data conversion and operates from a single 1.65 to 3.7V supply voltage.

The SX8650 features a built-in preprocessing algorithm for data measurements, which greatly reduces the host processing overhead and bus activity. This complete touchscreen solution includes four user-selectable operation modes which offer programmability on different configurations such as conversion rate and settling time, thus enable optimization in throughput and power consumption for a wide range of touch sensing applications.

The touch screen inputs have been specially designed to provide robust on-chip ESD protection of up to ±15kV in both HBM and Contact Discharge, and eliminates the need for external protection devices.

The SX8650 supports the Fast-mode I²C (400kbit/s) serial bus data protocol and includes 2 user-selectable slave addresses. A custom I2C address is possible on request.

The SX8650 is offered in two tiny packages: a 3.0 mm x 3.0 mm DFN and a 1.5 mm x 2.0 mm wafer-level chip-scale package (WLCSP).

APPLICATIONS

- Portable Equipment
- Mobile Communication Devices
- Cell phone, PDA, MP3, GPS, DSC
- Touch Screen Monitors

KEY PRODUCT FEATURES

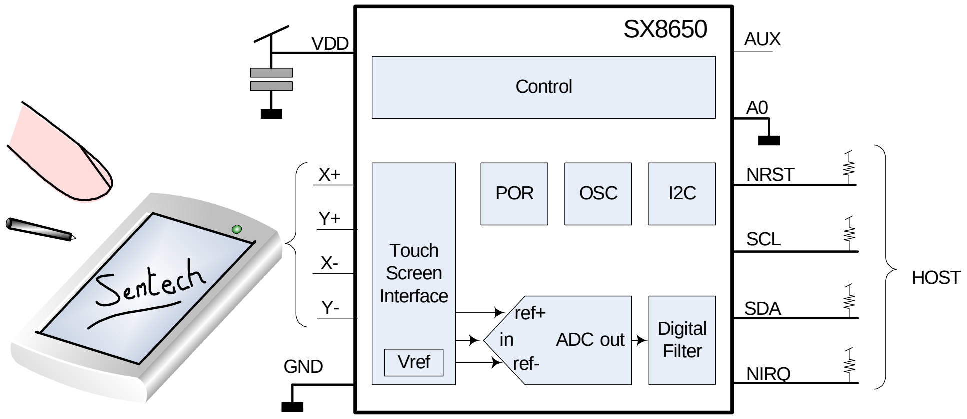
- Extremely Low Power Consumption:23uA@1.8V 8kSPS
- Superior On-chip ESD Protection
  - ➪±15kV HBM (X+,X-,Y+,Y-)
  - ➪±2kV CDM
  - ➪±25kV Air Gap Discharge
  - ➪±15kV Contact Discharge
  - ➪±300V MM
- Single 1.65V to 3.7V Supply/Reference
- Integrated Preprocessing Block to Reduce Host Loading and Bus Activity
- Four User Programmable Operation Modes provides Flexibility to address Different Application Needs
  - ➪Manual, Automatic, Pen Detect, Pen Trigger
- High Precision 12-bit Resolution
- Low Noise Ratiometric Conversion
- Selectable Polling or Interrupt Modes
- Touch Pressure Measurement
- 400kHz Fast-Mode I²C Interface
- Hardware Reset & I²C Software Reset
- -40℃ to 85℃ Operation
- 12-LD (3.0 mm x 3.0 mm) DFN Package
- 12 Ball (1.5 mm x 2.0 mm) WLCSP Package
- Pb-Free, Halogen Free, RoHS/WEEE compliant product
- Windows CE 6.0, Linux Driver Support Available

ORDERING INFORMATION

Part Number	Package
SX8650ICSTRT[1]	12 - Ball WLCSP (1.5 mm x 2.0 mm)
SX8650IWLTRT[1]	12 - Lead DFN (3.0 mm x 3.0 mm)

[1] 3000 Units / reel

Block Diagram



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1. General Description

1.1. Pin Diagram DFN

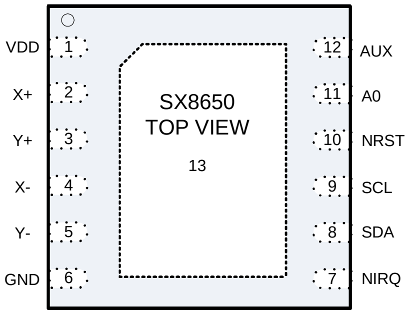


Figure 1. Pinout diagram, DFN

1.2. Marking Information DFN

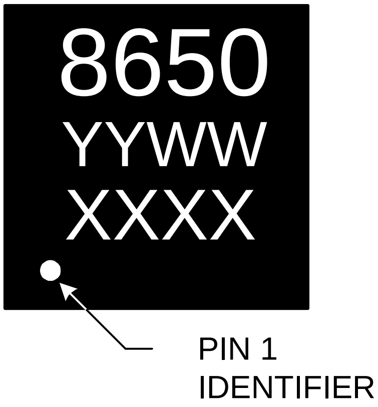
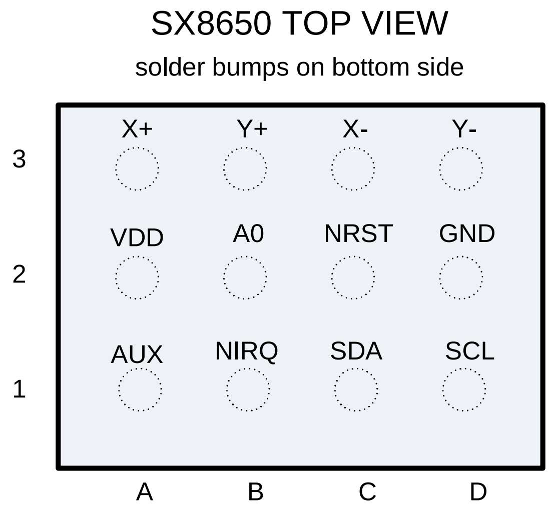


Figure 2. Marking information, DFN

On Figure 2, *YYWW* is the Date Code and *XXXX* is the Lot Number.

1.3. Pin Diagram WLCSP



	A	B	C	D
3	X+	Y+	X-	Y-
2	VDD	A0	NRST	GND
1	AUX	NIRQ	SDA	SCL

Figure 3. Pinout diagram, WLCSP

1.4. Marking Information WLCSP

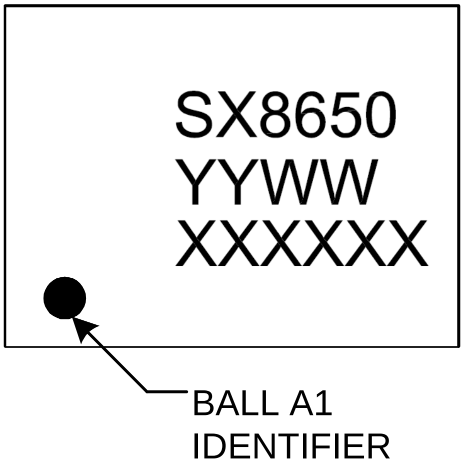


Figure 4. Marking information, WLCSP

On Figure 4, *YYWW* is the Date Code and *XXXXX* is the Lot Number.

1.5. Pin Description

Pin Number #		Name	Type	Description
DFN	WLCSP			
1	A2	VDD	Power	Input power supply connect to a 0.1uF capacitor to GND
2	A3	X+	Analog	X+ channel input
3	B3	Y+	Analog	Y+ channel input
4	C3	X-	Analog	X- channel input
5	D3	Y-	Analog	Y- channel input
6	D2	GND	Ground	Ground
7	B1	NIRQ	Digital Output / Open Drain Output	Interrupt output, active low. Need external pull-up resistor
8	C1	SDA	Digital Input / Open Drain Output	I2C data input/output
9	D1	SCL	Digital Input / Open Drain Output	I2C clock, input/output
10	C2	NRST	Digital Input / Output	Reset Input, active low. Need external 50k pull-up resistor
11	B2	A0	Digital Input	I2C slave address selection input
12	A1	AUX	Digital Input/Analog Input	Analog auxiliary input or conversion synchronization
13		GND	Ground	Die attach paddle, connect to Ground

Table 1. Pin description

1.6. Simplified Block Diagram

The SX8650 simplified block diagram is shown in Figure 5.

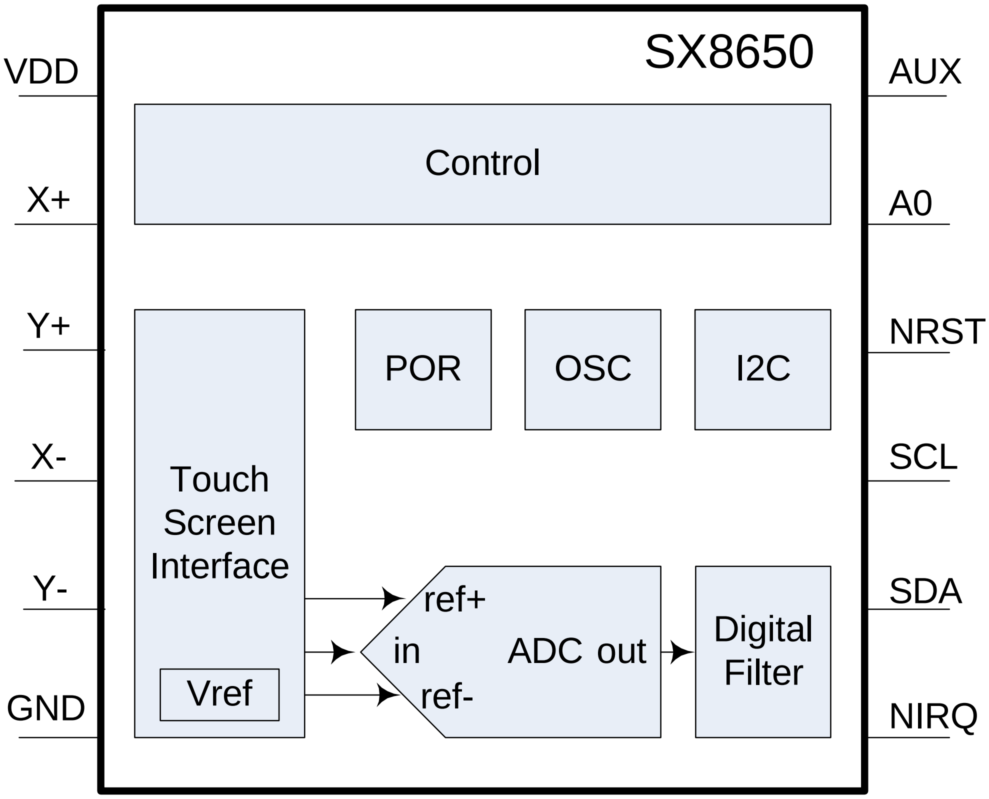


Figure 5. Simplified block diagram of the SX8650

2. Electrical Characteristics

2.1. Absolute Maximum Ratings

Stresses above the values listed in "Absolute Maximum Ratings" may cause permanent damage to the device.

This is a stress rating only and functional operation of the device at these, or any other conditions beyond the "Recommended Operating Conditions", is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter		Symbol	Min.	Max.	Unit
Supply Voltage		V_{DDABS}	-0.5	3.9	V
Input voltage (non-supply pins)		V_{IN}	-0.5	3.9	V
Input current (non-supply pins)		I_{IN}		10	mA
Operating Junction Temperature		T_{JCT}		125	℃
Reflow temperature		T_{RE}		260	℃
Storage temperature		T_{STOR}	-50	150	℃
ESD HBM (Human Body Model)	High ESD pins: X+, X-,Y+,Y-	ESD_{HBM1}	± 15[(i)]		kV
			± 8[(ii)]		kV
	All pins except high ESD pins: AUX,A0,NRST,NIRQ,SDA,SCL	ESD_{HBM2}	± 2[(ii)]		kV
ESD (Contact Discharge)	High ESD pins: X+, X-,Y+,Y-	ESD_{CD}	± 15		kV
Latchup		I_{LU}	± 100[(iii)]		mA

Table 2. Absolute Maximum Ratings

(i) Tested to TLP (10A)

(ii) Tested to JEDEC standard JESD22-A114

(iii) Tested to JEDEC standard JESD78

2.2. Recommended Operating Conditions

Parameter	Symbol	Min.	Max	Unit
Supply Voltage	V_{DD}	1.65V	3.7	V
Ambient Temperature Range	T_A	-40	85	℃

Table 3. Recommended Operating Conditions

2.3. Thermal Characteristics

Parameter	Symbol	Min.	Max	Unit
Thermal Resistance with DFN package - Junction to Ambient (i)	θ_{JA}		39	℃/W
Thermal Resistance with WLCSP package - Junction to Ambient (i)	θ_{JA}		65	℃/W

Table 4. Thermal Characteristics

(i) θ_{JA} is calculated from a package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under exposed pad (if applicable) per JESD51 standards.

2.4. Electrical Specifications

All values are valid within the recommended operating conditions unless otherwise specified.

Parameter	Symbol	Conditions	Min.	Typ	Max	Unit
Current consumption						
Manual	I_{pwd}	Manual (converter stopped, pen detection off, I2C listening, OSC stopped)		0.4	0.75	uA
Pen Detect	I_{pndt}	Pen detect mode (converter stopped, pen detection activated, device will generate interrupt upon detection, I2C listening, OSC stopped).		0.4	0.75	uA
Pen Trigger	I_{pntr}	Pen trigger mode (converter stopped, pen detection activated, device will start conversion upon pen detection. I2C listening, OSC stopped		0.4	0.75	uA
Automatic	I_{wt}	Automatic (converter stopped, pen detection off, I2C listening, OSC and timer on, device is waiting for timer expiry)		1.5		uA
Operation @8kSPS, VDD=1.8V	I_{opl}	X,Y Conv. RATE=4kSPS, N_{filt}=1 PowDly=0.5us, SetDly=0.5us		23	50	uA
Operation @42kSPS, VDD=3.3V	I_{oph}	X,Y Conv. RATE=3kSPS, N_{filt}=7 PowDly=0.5us, SetDly=0.5us		105	140	uA
Digital I/O						
High-level input voltage	V_{IH}		0.7V_{DD}		V_{DD}+0.5	V
Low-level input voltage	V_{IL}		V_{SS}-0.3		0.3V_{DD}	V
SDA / SCL Hysteresis of Schmitt trigger inputs VDD > 2 V VDD < 2 V	V_{hys}		0.05V_{DD} 0.1V_{DD}			V
Low-level output voltage	V_{OL}	I_{OL}=3mA, V_{DD}>2V I_{OL}=3mA, V_{DD}<2V	0 0		0.4 0.2V_{DD}	V
Input leakage current	L_I	CMOS input			±1	uA
AUX						
Input voltage range	V_{IAUX}		0		V_{DD}	V

Table 5. Electrical Specifications

Parameter	Symbol	Conditions	Min.	Typ	Max	Unit
Input capacitance	C_{X+},C_{X-},C_{Y+}, C_{Y-}			50		pF
	C_{AUX}			5		pF
Input leakage current	I_{IAUX}		-1		1	uA
Startup						
Power-up time	t_{por}	Time between rising edge VDD and rising NIRQ			1	ms
ADC						
Resolution	A_{res}		12			bits
Offset	A_{off}			±1		LSB
Gain error	A_{ge}	At full scale		0.5		LSB
Differential nonlinearity	A_{dnl}			±1		LSB
Integral nonlinearity	A_{inl}			±1.5		LSB
Resistors						
X+, X-, Y+, Y- resistance	R_{chn}	Touch Pad Biasing Resistance		5		Ohm
Pen detect resistance	R_{PNDT_00}	R_{PNDT} = 0		100		kOhm
	R_{PNDT_01}	R_{PNDT} = 1		200		kOhm
	R_{PNDT_10}	R_{PNDT} = 2		50		kOhm
	R_{PNDT_11}	R_{PNDT} = 3		25		kOhm
External components		**recommendations**				
Capacitor between VDD, GND	C_{vdd}	Type 0402, tolerance +/-50%		0.1		uF

Table 5. Electrical Specifications

2.5. Host Interface Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit
I2C TIMING SPECIFICATIONS (i)						
SCL clock frequency	f_{SCL}		0		400	kHz
SCL low period	t_{LOW}		1.3			us
SCL high period	t_{HIGH}		0.6			us
Data setup time	$t_{SU;DAT}$		100			ns
Data hold time	$t_{HD;DAT}$		0			ns
Repeated start setup time	$t_{SU;STA}$		0.6			us
Start condition hold time	$t_{HD;STA}$		0.6			us
Stop condition setup time	$t_{SU;STO}$		0.6			us
Bus free time between stop and start	t_{BUF}		1.3			us
Data valid time	$t_{VD;DAT}$				0.9	us
Data valid ack time	$t_{VD;ACK}$				0.9	us
Pulse width of spikes that must be suppressed by the input filter	t_{SP}				50	ns
I2C BUS SPECIFICATIONS						
Capacitive Load on each bus line SCL, SDA	C_b				400	pF

Table 6. Host Interface Specifications

Notes:

(i) All timing specifications refer to voltage levels (V_{IL}, V_{IH}, V_{OL}) defined in Table 5 unless otherwise mentioned.

2.6. Host Interface Timing Waveforms

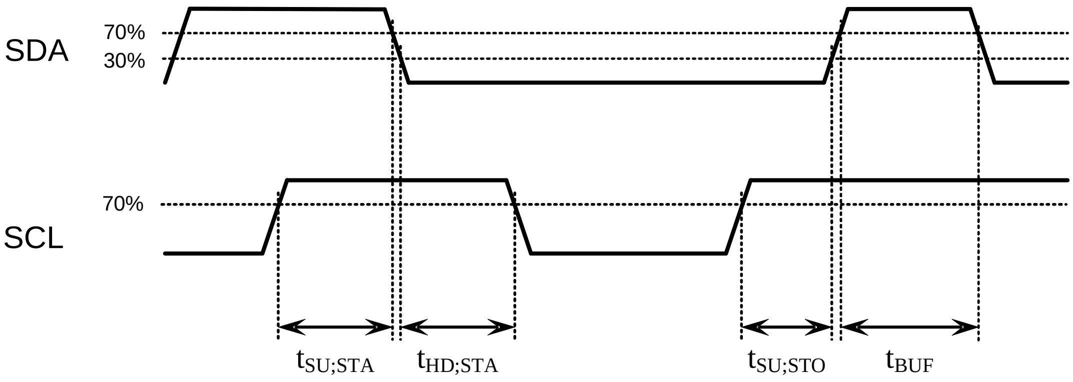


Figure 6. I2C Start and Stop timing

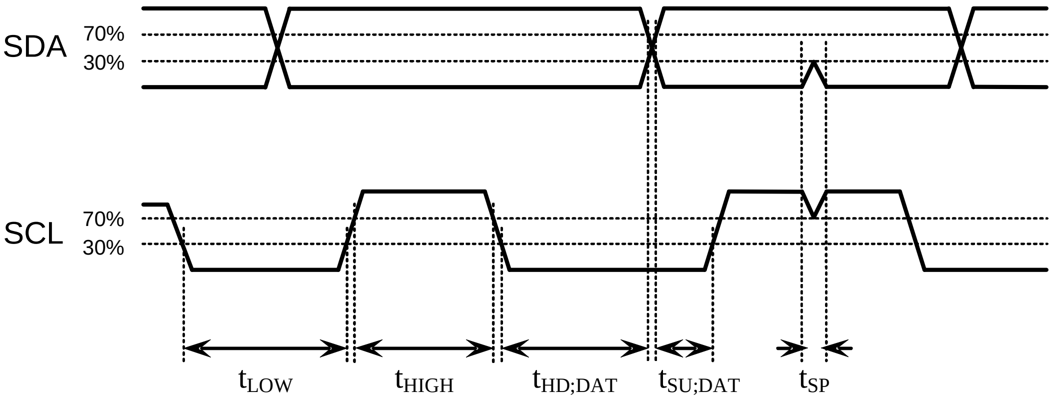
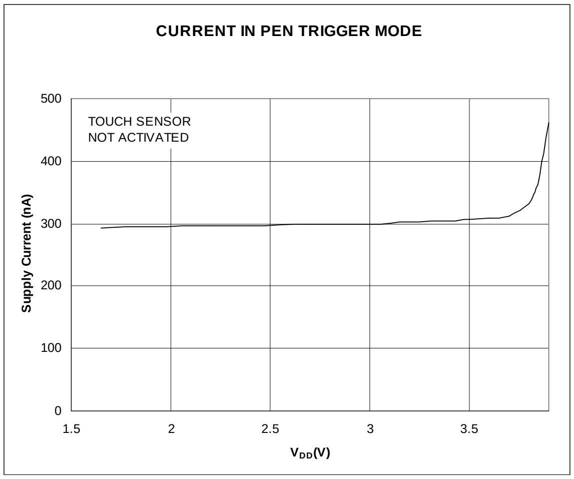
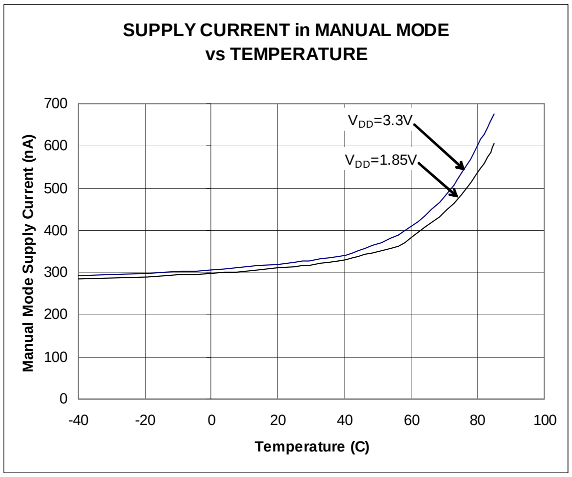


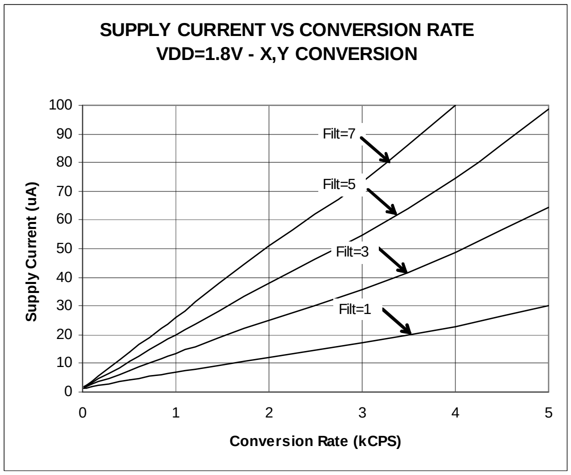
Figure 7. I2C Data timing

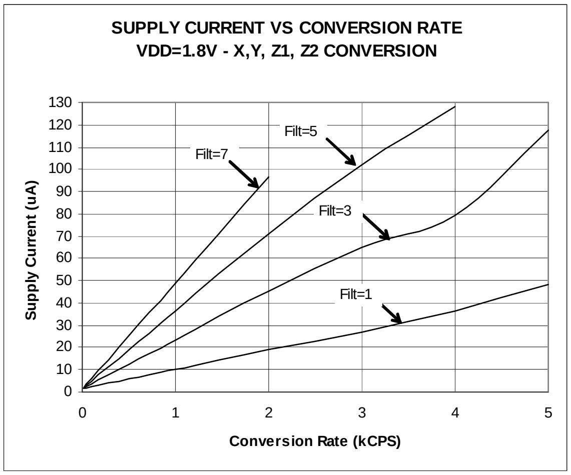
2.7. Typical Operating Characteristics

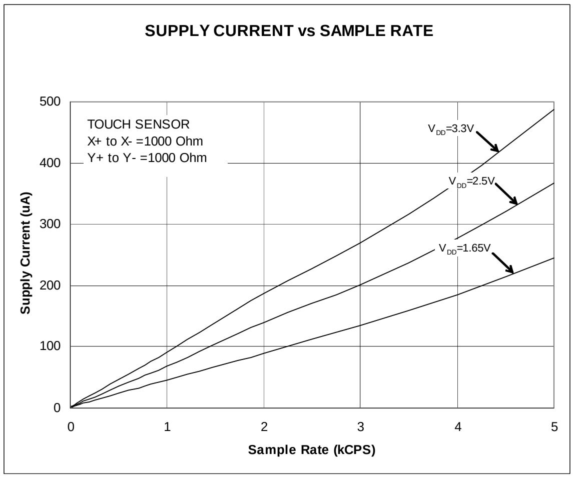
At Ta= -40℃ to +85℃, VDD=1.7V to 3.7V, PowDly=0.5 us, SetDly=0.5us, Filt=1, Resistive touch screen sensor current not taking in account, unless otherwise noted.





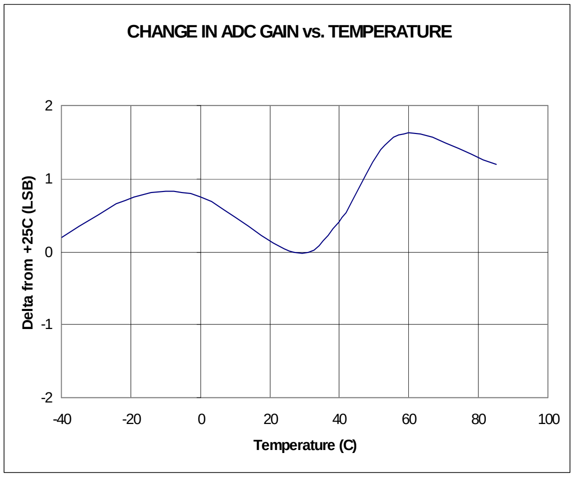


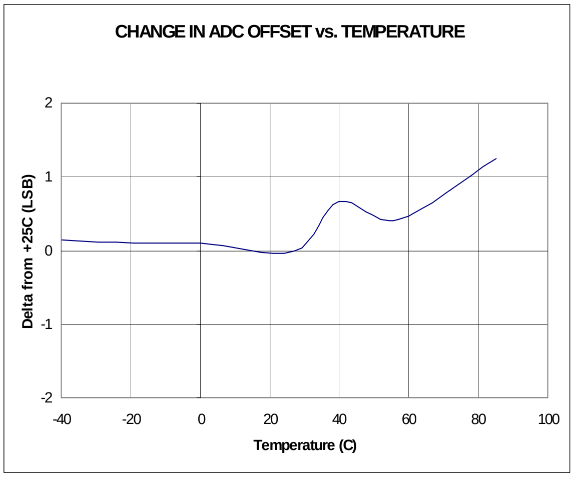


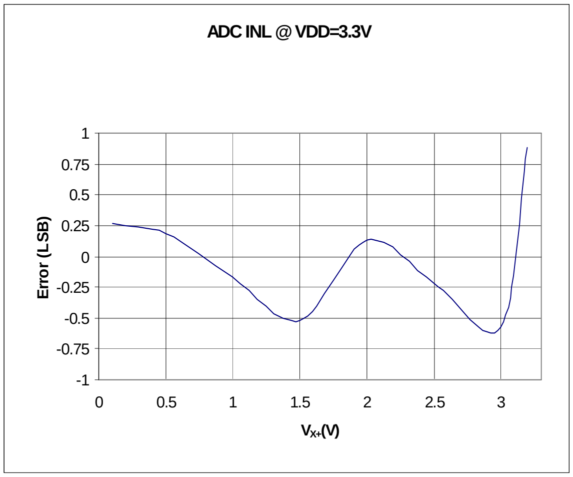


Typical Operating Characteristics (continued)

At Ta= -40℃ to +85℃, VDD=1.7V to 3.7V, PowDly=0.5 us, SetDly=0.5us, Filt=1, Resistive touch screen sensor current not taking in account, unless otherwise noted.







3. Functional Description

3.1. General Introduction

This section provides an overview of the SX8650 architecture, device pinout and a typical application.

The SX8650 is designed for 4-wire resistive touch screen applications (Figure 8).The touch screen or touch panel is the resistive sensor and can be activated by either a finger or stylus. The touch screen coordinates and touch pressure are converted into I2C format by the SX8650 for transfer to the host.

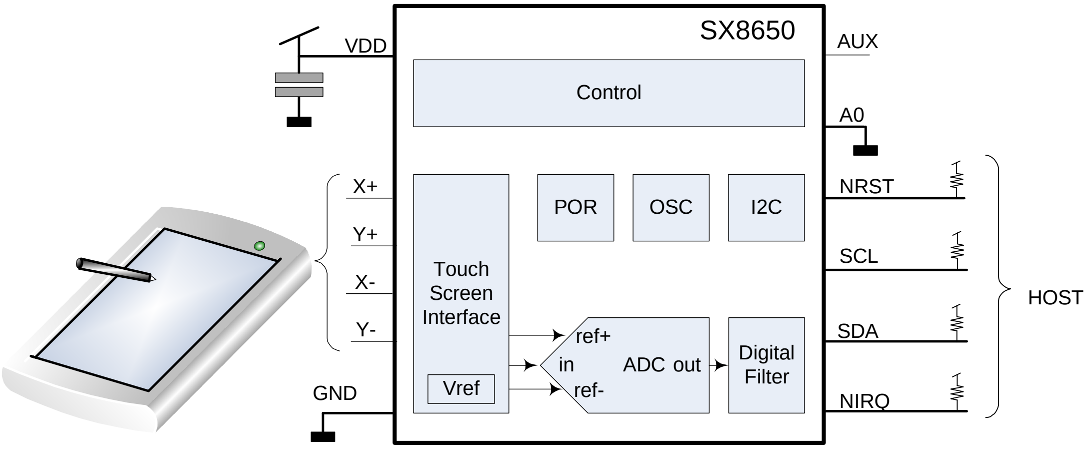


Figure 8. SX8650 with screen

3.2. Channel Pins

3.2.1. X+, X-, Y+. Y-

The SX8650's channel pins (X+, X-, Y+, Y-) directly connect to standard touch screen X and Y resistive layers. The SX8650 separately biases each of these layers and converts the resistive values into (X,Y) coordinates.

The channel pins are protected to VDD and GROUND.

Figure 9 shows the simplified diagram of the X+, X-, Y+, Y- pins.

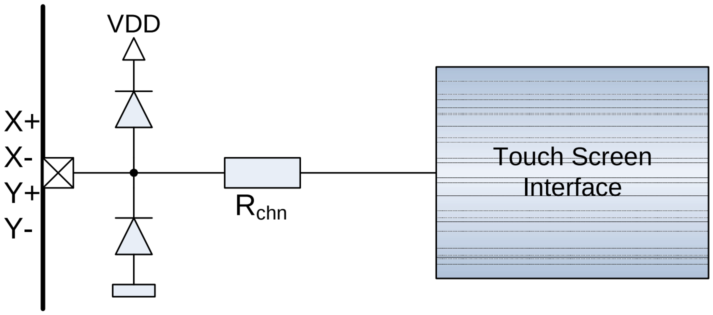


Figure 9. Simplified diagram of X+, X-, Y+, Y- pins

3.2.2. AUX

The SX8650 interface includes an AUX pin that serves two functions: an ADC input; and a start of conversion trigger. When used as an ADC, the single ended input range is from GND to VDD, referred to GND. When the AUX input is configured to start conversions, the AUX input can be further configured as a rising and / or falling edge trigger.

The AUX is protected to VDD and GROUND.

Figure 10 shows a simplified diagram of the AUX pin.

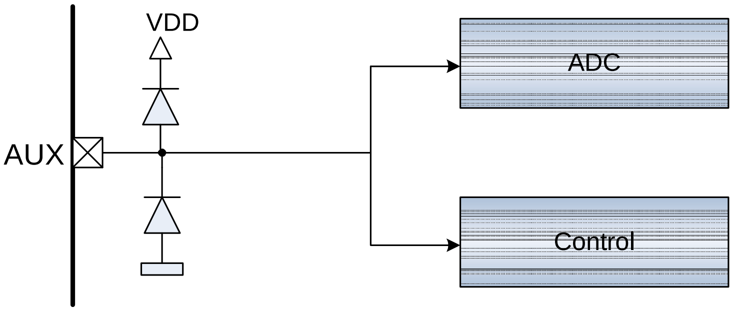


Figure 10. Simplified diagram of AUX

3.3. Host Interface and Control Pins

The SX8650 host and control interface consists of: NIRQ, I2C pins SCL and SDA, A0, and NRST.

3.3.1. NIRQ

The NIRQ pin is an active low, open drain output to facilitate interfacing to different supply voltages and thus requires an external pull-up resistor (1-10 kOhm). The NIRQ pin does not have protection to VDD.

The NIRQ function is designed to provide an interrupt to the host processor. Interrupts may occur when a pen is detected, or when channel data is available.

Figure 11 shows a simplified diagram of the NIRQ pin.

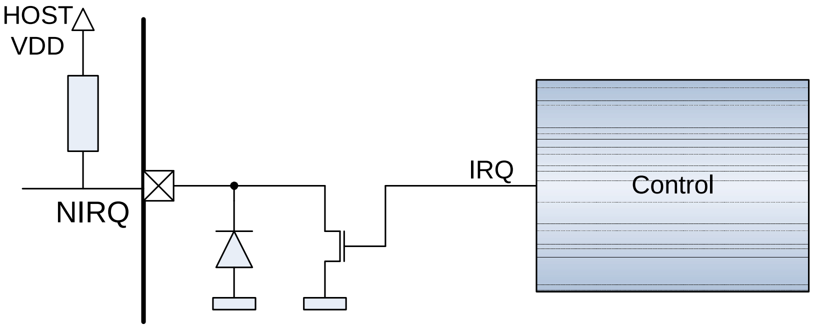


Figure 11. Simplified diagram of NIRQ

3.3.2. SCL

The SCL pin is a high-impedance input and open-drain output pin. The SCL pin does not have protection to VDD to conform to I2C slave specifications. An external pull-up resistor (1-10 kOhm) is required.

Figure 12 shows the simplified diagram of the SCL pin.

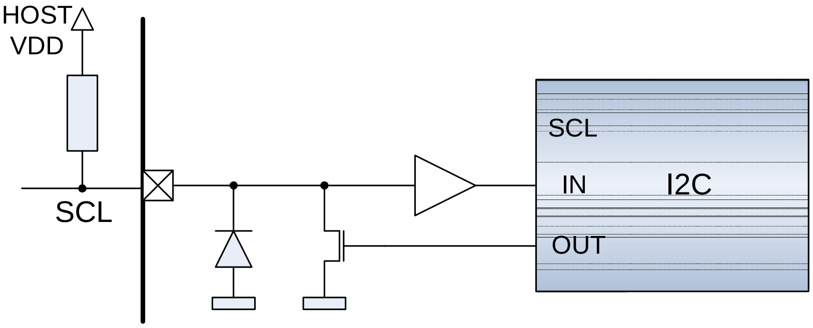


Figure 12. Simplified diagram of SCL

3.3.3. SDA

SDA is an I/O pin. It can be used as an open-drain output (with external pull-up resistor) or as an input. An external pull-up resistor (1-10 kOhm) is required.

The SDA I/O pin does not have protection to VDD to conform to I2C slave specifications.

Figure 13 shows a simplified diagram of the SDA pin.

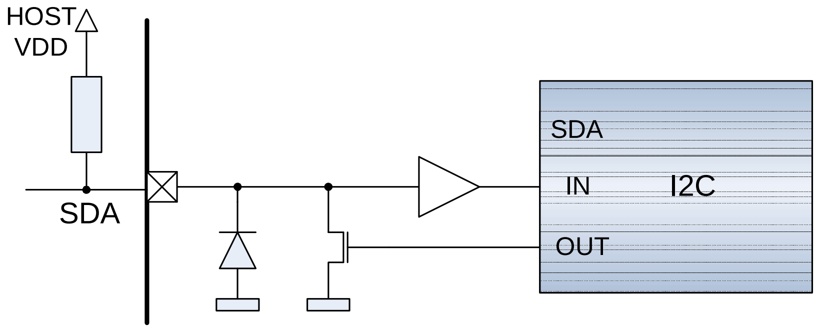


Figure 13. Simplified diagram of SDA

3.3.4. A0

The A0 pin is connected to the I2C address select control circuitry and is used to modify the device I2C address.

The A0 pin is protected to GROUND.

Figure 14 shows a simplified diagram of the A0 pin.

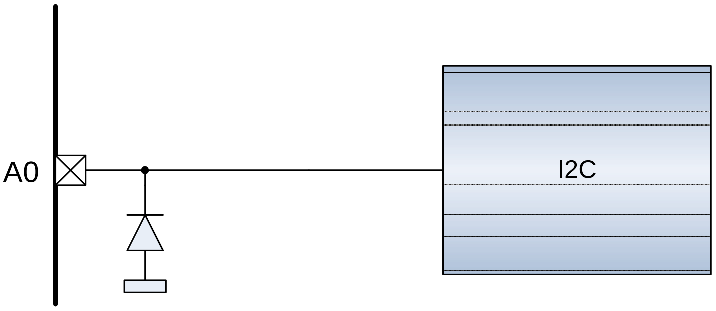


Figure 14. Simplified diagram of A0

3.3.5. NRST

The NRST pin is an active low input that provides a hardware reset of the SX8650's control circuitry.

The NRST pin is protected GROUND to enable interfacing with devices at a different supply voltages.

Figure 15 shows a simplified diagram of the NRST pin.

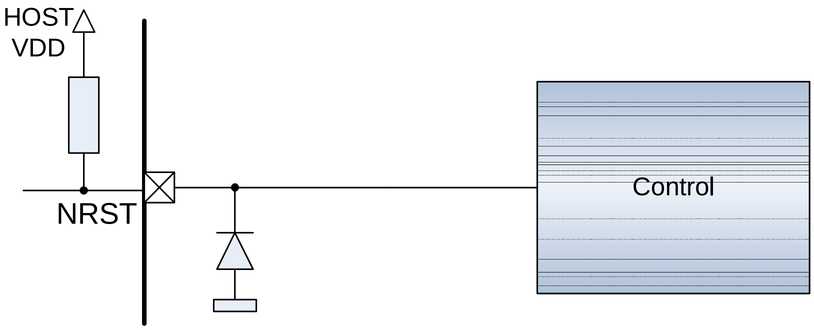


Figure 15. Simplified diagram of NRST

3.4. Power Management Pins

The SX8650's power management input consists of the following Power and Ground pins.

3.4.1. VDD

The VDD is a power pin and is the power supply for the SX8650.

The VDD has ESD protection to GROUND.

Figure 16 shows a simplified diagram of the VDD pin.

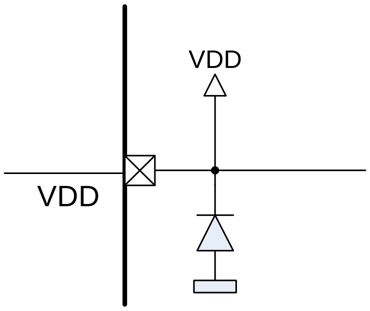


Figure 16. Simplified diagram of VDD

3.4.2. GND

The SX8650 has one power management ground pin, GND[1].

The GND has ESD protection to VDD.

Figure 17 shows a simplified diagram of the GND pin.

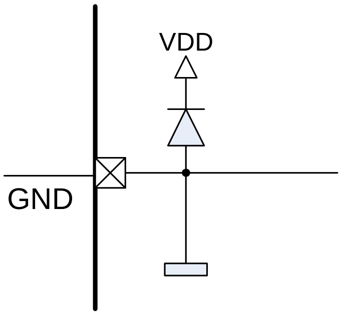


Figure 17. Simplified diagram of GND

[1] The die attach paddle on DFN is also connected to GND

4. Detailed Description

4.1. Touch Screen Operation

A resistive touch screen consists of two (resistive) conductive sheets separated by an insulator when not pressed. Each sheet is connected through 2 electrodes at the border of the sheet (Figure 18). When a pressure is applied on the top sheet, a connection with the lower sheet is established. Figure 19 shows how the Y coordinate can be measured. The electrode plates are connected through terminals X+, X- and Y+, Y- to an analog to digital converter (ADC) and a reference voltage. The resistance between the terminals X+ and X- is defined by Rxtot. Rxtot will be split in 2 resistors, R1 and R2, in case the screen is touched. The resistance between the terminals Y+ and Y- is represented by R3 and R4. The connection between the top and bottom sheet is represented by the touch resistance (R_T).

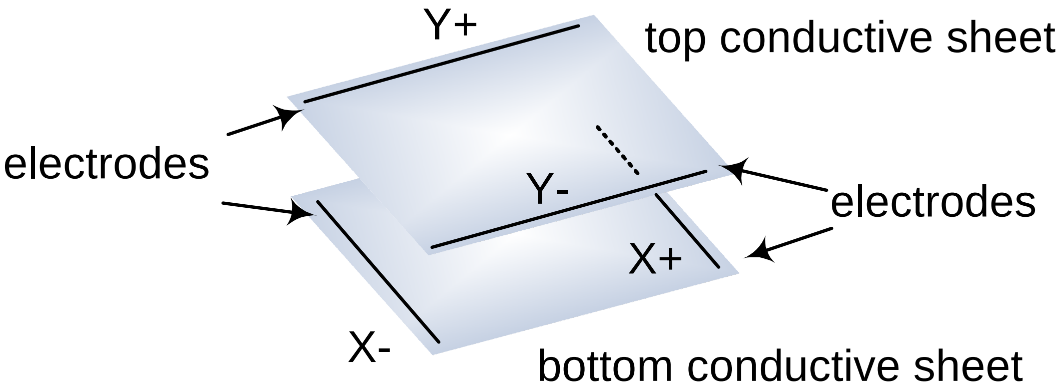


Figure 18. Touch Screen

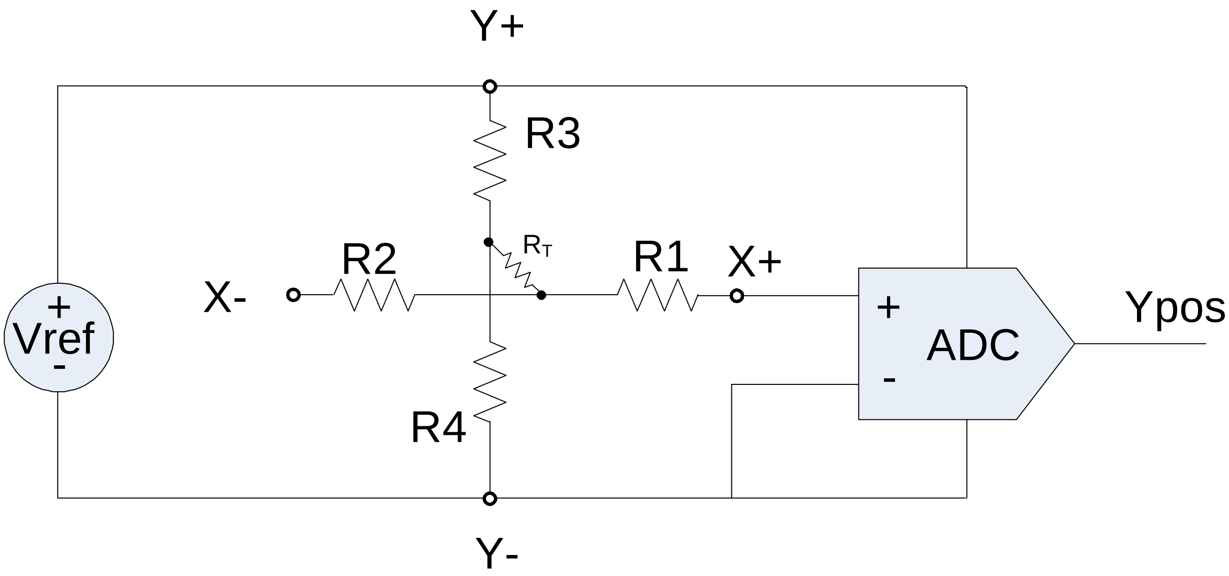


Figure 19. Touch Screen Operation ordinate measurement (Y)

4.2. Coordinates Measurement

The top resistive sheet (Y) is biased with a voltage source. Resistors R3 and R4 determine a voltage divider proportional to the Y position of the contact point. Since the converter has a high input impedance, no current flows through R1 so that the voltage X+ at the converter input is given by the voltage divider created by R3 and R4.

The X coordinate is measured in a similar fashion with the bottom resistive sheet (X) biased to create a voltage divider by R1 and R2, while the voltage on the top sheet is measured through R3. Figure 20 shows the coordinates measurement setup. The resistance R_T is the resistance obtained when a pressure is applied on the screen. R_T is created by the contact area of the X and Y resistive sheet and varies with the applied pressure.

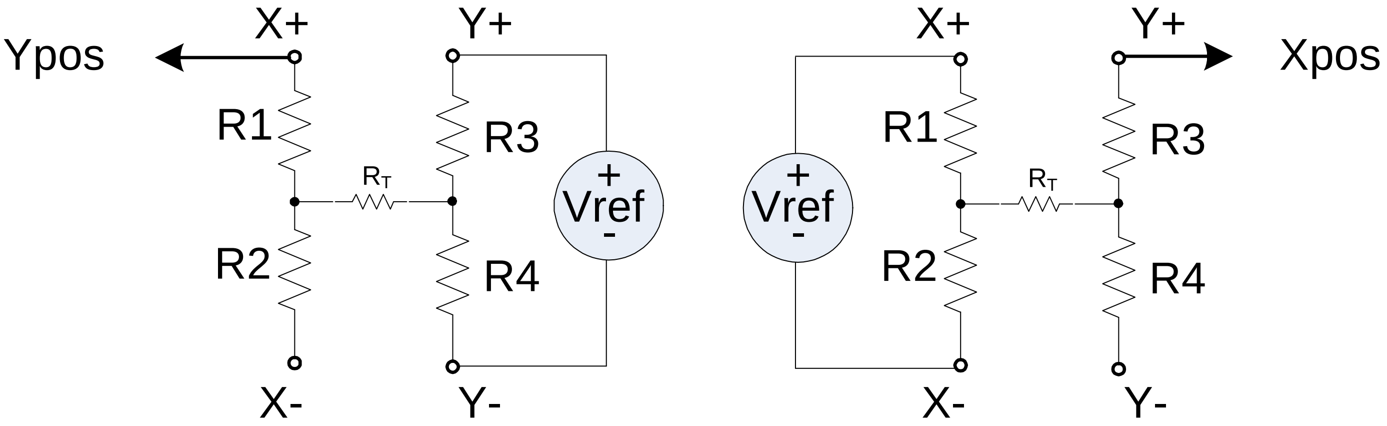


Figure 20. Ordinate (Y) and abscissa (X) coordinates measurement setup

The X and Y position are found by:

$$Xpos = 4095 \cdot \frac{R2}{R1 + R2}$$

$$Ypos = 4095 \cdot \frac{R4}{R3 + R4}$$

4.3. Pressure Measurement

The pressure measurement consists of two additional setups: z1 and z2 (see Figure 21).

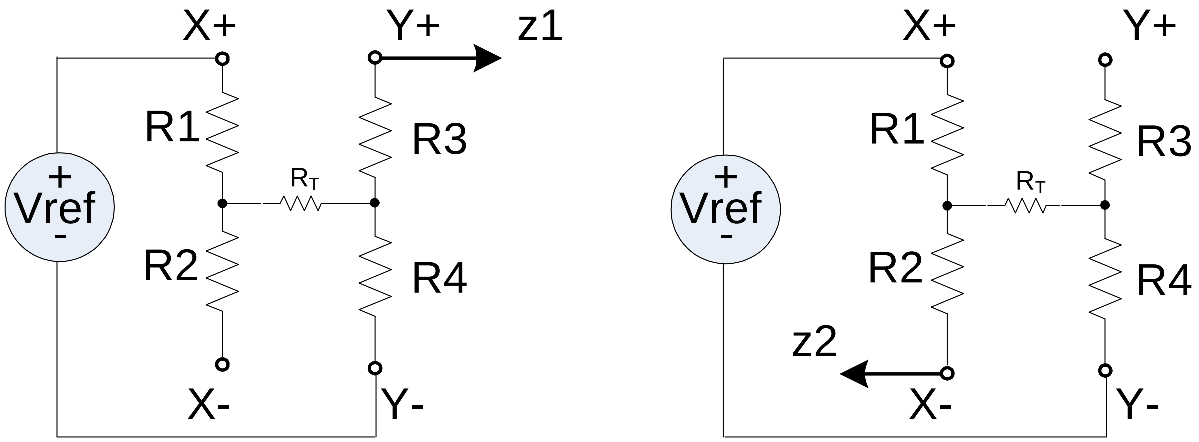


Figure 21. z1 and z2 pressure measurement setup

The corresponding equations for the pressure:

$$z1 = 4095 \cdot \frac{R4}{R1 + R4 + R_T}$$

$$z2 = 4095 \cdot \frac{R4 + Rt}{R1 + R4 + R_T}$$

The X and Y total sheet resistance (Rxtot, Rytot) are known from the touch screen supplier.

$$Rxtot = R1 + R2$$

$$Rytot = R3 + R4$$

R4 is proportional to the Y coordinate. The R4 value is given by the total Y plate resistance multiplied by the fraction of the Y position over the full coordinate range.

$$R4 = Rytot \cdot \frac{Ypos}{4095}$$

By re-arranging z1 and z2 one obtains

$$R_T = R4 \cdot \left[\frac{z2}{z1} - 1\right]$$

Which results in:

$$R_T = Rytot \cdot \frac{Ypos}{4095} \cdot \left[\frac{z2}{z1} - 1\right]$$

The touch resistance calculation above requires three channel measurements (Ypos, z2 and z1) and one specification data (Rytot).

An alternative calculation method is using Xpos, Ypos, one z channel and both Rxtot and Rytot shown in the next calculations.
R1 is inverse proportional to the X coordinate.

$$R1 = Rxtot \cdot \left[1 - \frac{Xpos}{4095}\right]$$

Substituting R1 and R4 into z1 and rearranging terms gives:

$$R_T = \frac{Rytot \cdot Ypos}{4095} \cdot \left[\frac{4095}{z1} - 1\right] - Rxtot \cdot \left[1 - \frac{Xpos}{4095}\right]$$

4.4. Pen Detection

If the touchscreen is powered between X+ and Y- through a resistor R_{PNDT}, no current will flow so long as pressure is not applied to the surface (see Figure 22). Node X+ will remain at the voltage reference voltage. When some pressure is applied, a current path is created and brings X+ to the level defined by the resistive divider determined by R_{PNDT} and the sum of R1, R_T and R4.

The X+ level is detected by a comparator followed by a S-R latch. R_{PNDT} should be set to a value greater than 7x(Rxtot + Rytot).

The pen detection will set the PENIRQ bit of the I2C status register and will activate (LOW) the NIRQ pin of the SX8650. The PENIRQ bit will be cleared and the NIRQ will be de-asserted as soon as the host reads the I2C status register.

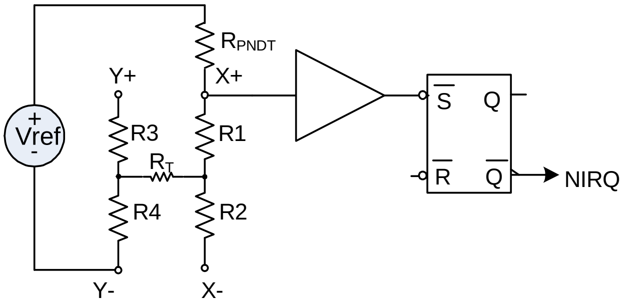


Figure 22. Pen detection

The resistor R_{PNDT} can be configured to 4 different values (see Table 9) to accommodate different screen resistive values.

4.5. Data Processing

The SX8650 offers 4 types of data processing which allows the user to make trade-offs between data throughput, power consumption and noise rejection.

The parameter FILT is used to select the filter order N_{filt} as seen in Figure 7. The noise rejection will be improved with a high order to the detriment of the power consumption. The effective coordinate throughput will remain the same for all filter configurations as the ADC will be enabled more often. For very high coordinate throughput rates the filter needs to be set to FILT=0 (see Table 7).

FILT	N_{filt}
0	1
1	3
2	5
3	7

Table 7. Filter order

Figure 23 shows the SX8650 configuration (FILT = 0) in which the ADC output samples, s_n are sent directly to the I2C interface. The FILT parameter can be setup through the I2C registers

.

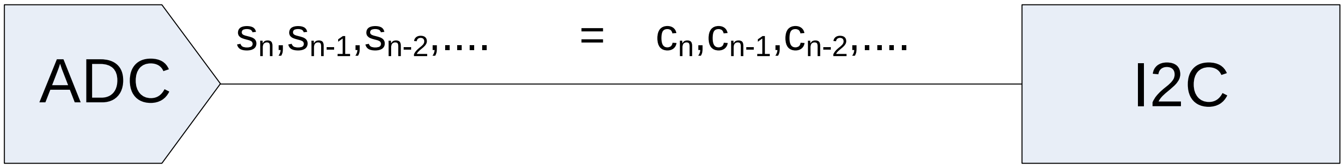

ADC
$s_n, s_{n-1}, s_{n-2}, \ldots = c_n, c_{n-1}, c_{n-2}, \ldots$
I2C

Figure 23. data processing, FILT = 0

In the case of FILT=1 three output samples of the ADC are averaged and the result is sent to the I2C.

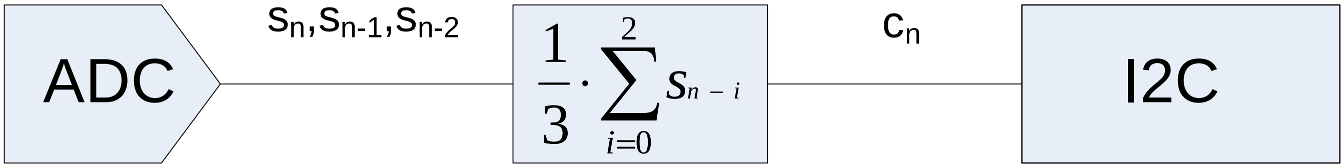


Figure 24. data processing, FILT = 1

For FILT=2 the averaging is done on five samples

.

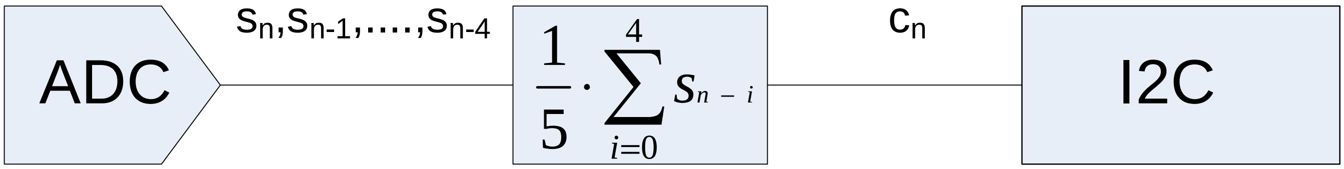

ADC
$s_n, s_{n-1}, \ldots, s_{n-4}$
$\frac{1}{5} \cdot \sum_{i=0}^{4} s_{n-i}$
c_n
I2C

Figure 25. data processing, FILT = 2

The FILT=3 will re-arrange seven samples out of the ADC in an ascending order and average the three center samples. Figure 26 shows an example of the ordering and averaging.

.

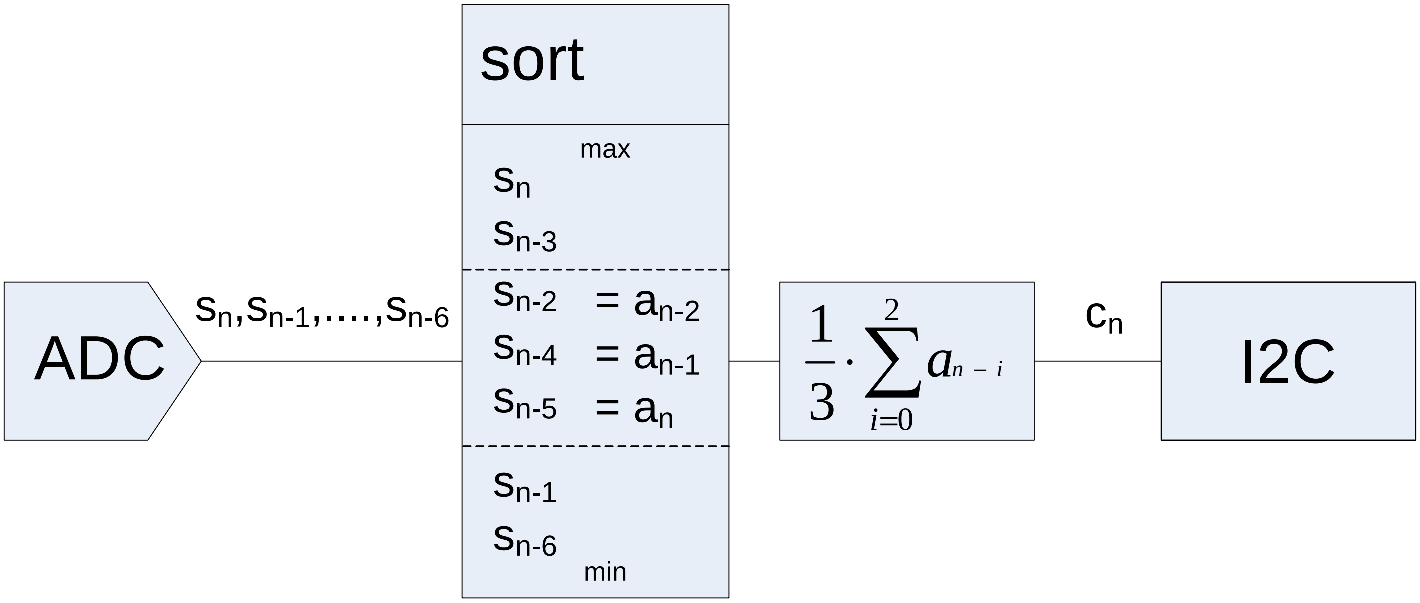


Figure 26. data processing, FILT = 3

4.6. Host Interface and Control

The host interface consists of I2C (SCL and SDA) and the NIRQ, A0, NRST signals.

The I2C implemented on the SX8650 is compliant with:
- Standard Mode (100 kbit/s) & Fast Mode (400 kbit/s)
- Slave mode
- 7 bit slave address

4.6.1. I2C Address

Pin A0 defines the LSB of the I2C address. It is shown on Figure 27.

.

SX8650 Slave Address(7:1) =

1	0	0	1	0	0	0	with pin A0 connected to ground
1	0	0	1	0	0	1	with pin A0 connected to VDD

Figure 27. I2C slave address

Upon request of the customer, a custom I2C address can be burned in the NVM.

The host uses the I2C to read and write data and commands to the configuration and status registers. During a conversion, the I2C clock can be stretched until the end of the processing.

Channel data read is done by I2C throughput optimized formats.

The supported I2C access formats are described in the next sections:
- I2C Write Registers
- I2C Read Registers
- I2C Host Commands
- I2C Read Channels

4.6.2. I2C Write Registers

The format for I2C write is given in Figure 28.

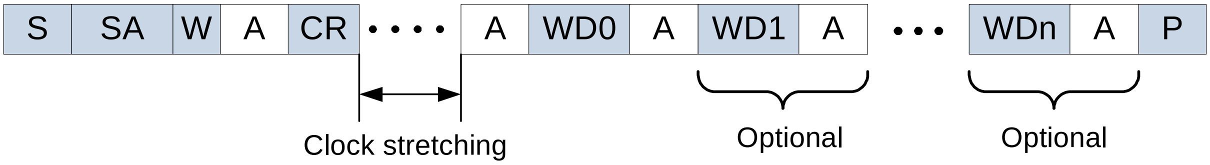
After the start condition [S], the SX8650 slave address (SA) is sent, followed by an eighth bit (W='0') indicating a Write.

The SX8650 then Acknowledges [A] that it is being addressed, and the host sends 8-bit Command and Register address consisting of the command bits '000' followed by the SX8650 Register Address (RA).

The SX8650 Acknowledges [A] and the host sends the appropriate 8-bit Data Byte (WD0) to be written.

Again the SX8650 Acknowledges [A].

In case the host needs to write more data, a succeeding 8-bit Data Byte will follow (WD1), acknowledged by the slave [A]. This sequence will be repeated until the host terminates the transfer with the Stop condition [P].



S:	Start condition
SA:	SX8650 Slave Address(7:1)
W:	'0'
A:	Acknowledge
CR:	'000' + Register Address(4:0)
WDn:	Write Data byte(7:0), 0...n
P:	Stop condition

▨	From host to SX8650
□	From SX8650 to host

Figure 28. I2C write register

The register address increments automatically when successive register data (WD1...WDn) is supplied by the host. This automatic increment can be used for the first 4 register addresses (see Table 8).

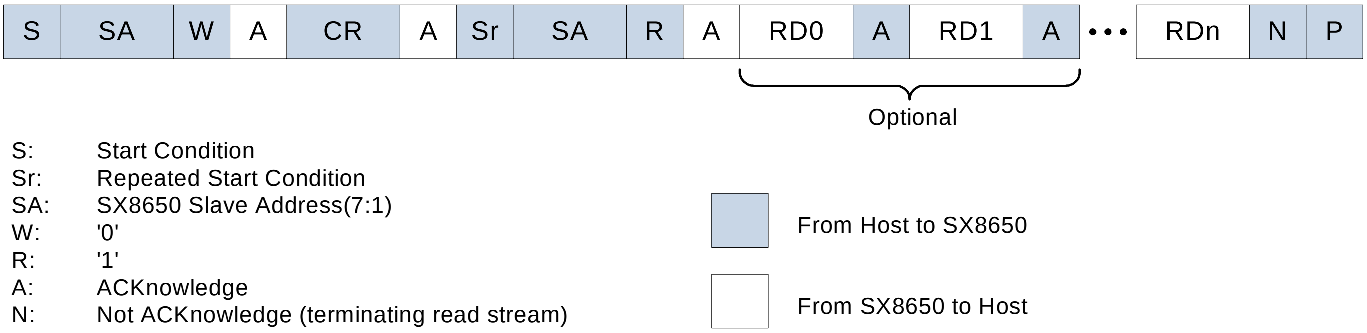
The correct sampling of the screen by the SX8650 and the host I2C bus traffic are events that might occur simultaneously. The SX8650 will synchronize these events by the use of clock stretching if that is required. The stretching occurs directly after the last received command bit (see Figure 28).

4.6.3. I2C Read Registers

The format for incremental I2C read for registers is given in Figure 29. The read has to start with a write of the read address.

After the start condition [S], the SX8650 Slave Address (SA) is sent, followed by an eighth bit (W='0') indicating a Write. The SX8650 then Acknowledges [A] that it is being addressed, and the host responds with a 8-bit CR Data consisting of '010' followed by the Register Address (RA). The SX8650 responds with an Acknowledge [A] and the host sends the Repeated Start Condition [Sr]. Once again, the SX8650 Slave Address (SA) is sent, followed by an eighth bit (R='1') indicating a Read.

The SX8650 responds with an Acknowledge [A] and the read Data byte (RD0). If the host needs to read more data it will acknowledge [A] and the SX8650 will send the next read byte (RD1). This sequence can be repeated until the host terminates with a NACK [N] followed by a stop [P].



S	SA	W	A	CR	A	Sr	SA	R	A	RD0	A	RD1	A	•••	RDn	N	P

S:	Start Condition
Sr:	Repeated Start Condition
SA:	SX8650 Slave Address(7:1)
W:	'0'
R:	'1'
A:	ACKnowledge
N:	Not ACKnowledge (terminating read stream)
CR:	'010' + Register Address(4:0)
RDn:	Read Data byte(7:0), 0...n
P:	Stop Condition

Figure 29. I2C read registers

The I2C read register format of Figure 29 is maintained until the Stop Condition. After the Stop Condition the SX8650 is performing succeeding reads by the compact read format of the I2C read channels described in the next section.

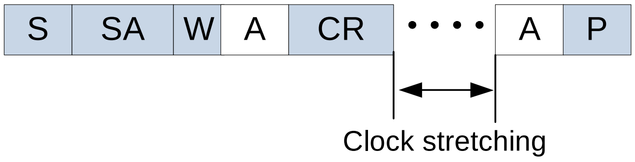
No clock stretching will occur for the I2C read registers.

4.6.4. I2C Host Commands

The format for I2C commands is given in Figure 30.

After the start condition [S], the SX8650 Slave Address (SA) is sent, followed by an eighth bit (W='0') indicating a Write. The SX8650 then Acknowledges [A] that it is being addressed, and the host responds with an 8-bit Data consisting of a '1' + command(6:0). The SX8650 Acknowledges [A] and the host sends a stop [P].

The exact definition of command(6:0) can be found in section [4.9]



S:	Start condition
SA:	SX8650 Slave Address(7:1)
W:	'0'
A:	Acknowledge
CR:	'1' + Command(6:0)
P:	Stop condition

▨	From host to SX8650
□	From SX8650 to host

Figure 30. I2C host command

The sampling of the screen by the SX8650 and the host I2C bus traffic are events that might occur simultaneously. The SX8650 will synchronize these events by the use of clock stretching if that is required. The stretching occurs directly after the last received command bit (see Figure 30).

4.6.5. I2C Read Channels

The host is able to read the channels with a high throughput, by the format shown in Figure 31.

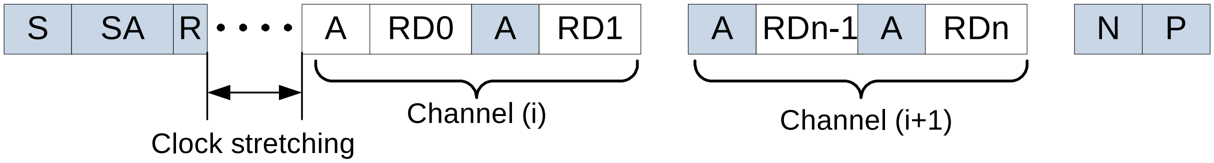
After the start condition [S], the SX8650 Slave Address (SA) is sent, followed by an eighth bit (R='1') indicating a read. The SX8650 responds with an Acknowledge [A] and the Read Data byte (RD0). The host sends an Acknowledge [A] and the SX8650 responds with the Read Data byte (RD1). If the host needs to read more data, it will acknowledge [A] and the SX8650 will send the next read bytes. This sequence can be repeated until the host terminates with a NACK [N] followed by a stop [P].

The channel data that can be read is defined by the last conversion sequence.

A maximum number of 10 data bytes is passed when all channels (X, Y, z1, z2 and AUX) are activated in the "I2CRegChanMsk".

The channel data is sent with the following order: X, Y, Z1, Z2, AUX. The first byte of the data contains the channel information as shown in Figure 32.

Typical applications require only X and Y coordinates, thus only 4 bytes of data will be read.



S:	Start condition
SA:	SX8650 Slave Address(7:1)
R:	'1'
A:	Acknowledge
N:	Not Acknowledge (terminating read stream)
RDn:	Read Data byte(7:0), 0...n
P:	Stop condition

▨	From host to SX8650
□	From SX8650 to host

Figure 31. I2C read channels

The sampling of the screen by the SX8650 and the host I2C bus traffic are events that might occur simultaneously. The SX8650 will synchronize these events by the use of clock stretching if that is required. The stretching occurs directly after the address and read bit have been sent for the I2C read channels command (see Figure 31).

4.6.6. Data Channel Format

Channel data is coded on 16 bits as shown in Figure 32

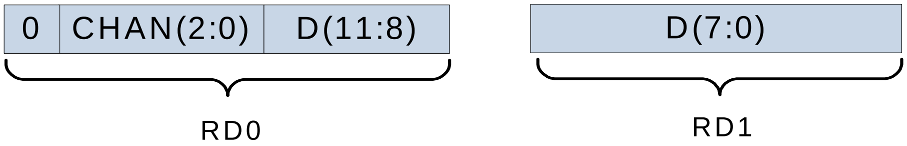


Figure 32. data channel format

The 3 bits CHAN(2:0) are defined in Table 12 and show which channel data is referenced. The channel data D(11:0) is of unsigned format and corresponds to a value between 0 and 4095.

4.6.7. Invalid Qualified Data

The SX8650 will return 0xFFFF data in case of invalid qualified data.

This occurs:

- when the SX8650 converted channels and the host channel readings do not correspond. E.g. the host converts X and Y and the host tries to read X, Y and z1 and z2.

- when a conversion is done without a pen being detected.

4.7. I2C Register Map

I2C register address RA(4:0)	Register	Description
0 0000	I2CRegCtrl0	Write, Read
0 0001	I2CRegCtrl1	Write, Read
0 0010	I2CRegCtrl2	Write, Read
0 0100	I2CRegChanMsk	Write, Read
0 0101	I2CRegStat	Read
1 1111	I2CRegSoftReset	Write

Table 8. I2C Register address

The details of the registers are described in the next sections.

4.8. Host Control Writing

The host control writing allows the host to change SX8650 settings. The control data goes from the host towards the SX8650 and may be read back for verification.

register	bits	default	description		
I2CRegCtrl0	7:4	0000	RATE	Set rate in coordinates per sec (cps) (± 20%) If RATE equals zero then Manual mode. if RATE is larger than zero then Automatic mode	
				0000: Timer disabled -Manual mode 0001: 10 cps 0010: 20 cps 0011: 40 cps 0100: 60 cps 0101: 80 cps 0110: 100 cps 0111: 200 cps	1000: 300 cps 1001: 400 cps 1010: 500 cps 1011: 1k cps 1100: 2k cps 1101: 3k cps 1110: 4k cps 1111: 5k cps
	3:0	0000	POWDLY	Settling time (± 10%): The channel will be biased for a time of POWDLY before each channel conversion	
				0000: Immediate (0.5 us) 0001: 1.1 us 0010: 2.2 us 0011: 4.4 us 0100: 8.9 us 0101: 17.8 us 0110: 35.5 us 0111: 71.0 us	1000: 0.14 ms 1001: 0.28 ms 1010: 0.57 ms 1011: 1.14 ms 1100: 2.27 ms 1101: 4.55 ms 1110: 9.09 ms 1111: 18.19 ms
I2CRegCtrl1	7:6	00	AUXAQC	00: AUX is used as an analog input 01: On rising AUX edge, wait POWDLY and start acquisition	10: On falling AUX edge, wait POWDLY and start acquisition 11: On rising and falling AUX edges, wait POWDLY and start acquisition
				The AUX trigger requires the manual mode.	
	5	1	CONDIRQ	Enable conditional interrupts 0: interrupt always generated at end of conversion cycle. If no pen is detected the data is set to 'invalid qualified'. 1: interrupt generated when pen detect is successful	
	4	0	reserved		
	3:2	00	RPDNT	Select the Pen Detect Resistor 00: 100 KOhm 01: 200 KOhm 10: 50 KOhm 11: 25 KOhm	
	1:0	00	FILT	Digital filter control 00: Disable 01: 3 sample averaging 10: 5 sample averaging 11: 7 sample acquisition, sort, average 3 middle samples	

Table 9. I2C registers

register	bits	default	description		
I2CRegCtrl2	7:4	0	reserved		
	3:0	0000	SETDLY	Settling time while filtering (± 10%) When filtering is enabled, the channel will initially bias for a time of POWDLY for the first conversion, and for a time of SETDLY for each subsequent conversion in a filter set.	
				0000: Immediate (0.5 us) 0001: 1.1 us 0010: 2.2 us 0011: 4.4 us 0100: 8.9 us 0101: 17.8 us 0110: 35.5 us 0111: 71.0 us	1000: 0.14 ms 1001: 0.28 ms 1010: 0.57 ms 1011: 1.14 ms 1100: 2.27 ms 1101: 4.55 ms 1110: 9.09 ms 1111: 18.19 ms
I2CRegChanMsk	7	1	XCONV	0: no sample 1: sample, report X channel	
	6	1	YCONV	0: no sample 1: sample, report Y channel	
	5	0	Z1CONV	0: no sample 1: sample, report Z1 channel	
	4	0	Z2CONV	0: no sample 1:sample, report Z2 channel	
	3	0	AUXCONV	0: no sample 1: sample, report AUX channel	
	0	0	reserved		
	0	0	reserved		
	0	0	reserved		
I2CRegStat	The host status reading allows the host to read the status of the SX8650. The data goes from the SX8650 towards the host. Host writing to this register is ignored.				
	7	0	CONVIRQ	0: no IRQ pending 1: End of conversion sequence IRQ pending IRQ is cleared by the I2C channel reading	
	6	0	PENIRQ	operational in pen detect mode 0: no IRQ pending 1: Pen detected IRQ pending IRQ is cleared by the I2C status reading	
	5:0	000000	reserved		
I2CRegSoftReset	7:0	0x00	If the host writes the value 0xDE to this register, then the SX8650 will be reset. Any other data will not affect the SX8650		

Table 9. I2C registers

4.9. Host Commands

The host can write to and read from registers of the SX8650 by the write and read commands as defined in Table 10.

W/R command name	CR(7:0)								Function
	7	6	5	4	3	2	1	0	
WRITE(RA)	0	0	0	RA(4:0)					Write register (see Table 8 for RA)
READ(RA)	0	1	0	RA(4:0)					Read register (see Table 8 for RA)

Table 10. I2C W/R commands

.The host can issue commands to change the operation mode or perform manual actions as defined in Table 11.

command name	CR(7:0)								Function
	7	6	5	4	3	2	1	0	
SELECT(CHAN)	1	0	0	0	x	CHAN(2:0)			Bias channel (see Table 12 for CHAN)
CONVERT(CHAN)	1	0	0	1	x	CHAN(2:0)			Bias channel (see Table 12 for CHAN) Wait POWDLY settling time Run conversion
MANAUTO	1	0	1	1	x	x	x	x	Enter manual or automatic mode.
PENDET	1	1	0	0	x	x	x	x	Enter pen detect mode.
PENTRG	1	1	1	0	x	x	x	x	Enter pen trigger mode.

Table 11. I2C commands

The channels are defined as in Table 12.

Channel	CHAN(2:0)			Function
	2	1	0	
X	0	0	0	X channel
Y	0	0	1	Y channel
Z1	0	1	0	First channel for pressure measurement
Z2	0	1	1	Second channel for pressure measurement
AUX	1	0	0	Auxiliary channel
reserved	1	0	1	
reserved	1	1	0	
SEQ	1	1	1	Channel sequentially selected from I2CRegChanMsk register, (see Table 8)

Table 12. channel definition

4.10. Power-Up

The NIRQ pin is kept low during SX8650 power-up.

During power-up, the SX8650 is not accessible and I2C communications are ignored.

As soon as NIRQ rises, the SX8650 is ready for I2C communication.

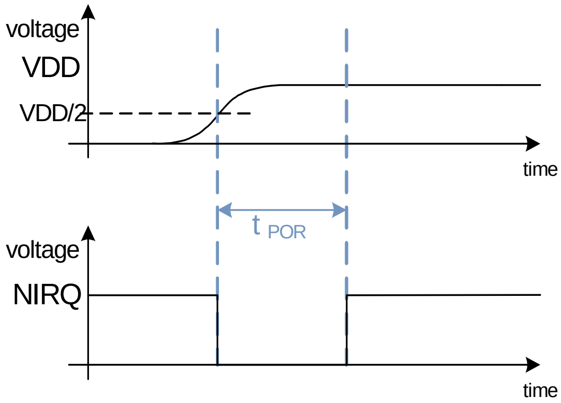


Figure 33. Power-up, NIRQ

4.11. Reset

The POR of the SX8650 will reset all registers and states of the SX8650 at power-up.

Additionally the host can reset the SX8650 by asserting the NRST pin (active low) and via the I2C bus.

If NRST is driven LOW, then NIRQ will be driven low by the SX8650. When NRST is released (or set to high) then NIRQ will be released by the SX8650.

The circuit has also a soft reset capability. When writing the code 0xDE to the register I2CRegSoftReset, the circuit will be reset.

5. Modes of Operation

The SX8650 has four operation modes that are configured using the I2C commands as defined in Table 11 and Table 9.

These 4 modes are:

- manual (command 'MANAUTO' and RATE=0),
- automatic (command 'MANAUTO' and RATE>0),
- pen detect (command 'PENDET'),
- pen trigger mode (command 'PENTRG').

At startup the SX8650 is set in manual mode.

In the manual mode the SX8650 is entirely stopped except for the I2C peripheral which accepts host commands. This mode requires RATE equal to be zero (RATE = 0, see Table 9).

In the automatic mode the SX8650 will sequence automatic channel conversions. This mode requires RATE to be larger than zero (RATE > 0, see Table 9).

In the PENDET mode the pen detection is activated. The SX8650 will generate an interrupt (NIRQ) upon pen detection and set the PENIRQ bit in the I2C status register. To quit the PENDET mode the host needs to configure the manual mode.

In the PENTRG mode the pen detection is activated and a channel conversion will start after the detection of a pen. The SX8650 will generate an interrupt (NIRQ) upon pen detection and set the CONVIRQ bit in the I2C status register. To quit the PENTRIG mode the host needs to configure the manual mode. The PENTRG mode offers the best compromise between power consumption and coordinate throughput.

5.1. Manual Mode

In manual mode (RATE=0) single actions are triggered by I2C commands. When a command is received, the SX8650 executes the associated task and waits for the next command. It is up to the host to sequence all actions such as: select an input channel, wait for a settling time, start conversion and read the result. The commands used in manual mode are typically SELECT and/or CONVERT as defined in Table 10. The CONVERT command should only be used with CONDIRQ=0.

If the SX8650 is not ready to execute the next command, clock starching occurs. Various timing diagrams show the operating sequence for examples of the manual mode.

The I2C and the NIRQ are describing the host interface signals. The 'bias', 'sample' and 'convert channel(s)' used on the following drawings are internal SX8650 signals and shown for illustration only.

5.1.1. CONVERT Command

The CONVERT command will bias the selected channel, wait the time specified by POWDLY and then convert the selected channel. The converted channel can be one single channel or channels in sequence depending on the CHAN(2:0) parameter. The reading of the channel(s) can be done over the I2C as described in Figure 31.

An example host I2C sequence for acquisition of the x channel using the CONVERT command is shown in Figure 34 and Figure 35. The settling time is determined by POWDLY

The init setup could be a I2C write sequence of:

I2CregCtrl1=0x00 // No filter, CONDIRQ = 0

I2CRegChanMsk = 0x80 // Acquisition of the X channel

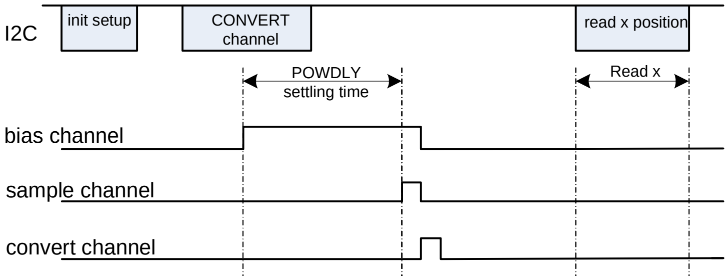


Figure 34. Conversion of a channel, no filter

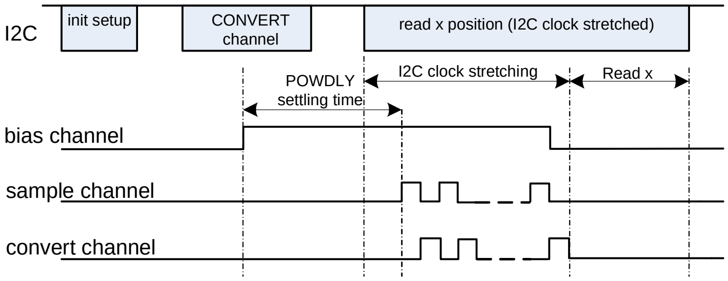


Figure 35. Conversion of a channel, digital filter enabled, clock starching required

5.1.2. SELECT Command

The host can define very long settling times by using the SELECT, CONVERT sequence. The host determines the settling time for each separate channel by the time interval between issuing the SELECT and CONVERT command. Therefore the POWDLY timing is not applicable and is ignored.

As soon as the channel is selected the corresponding channel will be biased. The settling time is determined by the interval between the host issuing the SELECT and the CONVERT commands. The host can proceed with a read channel command after the CONVERT command. In case the SX8650 is not ready to convert and filter, the clock of the I2C will be stretched by the SX8650 until data is available and can be read.

Figure 36 shows an example of I2C sequence using the SELECT, CONVERT sequence command. For an X-channel SELECT, issue the command: 0x80, followed with the corresponding CONVERT command: 0x90. The SX8650 will make the X-channel data available over the I2C.

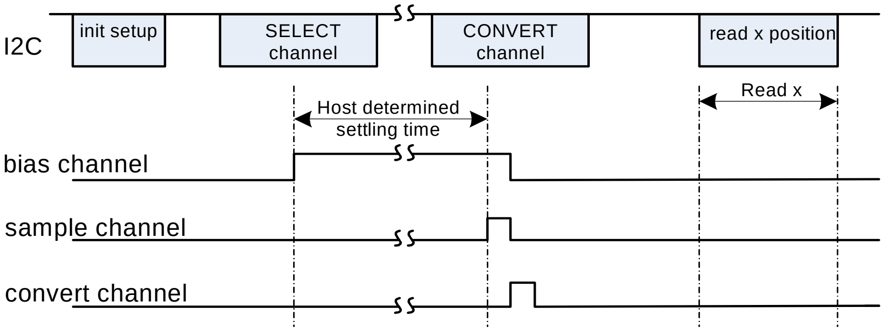


Figure 36. Conversion using the SELECT and CONVERT command

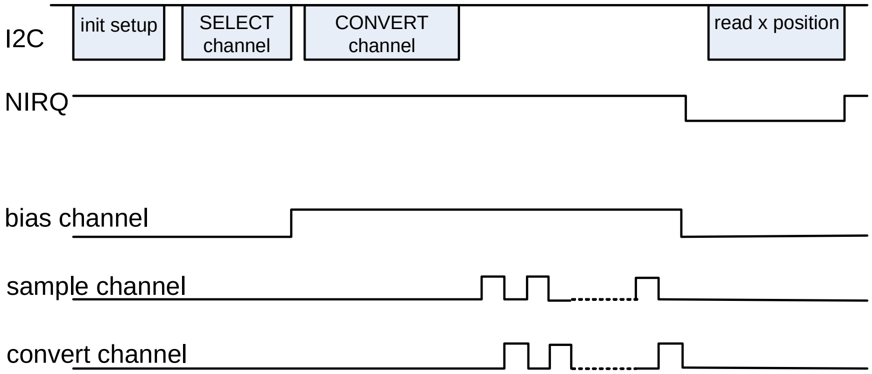


Figure 37. single conversion, filtering and interrupt signaling

In Figure 37 the host performs a single conversion and uses the interrupt (NIRQ) signal to read the available data. The clock stretching is not required and the I2C bus is free for other system traffic. Successive reads require the same diagram The init setup could be a I2C write sequence of:

I2CRegCtrl1 = 0x23 // Interrupt enable, seven samples filtering

I2CRegChanMsk = XCONV // Acquisition of X

5.2. Automatic mode

In automatic mode (RATE > 0) the SX8650 will automatically decide when to start acquisition, sequence all the acquisitions and alerts the host if data is available for download with a NIRQ. The host will read the channels and the SX8650 will start again with the next conversion cycle.

The fastest coordinate rate is obtained if the host reads the channels immediately after the NIRQ.

If the host reads faster than the NIRQ rate, I2C clock stretching occurs or invalid qualified data will be returned, see section [4.6.7]

To not loose data, the SX8650 will not begin conversion before the host read the channels. If after the NIRQ a delay superior to the sampling period is made by the host to read the channels a slower coordinate rate is obtained.

The interrupts will be always generated if the control CONDIRQ bit (see Table 9) is cleared to '0'. In case there is no pen detected on the screen then the coordinate data will be qualified as invalid, see section [4.6.7]. This result in a regular interrupt stream, as long as the host performs the read channel commands, independent of the screen being touched or not.

If the control CONVIRQ bit (see register I2CregStat Table 9) is set to '1' then the interrupts will only be generated if the pen detect occurred. This result in a regular interrupt stream, as long as the host performs the read channel commands, only when the screen is touched. When the screen is not touched, interrupts does not occur.

Figure 38 and Figure 39 show the automatic-sequential mode. After the first sample I2C to make the initialization, traffic is reduced as only I2C reads are required.

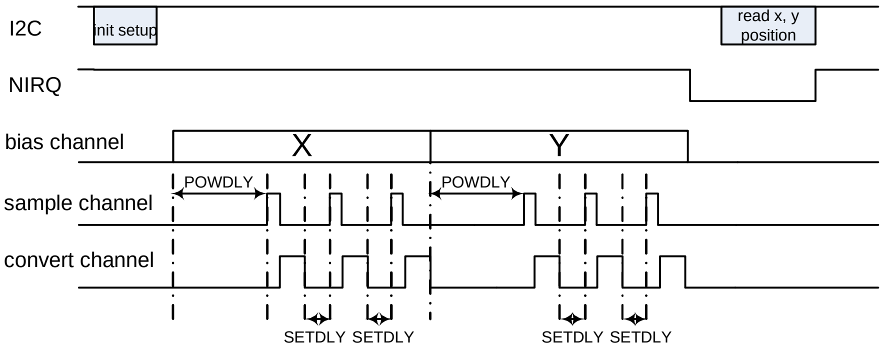


Figure 38. auto mode, sequential 2-channel conversion, 3 sample filtering and interrupt signaling, first conversion

Figure 38 shows the very first conversion of 2 channels. Figure 39 shows the subsequent conversions.

I2CRegCtrl0=0xB8 //1 kCPS RATE, 140us POWDLY

I2CRegCtrl1=0x21 // Interrupt enable, three samples filtering

I2CRegChanMsk=0xC0

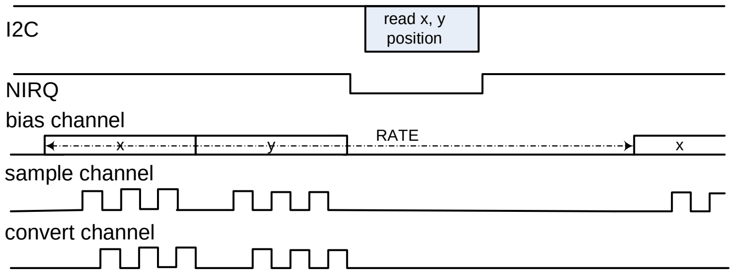


Figure 39. auto mode, sequential 2-channel conversion, 3 sample filtering and interrupt signaling, subsequent conversions

All succeeding conversions notifies the host by an interrupt signal and the host only needs to issue the I2C read command. The reads occur at the RATE interval.

5.3. PENDET Mode

The PENDET mode can be used if the host only needs to know if the screen has been touched or not and take from that information further actions. When pen detect circuitry is triggered the interrupt signal NIRQ will be generated and the status register bit 'PENIRQ' will be set. The bit is cleared by reading the status register I2CRegStat.

5.4. PENTRIG Mode

The PENTRIG mode offers the best compromise between power consumption and coordinate throughput.

In this mode the SX8650 will wait until a pen is detected on the screen and then starts the coordinate conversions. The host will be signalled only when the screen is touched and coordinates are available.

The coordinate rate in pen trigger mode is determined by the speed of the host reading the channels and the conversion times of the channels. The host performs the minimum number of I2C commands in this mode.

Figure 40 shows the PENTRIG mode. In this example, the host waits for the NIRQ interrupt to make the acquisition of the x,y data. After the first sample, I2C control traffic is reduced as only I2C reads are required.

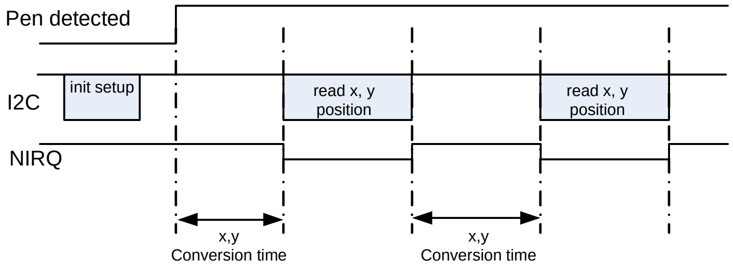


Figure 40. Pen trigger mode

6. Application Information

This section describes in more detail application oriented data.

6.1. Acquisition Setup

Prior to an acquisition, the SX8650 can be setup by writing the control registers. Registers are written by issuing the register write command. They can be read by issuing the read command. Please refer to the section [4.8].

If no registers are written, the circuit will start in manual mode.

6.2. Channel Selection

The SX8650 can be setup to start a single channel conversion or to convert several channels in sequence. For a single conversion, the channel to be converted is determined from the CHAN(2:0) field in the command word (defined in Table 12).

Several channels can be acquired sequentially by setting the CHAN(2:0) field to SEQ. The channels will be sampled in the order defined by register I2CRegChanMsk from MSB to LSB.

If a “one” is written in a channel mask, the corresponding channel will be sampled, in the opposite case, it is ignored and the next selected channel is chosen.

6.3. Noise Reduction

A noisy environment can decrease the performance of the controller. For example, an LCD display located just under the touch screen can adds a lot of noise on the high impedance A/D converter inputs.

6.3.1. POWDLY

Adding a capacitor from the touch screen drivers to ground is a solution to minimize external noise. A low-pass filter created by the capacitor may increase settling time. Therefore, use POWDLY to stretch the acquisition period. POWDLY can be estimated by the following formula.

$$PowDly = 10 \times Rtouch \times Ctouch$$

Rtouch is the sum of the panel resistances plus any significant series input resistance, Rxtot + Rytot + Ri.

Ctouch is the sum of the touch panel capacitance plus any noise filtering and routing capacitances.

6.3.2. SETDLY

A second method of noise filtering uses an averaging filter as described in section [4.5] (Data processing). In this case, the chip will sequence up to 7 conversions on each channel. The parameter SETDLY sets the settling time between the consecutive conversions (shown in Figure 41).

In most applications, SETDLY can be set to 0. In some particular applications, where accuracy of 1LSB is required and Ctouch is less than 100nF a specific value should be determined.

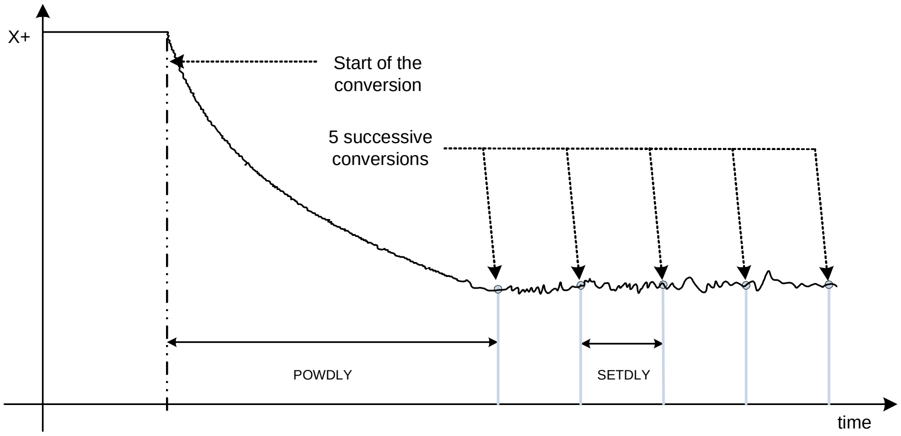


Figure 41. POWDLY and SETDLY timing with FILT=2

6.3.3. AUX Input

An alternate conversion trigger method can be used if the host system provides additional digital signals that indicate noisy or noise-free periods. The SX8650 can be set up to start conversions triggered by the AUX pin. A rising edge, a falling edge or both can trigger the conversion. To enter this mode, AUXACQ must be set to a different value than '00' as defined in Table 9. The AUX edge will first trigger the bias delay (POWDLY). Following the programmed delay, the channel acquisition takes place.

6.4. Channel Biasing

The touch screen surface presents a resistive and capacitive load, and therefore the screen bias needs to settle before an acquisition takes place. In the manual mode, the channels selected are biased when either a SELECT or CONVERT command is received.

The channel can be biased for an arbitrary amount of time by first sending a SELECT command and then a CONVERT command once the settling time requirement is met.

The SELECT command can be omitted if the large range of POWDLY settings cover the requirements. In the latter case, the CONVERT command alone is enough to perform an acquisition.

In the sequential mode, multiple channels are sampled. This requires programming the POWDLY field in register I2CRegCTRL0. The selected channel will be powered during POWDLY before a conversion is started. The channel bias is automatically removed after the conversion has completed.

6.5. Interrupt Generation

An interrupt (NIRQ) will be generated:

- during the power-up phase

- after completion of a conversion. CONVIRQ (bit [7] of I2CRegStat) will be set at the same time.

- when a pen detect is triggered, the SX8650 being in pen detect mode. PENIRQ (bit [6] of I2CRegStat) will be set at the same time.

The NIRQ will be released and then pulled high by the external pull-up resistor:

- when the power-up phase is finished

- the host reading all channels that were previously converted by the SX8650. CONVIRQ, will be cleared at the same time.

- the host reading the I2C status register, the SX8650 being in pen detect mode. PENIRQ, will be cleared at the same time.

An active NIRQ (low) needs to be cleared before any new conversions will occur.

6.6. Coordinate Throughput Rate

When the chip is not set to Automatic mode, the coordinate throughput rate depends on the following factors:

- the I2C communication time

- the conversion time

If the SX8650 is set to Automatic mode then the RATE settling must not be faster than the Raw Conversion Rate (RCR).

$$RCR(kCPS) = 1000/Tconv(us)$$

6.6.1. I2C Communication Time

The time to read the channel data by I2C depends of the mode set and if the clock is stretched or not.

Mode	Clock Stretching	T_{comm}(us)
MANUAL	No	$T_{SU;STA}$ -T_{LOW} + (29+18*Nchan)*T_{SCL}
MANUAL	Yes	-T_{LOW} + (21+18*Nchan)*T_{SCL}
PENTRIG[1]	No	$T_{SU;STA}$ -T_{LOW} + (9+18*Nchan)*T_{SCL}
PENTRIG[1]	Yes	-T_{LOW} + (1+18*Nchan)*T_{SCL}

Table 13.

[1] With the pen always down

The highest throughput will be obtained with a I2C frequency of 400kHz and clock stretching when all channels are sampled in PENTRIG mode.

The host should react to the NIRQ interrupt signal as quickly as possible by reading the channel data.

6.6.2. Conversion Time

The maximum possible throughput can be estimated with the following equation

$$Tconv(us) = 47 \cdot Tosc + N_{chan} \cdot (POWDLY + (N_{filt} - 1) \cdot SETDLY + (21N_{filt} + 1) \cdot Tosc)$$

with:

- N_{filt} = {1,3,5,7} based on the order defined for the filter FILT (see Figure 7).

- N_{chan} = {1,2,3,4,5} based on the number of channels defined in I2CRegChanMsk
- POWDLY = 0.5us to 18.19ms, settling time as defined in I2CRegCtrl0
- SETDLY = 0.5us to 18.19ms, settling time when filtering as defined in I2CRegCtrl2
- Tosc is the oscillator period (555ns +/- 15%)

The Coordinate Rate (CR) and Equivalent Coordinate Rate (ECR) which give the number of coordinates (X, Y, Z1, Z2) is given below

:

$$CR(kCPS) = 1000/T(us)$$

$$ECR(kCPS) = N_{chan} \cdot CR$$

The Sample Rate (SR) and Equivalent Sample Rate (ESR) which give the number of sample per second (X, Y, Z1, Z2) is given below

$$SR(kSPS) = N_{filt} \cdot CR$$

$$ESR(kSPS) = N_{chan} \cdot N_{filt} \cdot CR$$

Table 14 gives some examples of Coordinate Rate and Sample Rate for various setting in PENTRIG mode.

Nch [1..5]	Nfilt [1 3 5 7]	PowDly [uS]	SetDly [uS]	Tconv [uS]	Tcomm [uS]	Total [uS]	CR [kCPS]	ECR [kCPS]	SR [kSPS]	ESR [kSPS]
2.0	1.0	0.5	0.5	51.7	91.2	142.9	7.0	14.0	7.0	14.0
2.0	1.0	2.2	0.5	55.0	91.2	146.2	6.8	13.7	6.8	13.7
2.0	1.0	8.9	0.5	68.3	91.2	159.5	6.3	12.5	6.3	12.5
2.0	1.0	35.5	0.5	121.7	91.2	212.9	4.7	9.4	4.7	9.4
2.0	1.0	280.0	0.5	619.4	91.2	710.6	1.4	2.8	1.4	2.8
2.0	3.0	2.2	0.5	103.9	91.2	195.1	5.1	10.3	15.4	30.8
2.0	3.0	35.5	0.5	170.6	91.2	261.8	3.8	7.6	11.5	22.9
2.0	5.0	2.2	0.5	152.8	91.2	244.0	4.1	8.2	20.5	41.0
2.0	5.0	35.5	0.5	219.4	91.2	310.6	3.2	6.4	16.1	32.2
4.0	7.0	2.2	0.5	377.2	181.2	558.4	1.8	7.2	12.5	50.1
4.0	7.0	35.5	0.5	510.6	181.2	691.8	1.4	5.8	10.1	40.5
4.0	1.0	0.5	0.5	77.2	181.2	258.4	3.9	15.5	3.9	15.5
4.0	1.0	2.2	0.5	83.9	181.2	265.1	3.8	15.1	3.8	15.1
4.0	1.0	35.5	0.5	217.2	181.2	398.4	2.5	10.0	2.5	10.0
4.0	3.0	2.2	0.5	181.7	181.2	362.9	2.8	11.0	8.3	33.1
4.0	3.0	35.5	0.5	315.0	181.2	496.2	2.0	8.1	6.0	24.2
4.0	5.0	2.2	0.5	279.4	181.2	460.6	2.2	8.7	10.9	43.4
4.0	5.0	35.5	0.5	412.8	181.2	594.0	1.7	6.7	8.4	33.7
4.0	7.0	2.2	0.5	377.2	181.2	558.4	1.8	7.2	12.5	50.1
4.0	7.0	35.5	0.5	510.6	181.2	691.8	1.4	5.8	10.1	40.5

Table 14. Coordinate throughput examples

6.7. Application Schematic

A typical application schematic is shown in Figure 42

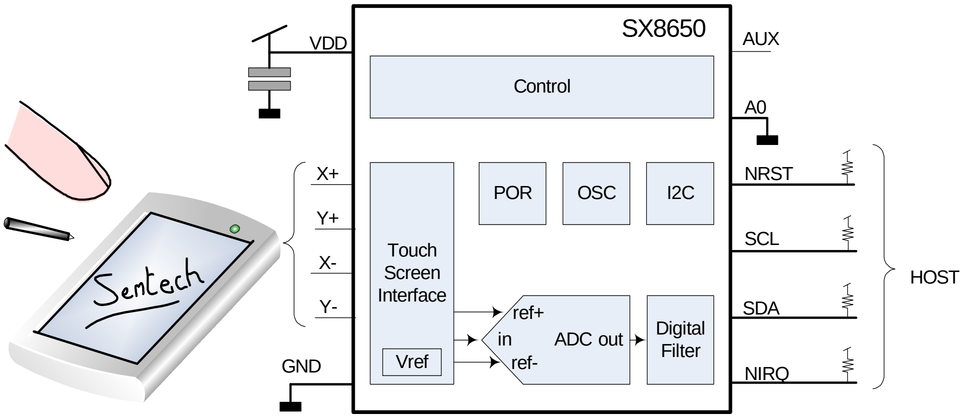


Figure 42. typical application

6.8. Application Examples

6.8.1. Soft Keyboard

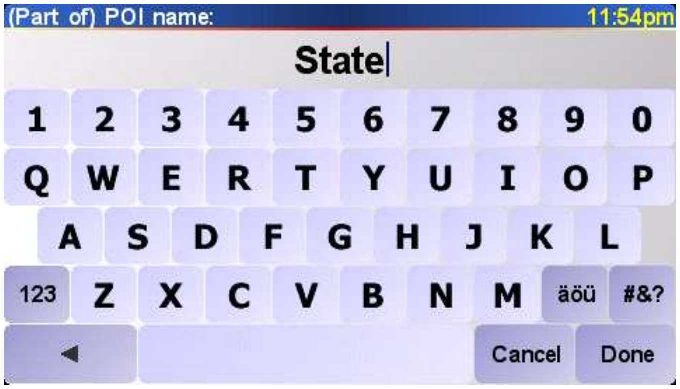


Figure 43. Keyboard

A keyboard application can be designed with the help of the SX8650. The data are entered by tapping keys on the keyboard with a stylus. The SX8650 send the key coordinates to the microcontroller which interpret them as a symbol.

When the keyboard is not activated, the chip stays in low power mode to save power.

6.8.2. Game

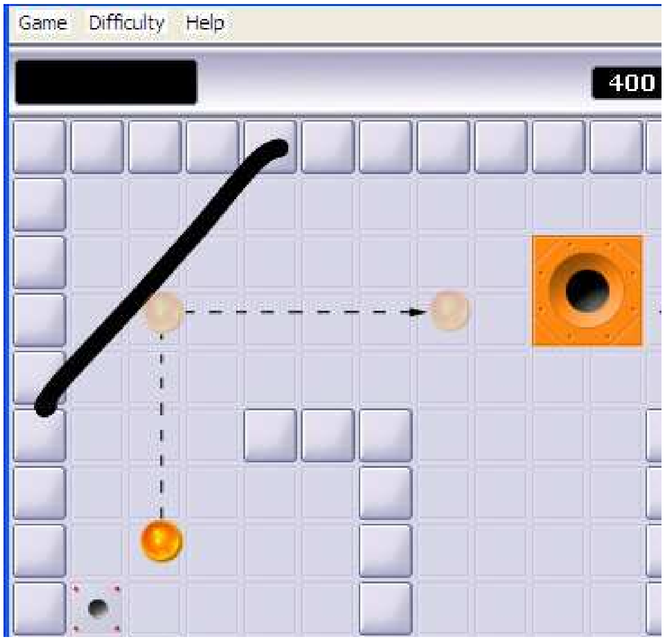


Figure 44. Game

Many kinds of game can be designed with touchscreen. With its high data throughput and its ability to sense pressure, SX8650 is the perfect controller for this kind of application.

6.8.3. Handwriting Application

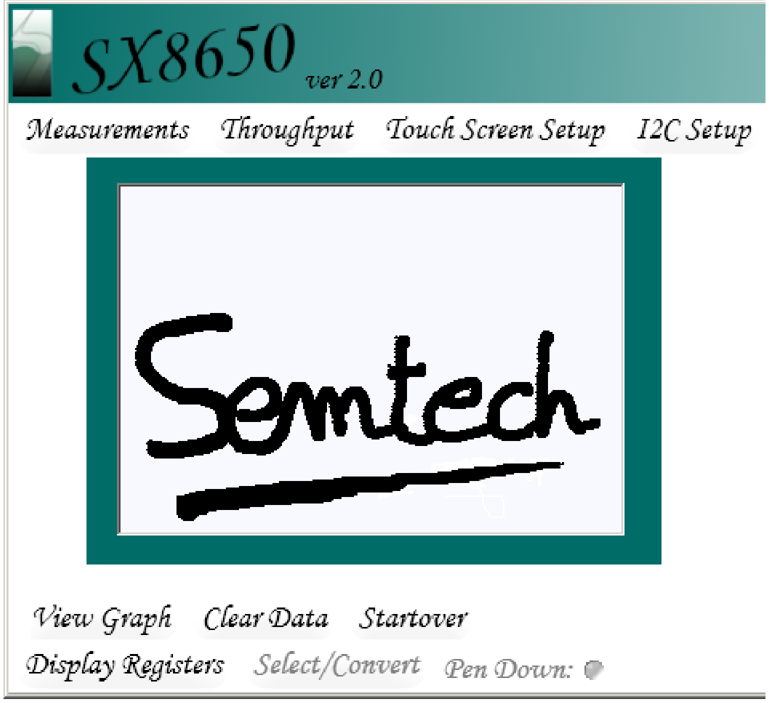


Figure 45. Handwriting application

An handwriting application needs a powerful microcontroller to run recognition algorithms. The SX8650 includes a preprocessing block to reduce host activity.

6.8.4. Slider Controls

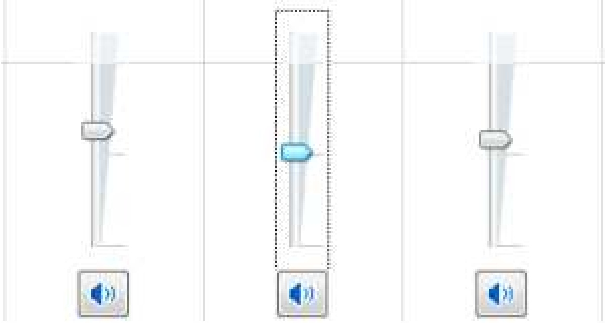


Figure 46. Slider controls

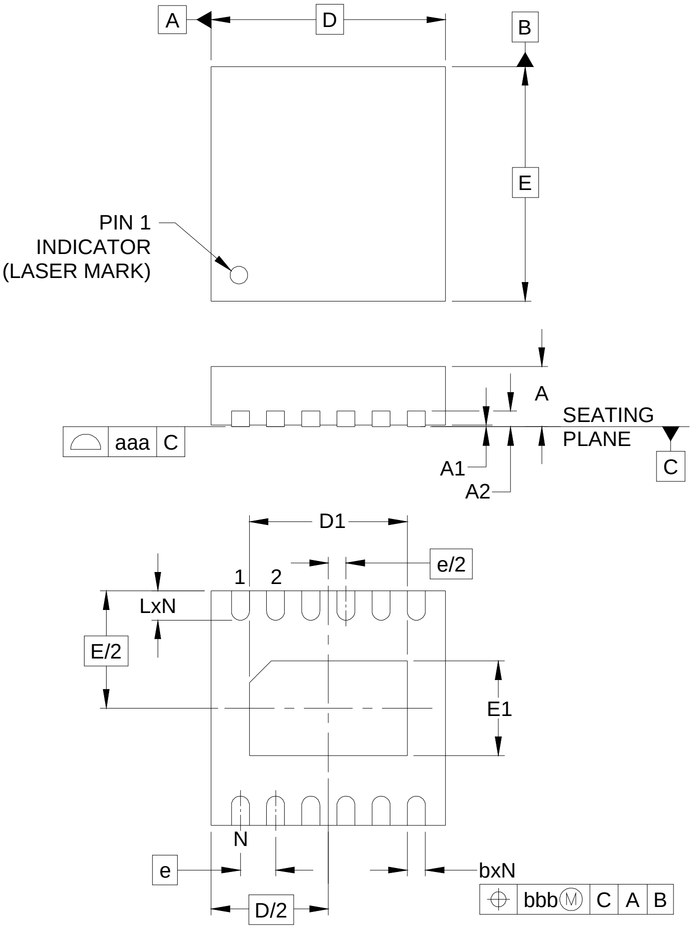
Every kind of controls such as rotative knob, slider, button could be emulated with a SX8650 associated to a touchscreen.

7. Packaging Information

7.1. Package Outline Drawing

7.1.1. DFN Package

The 12-Lead DFN (3mm x 3mm) package is shown in Figure 47



DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.028	.030	.031	0.70	0.75	0.80
A1	.000	.001	.002	0.00	0.02	0.05
A2		(.008)			(0.20)	
b	.006	.008	.010	0.15	0.20	0.25
D	.114	.118	.122	2.90	3.00	3.10
D1	.074	.079	.083	1.87	2.02	2.12
E	.114	.118	.122	2.90	3.00	3.10
E1	.042	.048	.052	1.06	1.21	1.31
e		.018 BSC			0.45 BSC	
L	.012	.016	.020	0.30	0.40	0.50
N		12			12	
aaa		.003			0.08	
bbb		.004			0.10	

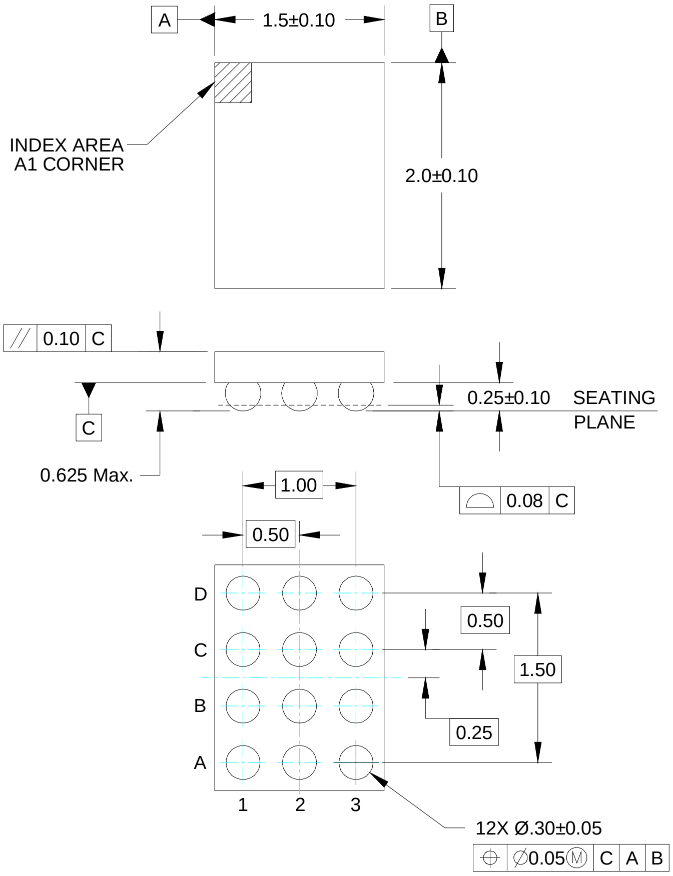
NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS TERMINALS.

Figure 47. DFN Package outline drawing

7.1.2. WLCSP Package

The WLCSP-W12 package as shown in Figure 48



NOTES:

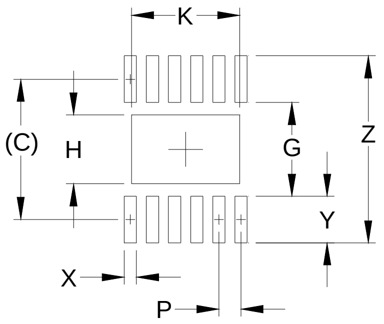
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS

Figure 48. WLCSP Package outline drawing

7.2. Land Pattern Drawing

7.2.1. DFN Land Pattern

The land pattern of 12-Lead DFN (3mm x 3mm) is shown in Figure 49.



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.112)	(2.85)
G	.075	1.90
H	.055	1.40
K	.087	2.20
P	.018	0.45
X	.010	0.25
Y	.037	0.95
Z	.150	3.80

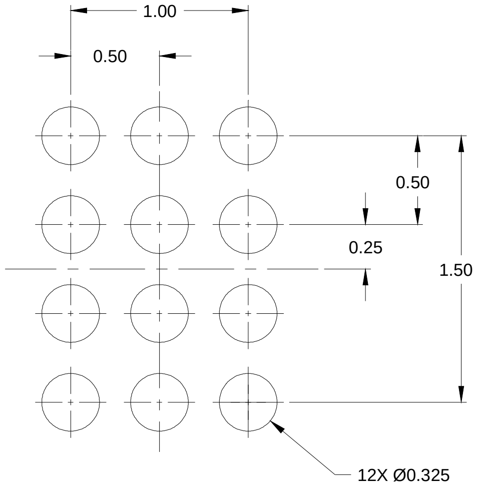
NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

Figure 49. DFN Land Pattern

7.2.2. WLCSP Land Pattern

The land pattern of WLCSP is shown on Figure 50



NOTES:

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Figure 50. WLCSP Land Pattern

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