National Semiconductor

December 2001

CLC532
High Speed 2:1 Analog Multiplexer

General Description

The CLC532 is a high speed 2:1 multiplexer with active input and output stages. The CLC532 innovative design employs a closed loop design which dramatically improves accuracy. This monolithic device is constructed using an advanced high performance bipolar process.

The CLC532 has been specifically designed to provide settling times of 17ns to 0.01%. Fast settling time, coupled with the adjustable bandwidth, and channel-to-channel isolation is better than 80dB @10MHz. Low distortion (−80dBc) makes the CLC532 an ideal choice for infrared and CCD imaging systems and spurious signal levels make the CLC532 a very suitable choice for both I/Q processors and receivers.

The CLC532 is offered in two industrial versions, CLC532AJP\AJE, specified from −40˚C to +85˚C and packaged in 14-pin plastic DIP14-pin and SOIC packages.

Enhanced Solutions (Military/Aerospace)

SMD Number: 5962-92035

*Space level versions also available.

*For more information, visit http://www.national.com/mil

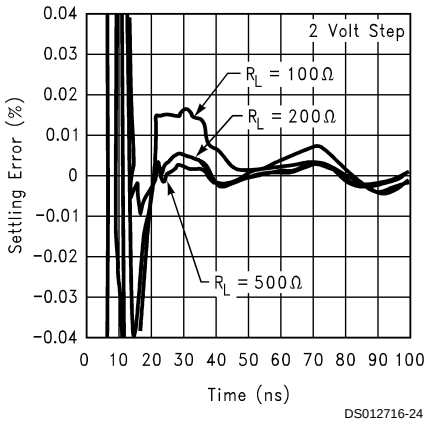
Features

- 17ns 12-bit settling time to .01%
- Low noise – 32µVrms
- High isolation – 80dB @ 10MHz
- Low distortion – 80dBc @ 5MHz
- Adjustable bandwidth–190MHz(max)

Applications

- Infrared system multiplexing
- CCD sensor signals
- Radar I/Q switching
- High definition video HDTV
- Test and calibration

Settling Time vs. R_L



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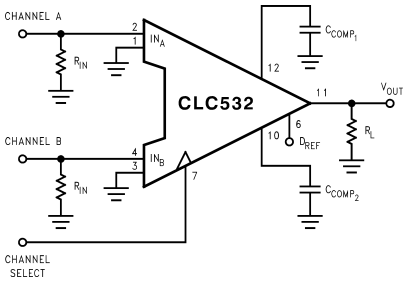
Typical Application



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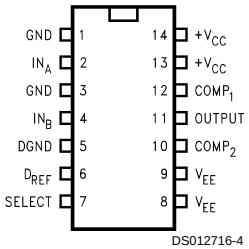
Connection Diagram



DS012716-4

Pinout
DIP & SOIC

Ordering Information

Package	Temperature Range Industrial	Part Number	Package Marking	NSC Drawing
14-Pin Plastic DIP	−40˚C to +85˚C	CLC532AJP	CLC532AJP	N14E
14-Pin Plastic SOIC	−40˚C to +85˚C	CLC532AJE	CLC532AJE	M14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Positive Supply Voltage ($+V_{CC}$)	−0.5V to +7.0V
Negative Supply Voltage ($-V_{EE}$)	+0.5V to −7.0V
Differential Voltage between any two GND's	200mV
Analog Input Voltage Range	$-V_{EE}$ to $+V_{CC}$
Digital Input Voltage Range	$-V_{EE}$ to $+V_{CC}$
Output Short Circuit Duration (Output Shorted to GND)	Infinite
Operating Temperature Range	−40˚C to +85˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Solder Duration (+300˚C)	10 sec
ESD Rating	<500V

Operating Ratings

Positive Supply Voltage ($+V_{CC}$)	+5v
Negative Supply Voltage ($-V_{EE}$)	−5.2V or −5.0V
Differential Voltage between any two GDN's	10mV
Analog Input Voltage Range	±2V
SELECT Input Voltage Range (TTL Mode)	0.0V to +3.0V
SELECT Input Voltage Range (ECL Mode)	−2.0V to 0.0V
C_{COMP}Range (Note 3)	5pF to 100pF
Thermal Resistance (θ_{JC})	
MDIP	55˚C/W
SOIC	35˚C/W
Thermal Resistance (θ_{JA})	
MDIP	100˚C/W
SOIC	105˚C/W

Electrical Characteristics

($+V_{CC}$ = +5.0V; $-V_{EE}$ = −5.2V; R_{IN} = 50Ω; R_L = 500Ω; C_{COMP} = 10pF; ECL Mode, pin 6 = NC)

Symbol	Parameter	Conditions	Typ	Max/Min Ratings (Note 2)			Units
Case Temperature		CLC532AJP/AJE	+25˚C	−40˚C	+25˚C	+85˚C	
Frequency Domain Response							
SSBW	-3dB Bandwidth	V_{OUT} <0.1V_{PP}	190	140	140	110	MHz
LSBW		V_{OUT} = 2V_{PP}	45	35	35	30	MHz
	Gain Flatness	V_{OUT} < 0.1V_{PP}					
GFP	Peaking	0.1MHz to 200MHz	0.2	0.7	0.7	0.8	dB
GFR	Rolloff	0.1MHz to 100MHz	1.0	1.8	1.8	2.6	dB
LPD	Linear Phase Deviation	DC to 100MHz	2.0				deg
DG	Differential Gain	C_{COMP} = 5pF; R_L = 150Ω	0.05				%
DP	Differential Phase	C_{COMP} = 5pF; R_L = 150Ω	0.01				deg
CT10	Crosstalk Rejection	2V_{PP}, 10MHz	80	75	75	74	dB
CT20		2V_{PP}, 20MHz	74	69	69	68	dB
CT30		2V_{PP}, 30MHz	68	63	63	62	dB
Time Domain Performance							
TRS	Rise and Fall Time	0.5V Step	2.7	3.3	3.3	3.8	ns
TRL		2V Step	10	12.5	12.5	14.5	ns
TS14	Settling Time	±0.0025%	35				ns
TSP	2V Step; from 50% V_{OUT}	±0.01%	17	24	24	27	ns
TSS		±0.1%	13	18	18	21	ns
OS	Overshoot	2.0V Step	2	5	5	6	%
SR	Slew Rate		160	130	130	110	V/µs
Switch Performance							
SWT10	Channel to Channel Switching	50% SELECT to 10% V_{OUT}	5	7	7	8	ns
SWT90	Time (2V Step at Output)	50% SELECT to 90% V_{OUT}	15	20	20	23	ns
ST	Switching Transient		30				mV
Distortion And Noise Performance							
HD2	2nd Harmonic Distortion	2V_{PP}, 5MHz	80	67	67	67	dBc
HD3	3rd Harmonic Distortion	2V_{PP}, 5MHz	86	68	68	68	dBc
	Equivalent Input Noise						
SNF	Spot Noise Voltage	>1MHz	3.1				nV/$\sqrt{Hz}$

Electrical Characteristics (Continued)

($+V_{CC}$ = +5.0V; $-V_{EE}$ = −5.2V; R_{IN} = 50Ω; R_L = 500Ω; C_{COMP} = 10pF; ECL Mode, pin 6 = NC)

Symbol	Parameter	Conditions	Typ	Max/Min Ratings (Note 2)			Units
Distortion And Noise Performance							
INV	Integrated Noise	1MHz to 100MHz	32	42	42	46	µVrms
SNC	Spot Noise Current		3				pA/$\sqrt{Hz}$
Static And DC Performance							
VOS	Analog Output Offset Voltage (Note 5)		1	6.5	3.5	5.5	mV
DVIO	Temperature Coefficient		15	90		20	µV/°C
VOSM	Analog Output Voltage Matching		TBD				mV
IBN	Analog Input Bias Current		50	250	120	120	µA
DIBN	Temperature Coefficient		0.3	2.0		0.8	µA/°C
IBNM	Analog Input Bias Current Matching (Note 5)		TBD				µA
RIN	Analog Input Resistance		200	90	120	120	kΩ
CIN	Analog Input Capacitance		2	3.0	2.5	2.5	pF
GA	Gain Accuracy (Note 5)	±2V	0.998	0.998	0.998	0.998	V/V
GAM	Gain Matching	±2V	TBD				V/V
ILIN	Integral Endpoint Non-Linearity	±1V (Full Scale)	0.02	0.05	0.03	0.03	%FS
VO	Output Voltage	No Load	±3.4	2.4	2.8	2.8	V
IO	Output Current		45	20	30	30	mA
RO	Output Resistance	DC	1.5	4.0	2.5	2.5	Ω
Digital Input Performance							
	ECL Mode (Pin 6 Floating)						
VIH1	Input Voltage Logic HIGH			−1.1	−1.1	−1.1	V
VIL1	Input Voltage Logic LOW			−1.5	−1.5	−1.5	V
IIH1	Input Current Logic HIGH		14	50	30	30	µA
IIL1	Input Current Logic LOW		50	270	110	110	µA
	TTL Mode (pin 6 = +5V)						
VIH2	Input Voltage Logic HIGH			2.0	2.0	2.0	V
VIL2	Input Voltage Logic LOW			0.8	0.8	0.8	V
IIH2	Input Current Logic HIGH		14	50	30	30	µA
IIL2	Input Current Logic LOW		50	270	110	110	µA
Power Requirements							
ICC	Supply Current ($+V_{CC}$ = +5.0V) (Note 5)	No Load	23	30	28	25	mA
IEE	Supply Current ($-V_{EE}$ = −5.2V) (Note 5)	No Load	24	31	30	26	mA
PD	Nominal Power Dissipation	No Load	240				mW
PSRR	Power Supply Rejection Ratio (Note 5)		73	60	64	64	dB

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

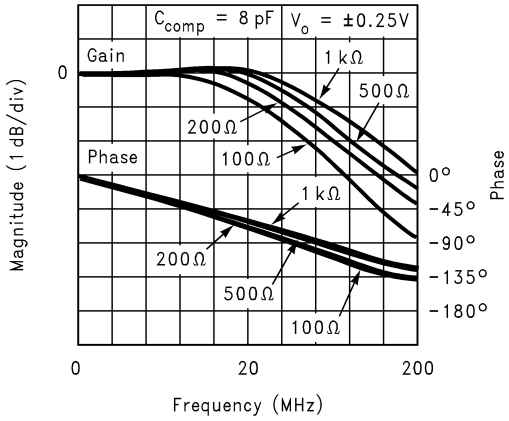
Note 3: The CLC532 does not require external C_{COMP} capacitors for proper operation.

Note 4: Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit maybe impaired. functional operability under any of these conditions is not necessarily implied. Exposure to maximum ratings for extended periods may affect device reliability.

Note 5: AJ: 100% tested at +25°C, sample tested at +85°C

Typical Performance Characteristics (+25˚C unless otherwise specified)

Small Signal/Phase vs. Load



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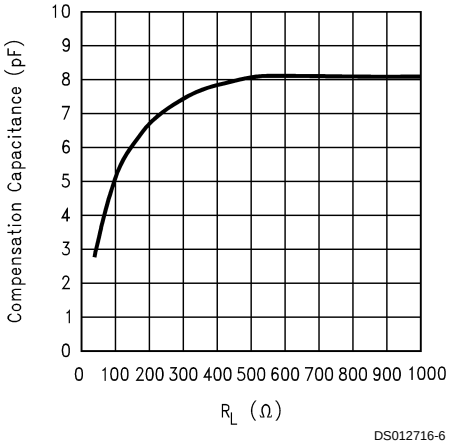
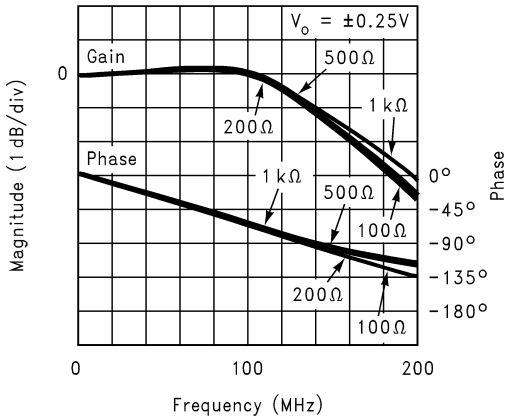
Recommended compensation Capacitance vs. Load



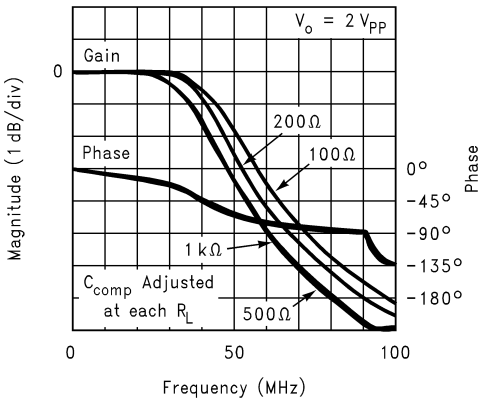
DS012716-6

Small Signal Gain/Phase vs. Load with Recommended C_{COMP}



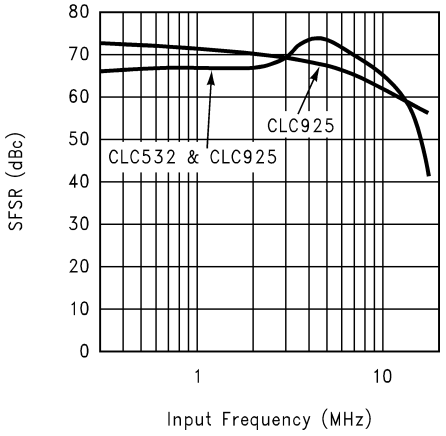
DS012716-7

Large Signal Frequency Response vs. Load



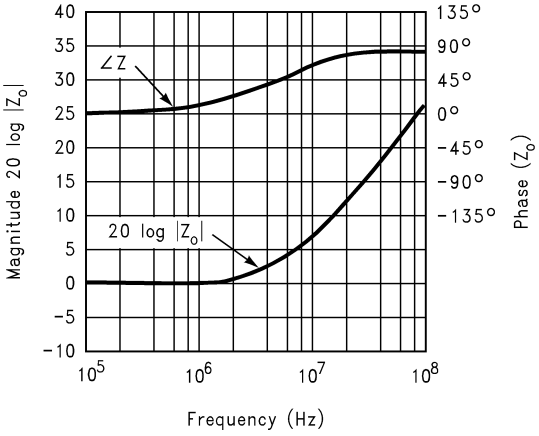
DS012716-8

SFRD vs. Input Frequency



DS012716-9

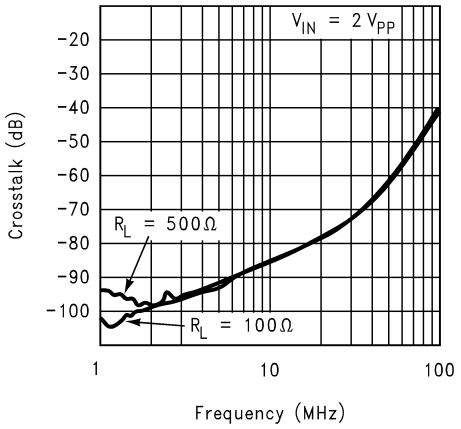
Output Impedance



DS012716-10

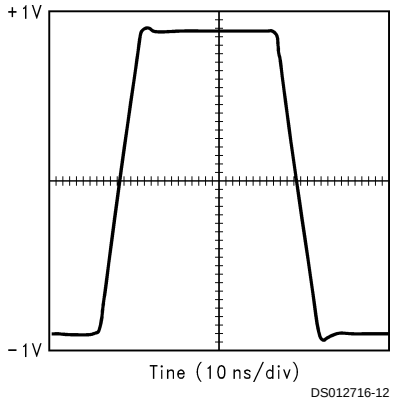
Typical Performance Characteristics (+25˚C unless otherwise specified) (Continued)

Channel to Channel Crosstalk



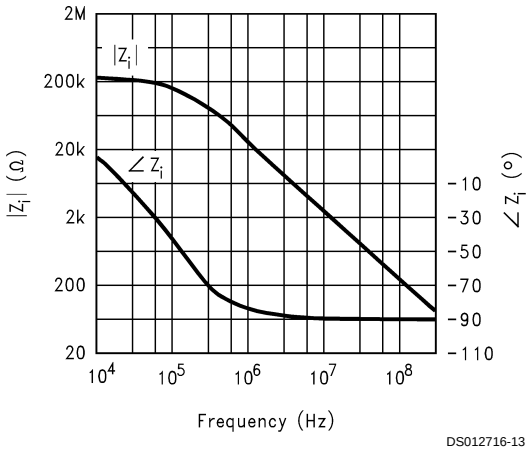
DS012716-11

Digitized Pulse Response



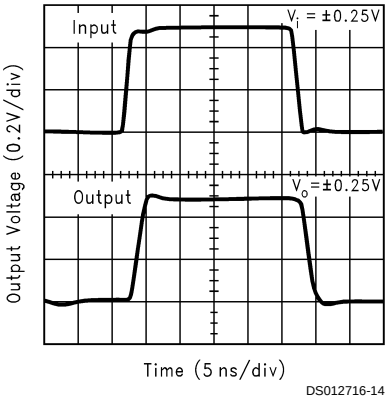
DS012716-12

Input Impedance



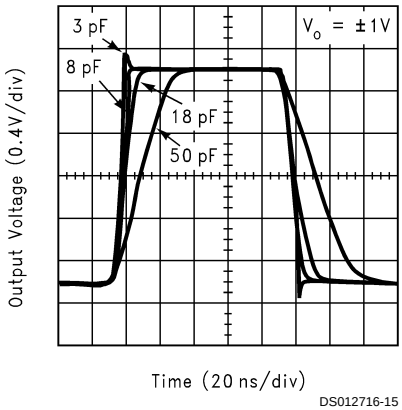
DS012716-13

Small Signal Pulse Response



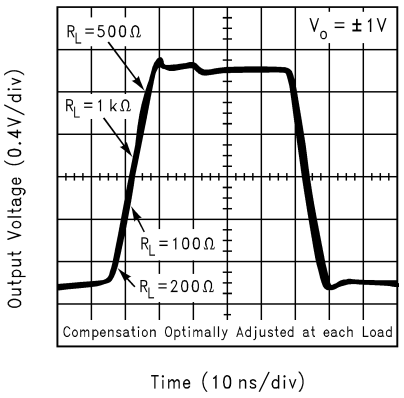
DS012716-14

Large Signal Pulse Response vs. C_{comp}



DS012716-15

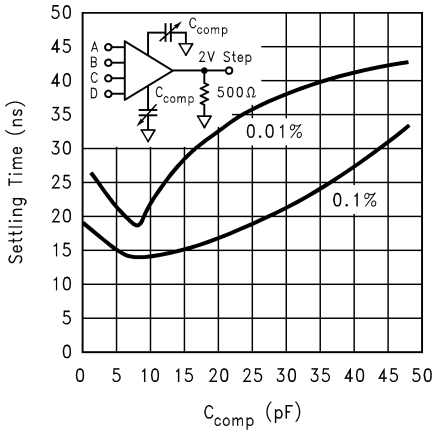
Large Signal Pulse Response vs. R_L



DS012716-16

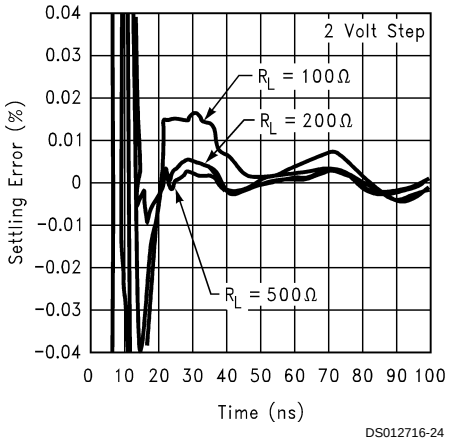
Typical Performance Characteristics (+25˚C unless otherwise specified) (Continued)

Settling Time vs C_{comp}



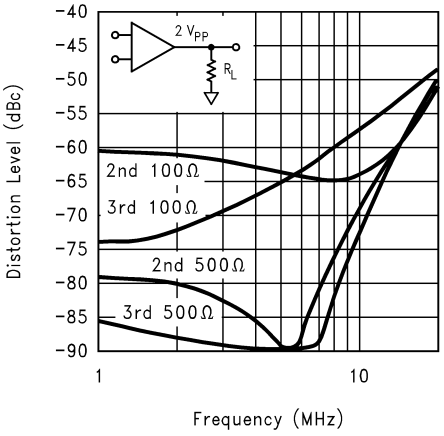
DS012716-17

Settling Time vs. R_L



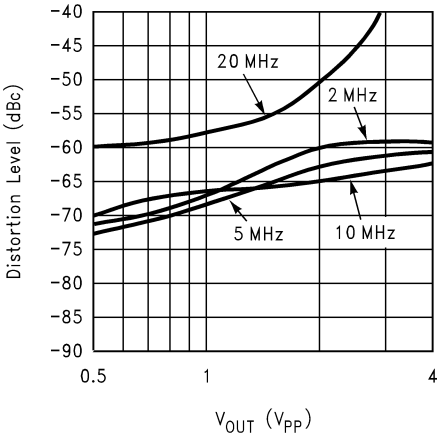
DS012716-24

2nd and 3rd Harmonic Distortion



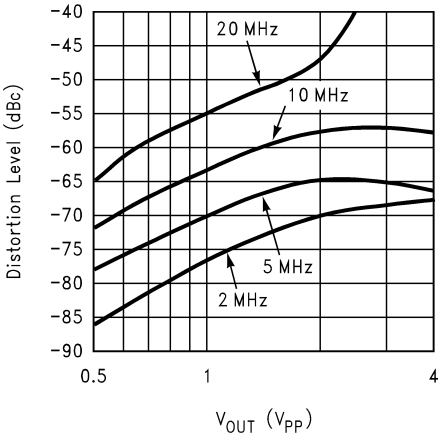
DS012716-18

2nd Harmonic Distortion vs. V_{OUT}; R_L = 100Ω



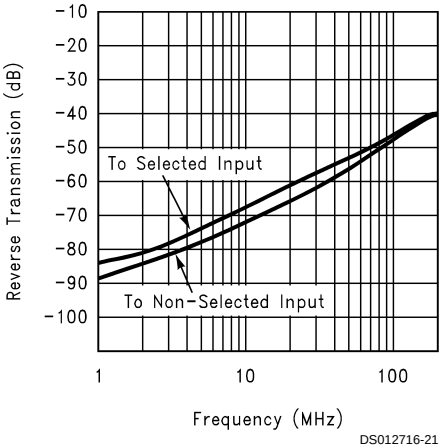
DS012716-19

3rd Harmonic Distortion vs. V_{OUT}; R_L = 100Ω



DS012716-20

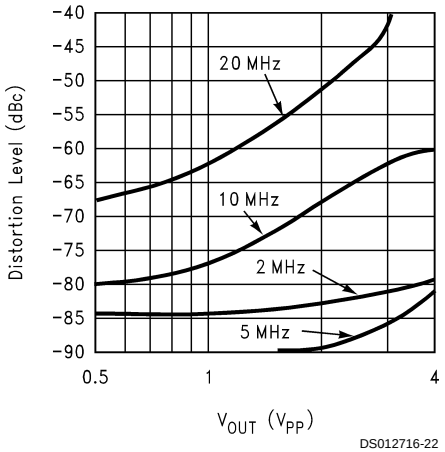
Reverse Transmission (S_{12})



DS012716-21

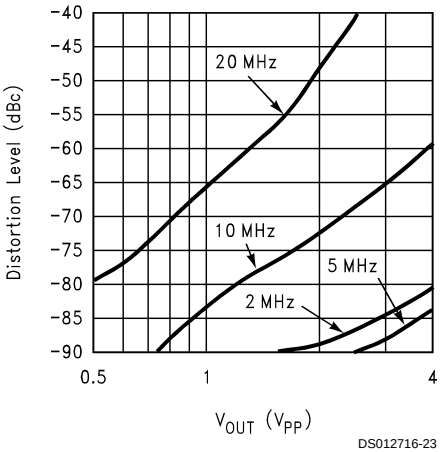
Typical Performance Characteristics (+25˚C unless otherwise specified) (Continued)

2nd Harmonic Distortion vs. V_{OUT}; R_L = 500Ω



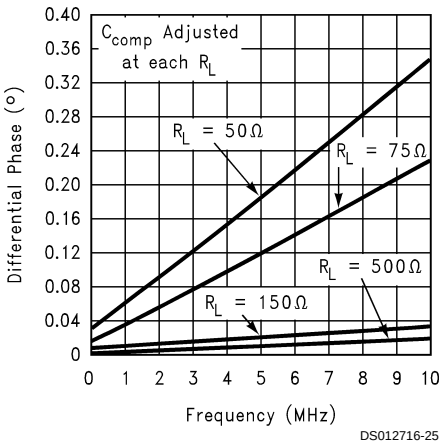
DS012716-22

3nd Harmonic Distortion vs. V_{OUT}; R_L = 500Ω



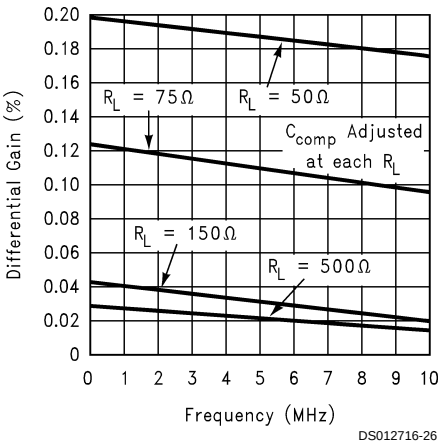
DS012716-23

Differential Phase vs. Frequency (Negative Sync)



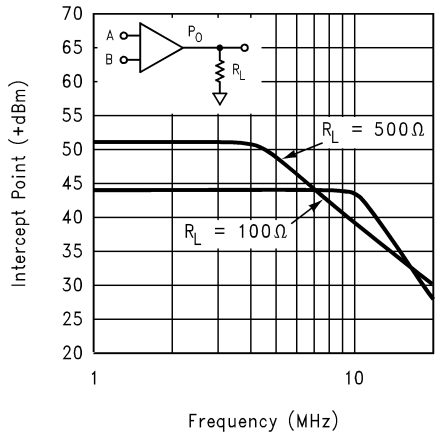
DS012716-25

Differintial Gain vs. Frequency (Negative Sync)



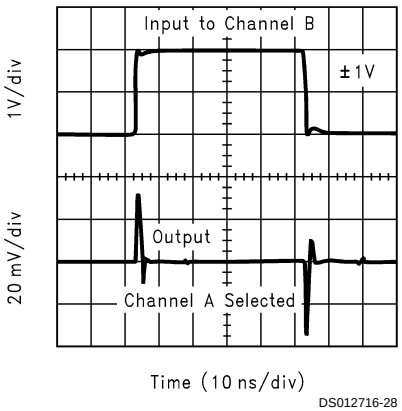
DS012716-26

2- Tone, 3rd Order Intermodulation Intercept



DS012716-27

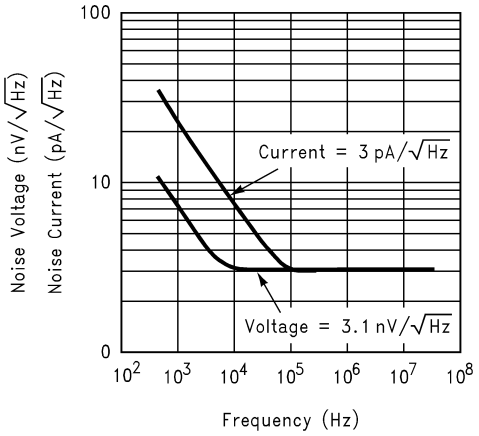
Transient Isolation



DS012716-28

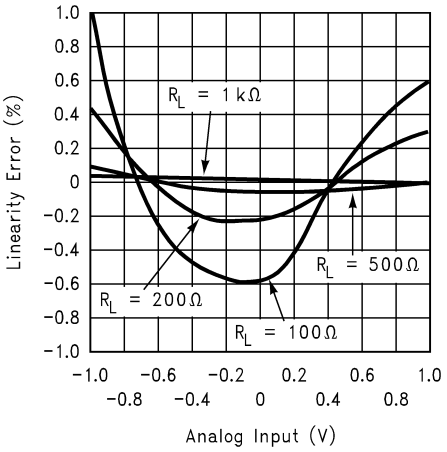
Typical Performance Characteristics (+25˚C unless otherwise specified) (Continued)

Equivalent Input Noise



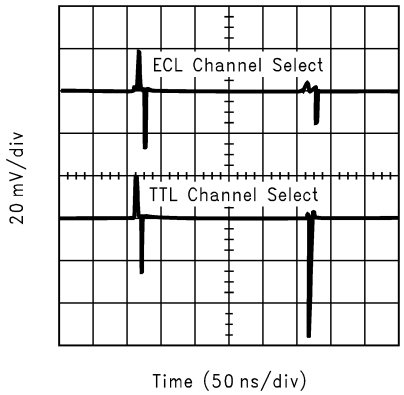
DS012716-29

Integral Linearity Error



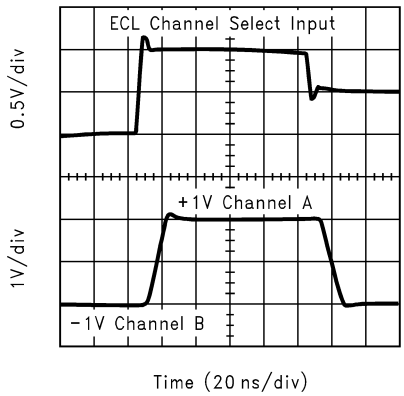
DS012716-30

Switching Transient (Grounded Inputs)



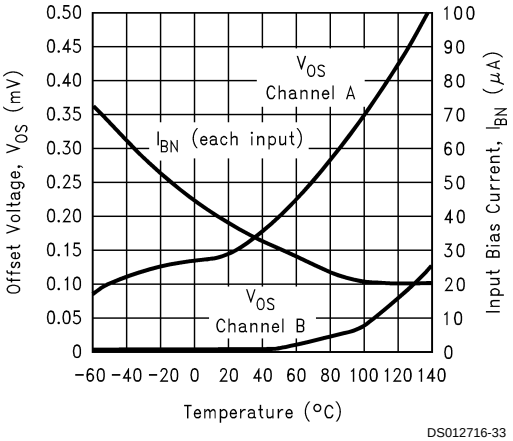
DS012716-31

Large signal Channel-to-Channel Switching



DS012716-32

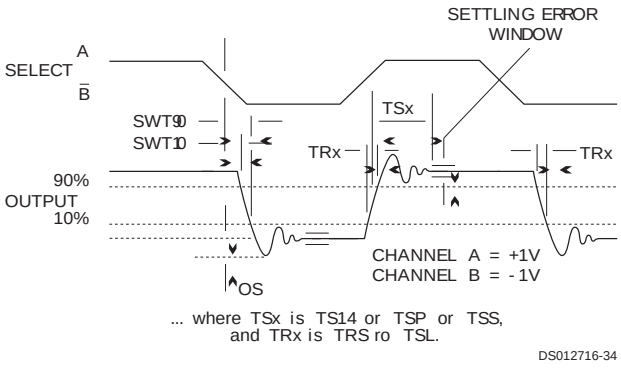
Typical DS Error vs. Temperature



DS012716-33

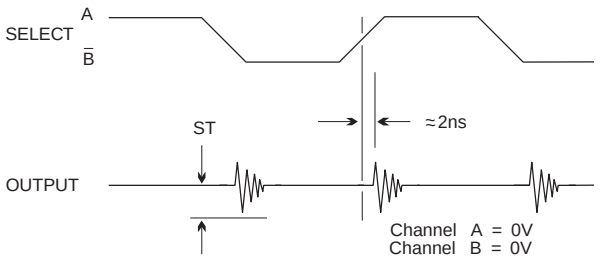
Application Information

System Timing Diagram



DS012716-34

System Transient Timing Diagram



DS012716-35

Operation

The CLC532 is a 2:1 analog multiplexer with high impedance buffered inputs, and a low distortion, output stage. The CLC532 employs a closed-loop design, which dramatically improves distortion performance. The channel SELECT control *Figure 1* determines which of the two inputs (IN_A or IN_B) is present at the OUTPUT. Beyond the basic multiplexer function, the CLC532 offers compatibility with either TTL or ECL logic families, as well as adjustable bandwidth.

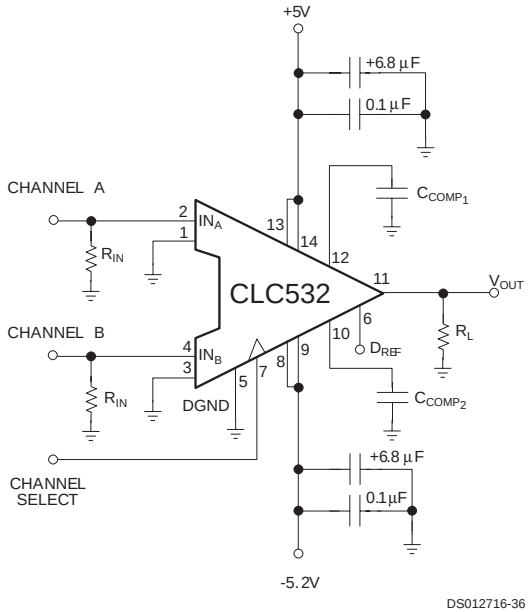


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FIGURE 1. Standard CLC532 Circuit Configuration

Digital Interface and Channel SELECT

The CLC532 functions with ECL, TTL and CMOS logic families, D_{REF} controls logic compatibility. In normal operation, D_{REF} is left floating, and the channel SELECT responds to ECL level signals, *Figure 2*. For TTL or CMOS level SELECT inputs (*Figure 3*), D_{REF} should be tied to +5V (the CLC532 incorporates an internal 2300Ω series isolation resistor for the D_{REF} input). For TTL or CMOS operation, the channel SELECT requires a resistor input network to prevent saturation of the channel select circuitry. Without this input network, channel SELECT logic levels above 3V will cause internal junction saturation and slow switching speeds.

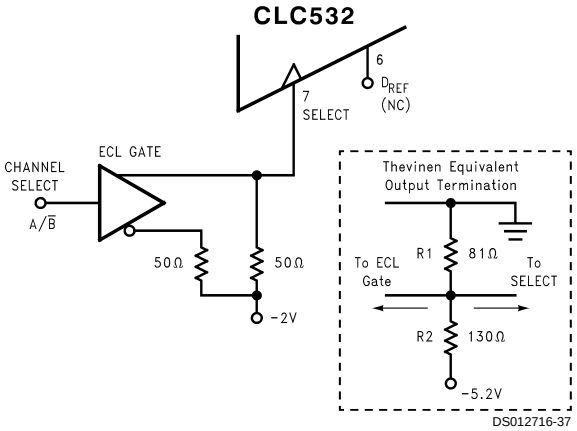

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FIGURE 2. ECL Level Channel SELECT Configuration

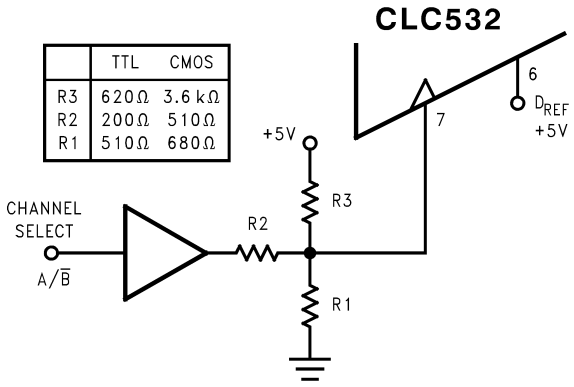

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FIGURE 3. TTL/CMOS Level Channel SELECT Configuration

Compensation

The CLC532 incorporates compensation nodes that allow both its bandwidth and its settling time/slew rate to be adjusted. Bandwidth and settling time/slew adjustments are linked, meaning that lowering the bandwidth also lowers slew rate and lengthens settling time. Proper compensation is necessary to optimize system performance. Time domain applications should generally be optimized for lowest RMS noise at the CLC532 output, while maintaining settling time and slew rate at adequate levels to meet system needs. Frequency Domain applications should generally be optimized for maximally flat frequency response.

Application Information (Continued)

Figure 4 below describes the basic relationship between settling time (T_S) and R_S for various values of load capacitance, C_L, where C_{COMP} = 10pF

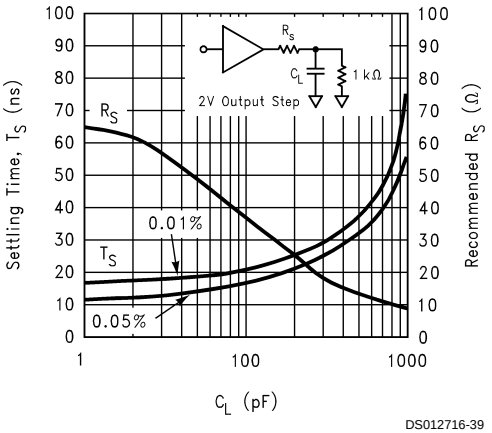


FIGURE 4. Settling Time and R_S vs. C_L

Figure 5 shows the resulting changes in bandwidth and slew rate for increasing values of C_{COMP}. The RMS noise at the CLC532 output can be approximated as:

$$OUTPUT_{NOISE_{RMS}} = (n_v)(\sqrt{1.57 * BW_{-3\,dB}})$$

where.... n_V = input spot noise voltage;

BW_{-3dB} = Bandwidth is from *Figure 5*.

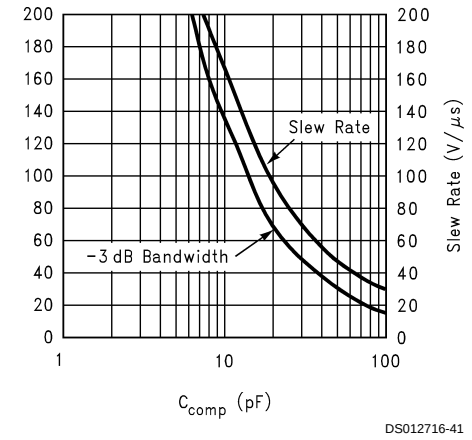


FIGURE 5. C_{COMP} for Maximally Flat Frequency Response

Power Supplies and Grounding

Proper power supply bypassing and grounding is essential to the CLC532's operation. 0.1µF to .1µF ceramic chip capacitor should be located very close to the individual power supply pins. Larger +6.8µF tantalum capacitors should be used within a few inches of the CLC532. The ground connections for these larger by-pass capacitors should be symmetrically located relative the CLC532 output load ground connection. Harmonic distortion can be heavily influenced by non-symmetric decoupling capacitor grounding. The smaller chip capacitors located directly at the power supply pins are not particularly susceptible to this effect.

Separation of analog and digital ground planes is not recommended. In most cases, a single low impedance ground plane will provide the best performance. In those special cases requiring separate ground planes, the following table indicates the signal and supply ground connections.

Pin	Functions	Ground Return
1,3	Shield/Supply Returns	Supplies and Inputs
5	D_{REF} Ground	D_{REF} Currents only

Input Shielding

The CLC532 has been designated for use in high speed wide dynamic range systems. Guarding traces and the use of the ground pins separating the analog inputs are recommended to maintain high isolation (*Figure 6*). Likely sources of noise and interference that may couple onto the inputs, are the logic signals and power supplies to the CLC532. Other types if clock and signal traces should not be overlooked, however.

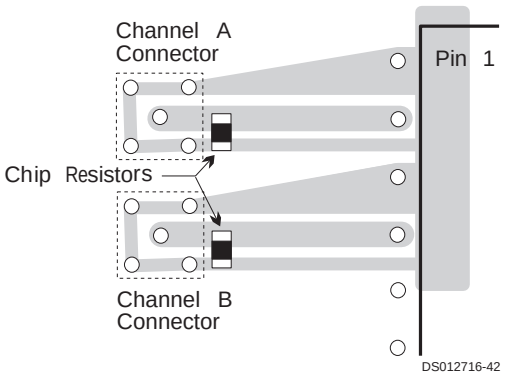


FIGURE 6. Alternate Layout Using Guard Ring

The general rule in maintaining isolation has two facets, minimize the primary return ground current path impedances back to the respective signal sources, while maximizing the impedance associated with common or secondary ground current return paths. Success or failure to optimize input signal isolation can be measured directly as the isolation between the input channels with the CLC532 removed from circuit. The channel-to -channel isolation of the CLC532 can never be better than the isolation level present at its inputs.

Special attention must be paid to input termination resistors. Minimizing the return current path that is common to both of the input termination resistors is essential. In the event that a ground return current from one input termination resistor is able to find a secondary path back to its signal source (which also happens to be common with either the primary or secondary return path for the second input termination resistor), a small voltage can appear across the second input termination resistor. The small voltage seen across the second input termination resistor will be highly correlated with the signal generating the initial return currents. This situation will severely degrade channel-to-channel isolation at the input of the CLC532, even if the CLC532 were removed from circuit. Poor isolation at the input will be transmitted directly to the output.

Use of "small" value input termination resistors will also improve channel-to-channel isolation. However, extremely low values (<25Ω) tend to stress the driving source's ability to provide a high-quality input signal to the CLC532. Higher values tend to aggravate any layout dependent crosstalk. 75Ω to 50Ω is a reasonable target, but the lower the better.

Application Information (Continued)

Combining Two Signals in ADC Applications

The CLC532 is applicable in a wide range of circuits and applications. A classic example of this flexibility is combining two or more signals for digitization by an analog-to-digital converter (ADC). A clear understanding of both the multiplexer and the ADC'S operation is needed to optimize this configuration.

To obtain the best performance from the combination, the output of the CLC532 must be an accurate representation of the selected input during the ADC conversion cycle. The time at which the ADC saples the input varies with the type is ADC that is being used.

Subranging ADCs usually have a Track-and-Hold (T/H) at their input. For a successful combination of the multiplexer and the ADC, the multiplexer timing and the T/H timing must be compatible. When the ADC is given a converter command, the T/H transitions from all caps Track mode to all caps Hold mode. The delay between the converter command and this transition is usually specified as Aperture Delay or as Sampling Time Offset.

To maximize the time that the multiplexer output has to settle, and that the T/H has to acquire the signal, the multiplexer should begin its transition from one input to the other immediately after the T/H transition into HOLD mode. Unfortunately it is during the initial portion of the HOLD period that a subranging ADC performs analog processing of the sampled signal. High slew rate transitions on the input during this time may have a detrimental effect on the conversion accuracy.

To minimize the effects of high input slew rates, one of two strategies that can employed. Strategy one applies when the sampling rate of the system is below the rated speed of the ADC. For this case, the CLC532 SELECT timing is delayed until after the multiplexer transition takes place, while the A/D has completed one conversion cycle and is waiting for the next convert command. As an example, if a CLC935 (15MSPS) ADC is being used at 10MSPS, the conversion takes place in the first 67ns after the CONVERT command. The next 33ns are spent waiting for the next CONVERT command. This quite period would be an ideal place to switch the multiplexer from one channel to the next.

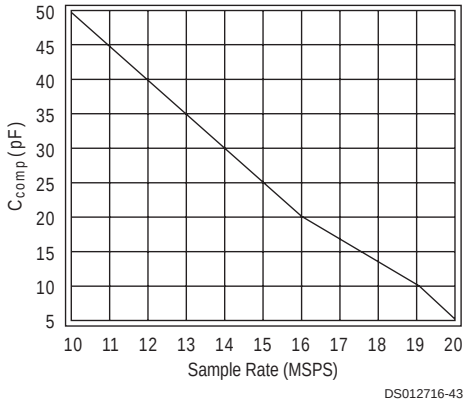


FIGURE 7. Recommend C_{COMP} vs. ADC Sample Rate

Strategy two involves lowering the slew rate at the input of the ADC so that less high frequency to feed through to the hold capacitor during HOLD mode. The CLC532 output signal can be slew limited by increasing its compensation capacitors. This approach also has the advantage of limiting the excess noise passed through the CLC532 to the ADC. *Figure 7* shows the recommended C_{COMP} values as a function of ADC sample rate. Since the optimal values will change from one ADC type to the next, this graph should be used as a starting point for C_{COMP} selection. Both C_{COMP} capacitors should be the same value to maintain output symmetry.

Flash ADCs are similar to subranging ADCs in that the sampling period is very brief. The primary difference is that the acquisition time of a flash converter is much shorter than that of a subranging ADC. It is only during this period that a flash converter is susceptible to interference from a rapidly changing analog input signal. With a flash ADC, the transition of the CLC532 output should be after the sampling instant ("See timing diagram for ADC Aperture Delay" after the CONVERT command).

Gain selection for an ADC

In many applications, such as RADAR, the dynamic range requirements may exceed the accuracy requirements. Since wide dynamic range ADC are also typically high accuracy ADCs, this often leads the designer into wrongly selecting an ADC which is a technical overkill and a budget buster. By using the CLC532 as a selectable-gain stage, a less expensive ADC can be used. As an example, if an application calls for 80dB of dynamic Range and 0.05% accuracy, rather than using a 14-bit converter, a 12-bit converter combined with the circuit in *Figure 8* will meet the same objective. The CLC532 is used to select between the analog input signal and a version of the input signal attenuated by 12dB. The circuit affords 14-bit dynamic range, 12-bit accuracy and 12-bit ease of implementation.

Application Information (Continued)

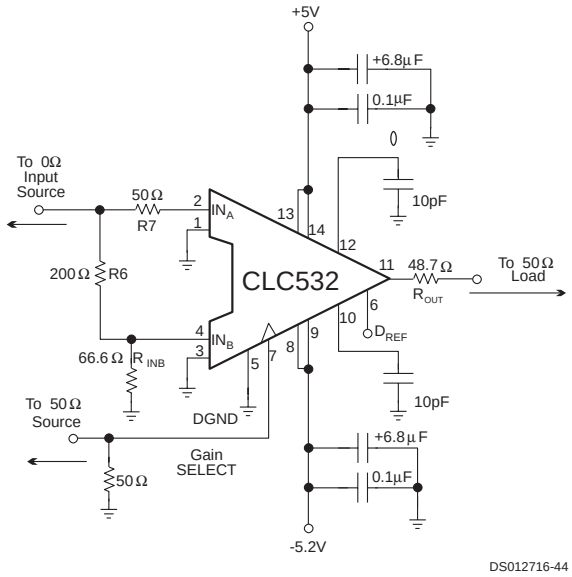


FIGURE 8. Selectable Gain Stage Improves ADC Dynamic Range

Full Wave Rectifier Circuit

The use of a diode rectifierintroduces significant distortion for signals that are small compared to the diode forward bias voltage. Therefore, when low distortion performance is needed, standard diode based circuits do not work well. The CLC532 can be configured to provide a very low distortion full wave rectifier. The circuit in*Figure 9* is used to select between an analog input signal and an inverted version of the input signal. The resulting output exhibits very little distortion for small scale signals up to several hundred kilohertz.

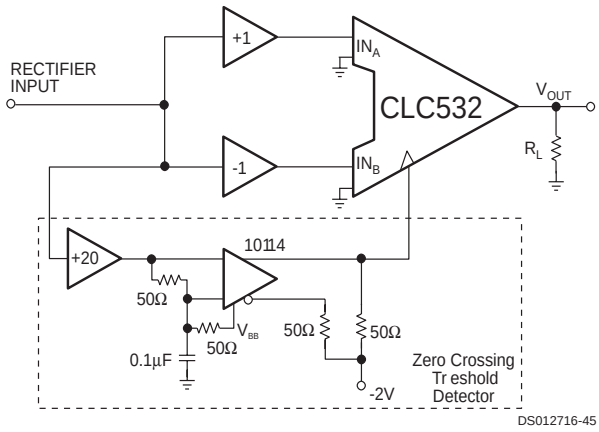


FIGURE 9. Low Distortion Full Wave Rectifier

Use of the CLC532 as a Mixer

A double balanced diode bridge mixer, as shown in *Figure 10*, operates by multiplying the RFsignal input by the LO input signal . This is done by using the LO signal phase to select either the forward or reverse path through the diode bridge. The result is an output where IF=RF when LO>0 and IF=−RF for LO<0. The same function can be obtained with-the CLC532 circuit shown in *Figure 11*. The CLC532 based circuit uses a digital LO making system design easier in those cases where the LO is digitally derived. Another advantage of the CLC532 based approach is excellent isolation between all three ports. (See the RF design awards article by Thomas Hack in January 1993 of RF Design.)

Application Information (Continued)

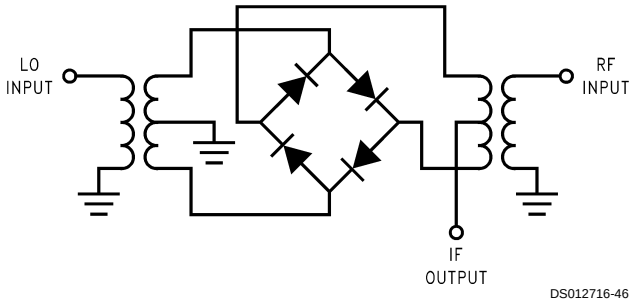


FIGURE 10. Typical Double-Balanced Mixer

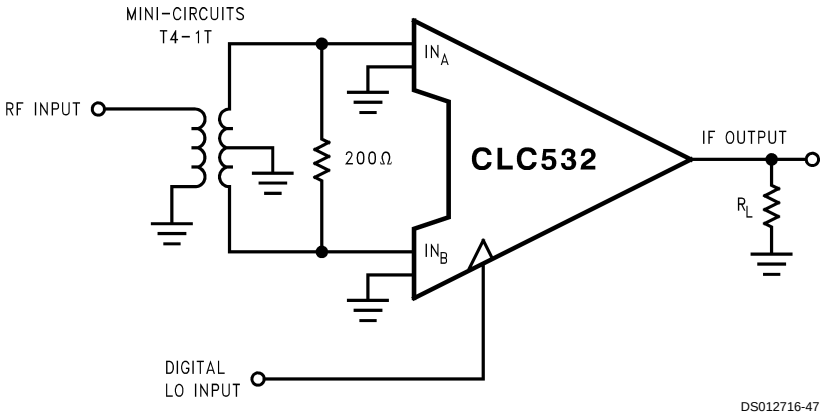
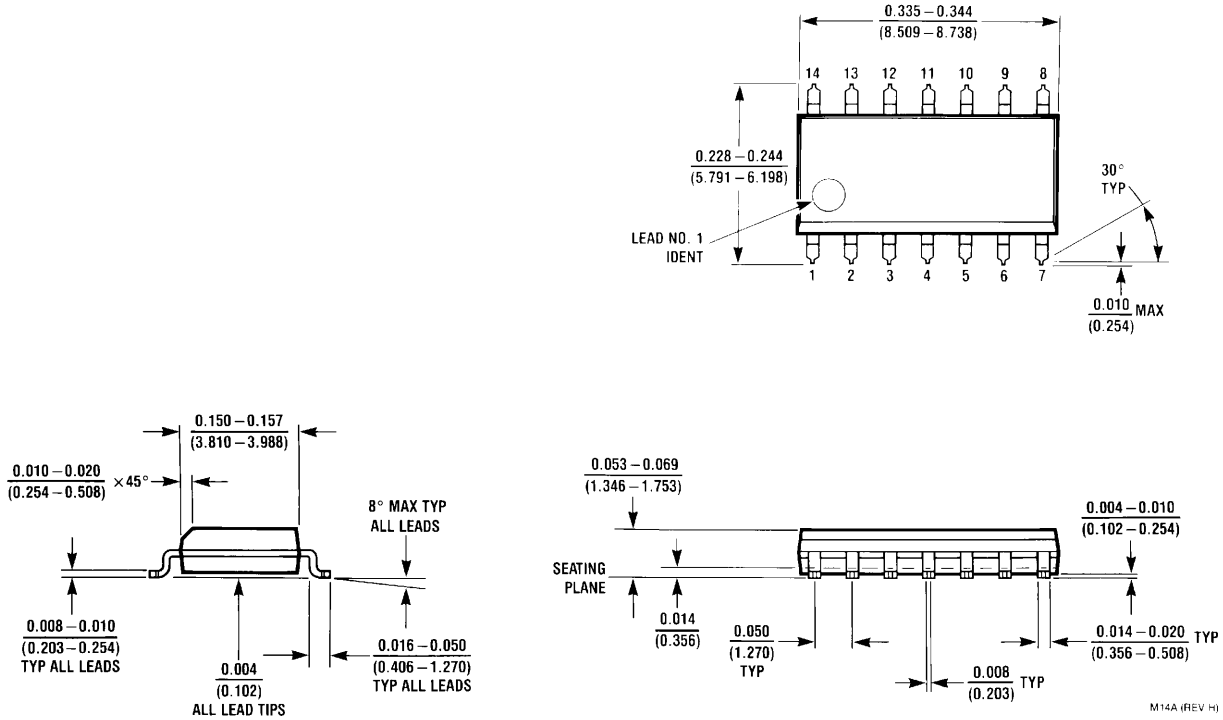


FIGURE 11. High-Isolation Mixer Implementation

Evaluation Board

An evaluation board (part number 730028) for CLC532 is available. This board can be used for fast, trouble-free, evaluation and characterization of the CLC532. Additionally, this board serves as a template for layout and fabrication information.

Physical Dimensions inches (millimeters) unless otherwise noted



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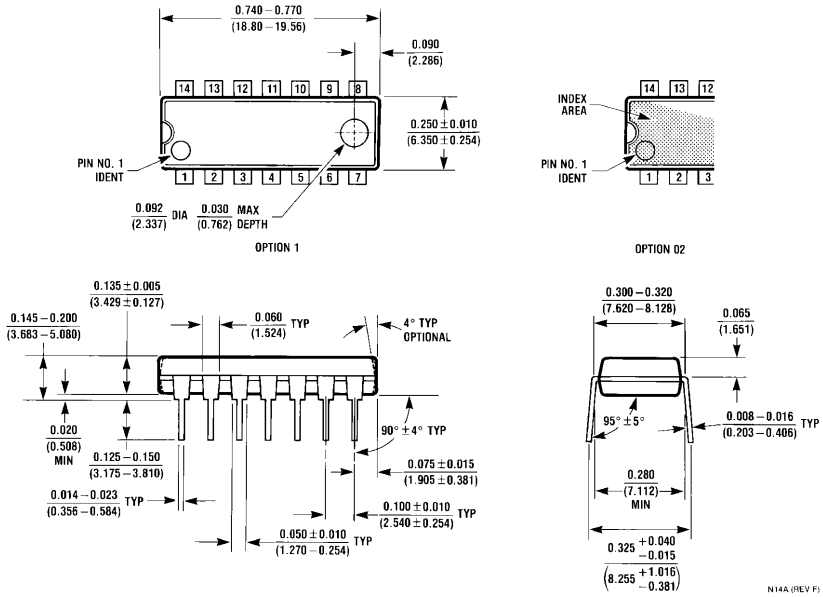

NS Package Number N14A

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