National Semiconductor

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CLC522
Wideband Variable Gain Amplifier

General Description

The CLC522 variable gain amplifier (VGA) is a dc-coupled, two-quadrant multipliers with differential voltage inputs and a single-ended voltage output. Two input buffers and an output operational amplifier are integrated with the multiplier core and make the CLC522 a complete VGA system that does not require external buffering.

The CLC522 provides the flexibility of externally setting the maximum gain with only two external resistors. Greater than 40dB gain control is easily achieved through a single high impedance voltage input. The CLC522 provides a linear (in Volts per Volt) relationship between the amplifier's gain and the gain-control input voltage.

The CLC522's maximum gain may be set anywhere over a nominal range of 2V/V to 100V/V. The gain control input then provides attenuation from the maximum setting. For example, set for a maximum gain of 100V/V, the CLC522 will provide a 100V/V to 1V/V gain control range by sweeping the gain control input voltage from +1 to −0.98V.

Set at a maximum gain of 10V/V, the CLC522 provides a 165MHz signal channel bandwidth and a 165MHz gain control bandwidth. Gain nonlinearity over a 40dB gain range is 0.5% and gain accuracy at A_{Vmax} = 10V/V is typically ±0.3%.

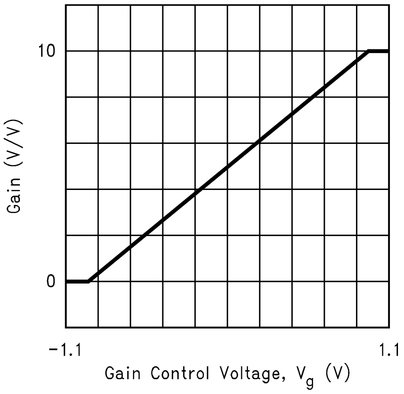
Features

- 330MHz signal bandwidth: A_{Vmax} = 2
- 165MHz gain control bandwidth
- 0.3° to 60MHz linear phase deviation
- 0.04% (−68dB) signal-channel non-linearity
- >40dB gain adjustment range
- Differential or single end voltage inputs
- Single-ended voltage output

Applications

- Variable attenuators
- Pulse amplitude equalizers
- HF modulators
- Automatic gain control & leveling loops
- Video production switching
- Differential line receivers
- Voltage controlled filters

Gain vs. Gain Control Voltage (V_g)



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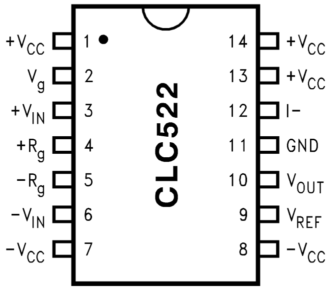
Connection Diagram



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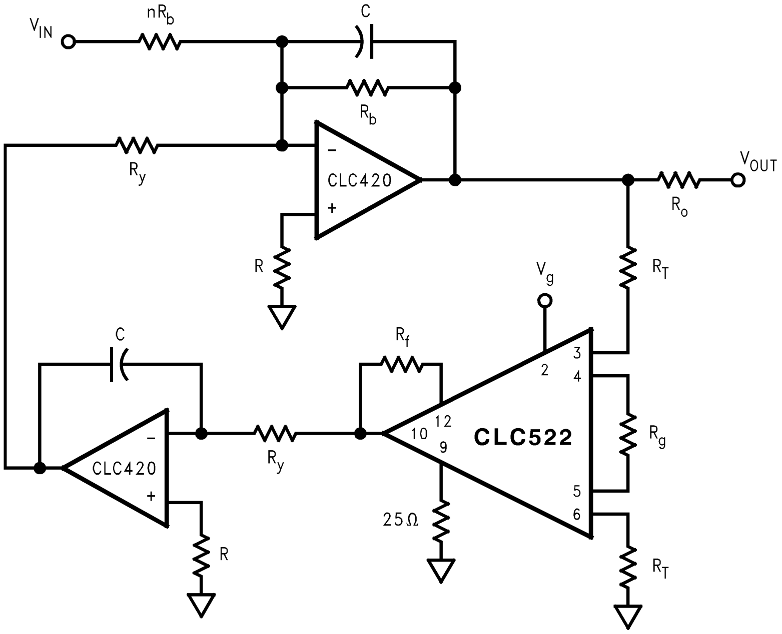
Pinout
DIP & SOIC

Typical Application



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2nd Order Tuneable Bandpass Filter

$$\frac{V_O}{V_{IN}} = \left(-\frac{1}{n}\right)\frac{s\dfrac{1}{CR_b}}{s^2 + s\dfrac{1}{CR_b} + \dfrac{k}{C^2R_y^2}}$$

$$k = 1.85\frac{R_f}{R_y}, \quad Q = \frac{\sqrt{kR_b}}{R_y}, \quad \omega_o = \frac{\sqrt{k}}{CR_y}$$

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Ordering Information

Package	Temperature Range Industrial	Part Number	Package Marking	NSC Drawing
14-pin plastic DIP	−40˚C to +85˚C	CLC522AJP	CLC522AJP	N14A
14-pin plastic SOIC	−40˚C to +85˚C	CLC522AJE	CLC522AJE	M14A, B

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	±7V
Short Circuit Current	80mA
Common-Mode Input Voltage	$\pm V_{CC}$
Maximum Junction Temperature	+200˚C
Storage TemperatureRange	−65˚C to +150˚C
Lead Temperature (Soldering 10 sec)	+300˚C

Operating Ratings

Thermal Resistance

Package	(θ_{JC})	(θ_{JA})
MDIP	55˚C/W	100˚C/W
SOIC	35˚C/W	105˚C/W

Electrical Characteristics

(V_{CC} = ±5 V; A_{Vmax} = +10; R_f = 1kΩ; R_g = 182Ω; R_L = 100Ω; V_g = +1.1V)

Symbol	Parameter	Conditions	Typ	Min/Max Ratings (Note 2)			Units
Ambient Temperature		CLC522AJE, AJP	+25˚C	+25˚C	0 to +70˚C	−40 to +85˚C	
Frequency Domain Response							
	-3dB Bandwidth (Note 7)	$V_{OUT} < 0.5V_{PP}$	165	120	115	110	MHz
		$V_{OUT} < 5.0V_{PP}$	150	100	95	90	MHz
	Gain Control Bandwidth (Note 5)	$V_{OUT} < 0.5V_{PP}$	165	120	115	110	MHz
	Gain Flatness	$V_{OUT} < 0.5V_{PP}$					
	Peaking (Note 7)	DC to 30MHz	0	0.1	0.1	0.1	dB
	Rolloff (Note 7)	DC to 30MHz	0.05	0.25	0.25	0.4	dB
	Linear Phase Deviation	DC to 60MHz	0.3	1.0	1.1	1.2	deg
	Feedthrough (Note 7), (Note 6)	30MHz	−62	−57	−57	−57	dB
Time Domain Response							
	Rise and Fall Time	0.5V Step	2.2	2.9	3.0	3.2	ns
		5.0V Step	3.0	5.0	5.0	5.0	ns
	Settling Time	2.0V Step to 0.1%	12	18	18	18	ns
	Overshoot	0.5V Step	2	15	15	15	%
	Slew Rate	4.0V Step	2000	1400	1400	1400	V/µs
Distortion And Noise Response							
	2nd Harmonic Distortion (Note 7)	$2V_{PP}$, 20MHz	−50	−44	−44	−44	dBc
	3rd Harmonic Distortion (Note 7)	$2V_{PP}$, 20MHz	−65	−58	−56	−54	dBc
	Equivalent Input Noise	1 to 200MHz	5.8	6.2	6.5	6.8	$nV/\sqrt{Hz}$
	Noise Floor	1 to 200MHz	−152	−150	−149	−149	dBm (1Hz)
Gain Accuracy							
	Signal Channel Nonlinearity (SGNL) (Note 4)	$V_{OUT} = \pm 2V_{PP}$	0.04	0.1	0.1	0.1	%
	Gain Control Nonlinearity (GCNL) (Note 4)	Full Range	0.5	2.0	2.2	3.0	%
	Gain Error (GACCU) (Note 4)	A_{Vmax} = +10	±0.0	±0.5	±0.5	±1.0	dB
	V_g High		+990	+990±60	+990±60	+990±60	mV
	V_g Low		−975	−975±80	−975±80	−975±80	mV
Static, DC Performance							
	V_{IN} Voltage Range	Common Mode	±2.2	±1.2	±1.2	±1.4	V
	Bias Current (Note 4)		9	21	26	45	µA
	Average Drift		65	-	175	275	nA/˚C
	Offset Current (Note 4)		0.2	2.0	3.0	4.0	µA
	Average Drift		5	-	30	40	nA/˚C
	Resistance		1500	650	450	175	kΩ
	Capacitance		1.0	2.0	2.0	2.0	pF

Electrical Characteristics (Continued)

(V_{CC} = ±5 V; A_{Vmax} = +10; R_f = 1kΩ; R_g = 182Ω; R_L = 100Ω; V_g = +1.1V)

Symbol	Parameter	Conditions	Typ	Min/Max Ratings (Note 2)			Units
Static, DC Performance							
	V_g Bias Current		15	38	47	82	µA
	Average Drift		125	-	300	600	nA/˚C
	Resistance		100	38	30	15	kΩ
	Capacitance		1.0	2.0	2.0	2.0	pF
	Output Voltage Range	R_L = ∞	±4.0	±3.7	±3.6	±3.5	V
	Current		±70	±47	±40	±25	mA
	Offset Voltage (Note 4)	A_{Vmax} = +10	25	85	95	120	mV
	Average Drift		100	-	350	400	µV/˚C
	Resistance		0.1	0.2	0.3	0.6	Ω
	I_{Rgmax}		1.8	1.37	1.26	1.15	mA
	Power Supply Sensitivity (Note 7)	Output Referred	10	40	40	40	mV/V
	Common Mode Rejection Ratio	Input Referred	70	59	59	59	dB
ICC	Supply Current (Note 4)	R_L = ∞	46	61	62	63	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Note 3: AJE (SOIC) is tested/guaranteed with R_f = 866Ω and R_g 165Ω

Note 4: J-level: spec. is 100% tested at +25˚C, sample tested at +85˚C.

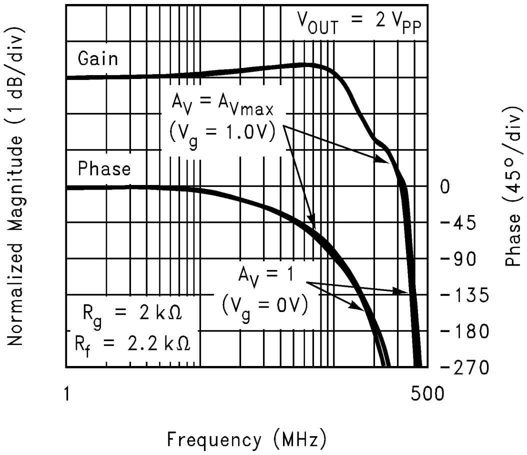
Note 5: Tested with V_{IN} = 0.2V and V_g <0.5V_{PP}

Note 6: Feedthrough is tested at maximum attenuation (i.e., V_g = −1.1V

Note 7: J-level, spec is sample tested at 25˚C.

Typical Performance Characteristics

Frequency Response (A_{Vmax} = 2)



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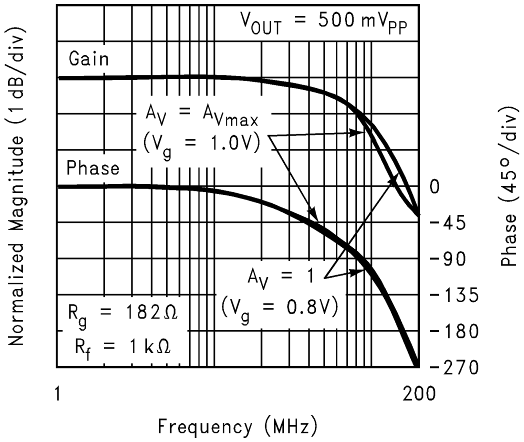
Frequency Response (A_{Vmax} =10)



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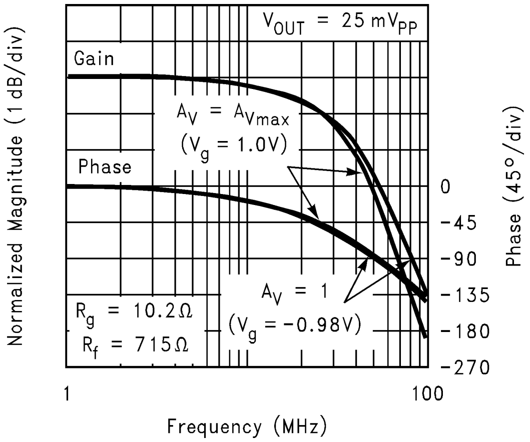
Typical Performance Characteristics (Continued)

Frequency Response (A_{Vmax} =100)



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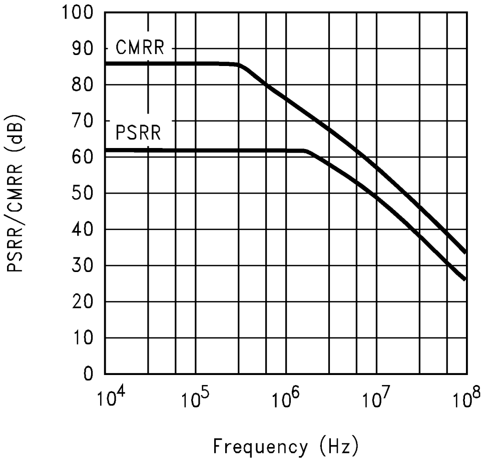
PSRR and CMRR (input Referred)



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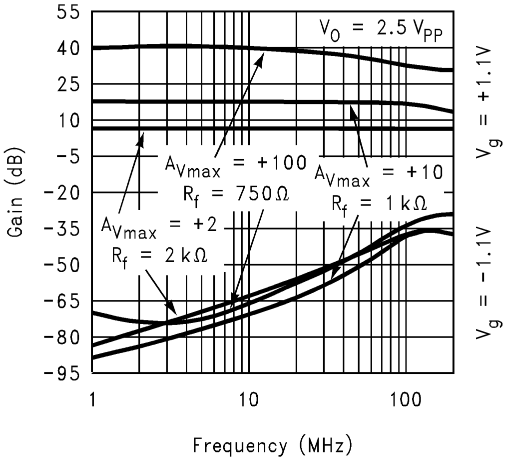
Feed-Through Isolation



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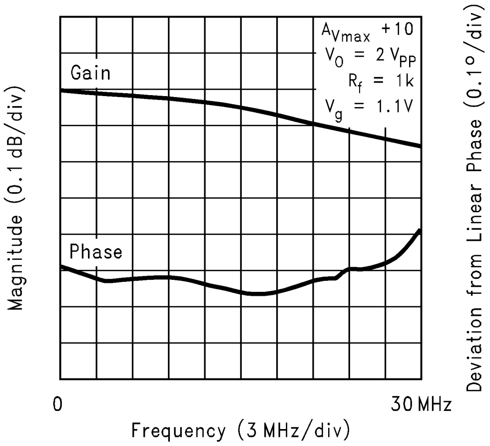
Gain Flatness & Linear Phase Deviation



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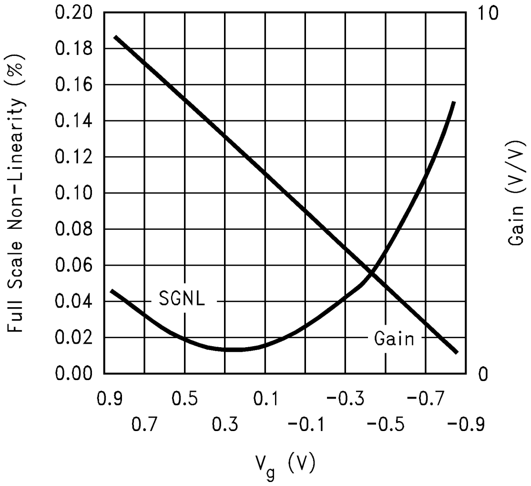
SGNL vs. V_g, Gain



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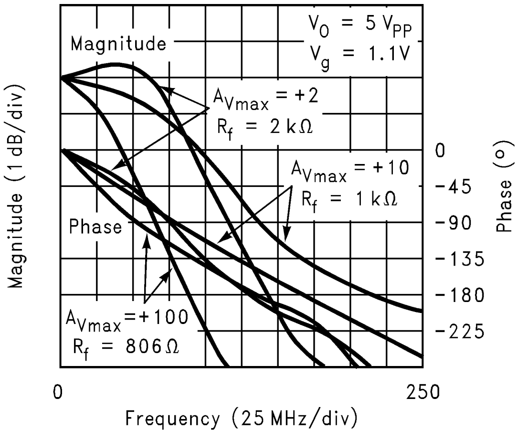
Large Signal Frequency Response



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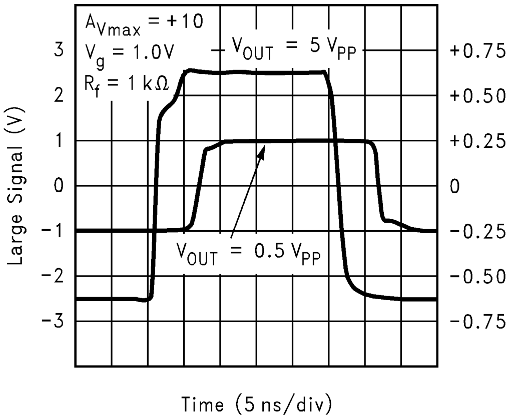
Typical Performance Characteristics (Continued)

Large & Small Signal Pulse Response



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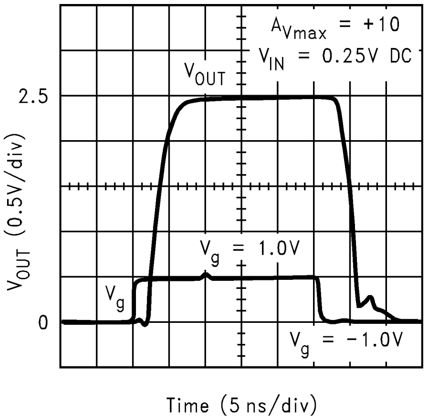
Gain Control Settling Time & Delay



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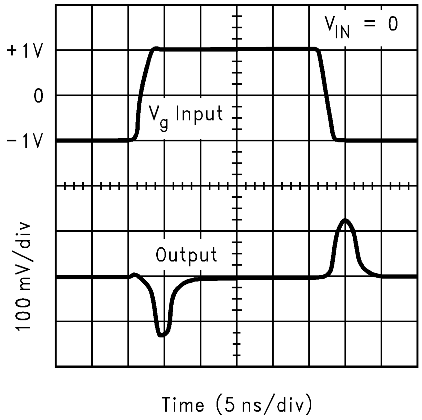
Gain Control Channel Feedthrough



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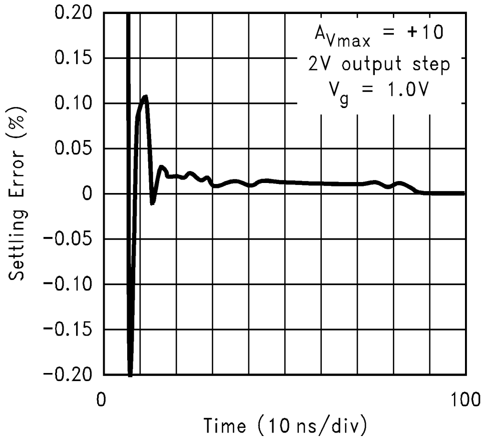
Short Term Settling Time



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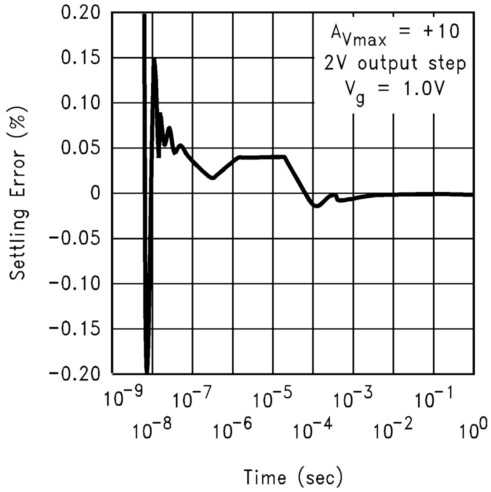
Long Term Settling Time



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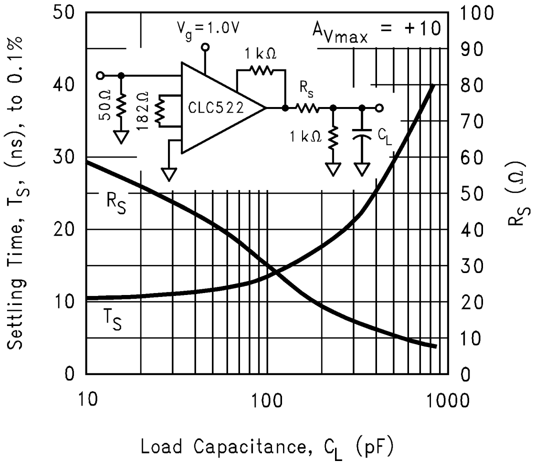
Settling Time vs. Capacitive Load



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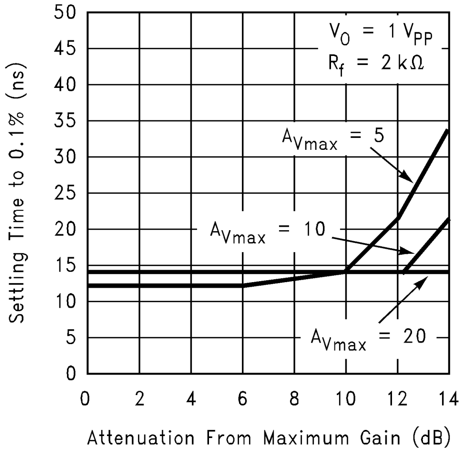
Typical Performance Characteristics (Continued)

Settling Time vs. Gain



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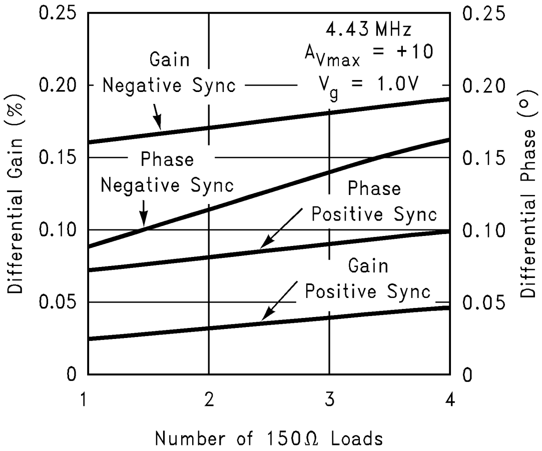
Differential Gain & Phase



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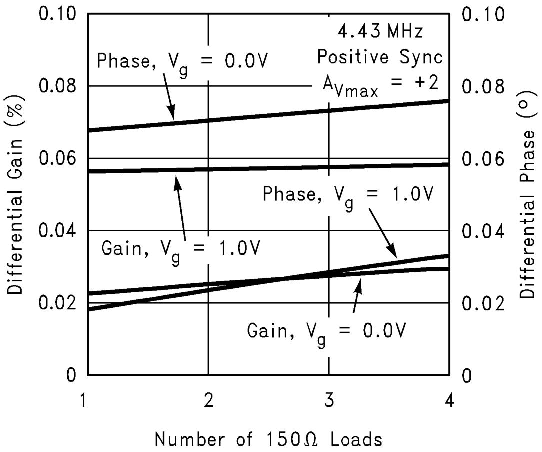
Differential Gain & Phase



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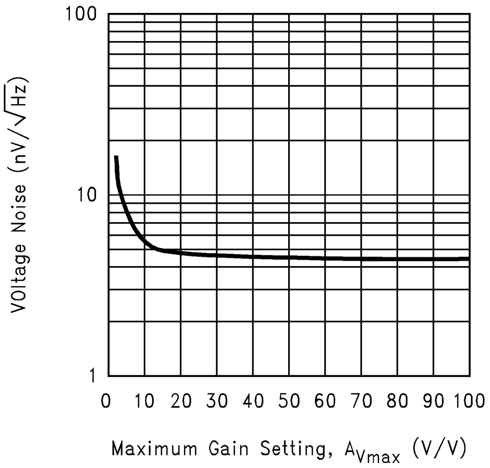
Input Referred Voltage Noise vs. A_{Vmax}



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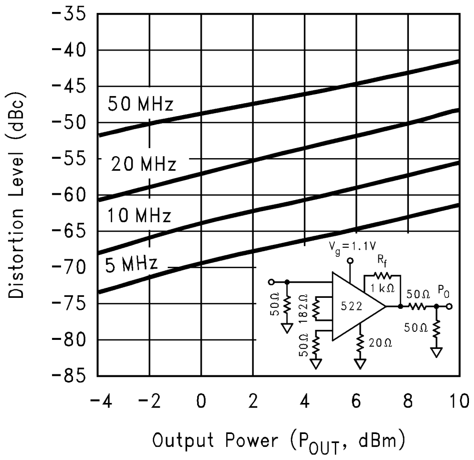
2nd Harmonic Distortion vs. P_{OUT}



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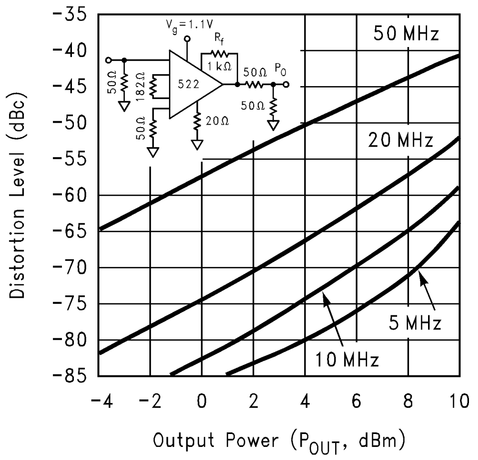
3rd Harmonic Distortion vs. P_{OUT}



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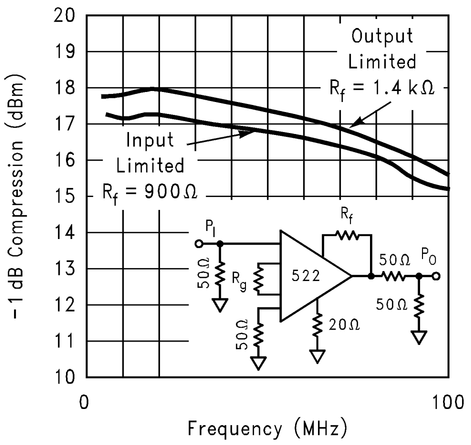
Typical Performance Characteristics (Continued)

−1dB Compression at Maximum Gain



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Application Division

Theory of Operation

The CLC522 is a linear wideband variable gain amplifier as illustrated in *Figure 1*. A voltage input signal may be applied differentially between the two inputs ($+V_{IN}$, $-V_{IN}$), or single-endedly by grounding one of the unused inputs.

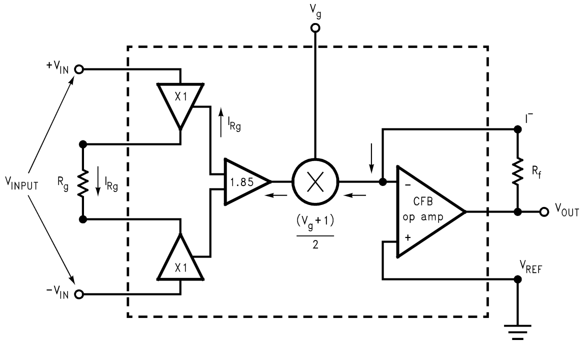

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FIGURE 1.

The CLC522 input buffers convert the input voltage to a current (I_{Rg}) that is a function of the differential input voltage (V_{INPUT} = $+V_{IN}-\ -V_{IN}$) and the value of the gain-setting resistor (R_g). This current (I_{Rg}) is then mirrored to a gain stage with a current gain of 1.85. The voltage controlled two-quadrant multiplier attenuates this current which is then converted to a voltage via the output amplifier. This output amplifier is a current-feedback op amp configured as a transimpedance amplifier. Its transimpedance gain is the feedback resistor (R_f). The input signal, output, and gain control are all voltages. The output voltage can easily be calculated as seen in Eq. 1.

$$V_{OUT} = I_{R_g} \bullet 1.85 \bullet \left[\frac{V_g + 1}{2}\right] \bullet R_f \tag{1}$$

$$\text{SINCE } I_{R_g} = \frac{V_{INPUT}}{R_g}$$

$$A_V = 1.85 \bullet \frac{R_f}{R_g} \bullet \left[\frac{V_g + 1}{2}\right] \tag{2}$$

The gain of the CLC522 is therefore a function of three external variables; R_g, R_f and V_g as expressed in Eq. 2. The gain control voltage (V) has an ideal input range of $-1V \le V_g + 1V$. At $V_g = +1V$, the gain of the CLC522 is at its maximum as expressed in Eq. 3.

$$A_{V_{max}} = 1.85 \frac{R_f}{R_g} \tag{3}$$

Notice also that Eq. 3 holds for both differential and single-ended operation.

Choosing R_f and R_g

R_g is calculated from Equation 4. $V_{input_{max}}$ is the maximum peak

$$R_g = \frac{V_{input_{max}}}{I_{R_{g_{max}}}} \tag{4}$$

input voltage (V_{pk}) determined by the application. I_{Rgmax} is the maximum allowable current through R_g and is typically 1.8mA. Once A_{Vmax} is determined from the minimum input and desired output voltages, R_f is then determined using Eq. 5. These values of R_f and R_g are

$$R_f = \frac{1}{1.85} * R_g * A_{V_{max}} \tag{5}$$

the minimum possible values that meet the input voltage and maximum gain constraints. Scaling the resistor values will decrease bandwidth and improve stability.

Application Division (Continued)

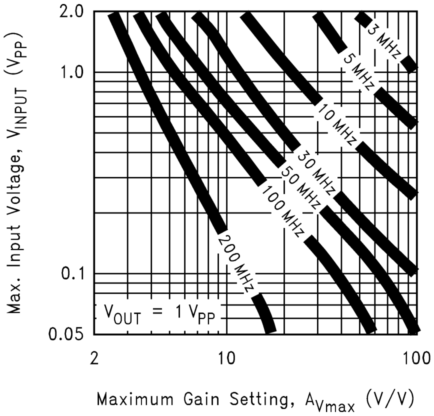

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FIGURE 2. Bandwidth vs. $V_{inputmax}$ vs. A_{vmax}

Figure 2 illustrates the resulting CLC522 bandwidths as a function of the maximum and minimum input voltages when V_{out} is held constant at $1V_{pp}$.

Adjusting Offsets

Treating the offsets introduced by the input and output stages of the CLC522 is easily accomplished with a two step process. The offset voltage of the output stage is treated by first applying −1.1Volts on V_g, which effectively isolates the input stage and multiplier core from the output stage.

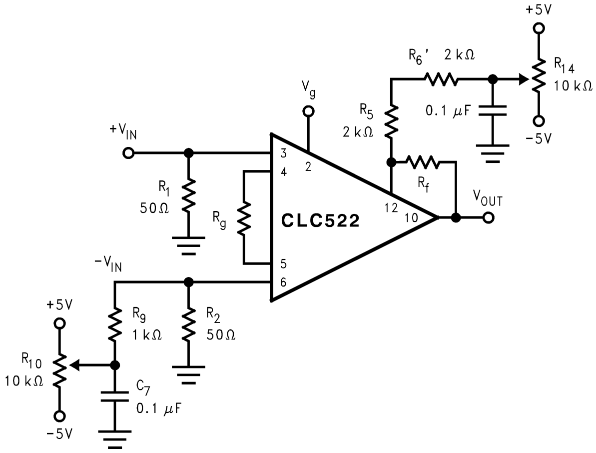

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FIGURE 3.

As illustrated in *Figure 3*, the trip pot located at R14 on the CLC522 Evaluation Board should then be adjusted in order to null the offset voltage seen at the CLC522's output (pin 10). Once this is accomplished, the offset errors introduced by the input stage and multiplier core can then be treated. The second step requires the absence of an input signal and matched source impedances on the two input pins in order to cancel the bias current errors. This done then +1.1Volts should be applied to V_g and the trip pot located at R10 adjusted in order to mull the offset voltage seen at the CLC522's output. If a more limited gain range is anticipated, the above adjustments should be made at these operating points.

Gain Errors

The CLC522's gain equation as theoretically expressed in Eq. 2 must include the device's error terms in order to yield the actual gain equation. Each of the gain error terms are specified in the Electrical Characteristics table and are defined below and illustrated in *Figure 4*.

GACCU : error of A_{Vmax}, expressed as ±dB.

GCNL : deviation from theoretical expressed as ±
.

V_{ghigh} : voltage on V_g producing A_{Vmax}.

V_{glow} : voltage on V_g producing $A_{Vmin} = 0V/V$.

ΔV_{ghigh}, ΔV_{glow} : error of V_{ghigh}, V_{glow} expressed as ±mV.

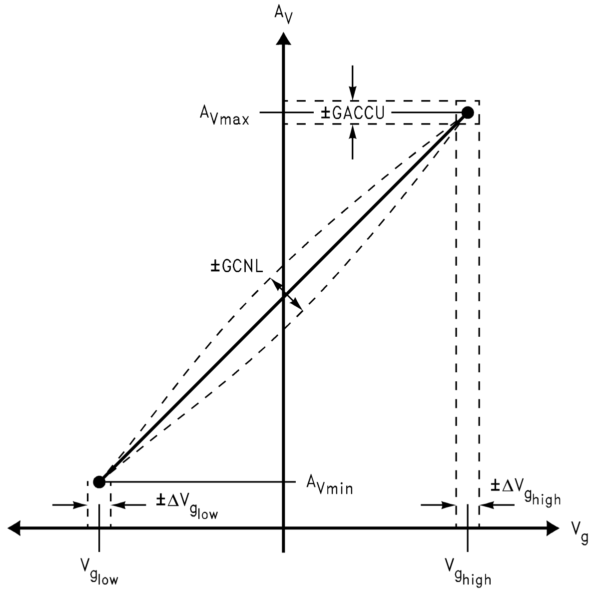

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FIGURE 4.

Combining these error terms with Eq. 2 gives the ″gain envelope″ equation and is expressed in Eq. 7. From the Electrical Characteristics table, the nominal endpoint values of V_g are: V_{ghigh} = 990mV and V_{glow} = −975mV.

$$A_v = A_{vmax}\left[10^{\frac{+GACCU}{20}}\frac{\left[V_g - V_{glow} \pm \Delta V_{glow}\right]}{\left[V_{ghigh} \pm \Delta V_{ghigh} - V_{glow} \pm \Delta V_{glow}\right]} \pm (1-V_g^2)\,GCNL\right] \tag{6}$$

Signal-Channel Nonlinearity

Signal-channel nonlinearity, SGNL, also known as integral endpoint linearity, measures the non-linearity of an amplifier's voltage transfer function. The CLC522's SGNL, as it is specified in the Electrical Characteristics table, is measured while the gain is set at its maximum (i.e. V_g=+1.1V). The Typical Performance Characteristics plot lableled ″SGNL & Gain vs V_g″ illustrates the CLC522's SGNL as V_g is swept through its full range. As can be seen in this plot, when the gain as reduced from A_{Vmax}, SGNL improves to <0.02%(−74cB) at V_g=0 and then degrades somewhat at the lowest gains.

Noise

Figure 5 describes the CLC522's input-referred spot noise density as a function of A_{Vmax}. The plot includes all the noise contributing terms. At A_{Vmax} = 10V/V, the CLC522 has a typical input referred spot noise density (e_{ni}) of $5.8nV/\sqrt{Hz}$. The input RMS voltage noise can be determined from the following single-pole model:

Application Division (Continued)

$$V_{RMS} = e_{in} * \sqrt{1.57 * (\text{-3dB bandwidth})} \quad (7)$$

Further discussion and plots of noise and the noise model is provided in Application Note OA-23. National also provides SPICE models that model internal noise and other parameters for a typical part.

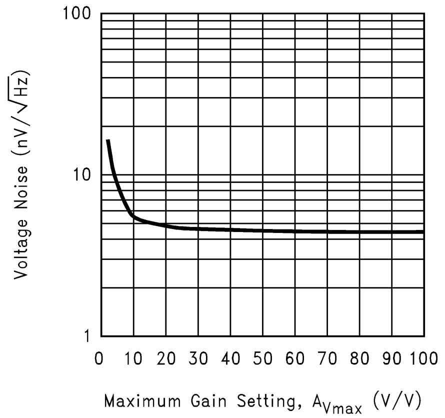

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FIGURE 5. Input referred Voltage Noise vs. $A_{V_{max}}$

Circuit Layout Considerations

Please refer to the CLC522 Evaluation Board literature for precise layout guidelines. Good high-frequency operation requires all of the de-coupling capacitors shown in to be placed as close as possible to the power supply pins in order to insure a proper high-frequency low-impedance bypass.

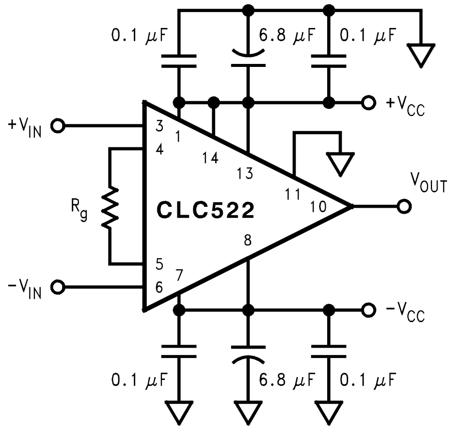

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FIGURE 6.

Adequate ground plane and low-inductive power returns are also required of the layout. Minimizing the parasitic capacitances at pins 3, 4, 5, 6, 9, 10 and 12 as shown in *Figure 7* will assure best high frequency performance.

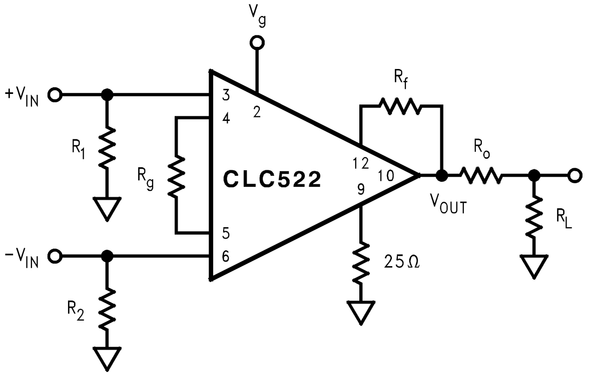

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FIGURE 7.

Vref (pin 9) to ground should include a small resistor value of 25 ohms or greater to buffer the internal voltage follower. The parasitic inductance of component leads or traces to pins 4, 5 and 9 should also be kept to a minimum. Parasitic or load capacitance, C_L, on the output (pin 10) degrades phase margin and can lead to frequency response peaking or circuit oscillation. This should be treated with a small series resistor between output (pin 10) and C_L(see the plot ″Settling Time vs. Capacitive Load″ for a recommended series resistance).

Component parasitics also influence high frequency results, therefore it is recommended to use metal film resistors such as RN55D or leadless components such as surface mount devices. High profile sockets are not recommended. If socketing is necessary, it is recommended to use low impedance flush mount connector jacks such as Cambion (P/N 450-2598).

Application Circuits

Four-Quadrant Multiplier

Applications requiring multiplication, squaring or other non-linear functions can be implemented with four-quadrant multipliers. The CLC522 implements a four-quadrant multiplier as illustrated in *Figure 8*.

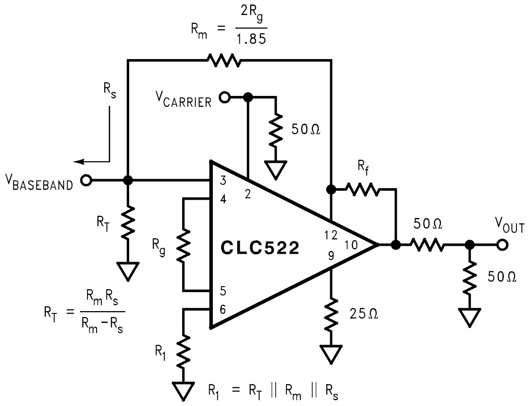

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FIGURE 8.

Application Division (Continued)

Frequency Shaping

Frequency shaping the bandwidth extension of the CLC522 can be accomplished using parallel networks connected across the R_g ports. The network shown in the *Figure 9* schematic will effectively extend the CLC522's bandwidth.

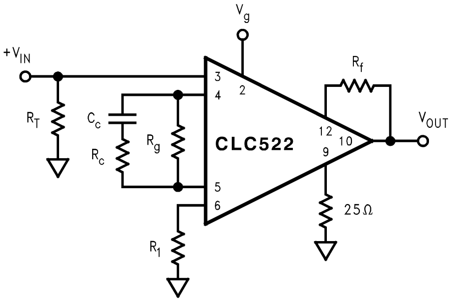

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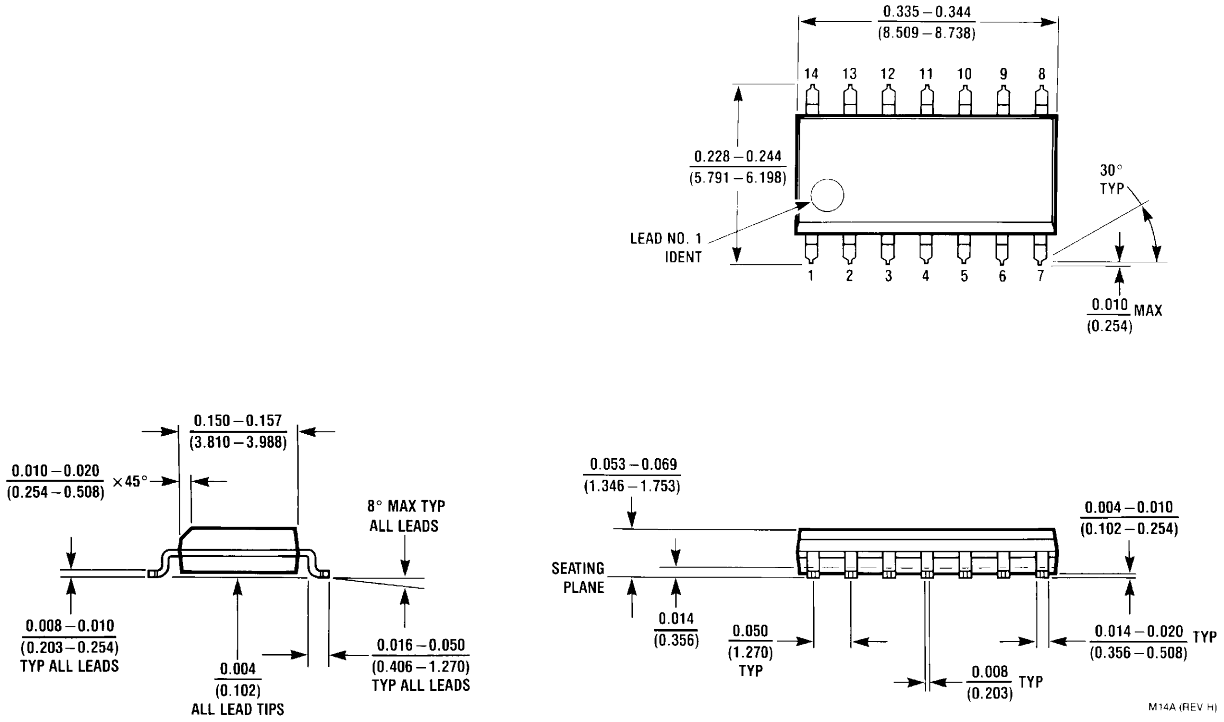
FIGURE 9.

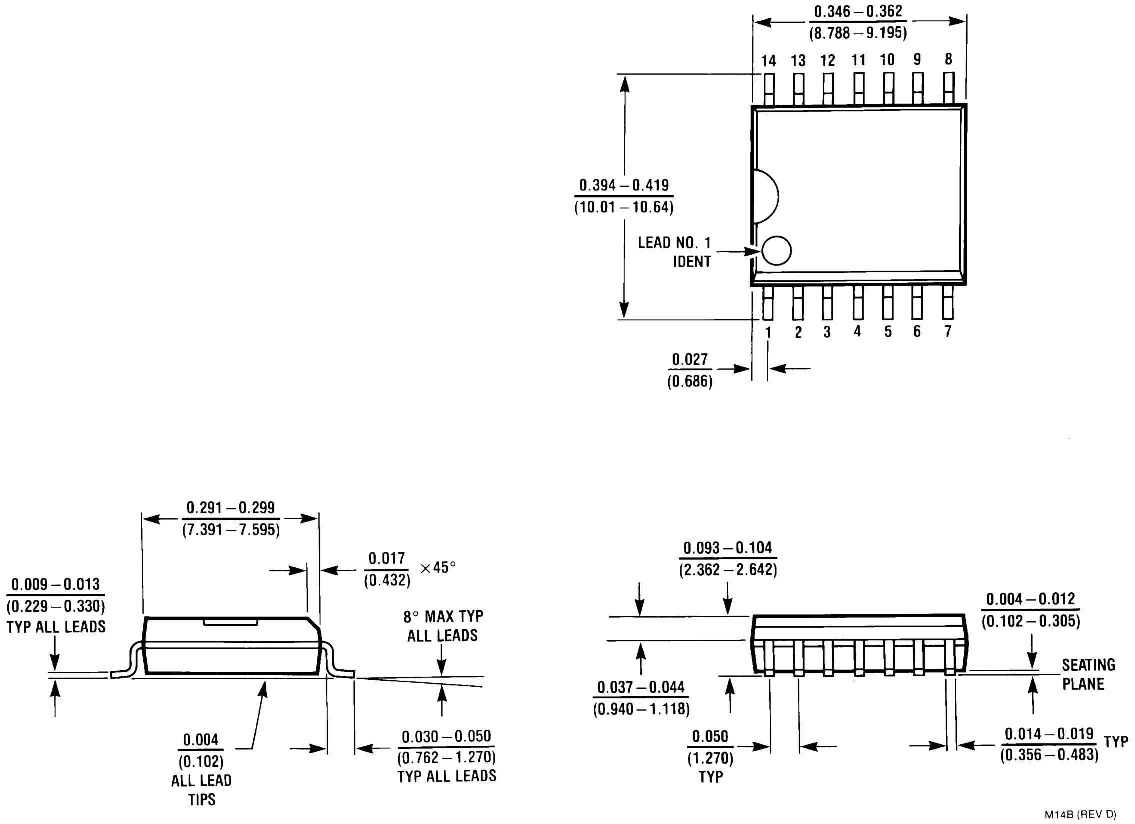
2nd Order Tuneable Bandpass Filter

The CLC522 Variable-Gain Amplifier placed into feedback loops provide signal processing functions such as 2nd order tuneable bandpass filters. The center frequency of the 2nd order bandpass illustrated on the front page is adjusted through the use of the CLC522's gain-control voltage, V_g. The integrators implemented with two CLC420s, provide the coefficients for the transfer function.

Physical Dimensions inches (millimeters) unless otherwise noted

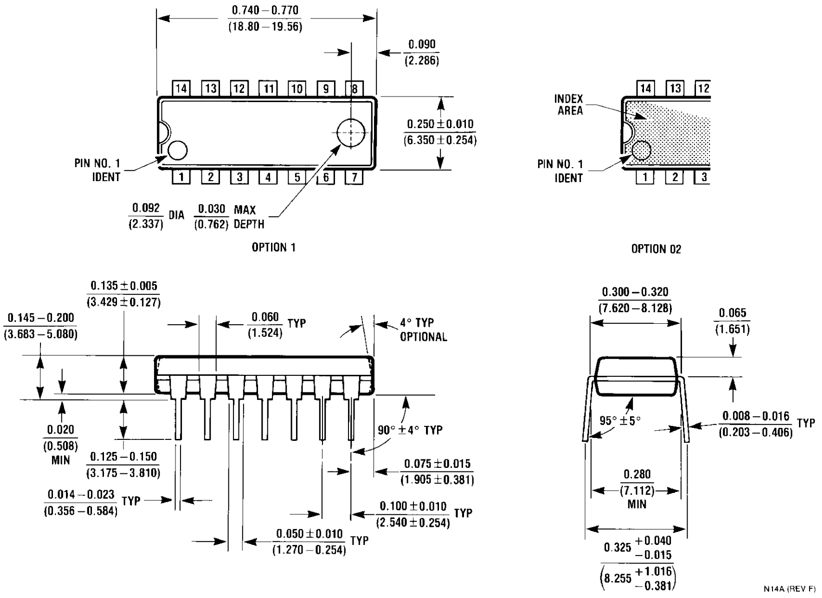


14-Pin SOIC
NS Package Number M14A



14-Pin SOIC
NS Package Number M14B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Pin MDIP
NS Package Number N14A

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National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
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Email: support@nsc.com
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National Semiconductor Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
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National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: ap.support@nsc.com

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