Data Sheet November 2003 FN6058

Dual SPDT CMOS Analog Switch

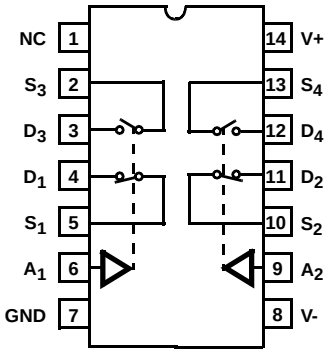
The HI-303/883 switch is a monolithic device fabricated using CMOS technology and the Intersil Dielectric Isolation process. This switch features break-before-make switching, low and nearly constant ON resistance over the full analog signal range, and low power dissipation.

The HI-303/883 is TTL compatible and has a logic “0” condition with an input less than 0.8V and a logic “1” condition with an input greater than 4.0V.

The HI-303/883 is pin-for-pin compatible with the industry standard Siliconix DG303. The device is available in a 14 pin Ceramic DIP. The HI-303/883 operates over the -55°C to +125°C temperature range.

Pinout

HI1-303/883 (CERAMIC DIP)
TOP VIEW



LOGIC	SW1 SW2	SW3 SW4
0	Off	On
1	On	Off

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Analog Signal Range (±15V Supplies). . . . . .±15V
- Low Leakage (+25°C) . . . . . .1nA (Max)
- Low Leakage (+125°C) . . . . . .100nA (Max)
- Low ON Resistance . . . . . 50Ω (Max)
- Charge Injection. . . . . 30pC (Typ)
- TTL Compatible
- System Switch Elements
- Low Operating Power
- Compatible with DG303

Applications

- Sample and Hold, i.e. Low Leakage Switching
- Op Amp Gain Switching, i.e. Low ON Resistance
- Portable, Battery Operated Circuits
- Low Level Switching Circuits
- Dual or Single Supply Systems

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 44V
$\pm V_{SUPPLY}$ to Ground (V+, V-) . . . . . ±22V
Analog Input Voltage, $(+V_S)$. . . . . $+V_{SUPPLY}$ +1.5V
$(-V_S)$ . . . . . $-V_{SUPPLY}$ -1.5V
Digital Input Voltage, $(+V_A)$ . . . . . $+V_{SUPPLY}$ +4V
$(-V_A)$ . . . . . $-V_{SUPPLY}$ -4V
Peak Current (S or D)
(Pulse at 1ms, 10% Duty Cycle Max). 40mA
Continuous Current 30mA
Junction Temperature . . . . . +175°C
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering 10 sec) . . . . . ≤275°C

Thermal Information

Thermal Resistance	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	88	24

Package Power Dissipation at 75°C
Ceramic DIP Package . . . . . 0.85W/°C
Package Power Dissipation Derating Factor above +75°C
Ceramic DIP Package . . . . . 11.36mW/°C

Recommended Operating Conditions

Operating Temperature Range . . . . . -55°C to +125°C
Operating Supply Voltage Range ($\pm V_{SUPPLY}$) . . . . . ±15V
Analog Input Voltage (V_S) . . . . . $\pm V_{SUPPLY}$
Logic Low Level (V_{AL}) . . . . . 0V to 0.8V
Logic High Level (V_{AH}) . . . . . 4.0V to $+V_{SUPPLY}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

TABLE 1. D.C. ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = −15V, GND = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE (°C)	MIN	MAX	UNITS
Switch "ON" Resistance	r_{DS}	V_{A1} = 4.0V, V_D = 10V, I_S = -10mA, V_{A2} = 0.8V, $S_1/S_2/S_3/S_4$	1	25	-	50	Ω
			2, 3	-55 to 125	-	75	Ω
		V_{A1} = 0.8V, V_D = -10V, I_S = 10mA, V_{A2} = 4.0V, $S_1/S_2/S_3/S_4$	1	25	-	50	Ω
			2, 3	-55 to 125	-	75	Ω
Source "OFF" Leakage Current	$I_{S(OFF)}$	V_S = +14V, V_D = -14V, V_{A1} = 0.8V, V_{A2} = 4.0V, $S_1/S_2/S_3/S_4$	1	25	-1	1	nA
			2, 3	-55 to 125	-100	100	nA
		V_S = -14V, V_D = +14V, V_{A1} = 4.0V, V_{A2} = 0.8V, $S_1/S_2/S_3/S_4$	1	25	-1	1	nA
			2, 3	-55 to 125	-100	100	nA
Drain "OFF" Leakage Current	$I_{D(OFF)}$	V_S = +14V, V_D = -14V, V_{A1} = 0.8V, V_{A2} = 4.0V, $S_1/S_2/S_3/S_4$	1	25	-1	1	nA
			2, 3	-55 to 125	-100	100	nA
		V_S = -14V, V_D = +14V, V_{A1} = 4.0V, V_{A2} = 0.8V, $S_1/S_2/S_3/S_4$	1	25	-1	1	nA
			2, 3	-55 to 125	-100	100	nA
Channel "ON" Leakage Current	$I_{D(ON)}$	V_D = V_S = +14V, V_{A1} = 4.0V, V_{A2} = 0.8V, $S_1/S_2/S_3/S_4$	1	25	-1	1	nA
			2, 3	-55 to 125	-100	100	nA
		V_D = V_S = -14V, V_{A1} = 0.8V, V_{A2} = 4.0V, $S_1/S_2/S_3/S_4$	1	25	-1	1	nA
			2, 3	-55 to 125	-100	100	nA
Low Level Input Current	I_{AL}	All Channels V_{AL} = 0.8V	1	25	-1.0	1.0	µA
			2, 3	-55 to 125	-1.0	1.0	µA
High Level Input Current	I_{AH}	All Channels V_{AH} = 4.0V	1	25	-1.0	1.0	µA
			2, 3	-55 to 125	-1.0	1.0	µA
Supply Current	$+I_{CC}$	All Channels V_A = 0.8V	1	25	-	10	µA
			2, 3	-55 to 125	-	100	µA
		V_{A1} = 0V, V_{A2} = 4.0V and V_{A1} = 4.0V, V_{A2} = 0V	1	25	-	0.5	mA
			2, 3	-55 to 125	-	1.0	mA
Supply Current	$-I_{CC}$	All Channels V_A = 0.8V	1	25	-10	-	µA
			2, 3	-55 to 125	-100	-	µA
		V_{A1} = 0V, V_{A2} = 4.0V and V_{A1} = 4.0V, V_{A2} = 0V	1	25	-10	-	µA
			2, 3	-55 to 125	-100	-	µA

TABLE 2. A.C. ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = −15V, GND = 0V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE (^oC)	MIN	MAX	UNITS
Turn “ON” Time	t_{ON}	C_L = 33pF, R_L = 300Ω	9	25	-	300	ns
			10, 11	55 to 125	-	500	ns
Turn “OFF” Time	t_{OFF}	C_L = 33pF, R_L = 300Ω	9	25	-	250	ns
			10, 11	55 to 125	-	450	ns

TABLE 3. ELECTRICAL PERFORMANCE SPECIFICATIONS (NOTE 1)

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = −15V, GND = 0V, Unused Pins are Grounded.

PARAMETERS	SYMBOL	CONDITIONS	NOTE	TEMPERATURE (^oC)	MIN	MAX	UNITS
Switches Input Capacitance	$C_{IS\ (OFF)}$	Measured Source to GND	1	25	-	28	pF
Driver Input Capacitance	C_{C1}	V_A = 0V	1	25	-	10	pF
	C_{C2}	V_A = 15V	1	25	-	10	pF
Switch Output Capacitance	C_{OS}	Measured Drain to GND	1	25	-	28	pF
Off Isolation	V_{ISO}	f = 1MHz, $V_{GEN} = 1V_{P-P}$	1	25	40	-	dB
Cross Talk	V_{CT}	f = 1MHz, $V_{GEN} = 1V_{P-P}$	1	25	40	-	dB
Charge Transfer	V_{CTE}	V_S = GND, C_L + 0.01µF	1	25	-	15	mV

NOTE:

1. Parameters listed in Table 2 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (Tables 1 and 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1 (Note 2), 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

NOTE:

2. PDA applies to Subgroup 1 only.

Test Circuits

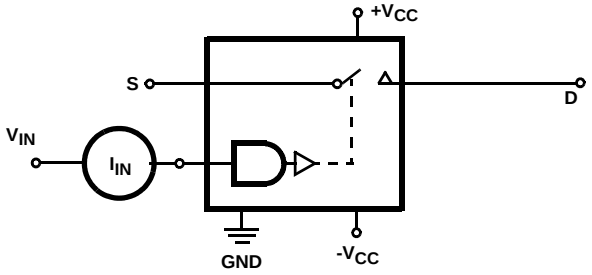


FIGURE 1. INPUT LEAKAGE CURRENT

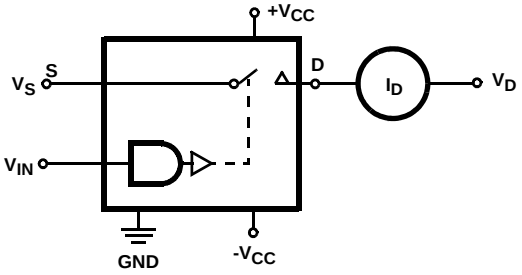


FIGURE 2. $I_{D\ (OFF)}$

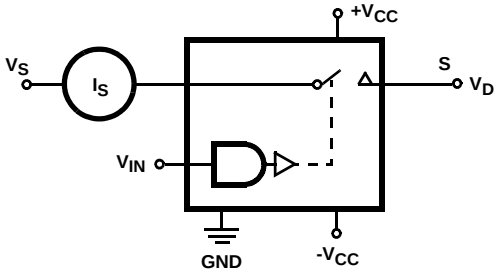


FIGURE 3. $I_{S\ (OFF)}$

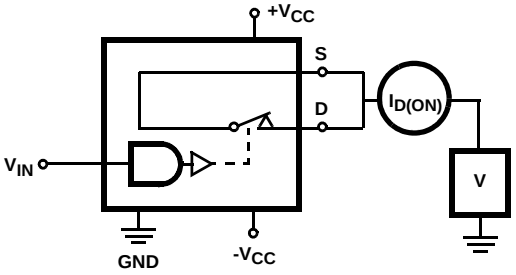


FIGURE 4. $I_{D\ (ON)}$

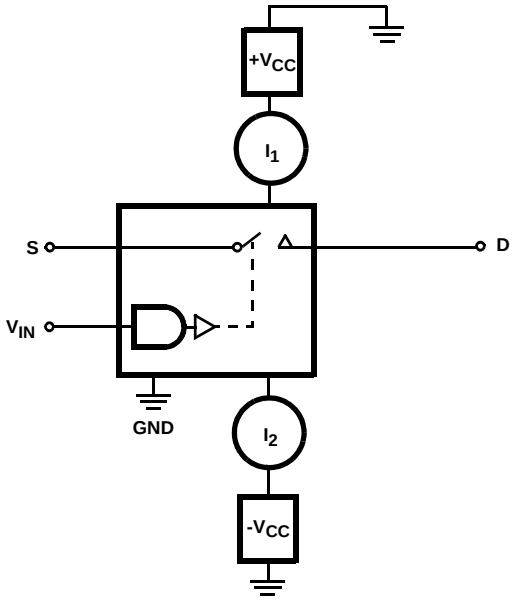
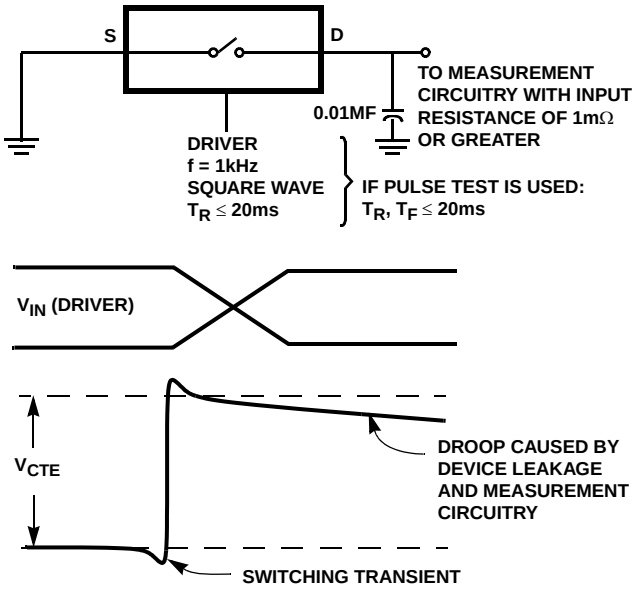


FIGURE 5. SUPPLY CURRENTS



NOTE: V_{CTE} may be a positive or negative value.

FIGURE 6. CHARGE TRANSFER ERROR

Test Circuits (Continued)

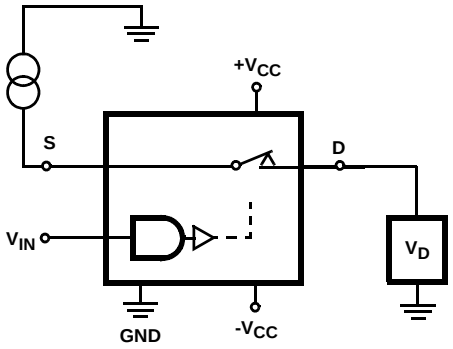


FIGURE 7. R_{DS}

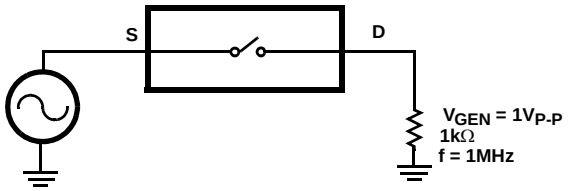


FIGURE 8. OFF CHANNEL ISOLATION

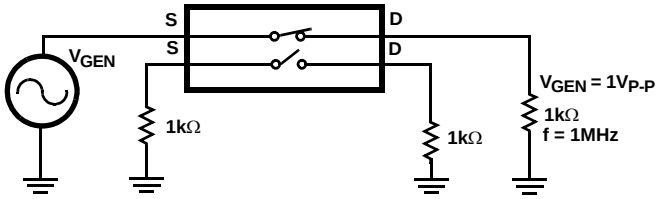


FIGURE 9. CROSSTALK BETWEEN CHANNELS

Test Waveforms

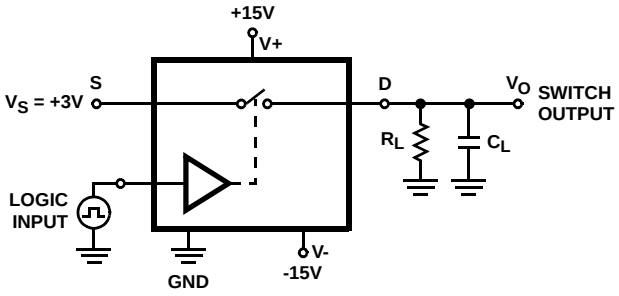


FIGURE 10.

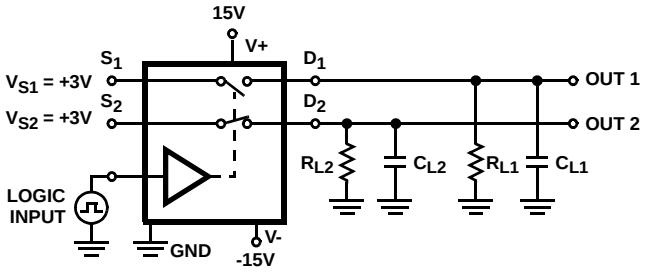


FIGURE 11.

Test Waveforms (Continued)

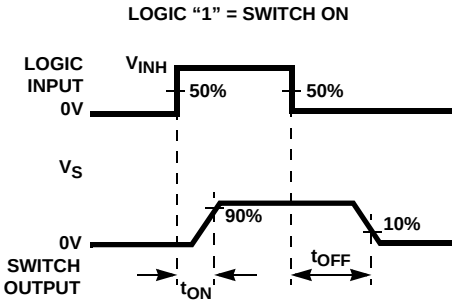


FIGURE 12. MEASUREMENT POINTS

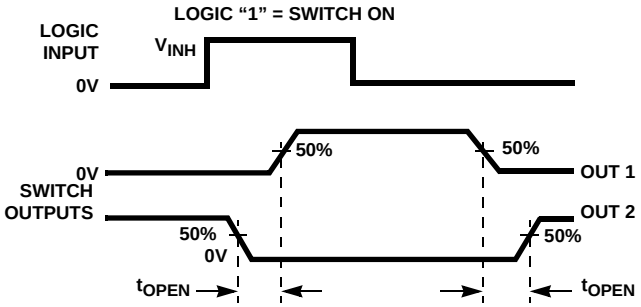
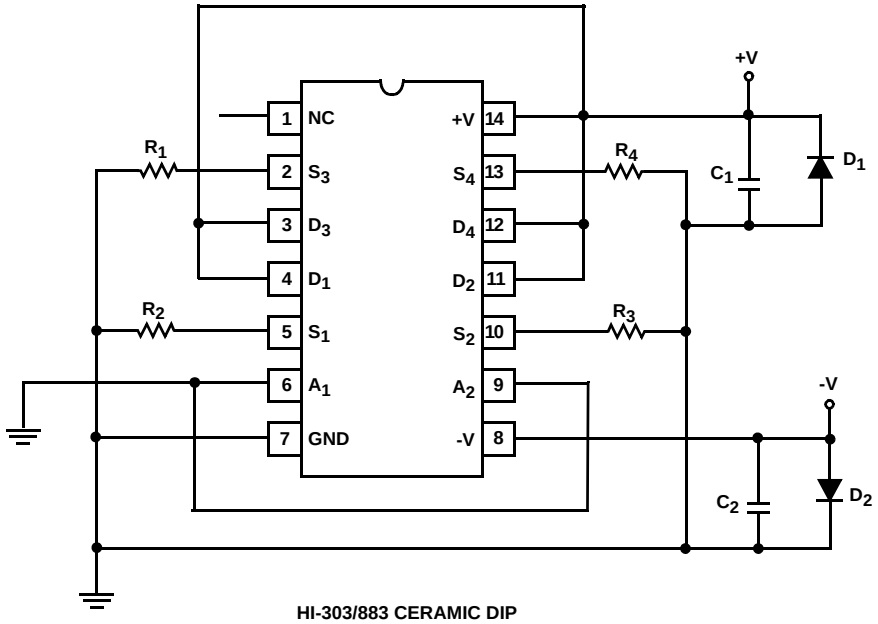


FIGURE 13. TTL LOGIC INPUT

NOTES:

3. $R_L = R_{L1} = R_{L2} = 300\Omega$; $C_L = C_{L1} = C_{L2} = 33pF$
4. $V_{INH} = 4V$
   RISETIME (0.4V to 3.6V) ≤ 20ns
   FALLTIME (3.6V to 0.4V) ≤ 20ns

Burn-In Circuit



HI-303/883 CERAMIC DIP

NOTES:

5. $R_1 = R_2 = R_3 = R_4 = 10k\Omega$, 5%, 1/4 or 1/2W
6. $C_1 = C_2 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
7. $D_1 = D_2$ = IN4002 (per board)
8. |(V+) - (V-)| = 30V

Schematic Diagram

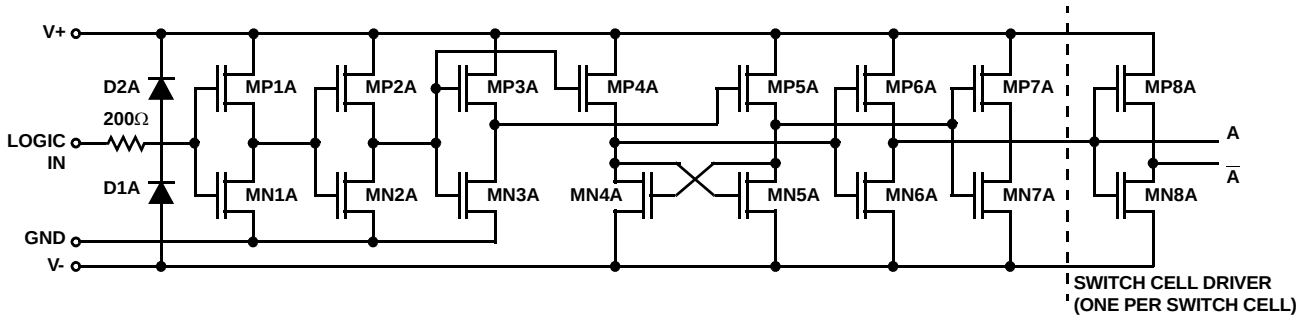


FIGURE 14. DIGITAL INPUT BUFFER AND LEVEL SHIFTER

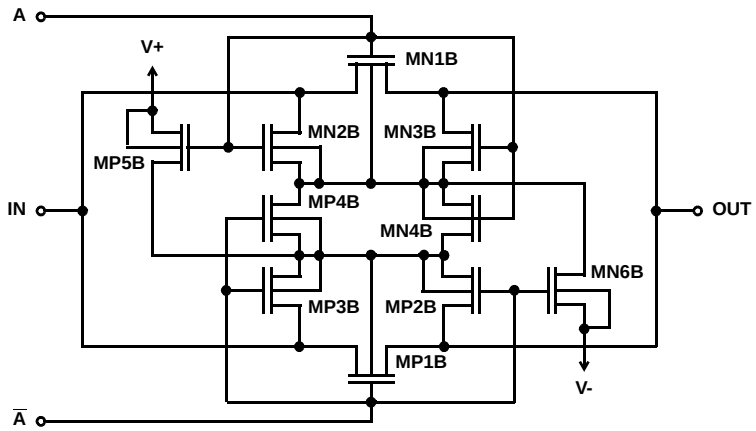


FIGURE 15. SWITCH CELL

Typical Performance Curves $T_A = 25^oC$, V+ = +15V, V- = -15V, Unless Otherwise Specified.

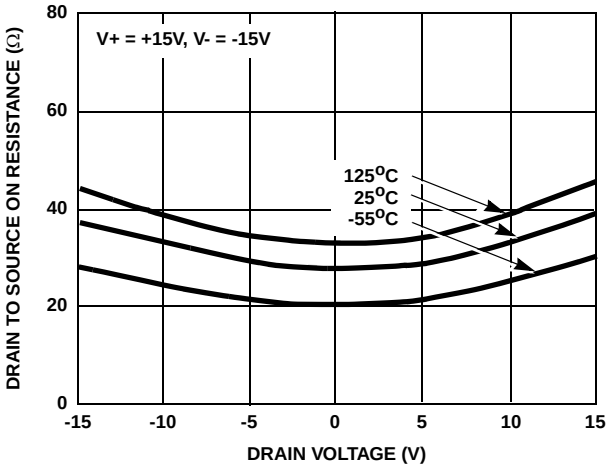


FIGURE 16. $r_{DS(ON)}$ vs V_D AND TEMPERATURE

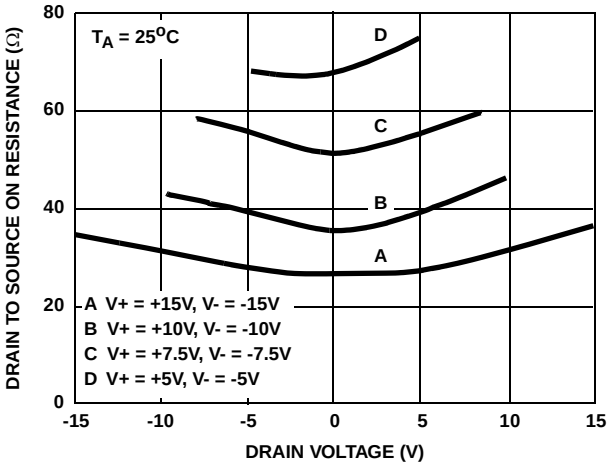


FIGURE 17. $r_{DS(ON)}$ vs V_D AND POWER SUPPLY VOLTAGE

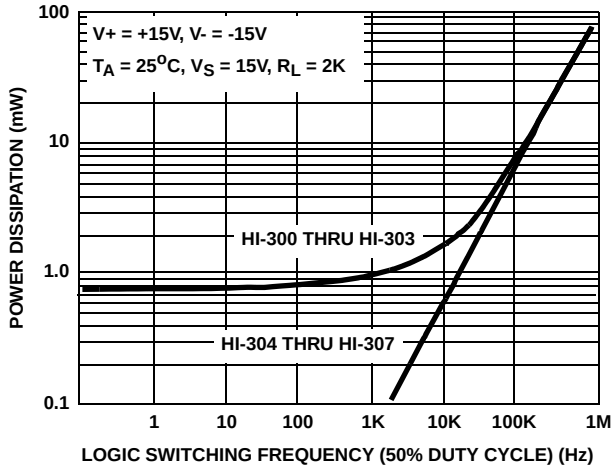


FIGURE 18. DEVICE POWER DISSIPATION vs SWITCHING FREQUENCY (SINGLE LOGIC INPUT)

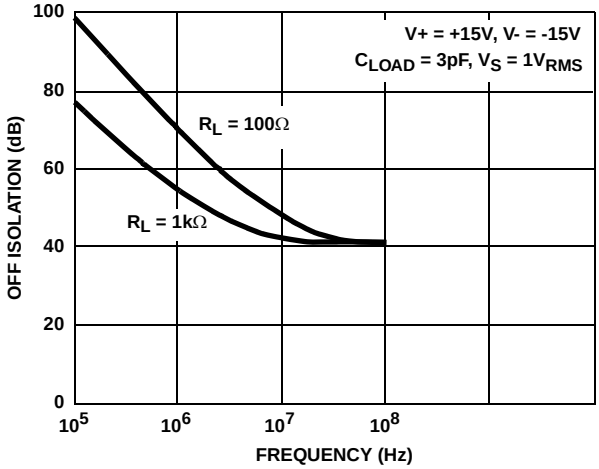


FIGURE 19. OFF ISOLATION vs FREQUENCY

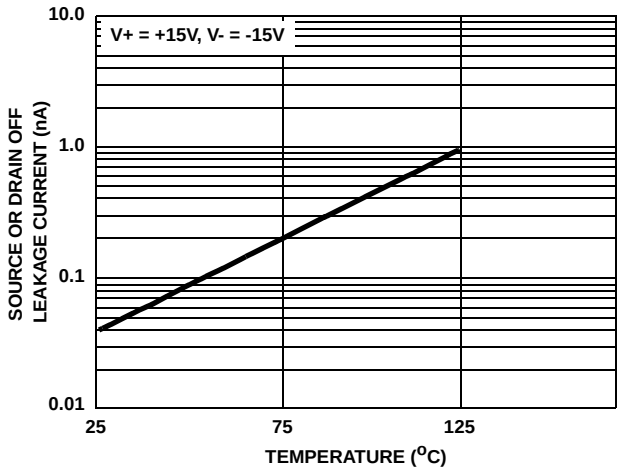


FIGURE 20. $I_{S(OFF)}$ OR $I_{D(OFF)}$ vs TEMPERATURE (Note)

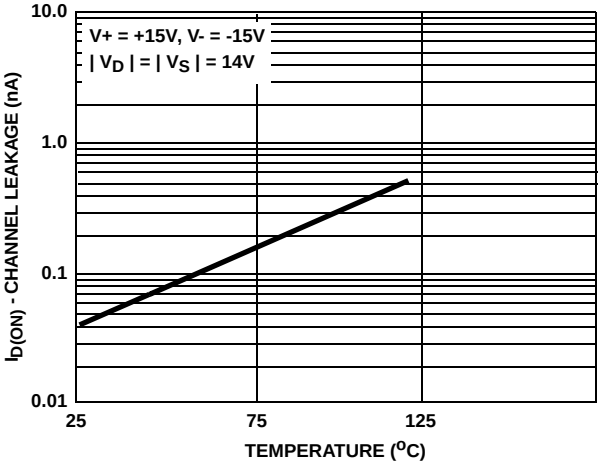


FIGURE 21. $I_{D(ON)}$ vs TEMPERATURE (Note)

NOTE:

The net leakage into the source or drain is the N-Channel leakage minus the P-Channel leakage. This difference can be positive, negative or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

Typical Performance Curves $T_A = 25^oC$, V+ = +15V, V- = -15V, Unless Otherwise Specified. **(Continued)**

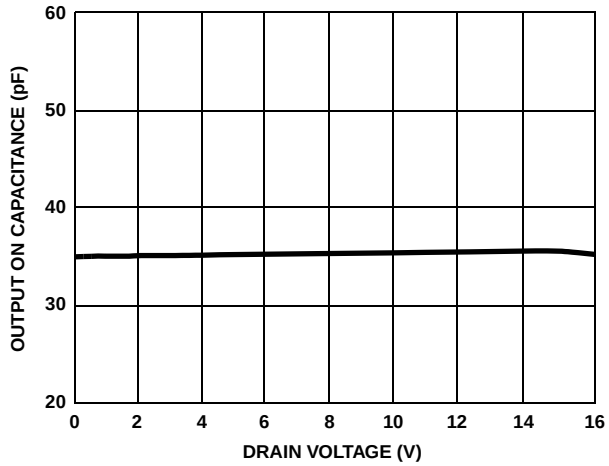


FIGURE 22. OUTPUT ON CAPACITANCE vs DRAIN VOLTAGE

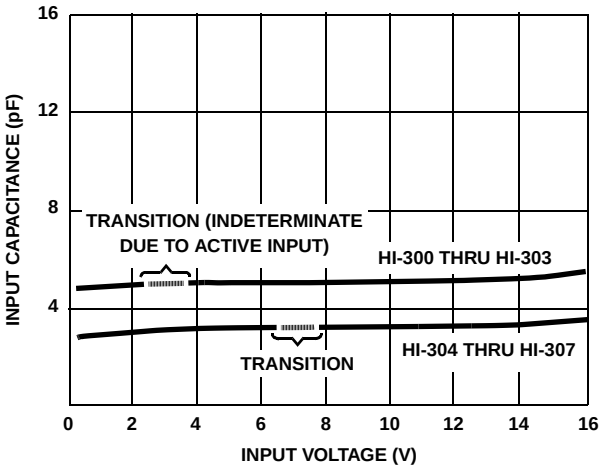


FIGURE 23. DIGITAL INPUT CAPACITANCE vs INPUT VOLTAGE

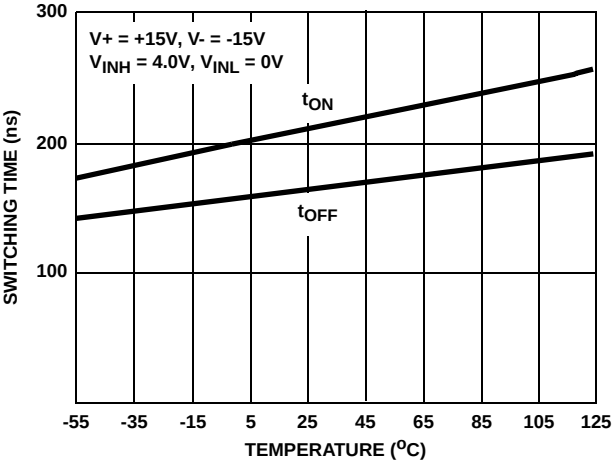


FIGURE 24. SWITCHING TIME vs TEMPERATURE

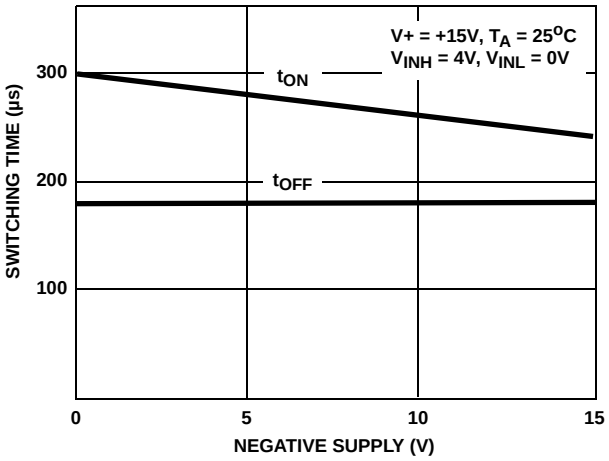


FIGURE 25. SWITCHING TIME vs NEGATIVE SUPPLY VOLTAGE

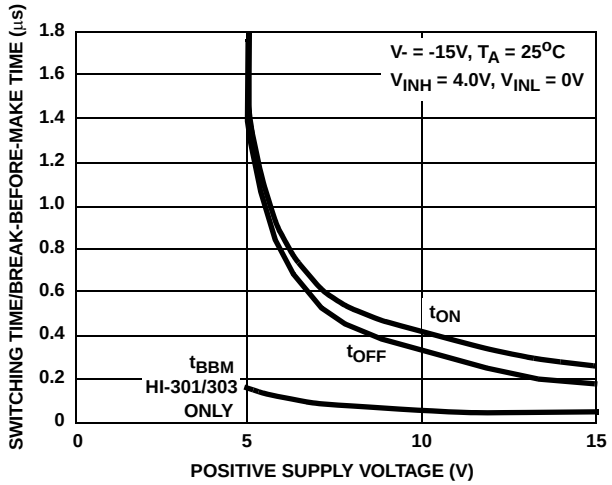


FIGURE 26. SWITCHING TIME AND BREAK-BEFORE-MAKE TIME vs POSITIVE SUPPLY VOLTAGE

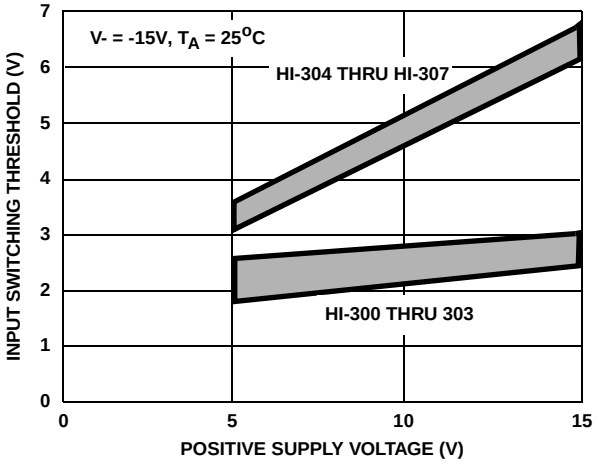


FIGURE 27. INPUT SWITCHING THRESHOLD vs POSITIVE SUPPLY VOLTAGE

Die Characteristics

DIE DIMENSIONS:

76 mils x 83.9 mils x 19 mils

METALLIZATION:

Type: Aluminum
Thickness: 16kÅ ±2kÅ

GLASSIVATION:

Type: Nitride
Thickness: 7kÅ ±0.7kÅ

DIE ATTACH:

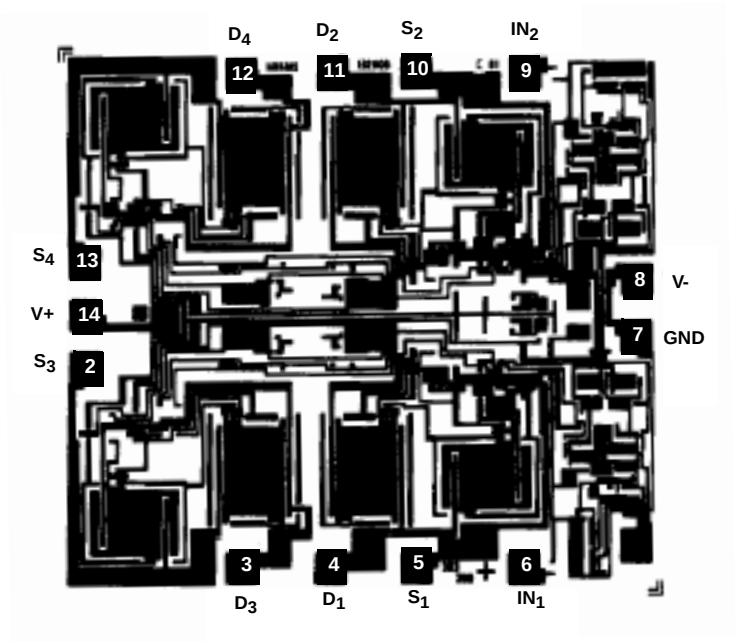
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP - 460°C (Max)

WORST CASE CURRENT DENSITY:

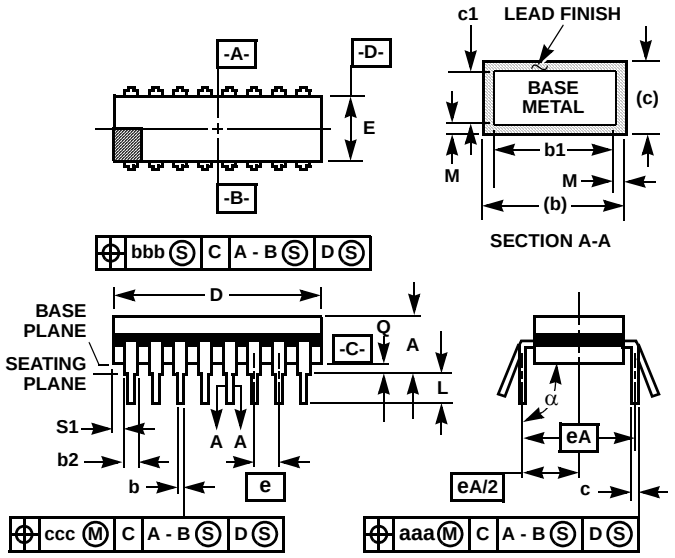
$3.9 \times 10^5 A/cm^2$ at 30mA
This device meets Glassivation Integrity Test requirement per MIL-STD-883 Method 2021 and MIL-M-38510 paragraph 3.5.5.4

Metallization Mask Layout

HI-303/883



Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

9. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
10. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
11. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
12. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
13. This dimension allows for off-center lid, meniscus, and glass overrun.
14. Dimension Q shall be measured from the seating plane to the base plane.
15. Measure dimension S1 at all four corners.
16. N is the maximum number of terminal positions.
17. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
18. Controlling dimension: INCH.

F14.3 MIL-STD-1835 GDIP1-T14 (D-1, CONFIGURATION A)
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SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.785	-	19.94	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	14		14		8

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