intersil

HI7131, HI7133

$3^1/_2$ Digit, Low Power, High CMRR, LCD/LED Display-Type A/D Converters

August 1997

Features

- **120dB CMRR Equal to ±0.01 Count/V of Common Mode Voltage Error**
- **Fast Recovery from Input Overrange Results "Correct First-Reading" After Overload**
- **Guaranteed 0000 Reading for 0V Input**
- **True Polarity at Zero for Precise Null Detection**
- **1pA Input Current (Typ)**
- **True Differential Input and Reference**
- **Single or Dual Supply Operation Capability**
- **Direct LCD Display Drive - HI7131**
- **Direct LED Display Drive - HI7133**
- **Low Noise, 15µV_{P-P} Without Hysteresis or Overrange Hangover**
- **Low Power Dissipation, Guaranteed Less Than 1mW, Results 8000 Hours (Typ) 9V Battery Life**
- **No Additional Active Components Required**

Applications

- **Handheld Instruments**
- **Basic Measurements: Voltage, Current, Resistance Pressure, Temperature, Fluid Flow and Level, pH, Weight, Light Intensity**
- **DMMs and DPMs**

Description

The Intersil HI7131 and HI7133 are $3^1/_2$ digit, A/D converters that have been optimized for superior DC Common Mode Rejection (CMRR) when used with a split ±5V supply or a single 9V battery. The HI7131 contains all the necessary active components on a single IC to directly interface an LCD (Liquid Crystal Display). The supply current is under 100µA and is ideally suited for battery operation. The HI7133 contains all the necessary active components on a single IC to directly interface an LED (Light Emitting Diode).

The HI7131 and HI7133 feature high accuracy performance like, 120dB of CMRR, auto-zero to less than 10µV of offset, fast recovery from over load, zero drift of less than 1µV/^{o}C, input bias current of 10pA maximum, and rollover error of less than one count. A true differential signal and reference inputs are useful features in all systems, but gives the designer an advantage when measuring load cells, strain gauges and other bridge-type transducers.

The HI7131 and HI7133 are supplied in a 40 lead plastic DIP and a 44 lead metric plastic quad flatpack package.

Ordering Information

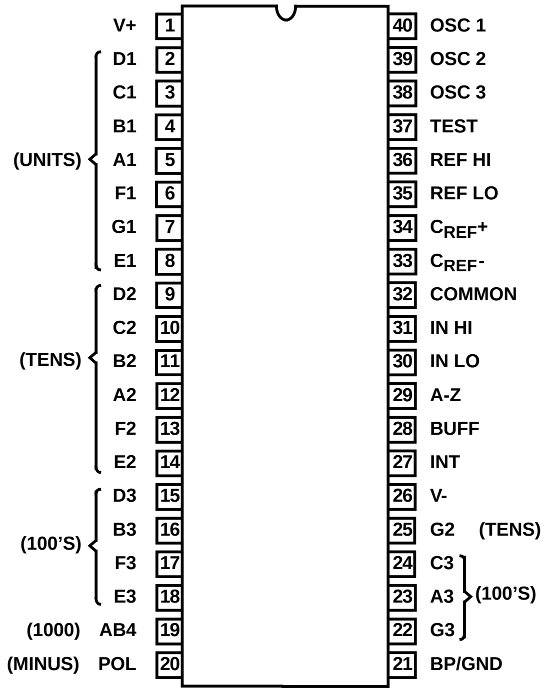
PART NO.	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI7131CPL	0 to 70	40 Ld PDIP	E40.6
HI7131CM44	0 to 70	44 Ld MQFP	Q44.10x10
HI7133CPL	0 to 70	40 Ld PDIP	E40.6
HI7133CM44	0 to 70	44 Ld MQFP	Q44.10x10

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

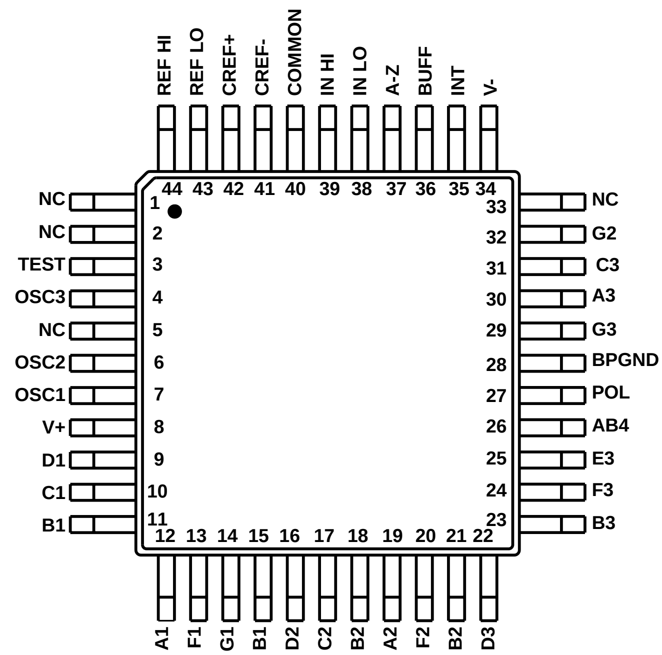
File Number 3373.2

Pinouts

HI7131CPL, HI7133CPL
(PDIP)
TOP VIEW



HI7131CM44, HI7133CM44
(MQFP)
TOP VIEW



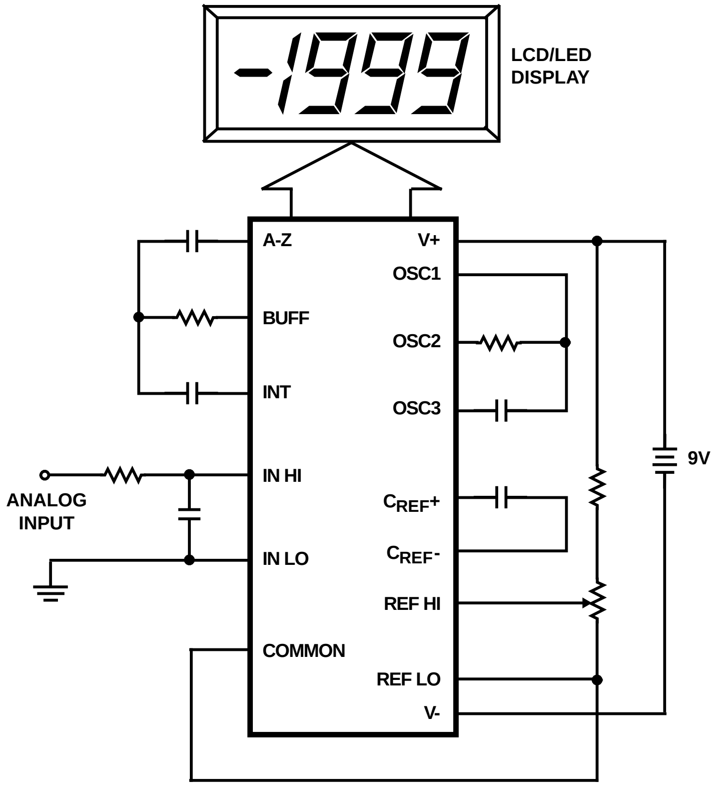
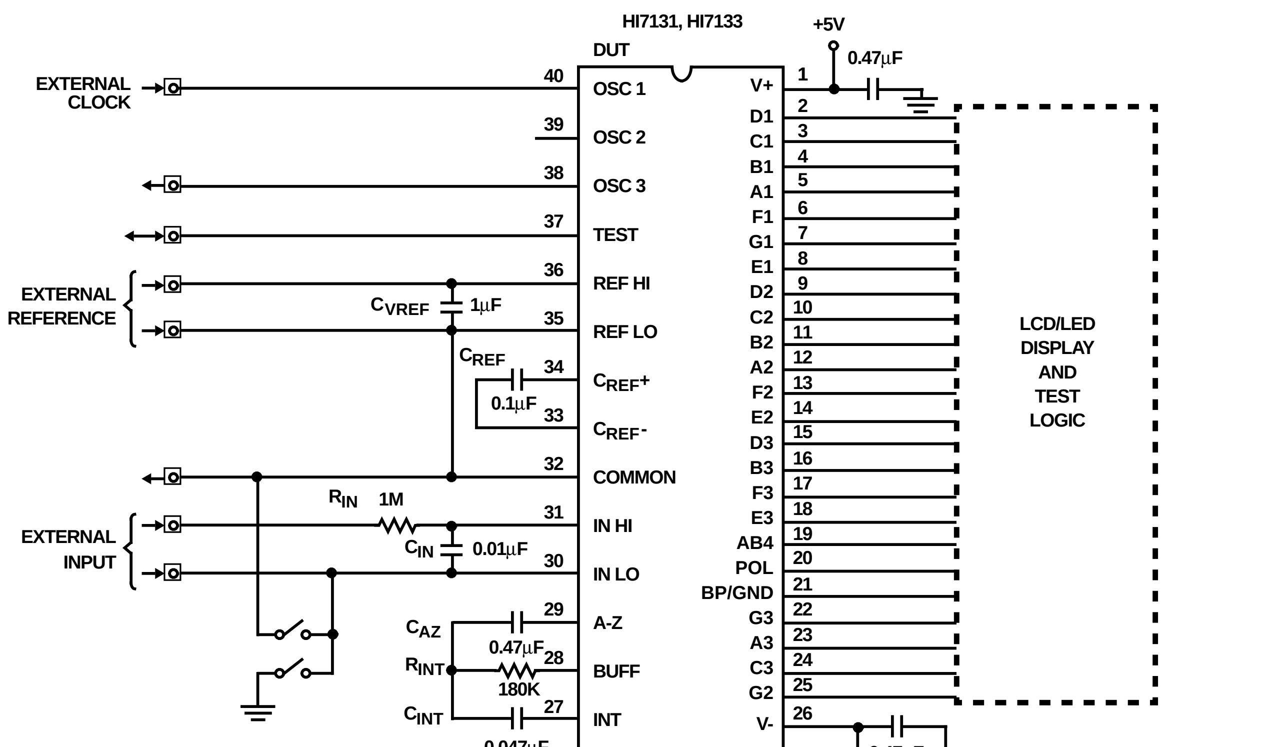


FIGURE 89. TYPICAL APPLICATION CIRCUIT



Critical Components General Specifications:

1. C_{INT}: Low dielectric absorption capacitor, polypropylene or similar
2. C_{AZ}, C_{REF}, C_{IN}: Low leakage capacitors

C_{IN} = 0.01µF C_{AZ} = 0.47µF
C_{REF} = 0.1µF C_{VRH} = 1µF
C_{INT} = 0.047µF R_{IN} = 1MΩ
R_{INT} = 180kΩ

FIGURE 90. TEST CIRCUIT

Absolute Maximum Ratings

Supply Voltage, V+ to V- . . . . +15V
Signal Inputs, Pin# 30, 31 (Note 1). V+ to V-
Reference Inputs, Pin# 35, 36 . . . . V+ to V-
Clock Input, OSC1, Pin# 40 (Note 2) . . . . TEST pin to V+
All Other Analog Leads, Pin# 27-29, 32-34 . . . . V+ to V-
All Other Digital Leads,
Pin# 2-25, 38, 39 (Note 2). . . . . TEST Pin to V^+

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} ($^oC/W$)
PDIP Package	50
MQFP Package	80

Maximum Junction Temperature . . . . 150^{o}C
Maximum Storage Temperature Range . . . . -65^{o}C to 150^{o}C
Maximum Lead Temperature, PDIP Package (Soldering 10s) 300^{o}C
(MQFP - Lead Tips Only)

Operating Conditions

Operating Temperature, T_A. . . . . .0^{o}C to 70^{o}C

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Input voltages may exceed the supply voltages provided the input current is limited to ±100µA.
2. TEST pin is connected to internally generated digital ground through a 500Ω resistor (see text for TEST pin description).
3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

(Notes 5, 6, 7) T_A = 25^{o}C. Device is Tested in the Circuit Shown in Figure 2. Full Scale Range (FSR) = 200.0mV, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY					
Zero Input Reading	V_{IN} = 0V	-000	±000	+000	Reading
Ratiometric Reading	$V_{IN\ HI} = V_{REF\ HI}$, $V_{IN\ LO} = V_{REF\ LO} = V_{COMMON}$ $V_{REF\ HI} - V_{REF\ LO}$ = 100mV	999	999/ 1000	1001	Reading
Rollover Error	V_{IN} = ±199mV	-	±0.2	±1	Count
Linearity Error	FSR = 200mV or 2V (Notes 5, 8)	-	±0.2	±1	Count
Zero Input Reading Drift	V_{IN} = 0V Over Full Temperature Range (Notes 5, 8)	-	±0.2	±1 ±0.01	µV/^{o}C Count/^{o}C
Scale Factor Temperature Coefficient	V_{IN} = 199mV, Over Full Temperature Range, Reference Drift Not Included (Notes 5, 8)	-	±1	±5 ±0.01	ppm/^{o}C Count/^{o}C
Equivalent Input Noise (Peak-To-Peak Value Not Exceeded 95% of the Time)	V_{IN} = 0V (Notes 5, 8)	-	15 0.15	-	µV Count
INPUT					
Common Mode Voltage Sensitivity	V_{CM} = ±1V, V_{IN} = 0V (Notes 5, 6, 8, 9)	-	-	1 0.01	µV/V Count/V
Input Leakage Current	V_{IN} = 0V (Notes 5, 8)	-	1	10	pA
Overload Recovery Period	V_{IN} Changing from ±10V to 0V (Notes 5, 8)	-	-	1	Conversion Cycle
COMMON PIN					
COMMON Pin Voltage (With Respect to V+, i.e., V+ - V_{COMMON})	V+ to V- = 10V	2.4	2.8	3.2	V
COMMON Pin Voltage Temperature Coefficient	V+ to V- = 10V (Notes 5, 8)	-	150	-	ppm/^{o}C
COMMON Pin Sink Current	+0.1V Change on V_{COMMON} (Note 5)	-	3	-	mA
COMMON Pin Source Current	-0.1V Change on V_{COMMON} (Note 5)	-	1	-	µA

Electrical Specifications (Notes 5, 6, 7) $T_A = 25^oC$. Device is Tested in the Circuit Shown in Figure 2. Full Scale Range (FSR) = 200.0mV, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DISPLAY DRIVER (HI7131)					
Peak-To-Peak Segment Drive Voltage	V+ to V- = 10V	4	5	6	V
Peak-To-Peak Backplane Drive Voltage		4	5	6	V
POWER SUPPLY (Nominal Supply Voltage; V+ to V- = 10V)					
Supply Current (Does Not Include COMMON Pin Current)	V_{IN} = 0V (Note 10) Oscillator Frequency = 16kHz	-	70	100	µA
Power Dissipation Capacitance	VS Clock Frequency (Notes 5, 8)	-	40	-	pF
DISPLAY DRIVER (HI7133)					
Segment Sink Current (Except Pins 19 and 20)	V+ = +5.0V Driver Pin Voltage = 3.0V	5	8.5	-	mA
Pin 19 Sink Current		10	16	-	mA
Pin 20 Sink Current		4	7	-	mA
POWER SUPPLY Nominal Supply Voltage; V+ = +5V, V- = -5V, Both Respect to GND Pin					
V+ Supply Current (Note 10)	V_{IN} = 0V Oscillator Frequency = 16kHz Does Not Include COMMON Pin and Display Current	-	70	100	µA
V- Supply Current (Notes 5, 10)		-	40	-	µA
Power Dissipation Capacitance	Versus Clock Frequency (Notes 5, 8)	-	40	-	pF

NOTES:

4. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
5. All typical values have been characterized but not tested.
6. See “Parameters Definition” section.
7. Count is equal to one number change in the least significant digit of the display.
8. Parameter not tested on a production basis, guaranteed by design and/or characterization.
9. See “Differential Input” section.
10. 48kHz oscillator increases current by 20µA (Typ).

Design Information Summary Sheet

- **OSCILLATOR FREQUENCY**

  $f_{OSC} \approx 0.45/RC_{(OSC)}$
  $C_{OSC} \geq 50pF$
  $R_{OSC} > 50k\Omega$
  $C_{OSC} = 50pF$, $R_{OSC} = 180k\Omega$; f_{OSC} (Typ) = 48kHz

- **CLOCK FREQUENCY**

  $f_{CLOCK} = f_{OSC}/4$

- **CLOCK PERIOD**

  $t_{CLOCK} = 1/f_{CLOCK}$

- **CONVERSION CYCLE**

  $T_{CYC} = 4000 \times t_{CLOCK} = 16000 \times t_{OSC}$
  For f_{OSC} = 40kHz; T_{CYC} = 400ms

- **SIGNAL INTEGRATION PERIOD**

  $T_{INT} = 1000 \times t_{CLOCK}$

- **60/50Hz REJECTION CRITERIA**

  T_{INT} / t_{60Hz} or T_{INT} / t_{50Hz} = Integer

- **OPTIMUM FULL SCALE ANALOG INPUT RANGE**

  V_{INFS} = 200mV to 2V

- **INPUTS VOLTAGE RANGE**
  $(V- + 1V) < V_{IN\ LO}$ or $V_{IN\ HI} < (V+ - 1V)$

- **MAXIMUM INTEGRATION CURRENT**

  $I_{INT(MAX)} = V_{INFS} / R_{INT}$
  Maximum integration current should be the maximum buffer output current with no nonlinearity effect.
  Maximum Buffer Output Current = 1µA

- **INTEGRATOR MAXIMUM OUTPUT VOLTAGE SWING**

  $V_{INT(MAX)} = (T_{INT}) (I_{INT(MAX)})/C_{INT}$
  $(V- + 0.5) < V_{INT(MAX)} < (V+ - 0.5)$
  (Typ) $V_{INT(MAX)}$ = 2V

- **INTEGRATING RESISTOR**

  $R_{INT} = V_{INFS} / I_{INT(MAX)}$

- **INTEGRATING CAPACITOR**

  $C_{INT} = (T_{INT}) (I_{INT(MAX)}) / V_{INT(MAX)}$

- **AUTO-ZERO CAPACITOR VALUE**

  REFERENCE CAPACITOR VALUE
  $0.1\mu F < C_{REF} < 1\mu F$

- **REFERENCE INPUTS VOLTAGE RANGE**

  $V- < V_{REFLO}$ or $V_{REFHI} < V+$

- **REFERENCE VOLTAGE**

  $V_{REF} = V_{INFS}/2$

- **COMMON PIN VOLTAGE**

  V_{COMMON} = V+ - 2.8, (Typ), V_{COMMON} is regulated and can be used as a reference. It is biased between V+ and V- and regulation is lost at (V+ -V-) < 6.8V. V_{COMMON} pin does not have sink capability and can be externally pulled down to lower voltages.

- **DISPLAY TYPE**

  LCD, Non-Multiplexed

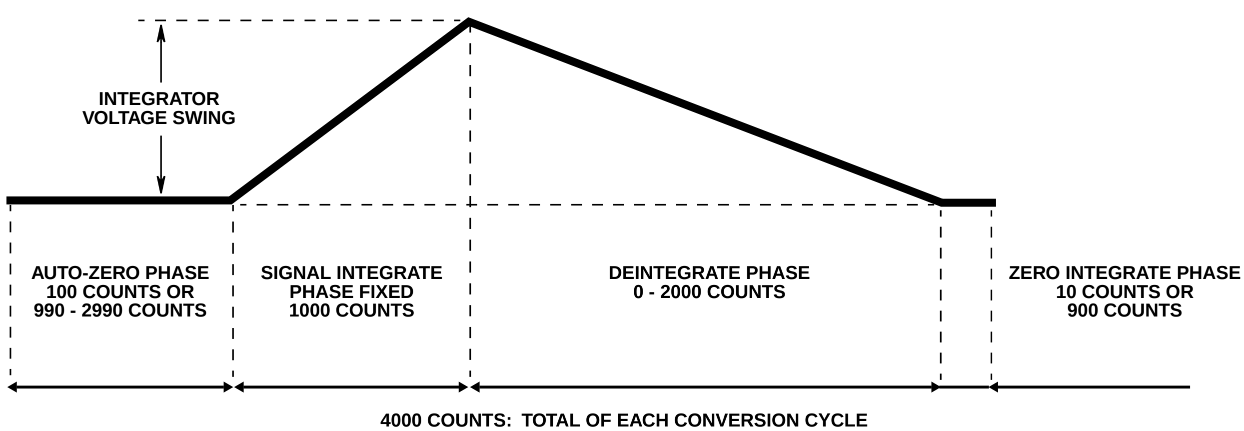
- **POWER SUPPLY, V+ TO V-**

  Single +9V or 5V Nominal, +5V to +12V Functional

- **DISPLAY READING**

  Reading = $1000 \times (V_{IN} / V_{REF})$
  Maximum Reading = 1999, for $V_{IN} = 1.999 \times V_{REF}$

Typical Integrator Amplifier Output Waveform (INT Pin)



NOTE: 1 Count = 1 Clock Cycle = 4 Oscillator Cycles.

Pin Descriptions

PIN NUMBER		NAME	FUNCTION	DESCRIPTION
40 PIN DIP	44 PIN FLATPACK			
1	8	V+	Supply	Power Supply.
2	9	D1	Output	Driver Pin for Segment “D” of the display units digit.
3	10	C1	Output	Driver Pin for Segment “C” of the display units digit.
4	11	B1	Output	Driver Pin for Segment “B” of the display units digit.
5	12	A1	Output	Driver Pin for Segment “A” of the display units digit.
6	13	F1	Output	Driver Pin for Segment “F” of the display units digit.
7	14	G1	Output	Driver Pin for Segment “G” of the display units digit.
8	15	E1	Output	Driver Pin for Segment “E” of the display units digit.
9	16	D2	Output	Driver Pin for Segment “D” of the display tens digit.
10	17	C2	Output	Driver Pin for Segment “C” of the display tens digit.
11	18	B2	Output	Driver Pin for Segment “B” of the display tens digit.
12	19	A2	Output	Driver Pin for Segment “A” of the display tens digit.
13	20	F2	Output	Driver Pin for Segment “F” of the display tens digit.
14	21	E2	Output	Driver Pin for Segment “E” of the display tens digit.
15	22	D3	Output	Driver pin for segment “D” of the display hundreds digit.
16	23	B3	Output	Driver pin for segment “B” of the display hundreds digit.
17	24	F3	Output	Driver pin for segment “F” of the display hundreds digit.
18	25	E3	Output	Driver pin for segment “E” of the display hundreds digit.
19	26	AB4	Output	Driver pin for both “A” and “B” segments of the display thousands digit.
20	27	POL	Output	Driver pin for the negative sign of the display.
21	28	BP/GND	Output	Driver pin for the LCD backplane/Power Supply Ground.
22	29	G3	Output	Driver pin for segment “G” of the display hundreds digit.
23	30	A3	Output	Driver pin for segment “A” of the display hundreds digit.
24	31	C3	Output	Driver pin for segment “C” of the display hundreds digit.
25	32	G2	Output	Driver pin for segment “G” of the display tens digit.
26	34	V-	Supply	Negative power supply.
27	35	INT	Output	Integrator amplifier output. To be connected to integrating capacitor.
28	36	BUFF	Output	Input buffer amplifier output. To be connected to integrating resistor.
29	37	A-Z	Input	Integrator amplifier input. To be connected to auto-zero capacitor.
30 31	38 39	IN LO IN HI	Input	Differential inputs. To be connected to input voltage to be measured. LO and HI designators are for reference and do not imply that LO should be connected to lower potential, e.g., for negative inputs IN LO has a higher potential than IN HI.
32	40	COMMON	Supply/ Output	Internal voltage reference output.
33 34	41 42	C_{REF}- C_{REF}+		Connection pins for reference capacitor.
35 36	43 44	REF LO REF HI	Input	Input pins for reference voltage to the device. REF HI should be positive reference to REF LO.
37	3	TEST	Input	Display test. Turns on all segments when tied to V+.
38 39 40	4 6 7	OSC3 OSC2 OSC1	Output Output Input	Device clock generator circuit connection pins.

Definition of Specifications

Count

A Count is equal to one number change in the least significant digit of the display. The analog size of a count referred to ADC input is:

$$\text{Analog Count Size} = \frac{\text{Full Scale Range}}{\text{Max Reading} + 1},$$

Max reading +1 for a $3^1/_2$ digit display is 2000 (1999+1).

Zero Input Reading

The reading of the ADC display when input voltage is zero and there is no common mode voltage, i.e., the inputs are shorted to COMMON pin.

Ratiometric Reading

The reading of the ADC display when input voltage is equal to reference voltage, i.e., IN HI tied to REF HI and IN LO tied to REF LO and COMMON pins. The accuracy of reference voltage is not important for this test.

Rollover Error

Difference in the absolute value reading of ADC display for equal magnitude but opposite polarity inputs. The input voltage should be close to full scale, which is the worst case condition.

Linearity

Deviation of the ADC transfer function (output reading versus input voltage transfer plot) from the best straight line fitted to ADC transfer plot.

Scale Factor Temperature Coefficient

The rate of change of the slope of ADC transfer function due to the change of temperature.

Equivalent Input Noise

The total random uncertainty of the ADC for converting a fixed input value to an output reading. This uncertainty is referred to input as a noise source which produces the equivalent effect. It is given for zero input and is expressed as Peak-to-Peak noise value and submultiples of Counts.

Overload Recovery Period

A measure of how fast the ADC will display an accurate reading when input changes from an overload condition to a value within the range. This is given as the number of conversion cycles required after the input goes within the range.

Theory of Operation

The HI7131 and HI7133 are dual-slope integrating type A/D converters. As the name implies, its output represents the integral or average of the input signal. A basic block diagram of a dual-slope integrating converter is shown in Figure 3. A conventional conversion cycle has two distinct phases:

First, the input signal is integrated for a fixed interval of time. This is called the signal integration phase. In this phase, the input of the integrator is connected to the input signal through the switch. During this time, charge builds up on C_{INT}, which is proportional to the input voltage.

The next phase is to discharge C_{INT}. This is called reference integration or deintegration phase, with the use of a fixed reference voltage. The time it takes to discharge the C_{INT} is directly proportional to the input signal. This time is converted to a digital readout by means of a BCD counter, driven by a clock oscillator. During this phase, the integrator input is connected to an opposite polarity reference voltage through the switch to discharge C_{INT}.

Notice that during the integration phase, the rate of charge built up on the capacitor is proportional to the level of the input signal, and there is a fixed period of time to integrate the input. However, during the discharge cycle the rate of discharge is fixed and there is a variable time period for complete discharge.

A $3^1/_2$ digit BCD counter is shown in the block diagram, the period of integration is determined by 1000 counts of this counter. Just prior to a measurement, the counter is reset to zero and C_{INT} has no charge. At the beginning of the measurement, the control logic enables the counter and the integrator input is connected to the input node. Charge begins accumulating on C_{INT} and the output of the integrator moves down or up respectively for positive or negative inputs. This process continues until the counter reaches 1000 counts. This will signal the control logic for the start of the deintegrating cycle. The control logic resets the counter and connects the integrator input to a reference voltage opposite to that of the input signal. The charge accumulated on C_{INT} is now starting to be removed and the counter starts to count up again. As soon as all the charge is removed, the output of the integrator reaches 0V. This is detected by the comparator and the control logic is signaled for the end of a measurement cycle. At this time the number accumulated in the counter is the representation of the input signal. This number will be stored on the latches and displayed until the end of the next measurement cycle.

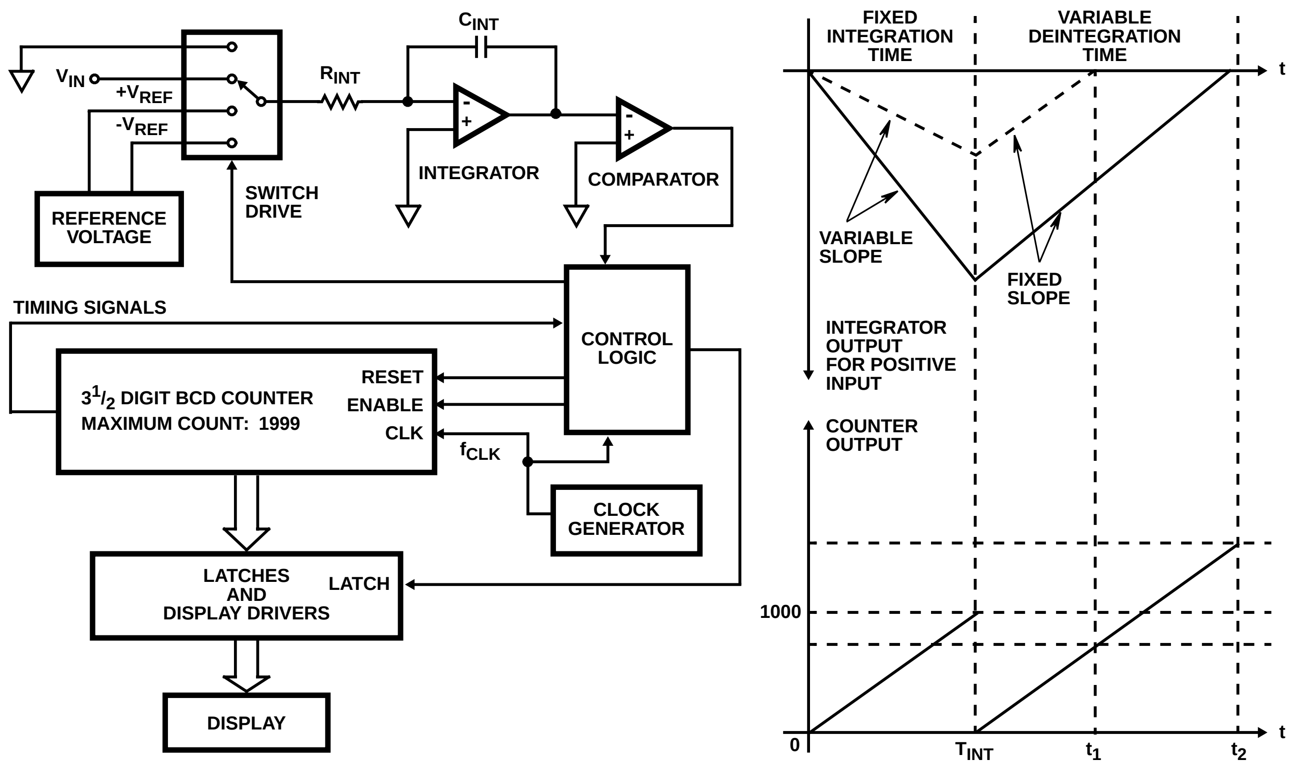


FIGURE 91. DUAL SLOPE INTEGRATING A/D CONVERTER

Figure 3 shows a typical waveform of the integrator output for 2 different positive input values and the associated representation of the counter output for those inputs. T_{INT} is the time period of integrating phase. t_1 and t_2 are the end of measurement for 2 different inputs.

The dual slope integrating technique puts the primary responsibility for accuracy on the reference voltage. The values of R_{INT} and C_{INT} and the clock frequency (f_{CLK}) are not important, provided they are stable during each conversion cycle. This can be expressed mathematically as follows:

$$\Delta V_{INT} = \frac{1}{R_{INT}C_{INT}} \int_0^{T_{INT}} V_{IN} dt = \frac{1}{R_{INT}C_{INT}} \int_0^{T_{DEINT}} V_{REF} dt$$

$$\Delta V_{INT} = \frac{\overline{V_{IN}} T_{INT}}{R_{INT}C_{INT}} = \frac{V_{REF} t_{DEINT}}{R_{INT}C_{INT}}$$

$\overline{V_{IN}}$: Input Average Value During Integration Time

$$T_{INT} = 1000\left(\frac{1}{f_{CLK}}\right)$$

$$t_{DEINT} = \text{Accumulated Counts}\left(\frac{1}{f_{CLK}}\right)$$

$$\text{Accumulated Counts} = 1000\frac{\overline{V_{IN}}}{V_{REF}} = \text{Display Reading}$$

It can be seen that the output reading of the ADC is only proportional to the ratio of V_{IN} over V_{REF}. The last equation also demonstrates that for the maximum display reading (i.e., 1999) we will have V_{IN} = 1.999 V_{REF}. This implies that in this configuration the full scale range of the converter is twice its reference voltage.

The inherent advantages of integrating A/D converters are; very small nonlinearity error, no possibility of missing codes and good high frequency noise rejection.

Furthermore, the integrating converter has extremely high normal mode rejection of frequencies whose periods are an integral multiple of the integrating period (T_{INT}). This feature can be used to reject the line frequency related noises which are riding on input voltage by appropriate selection of clock frequency. This is shown in Figure 4.

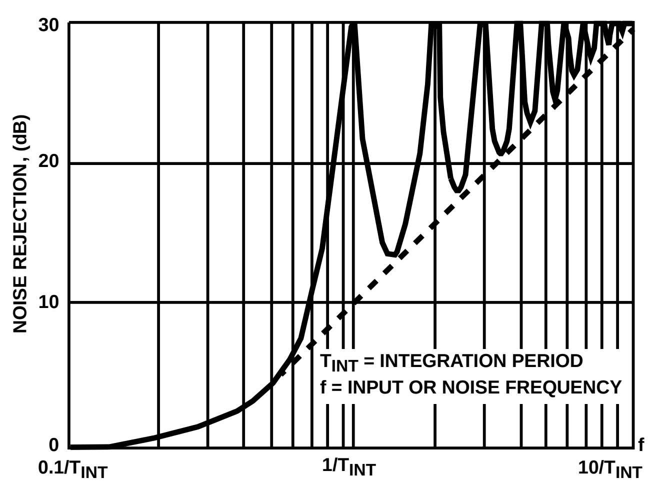


FIGURE 92. NOISE REJECTION FOR INTEGRATING TYPE A/D CONVERTER

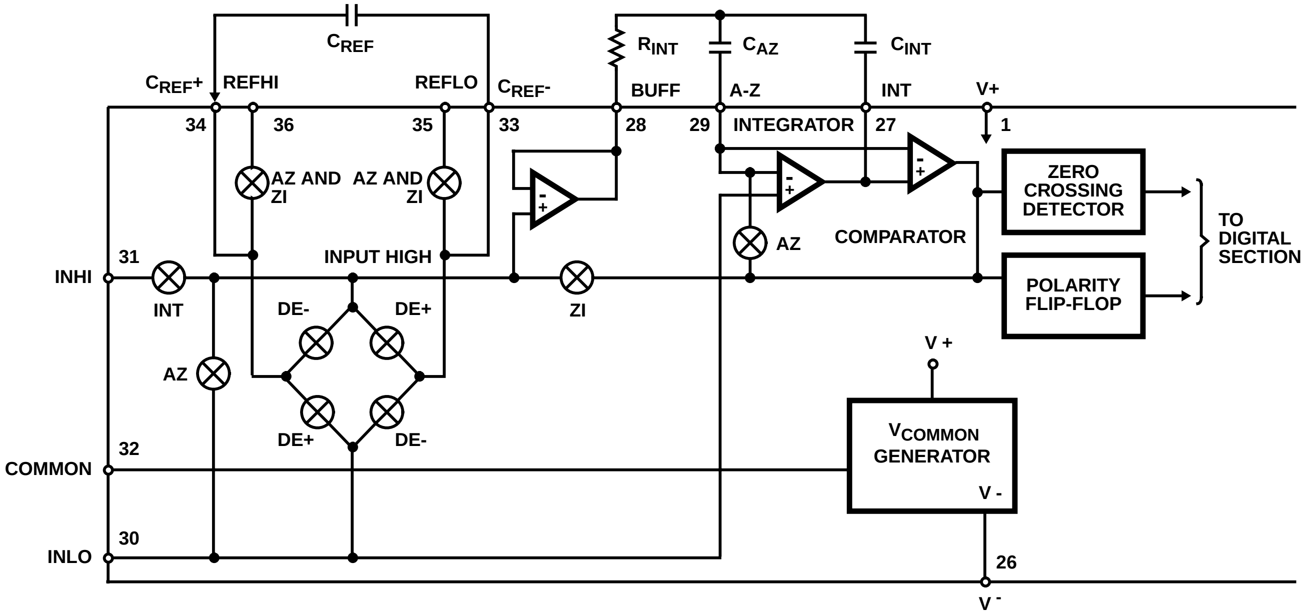


FIGURE 93A. HI7131 AND HI7133 ANALOG SECTION FUNCTIONAL DIAGRAM

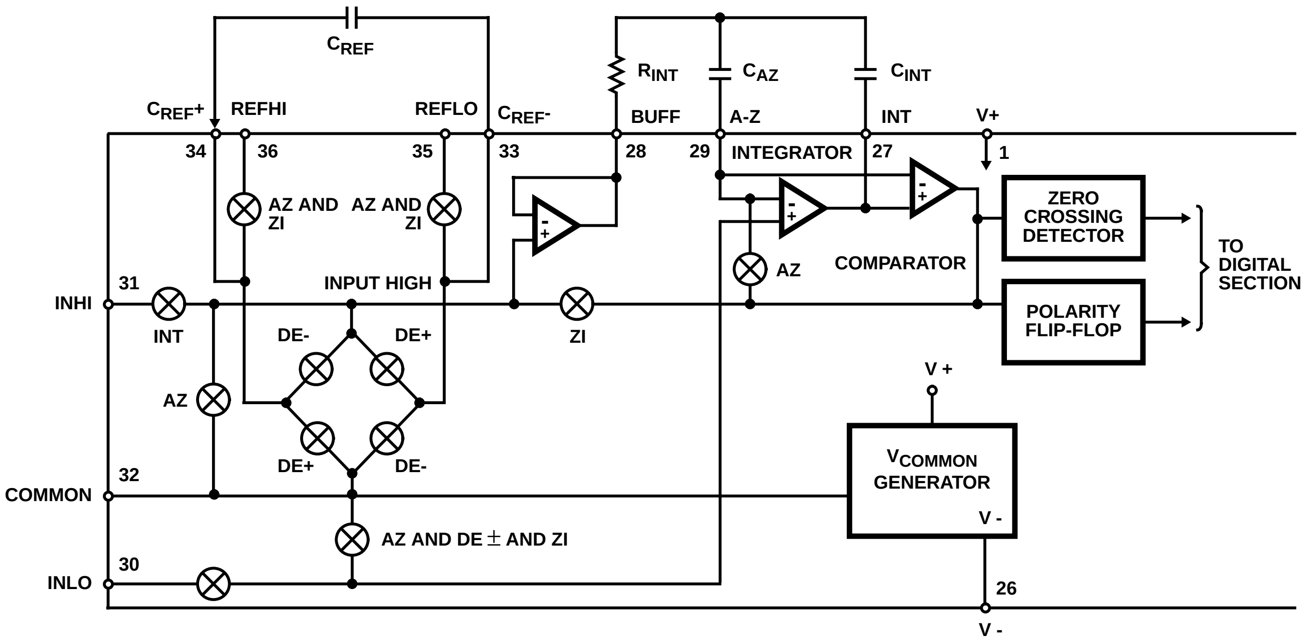


FIGURE 93B. ICL7136 AND ICL7137 ANALOG SECTION FUNCTIONAL DIAGRAM

FIGURE 93. HI7131, HI7133 vs ICL7136, ICL7137 ANALOG SECTIONS

HI7131/33 vs ICL7136/37

Figure 5 shows the analog front end block diagram of both HI7131/33 and ICL7136/37. The difference is the common reference voltage generator connection and 2 extra analog switches in the ICL7136. The HI7131 architecture uses the INLO as the reference point of the integrator (non-inverting input of the integrator amplifier) in all the phases of the conversion cycle. The ICL7136 uses INLO as a reference point only during integration cycle and COMMON pin is used as the integrator reference point during auto-zero, deintegrate, and zero integrate phases.

The circuit configuration of the HI7131 results in a superior 120dB rejection of DC common mode on the inputs. However, the HI7131 has reduced AC common mode noise rejection, since the noise on the INLO input can cause errors during the deintegration phase.

The circuit configuration of the ICL7136 is unaffected by the AC noise riding on the inputs, but the DC common mode rejection on the input is only 86dB.

Analog Section Description

Figure 5A shows a simplified diagram of the analog section of the HI7131 and HI7133. The circuit performs basic phases of dual slope integration. Furthermore, the device incorporates 2 additional phases called “Auto-Zero” and “Zero Integrate”. The device accepts differential input signals and reference voltages. Also, there is a reference voltage generator which sets the COMMON pin 2.8V below the V+ supply. A complete conversion cycle is divided into the following four phases:

1. Auto-Zero (A/Z)
2. Signal Integrate (INT)
3. Deintegrate or Reference Integrate (DE±)
4. Zero Integrate (ZI)

Digitally controlled analog switches direct the appropriate signals for each phase of the conversion.

Auto-Zero Phase

During auto-zero three things occur. First, IN HI is disconnected from the device internal circuitry and internally shorted to IN LO. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} and integrating capacitor C_{INT} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A/Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

Signal Integrate Phase

During signal integrate the auto-zero loop is opened and the internal INPUT HIGH is connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide input common mode range: up to 1V from either supply. At the end of this phase, the polarity of the integrated signal is determined.

Deintegrate Phase

During this phase the IN LO and the internal INPUT HIGH are connected across the previously charged reference capacitor. The bridge type circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. As specified before, the digital reading displayed is:

$$\text{DIGITAL READING} = 1000\left(\frac{V_{INHI} - V_{INLO}}{V_{REFHI} - V_{REFLO}}\right).$$

Zero Integrate Phase

This phase is provided to eliminate overrange hangover and causes fast recovery from heavy overrange. During this phase a feedback loop is closed around the system by connecting comparator output to internal INPUT HIGH. This will discharge the integrator capacitor (C_{INT}), causing the integrator output return to zero. During this phase the reference capacitor is also connected to reference input, charging to the reference voltage.

A typical integrator output voltage during different phases is shown on the “Design Information Summary Sheet.” This integrator output is for negative inputs and is referred to IN LO. For positive inputs the integrator output will go negative.

Digital Section Description

Figure 6 shows the block diagram of the digital section of the HI7131. The diagram shows the clock generator, control logic, counters, latches and display decoder drivers. An internal digital ground is generated from a 6V Zener diode and a large P-Channel source follower. This supply is capable of absorbing the relatively large capacitive currents when the LCD backplane (BP) and segment drivers are switched.

Display Drivers

A typical segment output driver consists of P-Channel and N-Channel MOSFETs.

An LCD consists of a backplane (BP) and segments. BP covers the whole area under the segments. Because of the nature of the LCDs, they should be driven by square waves. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60Hz square-wave with a nominal amplitude of 5V. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments. The polarity indication is “ON” for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

The HI7131 is a direct display drive (versus multiplexed) and each segment in each digit has its own segment driver. The display font and the segment assignment on the display are also shown in Figure 6.

Figure 6 shows the block diagram of the digital section of the HI7133. The diagram shows the clock generator, control logic, counters, latches and display decoder drivers. The supply rails of the digital circuitry are V+ and GND.

Display Drivers

A typical segment output consists of a P-Channel and an N-Channel MOSFET. This configuration is designed to drive common anode LED displays. The nominal sink current for each segment is 8mA, a typical value for instrument size common anode LED displays. The driver for the thousand digit is twice as big as other segments and can sink 16mA since it is actually driving 2 segments. The sink current for the polarity driver is 7mA. The polarity driver is on for negative inputs. The HI7133 is a direct display drive (versus multiplexed) and each segment in each digit has its own segment driver. The display font and the segment assignment on the display are also shown in Figure 7.

Clock Generator

The clock generator circuit basically includes 2 CMOS inverters and a divide-by-4 counter. It is designed to be used in 2 different basic configurations.

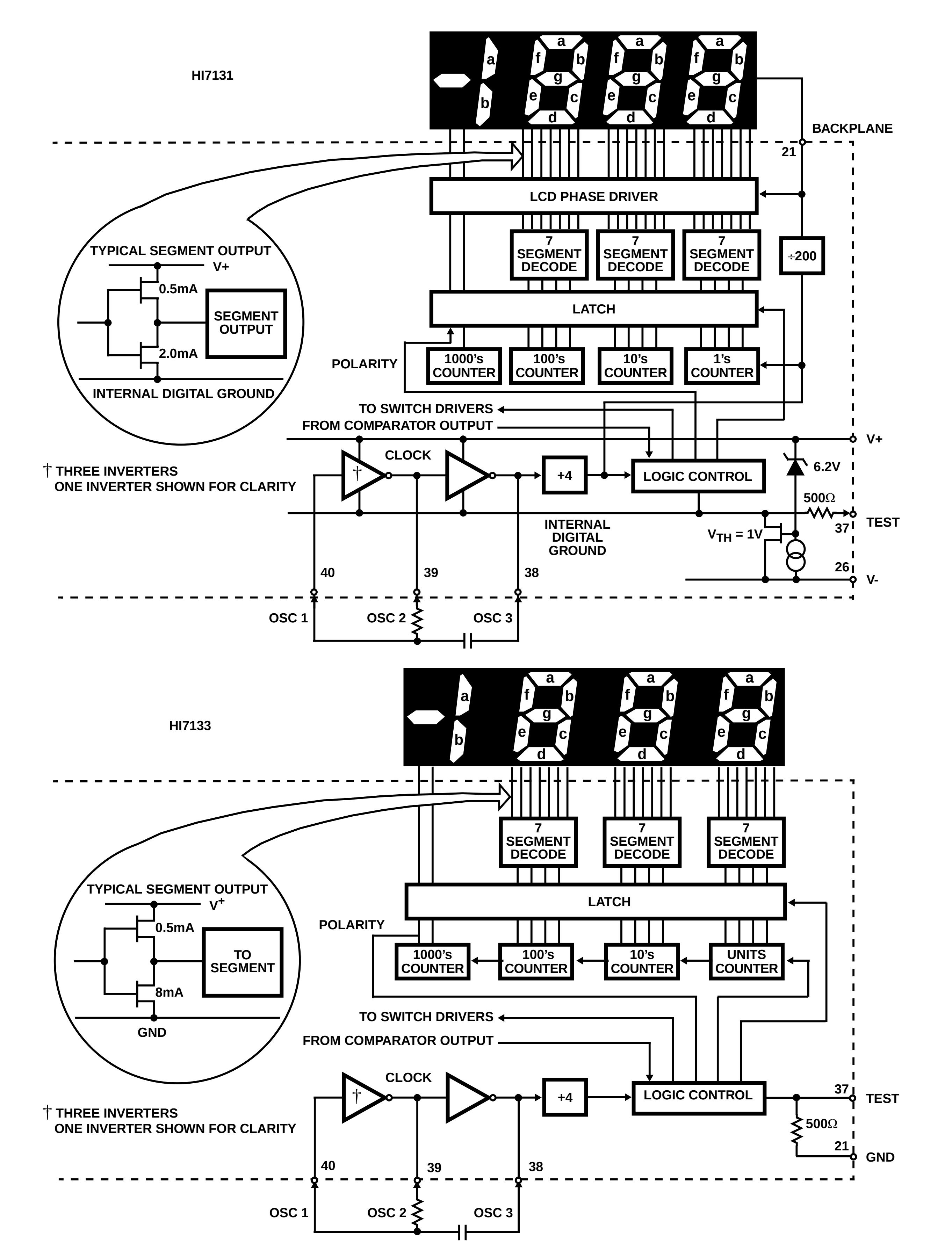


FIGURE 94. DIGITAL SECTION

1. Figure 7A, an External Oscillator Driving OSC 1.
2. Figure 7B, an RC Oscillator Using All 3 Oscillator Circuit Pins.

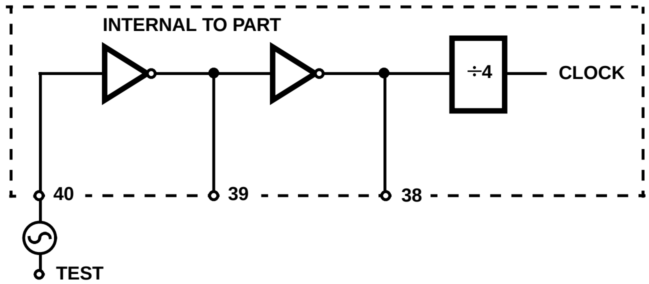


FIGURE 95A. EXTERNAL SIGNAL

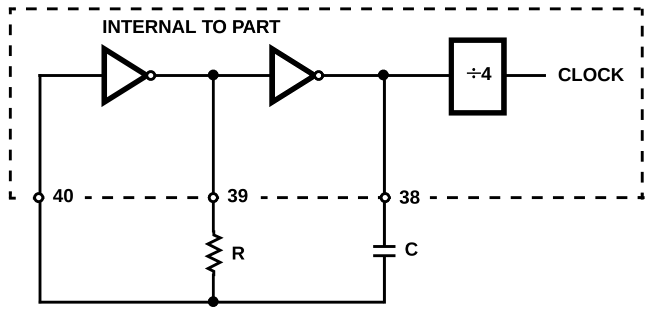


FIGURE 95B. RC OSCILLATOR

FIGURE 95. CLOCK CIRCUITS

The oscillator output frequency is divided by 4 before it clocks the rest of the digital section. Notice that there are 2 separate frequencies which are referred to as; oscillator frequency (f_{OSC}) and clock frequency (f_{CLK}) with the relation of:

$$f_{CLK} = \frac{f_{OSC}}{4}$$

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. For 60Hz, rejection oscillator frequencies of 120kHz, 80kHz, 60kHz, 48kHz, 40kHz, $33^1/_3$kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of, 100kHz, $66^2/_3$kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/sec) will reject both 50Hz and 60Hz (also 400Hz and 440Hz).

For the RC oscillator configuration the relationship between oscillator frequency, R and C values are:

$$f_{OSC} \approx \frac{0.45}{R_{OSC} C_{OSC}}$$

(R in Ohms and C in Farads.)

System Timing

As it has been mentioned, the oscillator output is divided by 4 prior to clocking the digital section and specifically, the internal decade counters. The control logic looks at the counter outputs and comparator output (see analog section) to form the appropriate timing for 4 phases of conversion cycle.

The total length of a conversion cycle is equal to 4000 counts and is independent of the input signal magnitude or full scale range. Each phase of the conversion cycle has the following length:

Auto-Zero Phase

100 counts in case an overrange is detected. 990 to 2990 counts for normal conversion. For those inputs which are less than full scale, the deintegrate length is less than 2000 counts. Those extra counts on deintegrate phase are assigned to auto-zero phase to keep the conversion cycle constant.

Signal Integrate Phase

1000 counts, a fixed period of time. The time of integration can be calculated as:

$$T_{INT} = 1000\left(\frac{1}{f_{CLK}}\right) = 4000\left(\frac{1}{f_{OSC}}\right).$$

Deintegrate Phase

0 to 2000 counts, variable length phase depending on the input voltage.

Zero Integrate Phase

10 counts in case of normal conversion. 900 counts in case an overrange is detected.

Functional Considerations of Device Pins

COMMON Pin

The COMMON pin is the device internal reference generator output.

The COMMON pin sets a voltage that is about 2.8V less than the V+ supply rail. This voltage (V+ - V_{COMMON}) is the on-chip reference which can be used for setting converter reference voltage.

Within the IC, the COMMON pin is tied to an N-Channel transistor capable of sinking up to 3mA of current and still keeping COMMON voltage within the range. However, there is only 1µA of source current capability. The COMMON pin can be used as a virtual ground in single supply applications when the external analog signals need a reference point in between the supply rails. If higher sink and source current capability is needed for virtual ground a unity gain op-amp can be used as a buffer.

Differential Inputs (IN LO, IN HI)

The input can accept differential voltages anywhere within the common mode range of the input amplifier, or specifically from 1V below the positive supply to 1V above the negative supply. In this range, the system has a CMRR of 120dB (Typ). However, care must be exercised to assure the integrator output does not saturate. This is illustrated in Figure 8, which shows how common mode voltage affects maximum swing on the integrator output. Figure 8 shows the circuit configuration during conversion. In this figure, common mode voltage is considered as a voltage on the IN LO pin referenced to (V+ - V-) / 2, which is usually the GND in a dual supply system.

A worst case condition would be a large positive common-mode voltage with a near full scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator output swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing to within 0.3V of either supply without loss of linearity.

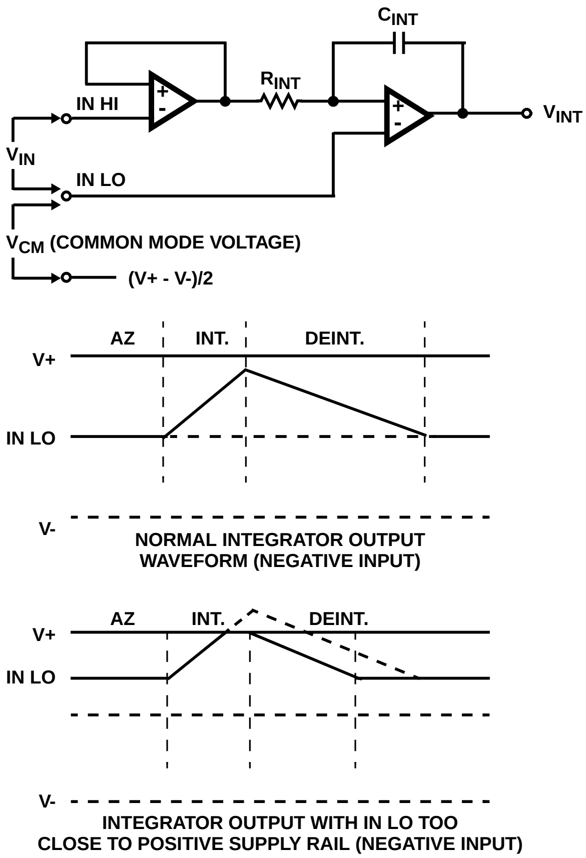


FIGURE 96. COMMON MODE VOLTAGE CONSIDERATION

Differential Reference (REF HI, REF LO) and Reference Capacitor Pins (C_{REF}+, C_{REF}-)

As was discussed in the analog section (Figure 5), the differential reference pins are connected across the reference capacitor (connected to pins C_{REF}+ and C_{REF}-) to charge it during the zero integrate and the auto-zero phase. Then the reference capacitor is used as either a positive or negative reference during the deintegrate phase. The reference capacitor acts as a flying capacitor between the reference voltage and integrator inputs in the deintegrate phase.

The common mode voltage range for the reference inputs is V+ to V-. The reference voltage can be generated anywhere within the power supply range of the converter. The main source of rollover error is reference common mode voltage caused by the reference capacitor losing or gaining charge to or from stray capacitance on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called upon to deintegrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This change in reference for positive or negative input voltage will give a rollover error. However, by selecting the reference capacitor such that it is large enough in comparison to the stray capacitances, this error can be held to less than 0.5 counts worst case. See the "Component Value Selection" section for auto-zero capacitor value.

TEST Pin

The TEST pin serves two functions. It is coupled to the internally generated digital ground through an effective 500Ω resistor. Thus, it can be used as the digital ground for external digital circuits such as segment drivers for decimal points or any other annunciator the user may want to include on the LCD display. For these applications the external digital circuit should be supplied between V+ and TEST pin. Figures 9 and 10 show such an application. In Figure 9 a MOSFET transistor is used to invert the BP signal to drive the decimal point. The MOSFET can be any general purpose type with a threshold voltage less than 3.5V and ON resistance less than 500Ω. Figure 10 uses an CMOS IC XOR gate to generate controllable decimal point drives. No more than a 1mA load should be applied to TEST pin by any external digital circuitry.

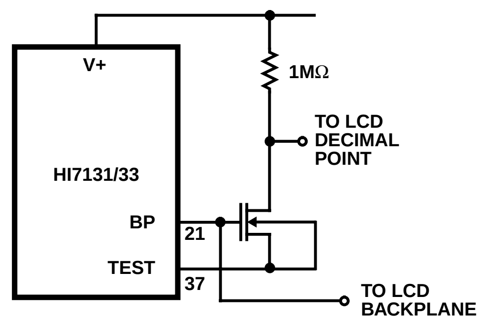


FIGURE 97. SIMPLE INVERTER FOR FIXED DECIMAL POINT DRIVE

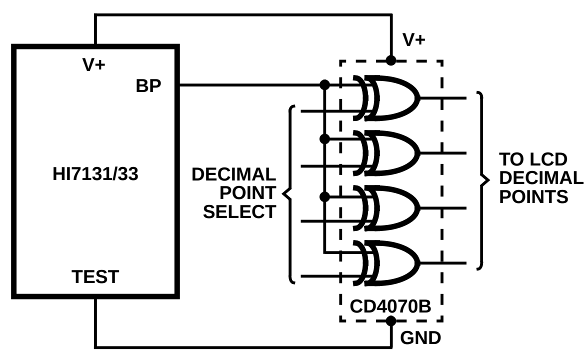


FIGURE 98. EXCLUSIVE "OR" GATE FOR DECIMAL POINTS AND ANNUNCIATORS DRIVE

The second function of the TEST pin is the "lamp test". When the TEST pin is pulled high (to V+) all segments will be turned on and the display should read -1888. The test pin will sink about 10mA under these conditions.

CAUTION: In the lamp test mode, the segments have a constant DC voltage (no square-wave). This may burn the LCD display if maintained for extended periods.

Component Selection

Integrating resistors and capacitors (R_{INT}, C_{INT}): A guideline to achieving the best performance from an integrating A/D converter is to try to reduce the value of R_{INT}, increase the value of C_{INT}, while having the highest possible voltage swing at the output of the integrator. This will reduce the sensitivity of the circuit to noise and leakage currents. In addition to these guidelines the circuit limitations should also be considered.

To determine R_{INT}, the imposed circuit limitation is the maximum output drive current of the buffer amplifier (see Figure 5) while maintaining its linearity. This current for the buffer amplifier is about 1µA. The R_{INT} resistor can be calculated from the expression:

$$R_{INT} = \frac{V_{IN}(\text{Full Scale})}{1\mu A}$$

The standard optimum values for R_{INT} are 180kΩ for 200mV full scale and 1.8MΩ for 2V full scale. Type of resistor and its absolute value is not critical to the accuracy of conversion, as was discussed previously.

The integrating capacitor should be selected to yield the maximum allowable voltage range to the integrator output (INT pin). The maximum allowable range does not saturate the integrator output. The integrator output can swing up or down to 0.3V from either supply rail and still maintain its linearity.

A nominal ±2V maximum range is optimum. The maximum range values are selected in order to leave enough room for all the component and circuit tolerances and for a reasonable common mode voltage range. The C_{INT} value can now be calculated as:

$$C_{INT} = \frac{T_{INT} I_{INT}}{V_{INTMAX}},$$

Where T_{INT} depends on clock frequency and was discussed before and I_{INT} is expressed as:

$$I_{INT} = \frac{V_{IN}(\text{Full Scale})}{R_{INT}}.$$

For 48kHz nominal oscillator frequency (12kHz clock internal frequency), R_{INT} equals 180kΩ for 1.8MΩ for the above mentioned swing, the optimum value for C_{INT} is 0.047µF.

An additional requirement of the integrating capacitor is to choose low dielectric absorption. This will minimize the converter's rollover, linearity and gain error. Furthermore, the integrating capacitor should also have low leakage current. Different types of capacitors are adequate for this application; polypropylene capacitors provide undetectable errors at reasonable cost and size. The absolute value of C_{INT} does not have any effect on accuracy.

Auto-Zero Capacitor (C_{AZ})

The value of the auto-zero capacitor has some influence on the noise of the converter. A larger value C_{AZ} has less sensitivity to noise. For 200mV full scale (resolution of 100µV), where noise is important, a 0.47µF or greater is recommended. On the 2V full scale, (resolution of 1mV), a 0.047µF capacitor is adequate for low noise.

The auto-zero capacitor should be a low leakage type to hold the voltage during conversion cycle. A mylar or polypropylene capacitor is recommended for C_{AZ}.

Reference Capacitor (C_{REF})

As discussed earlier, the input to the integrator during the deintegrate phase is the voltage at the reference capacitor. The sources of error related to the reference capacitor are stray capacitances at the C_{REF} terminals, and the leakage currents. Where a large common mode voltage exists for V_{REF}, the stray capacitances increase the rollover error by absorbing or pumping charge onto C_{REF} when positive or negative inputs are measured. Leakage of the capacitor itself or leakages through circuit boards will drop the voltage across C_{REF} and cause gain and rollover errors. The circuit boards should be designed to minimize stray capacitances and should be well cleaned to reduce leakage currents.

A 0.1µF capacitor for C_{REF} should work properly for most applications. When common mode voltage exists or at higher temperatures (where device leakage currents increase) a 1.0µF reference capacitor is recommended to reduce errors. The C_{REF} capacitor can be any low leakage type, a mylar capacitor is adequate.

Those applications which have variable reference voltage should also use a low dielectric absorption capacitor such as polypropylene, for example, a ratiometric measurement of resistance.

Oscillator Components

When an RC type of oscillator is desired, the oscillator frequency is approximately expressed by:

$$f_{OSC} = \frac{0.45}{RC},$$

(R in Ohms and C in Farads), where R > 50kΩ and C > 50pF. For 40kHz frequency which gives 2.5 readings per second, use 100K and 100pF or use 180kΩ and 50pF for lower power loss.

There is a typical variation of about 5% between oscillator frequencies of different parts. The oscillator frequency will decrease 1% for each 25°C rise. For those applications in which normal mode rejection of 60Hz or 50Hz line frequency is critical, a crystal or a precision external oscillator should be used.

Reference Voltage Selection

For a full scale reading the input signal is required to be twice the reference voltage. To be more precise, the full scale reading (±1999) takes place when the input is 1.999 times the V_{REF}. V_{REF} is the potential difference between REF HI and REF LO inputs. Thus, for the nominal 200mV and 2V ranges, V_{REF} should be 100mV and 1V respectively.

In many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0mV, the designer should use the input voltage directly and adjust the V_{REF} for 0.341V. Suitable values for integrating resistor and capacitor would be 620kΩ and 0.047μF. This makes the system slightly quieter and also avoids a divider network on the input.

The on-chip voltage reference (V+ - V_{COMMON}) is normally used to provide the converter reference voltage. However, some applications may desire to use an external reference generator. Various possible schemes exist for reference voltage settings. Figure 11 shows the normal way of using on-chip reference and also a way of using external reference. The value of resistors on both circuit depends on the converter input voltage range. Refer to "Typical Applications" section for various schemes.

Typical Applications

The HI7131 and HI7133 A/D Converters may be used in a wide variety of configurations. The following application circuits show some of the possibilities, and serves to illustrate the exceptional versatility of these devices.

The following application notes contain very useful information on understanding and applying these parts and are available from Intersil Corporation.

Application Notes

NOTE #	DESCRIPTION	AnswerFAX DOC. #
AN016	"Selecting A/D Converters"	9016
AN017	"The Integrating A/D Converter"	9017
AN018	"Do's and Don'ts of Applying A/D Converters"	9018
AN032	"Understanding the Auto-Zero and Common Mode Performance of the ICL7136/7/9 Family"	9032
AN052	"Tips for Using Single Chip $3^1/_2$ Digit A/D Converters"	9052

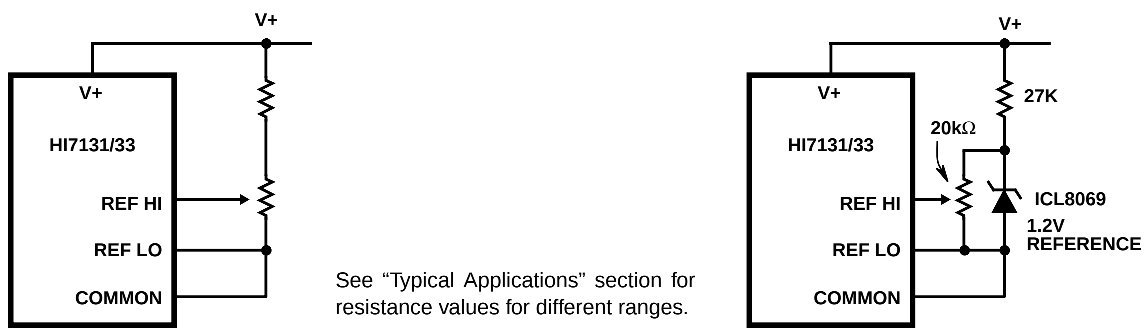
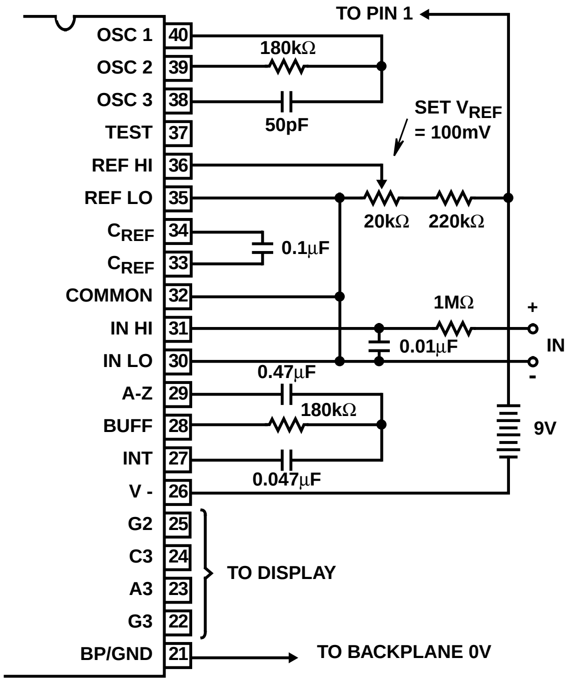


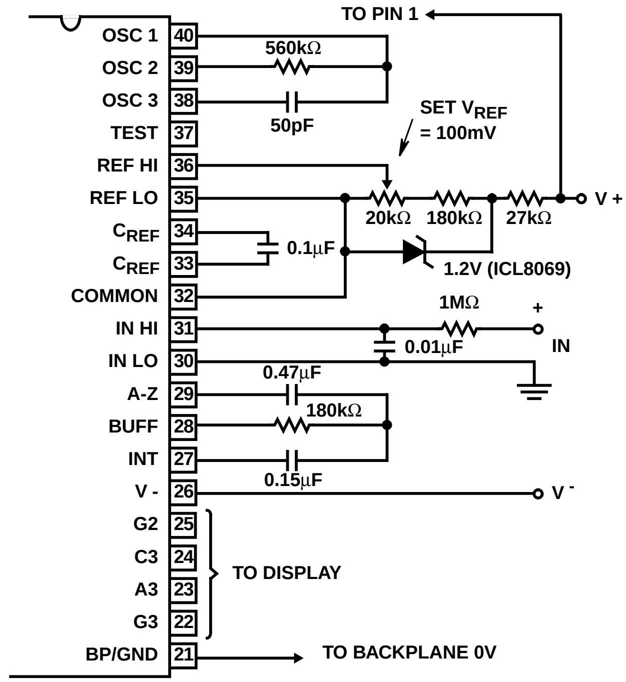
FIGURE 99. HI7131 TYPICAL REFERENCE CIRCUITS

Typical Applications



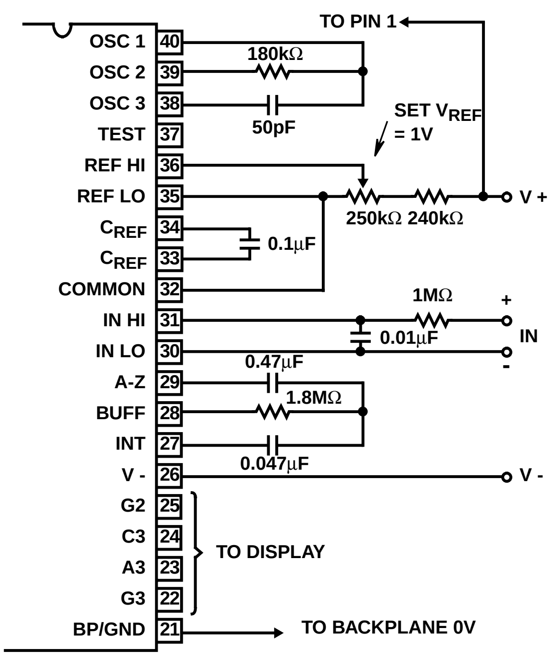
Values shown are for 200mV full-scale, 3 readings/sec., floating supply voltage (9V battery).

FIGURE 100. HI7131 AND HI7133 USING THE INTERNAL REFERENCE



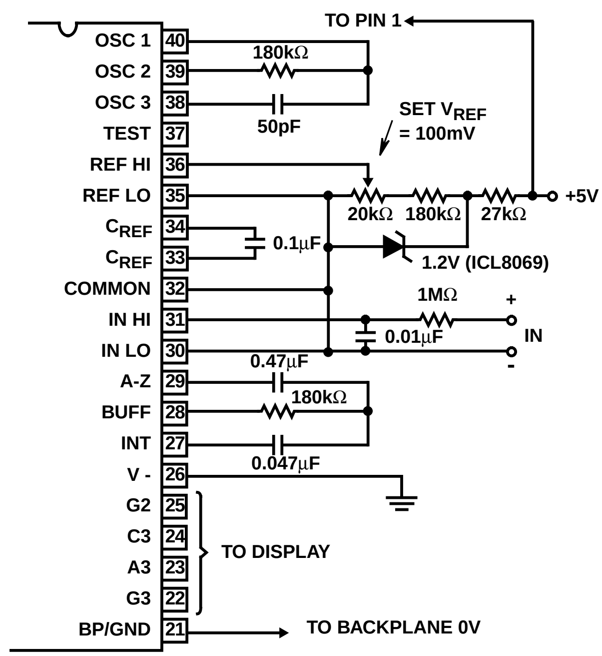
IN LO is tied to supply GND establishing the correct common-mode voltage. COMMON acts as a pre-regulator for the reference. Values shown are for 1 reading/sec.

FIGURE 101. HI7131 AND HI7133 WITH AN EXTERNAL BAND-GAP REFERENCE (1.2V TYPE)



For 1 reading/sec., change C_{INT}, R_{OSC} to values of Figure 12.

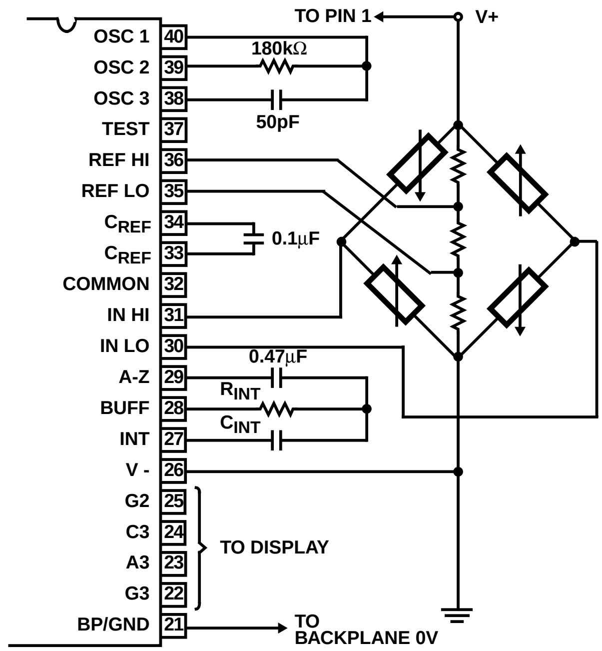
FIGURE 102. RECOMMENDED COMPONENT VALUES FOR 2.000V FULL-SCALE, 3 READINGS/SEC



An external reference must be used in this application, since the voltage between V+ and V- is insufficient for correct operation of the internal reference. COMMON holds the IN LO almost at the middle of the supply, ≈ 2.7V.

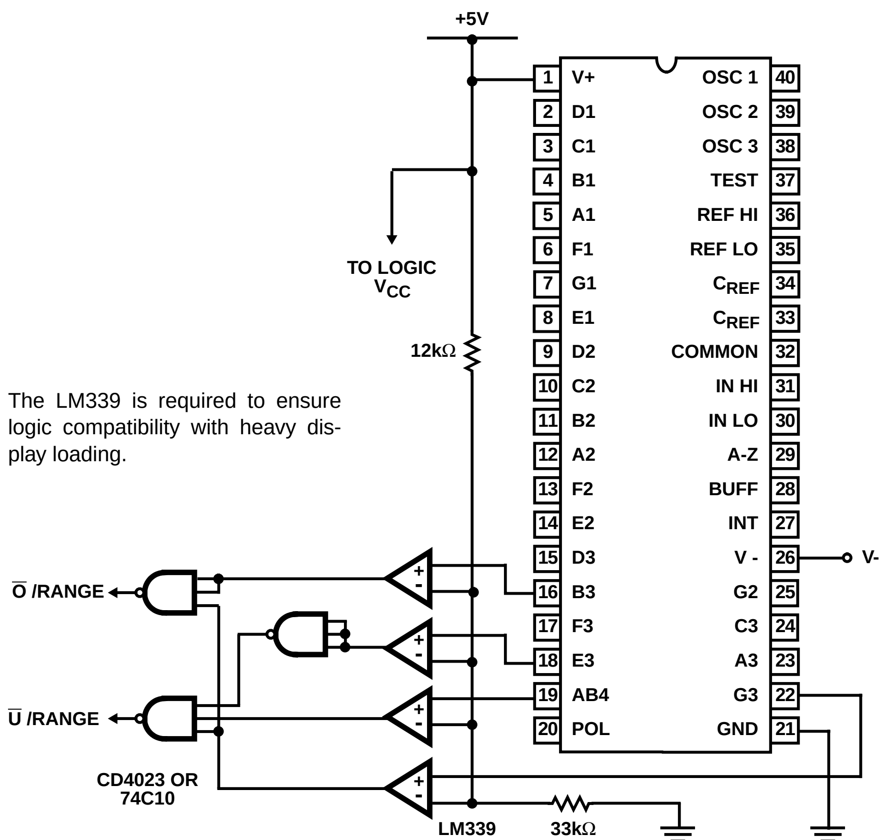
FIGURE 103. HI7131 AND HI7133 OPERATED FROM SINGLE +5V SUPPLY

Typical Applications (Continued)



The resistor values within the bridge are determined by the desired sensitivity.

FIGURE 104A. HI7131 AND HI7133 MEASURING RATIOMETRIC VALUES OF QUAD LOAD CELL

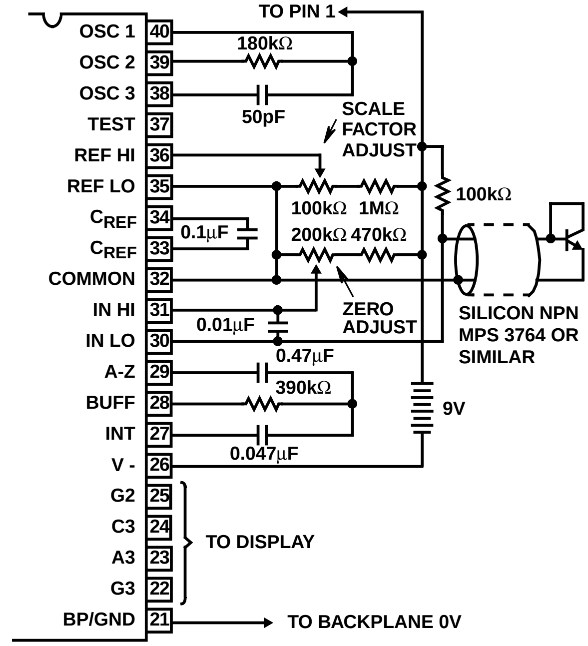


The LM339 is required to ensure logic compatibility with heavy display loading.

FIGURE 104B. CIRCUIT FOR DEVELOPING UNDERRANGE AND OVERRANGE SIGNALS FROM HI7133 OUTPUTS

FIGURE 104.

Typical Applications (Continued)



A silicon diode-connected transistor has a temperature coefficient of about -2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for a 100.0 reading. See AD590 data sheets for alternative circuits.

FIGURE 105A. HI7131 AND HI7133 USED AS A DIGITAL CENTIGRADE THERMOMETER

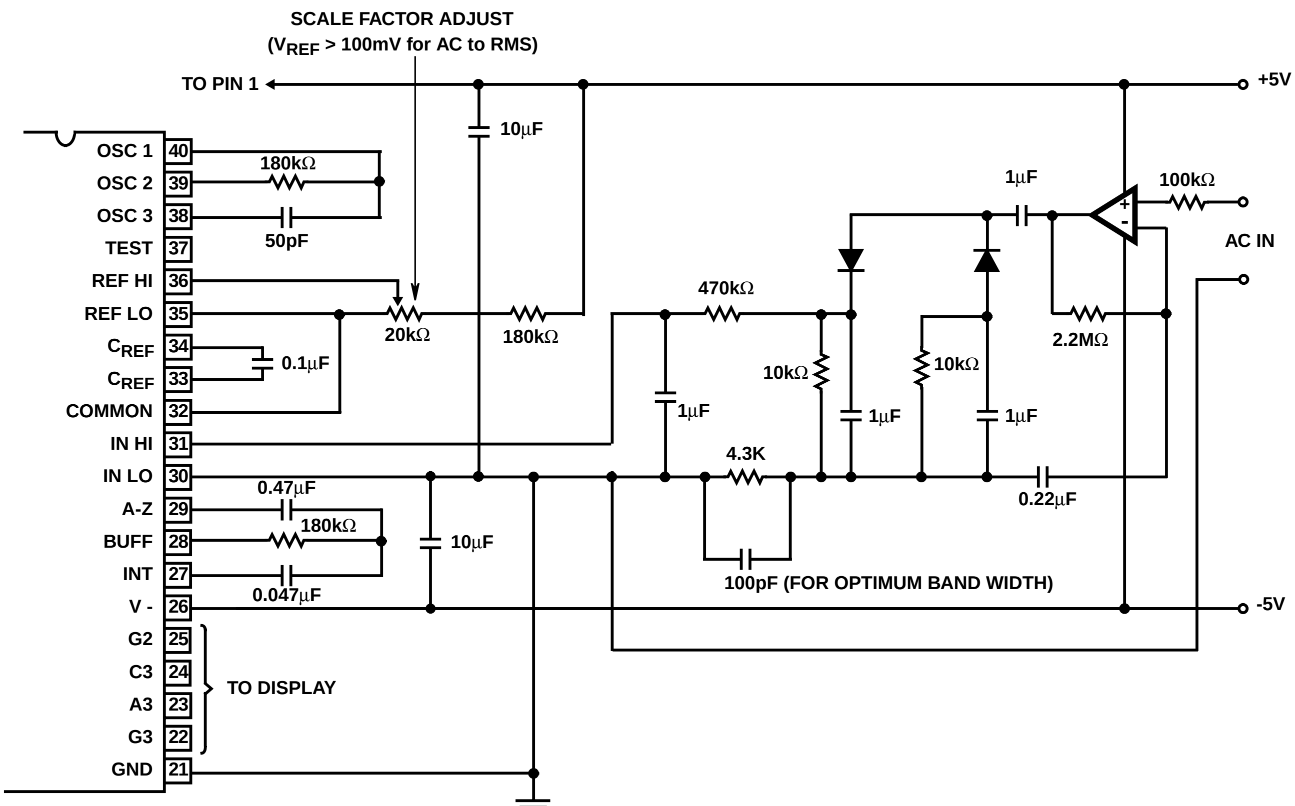
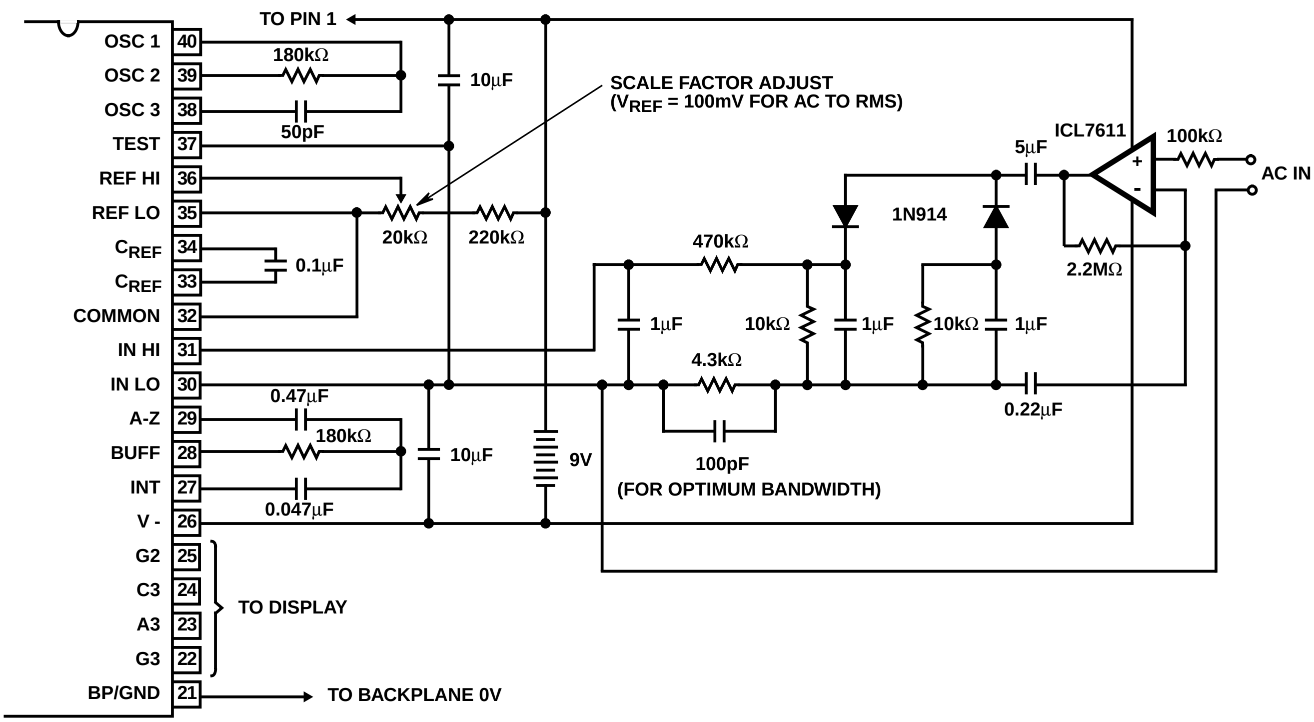


FIGURE 105B. AC TO DC CONVERTER AND HI7133 FOR RMS DISPLAY

FIGURE 105.

Typical Applications (Continued)



Test is used as a common-mode reference level to ensure compatibility with most op amps.

FIGURE 106. AC TO DC CONVERTER WITH HI7131 AND HI7133

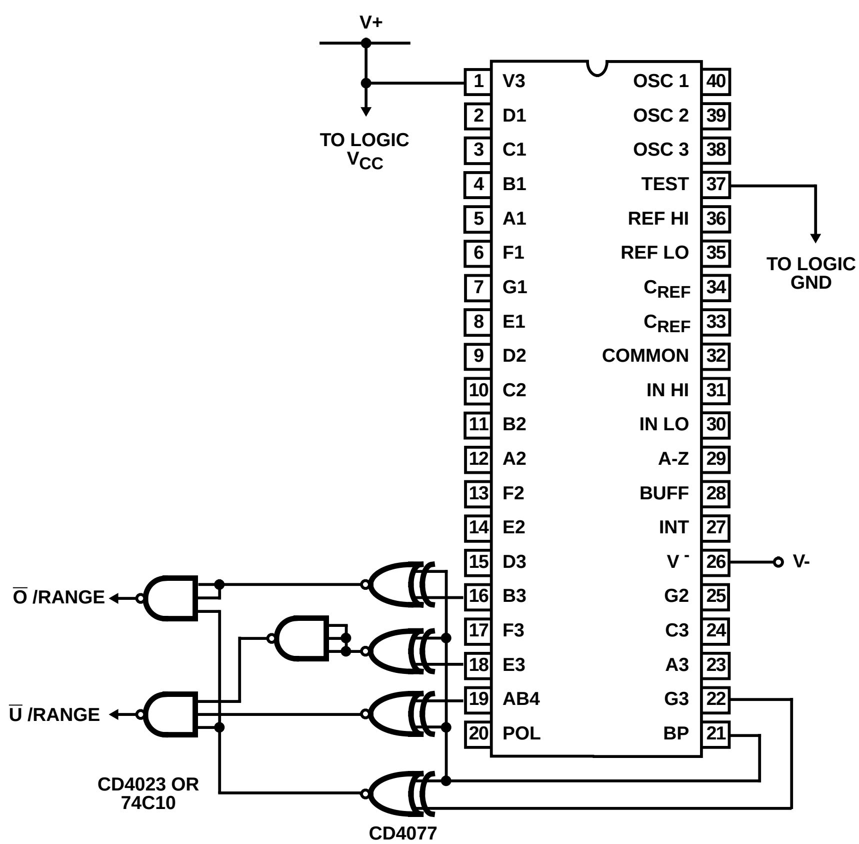


FIGURE 107. CIRCUIT FOR DEVELOPING UNDERRANGE AND OVERRANGE SIGNALS FROM HI7131 OUTPUTS

Die Characteristics

DIE DIMENSIONS:

127 mils x 149 mils

METALLIZATION:

Type: Al
Thickness: 10kÅ ±1kÅ

PASSIVATION:

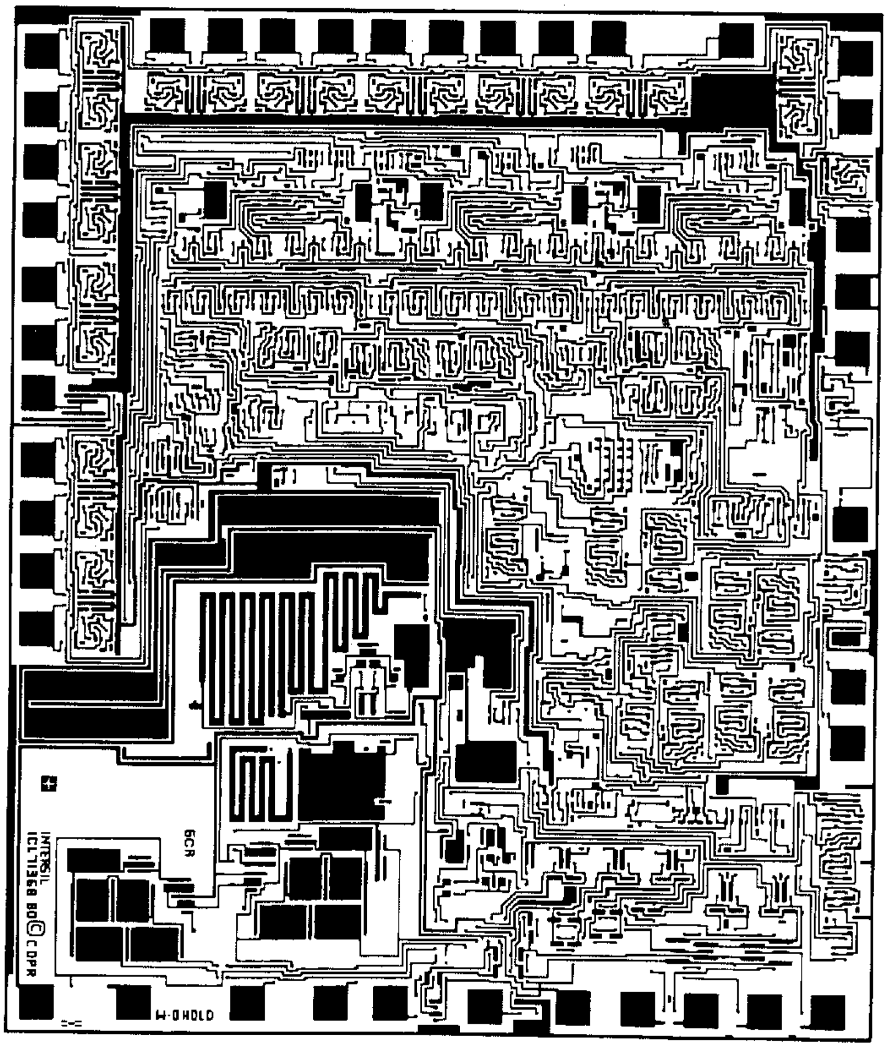
Type: PSG Nitride
Thickness: 15kÅ ±3kÅ

WORST CASE CURRENT DENSITY:

9.1×10^4 A/cm^2

Metallization Mask Layout

HI7131, HI7133



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.