FailSafe™
Communications Clock Generator

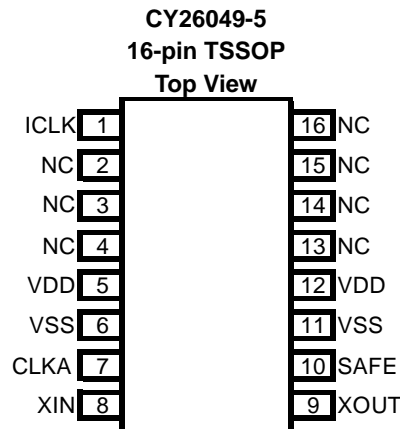| Features	Benefits
• **Fully integrated phase-locked loop (PLL)**	• **Integrated high-performance PLL tailored for telecommunications frequency synthesis eliminates the need for external loop filter components**
• **FailSafe™ output**	• **When reference is off, DCXO maintains clock outputs and SAFE pin indicates FailSafe conditions**
• **PLL driven by a crystal oscillator.**	• **DCXO maintains continuous operation should the input reference clock fail** • **Glitch-free transition simplifies system design**
• **76.8-MHz output from 19.2-MHz input.**	• **Works with commonly available, low-cost 19.2-MHz crystal**
• **Low-jitter, high-accuracy outputs**	• **Zero-ppm error for all output frequencies**
• **3.3 V ± 5% operation**	• **Compatibility across industry standard design platforms**
• **16-lead TSSOP**	• **Industry standard package with 6.4 x 5.0 mm footprint and a height profile of just 1.1 mm**

Logic Block Diagram
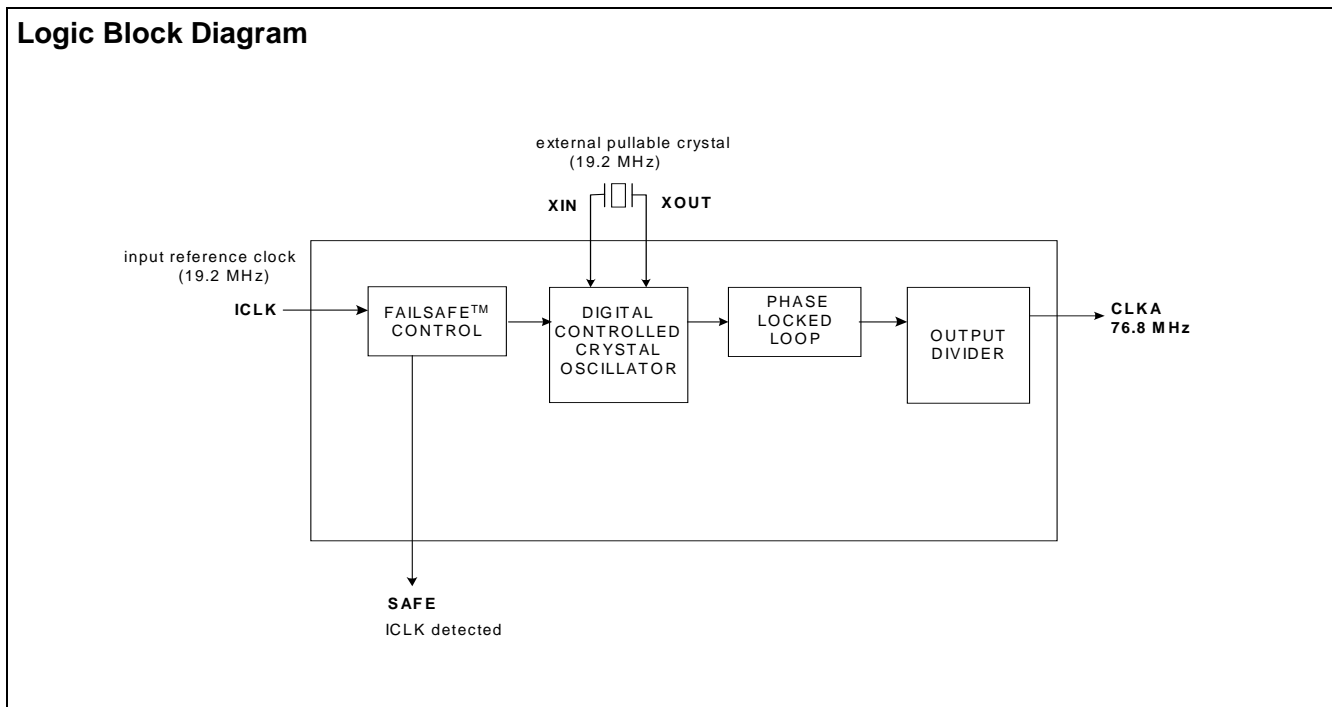
Description

CY26049 is a FailSafe frequency synthesizer with a reference clock input and 76.8-MHz output. The device provides an optimum solution for applications where continuous operation is required in the event of a primary clock failure. The continuous, glitch-free operation is achieved by using a DCXO, which serves as a primary clock source. The FailSafe control circuit synchronizes the DCXO oscillator with the reference as long as the reference is within the pull range of the crystal.

In the event of a reference clock failure the DCXO maintains the last frequency of the reference clock. The unique feature of the CY26049-5 is that the DCXO is in fact the primary clocking source. When the reference clock is restored, the DCXO automatically resynchronizes to the reference. The status of the reference clock input, as detected by the CY26049-5, is reported by the SAFE pin.

Selector Guide

Part Number	Input Frequency Range	Outputs	Output Frequencies
CY26049ZC-5	Reference Input Clock: 19.2 MHz Crystal: 19.2-MHz pullable Crystal per Cypress Specification	1	76.8 MHz

Pin Configuration

CY26049-5
16-pin TSSOP
Top View

```
        ┌───────────┐
ICLK  1 │           │ 16  NC
  NC  2 │           │ 15  NC
  NC  3 │           │ 14  NC
  NC  4 │           │ 13  NC
 VDD  5 │           │ 12  VDD
 VSS  6 │           │ 11  VSS
CLKA  7 │           │ 10  SAFE
 XIN  8 │           │  9  XOUT
        └───────────┘
```

Pin Description

| Pin Number	Pin Name	Pin Description
1	ICLK	Reference Input Clock - 19.2-MHz clock
2	NC	No Connect
3	NC	No Connect
4	NC	No Connect
5	VDD	Connect to 3.3V power supply
6	VSS	Ground
7	CLKA	Clock Output; 76.8 MHz
8	XIN	19.2-MHz Pullable Crystal Input
9	XOUT	19.2-MHz Pullable Crystal Output
10	SAFE	High = reference ICLK within range, Low = reference ICLK out of range
11	VSS	Ground
12	VDD	Connect to 3.3V power supply.
13	NC	No Connect
14	NC	No Connect
15	NC	No Connect
16	NC	No Connect

Recommended Pullable Crystal Specifications

Parameter	Name	Min.	Typ.	Max.	Unit
CL_{XTAL}	Crystal Nominal Load Capacitance		14		pF
C0/C1				250	
ESR	Equivalent Series Resistance		30	50	Ω
T_o	Operating Temperature	0		70	°C
Crystal Accuracy	Crystal Initial Accuracy		±20	±50	ppm
TT_s	Stability Over Temperature and Aging		±20	±50	ppm
C_O	Shunt Capacitance		6	7	pF
C_{LBRD}	Stray Capacitance—On XIN/XOUT		2		pF

All applicable DC and AC characteristics are as described in the CY26049-36 data sheet.

Ordering Information

Ordering Code	Package Type	Operating Temperature Range
CY26049ZC-5	16-lead TSSOP	Commercial 0 to 70°C
CY26049ZC-5T	16-lead TSSOP—Tape and Reel	Commercial 0 to 70°C

Package Drawing and Dimensions

16-lead Thin Shrunk Small Outline Package (4.40 MM Body) Z16
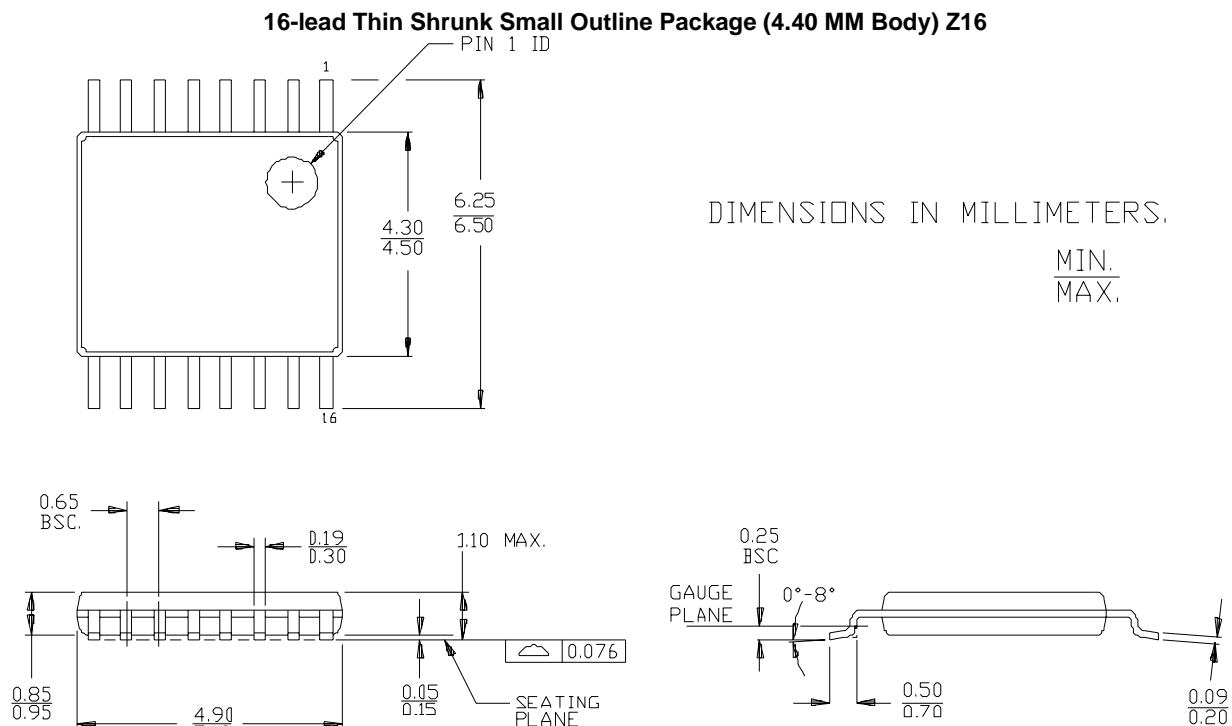
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Document History Page

Document Title: CY26049-5 FailSafe™ Communications Clock Generator Document Number: 38-07485				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	119591	10/31/02	CKN	New Data Sheet