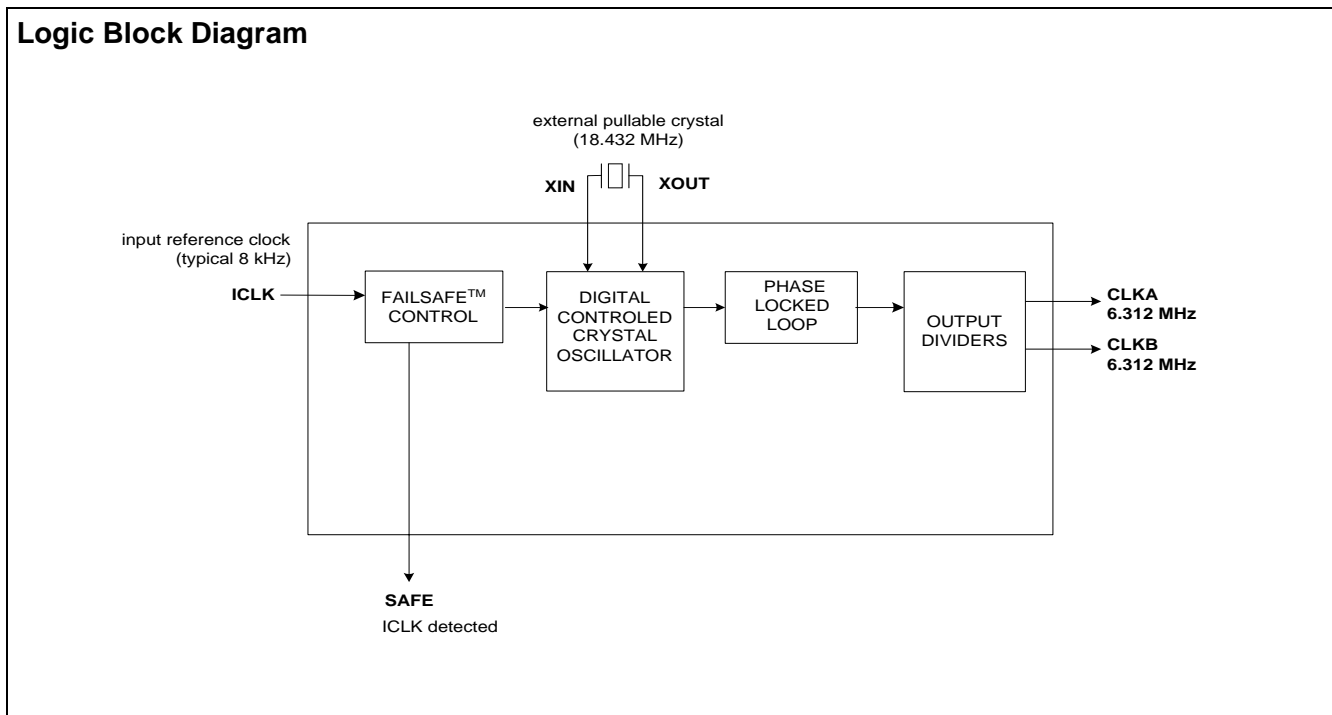




FailSafe™ Communications Clock Generator

Features	Benefits
<ul style="list-style-type: none"> Fully integrated phase-locked loop (PLL) 	<ul style="list-style-type: none"> Integrated high-performance PLL tailored for telecommunications frequency synthesis eliminates the need for external loop filter components
<ul style="list-style-type: none"> FailSafe™ output 	<ul style="list-style-type: none"> When reference is off, DCXO maintains clock outputs and SAFE pin indicates FailSafe conditions
<ul style="list-style-type: none"> PLL driven by a crystal oscillator 	<ul style="list-style-type: none"> DCXO maintains continuous operation should the input reference clock fail Glitch-free transition simplifies system design
<ul style="list-style-type: none"> Two 6.312-MHz outputs from 8-kHz input 	<ul style="list-style-type: none"> Works with commonly available, low-cost 18.432-MHz crystal
<ul style="list-style-type: none"> Low-jitter, high-accuracy outputs 	<ul style="list-style-type: none"> Zero-ppm error for all output frequencies
<ul style="list-style-type: none"> 3.3 V ± 5% operation 	<ul style="list-style-type: none"> Compatibility across industry standard design platforms
<ul style="list-style-type: none"> 16-lead TSSOP 	<ul style="list-style-type: none"> Industry standard package with 6.4 x 5.0 mm footprint and a height profile of just 1.1 mm

Logic Block Diagram



Description

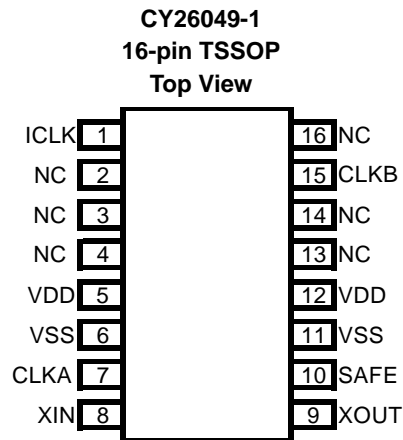
CY26049 is a FailSafe frequency synthesizer with a reference clock input and 6.312-MHz output. The device provides an optimum solution for applications where continuous operation is required in the event of a primary clock failure. The continuous, glitch-free operation is achieved by using a DCXO, which serves as a primary clock source. The FailSafe control circuit synchronizes the DCXO oscillator with the

reference as long as the reference is within the pull range of the crystal.

In the event of a reference clock failure the DCXO maintains the last frequency of the reference clock. The unique feature of the CY26049-1 is that the DCXO is in fact the primary clocking source. When the reference clock is restored, the DCXO automatically resynchronizes to the reference. The status of the reference clock input, as detected by the CY26049-1, is reported by the SAFE pin.

Selector Guide

Part Number	Input Frequency Range	Outputs	Output Frequencies
CY26049ZC-1	Reference Input Clock: 8 kHz Crystal: 18.432-MHz pullable Crystal per Cypress Specification	2	6.312 MHz

Pin Configuration

Pin Description

Pin Number	Pin Name	Pin Description
1	ICLK	Reference Input Clock—8-kHz clock
2	NC	No Connect
3	NC	No Connect
4	NC	No Connect
5	VDD	Connect to 3.3V power supply
6	VSS	Ground
7	CLKA	Clock Output; 6.312 MHz
8	XIN	18.432-MHz Pullable Crystal Input
9	XOUT	18.432-MHz Pullable Crystal Output
10	SAFE	High = reference ICLK within range, Low = reference ICLK out of range
11	VSS	Ground
12	VDD	Connect to 3.3V power supply.
13	NC	No Connect
14	NC	No Connect
15	CLKB	Clock Output; 6.312 MHz
16	NC	No Connect

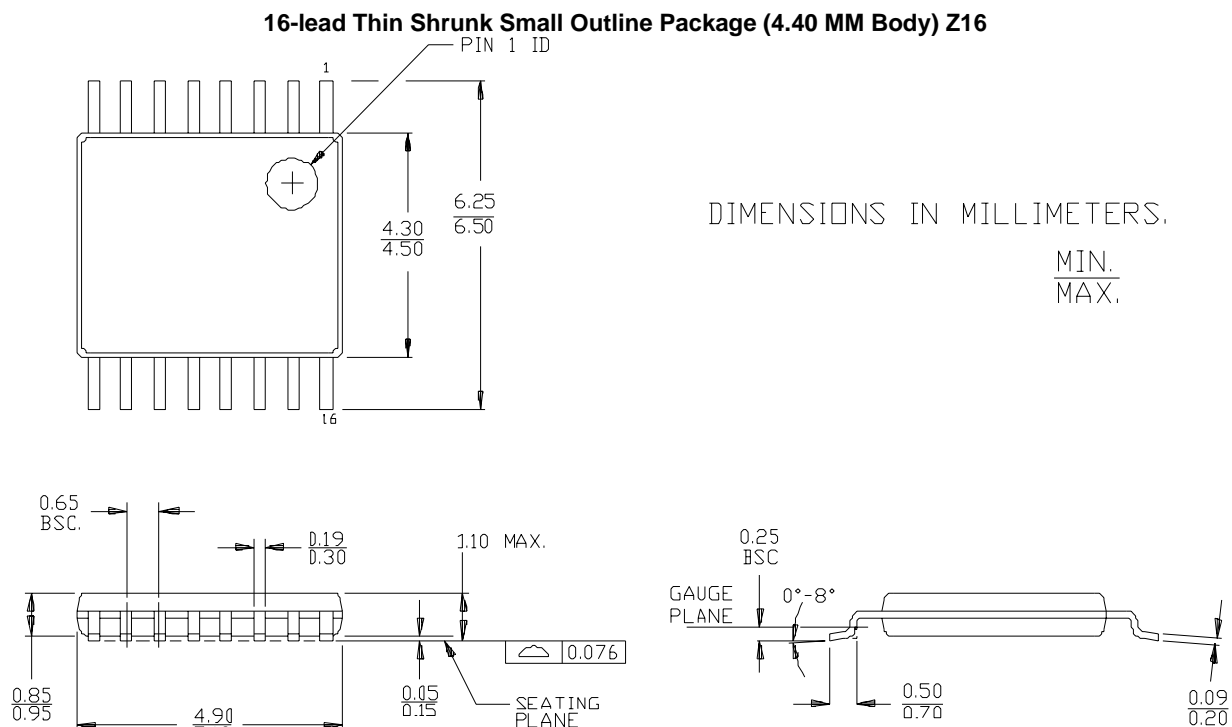
Recommended Pullable Crystal Specifications

Parameter	Name	Min.	Typ.	Max.	Unit
CL _X TAL	Crystal Nominal Load Capacitance	14	16	20	pF
C ₀ /C ₁				250	
T _o	Operating Temperature	0		70	°C
Crystal Accuracy	Crystal Initial Accuracy		±20	±50	ppm
TT _s	Stability Over Temperature and Aging		± 20	±50	ppm
C _O	Shunt Capacitance		5	7	pF
C _{LBRD}	Stray Capacitance—on XIN/XOUT		2		pF

All applicable DC and AC characteristic are as described in the CY26049-36 data sheet.

Ordering Information

Ordering Code	Package Type	Operating Temperature Range
CY26049ZC-1	16-lead TSSOP	Commercial 0 to 70°C
CY26049ZC-1T	16-lead TSSOP—Tape and Reel	Commercial 0 to 70°C

Package Drawing and Dimensions


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Document History Page

Document Title: CY26049-1 FailSafe™ Communications Clock Generator Document Number: 38-07488				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	120007	11/01/02	CKN	New Data Sheet