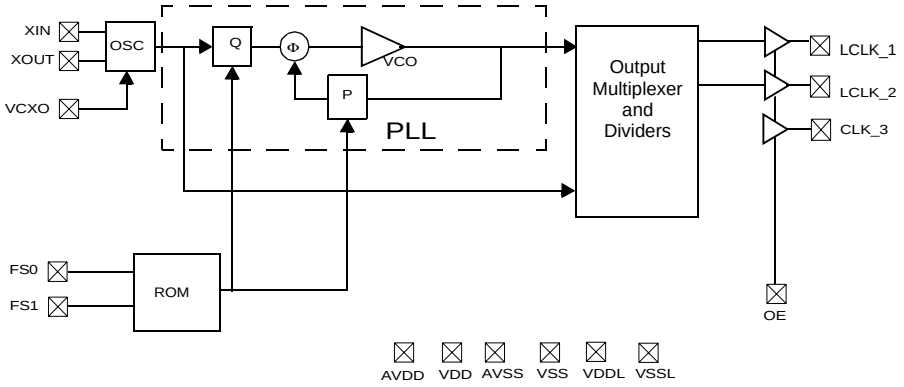
CY2413

Set Top Box
Clock Generator with VCXO

Features	Benefits
• **Low jitter, high accuracy outputs**	Meets critical timing requirements in complex system designs
• **VCXO with analog adjust**	Large ±150 ppm range, better linearity
• **3.3V Operation with 2.5 V Output Option**	Enables application compatibility

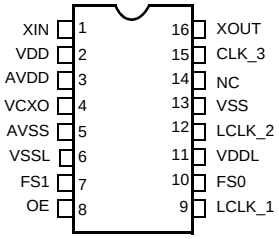
Part Number	Outputs	Input Frequency Range	Output Frequency Range
CY2413-1	3	13.5-MHz pullable Crystal per Cypress Specification	13.5-, 27-, 36-, and 54-MHz selectable output frequencies
CY2413-2	2	13.5-MHz pullable Crystal per Cypress Specification	27-, and 54-MHz output frequencies

Logic Block Diagram CY2413-1

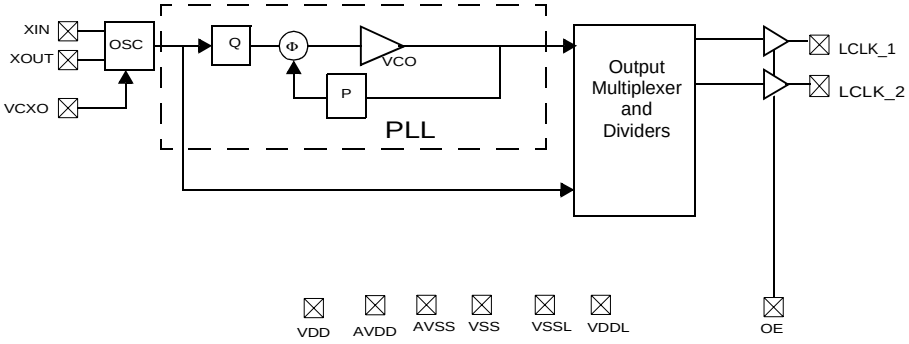


Pin Configuration

CY2413-1
16-pin TSSOP

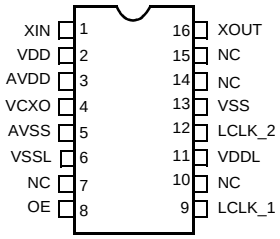


Logic Block Diagram CY2413-2



Pin Configuration

CY2413-2
16-pin TSSOP



Pin Summary - CY2413-1

Name	Pin Number	Description
XIN	1	Reference Crystal Input
V_{DD}	2	Voltage Supply
A_{VDD}	3	Analog Voltage Supply
VCXO	4	Input Analog control voltage for VCXO
AV_{SS}	5	Analog Ground
V_{SSL}	6	LCLK Ground
FS1	7	Frequency Select
OE	8	Output Enable
LCLK_1	9	Configurable Clock output 1 at VDDL level
FS0	10	Frequency Select
VDDL	11	LCLK Voltage Supply (2.5V or 3.3V)
LCLK_2	12	Configurable Clock output 2 at VDDL level
VSS	13	Ground
NC	14	No Connect
CLK_3	15	Configurable Clock output 3
XOUT[1]	16	Reference Crystal Output

Frequency Select Table - CY2413-1

FS1	FSO	Input	LCLK_1	LCLK_2	CLK_3
0	0	13.5	54	36	off
0	1	13.5	13.5	36	13.5
1	0	13.5	27	54	13.5
1	1	13.5	27	27	13.5

Note:
1. Float XOUT if XIN is externally driven

Pin Summary– CY2413-2

Name	Pin Number	Description
XIN	1	Reference Crystal Input
V_{DD}	2	Voltage Supply
AV_{DD}	3	Analog Voltage Supply
VCXO	4	Input Analog control voltage for VCXO
AV_{SS}	5	Analog Ground
V_{SSL}	6	LCLK Ground
NC	7	No Connect
OE	8	Output Enable
LCLK_1	9	54-MHz Clock output 1 at VDDL level
NC	10	No Connect
V_{DDL}	11	LCLK Voltage Supply (2.5V or 3.3V)
LCLK_2	12	27-MHz Clock output 2 at VDDL level
V_{SS}	13	Ground
NC	14	No Connect
NC	15	No Connect
XOUT[1]	16	Reference Crystal Output

Pullable Crystal Specifications

Parameter	Name	Min.	Typ.	Max.	Unit
CR_{load}	Crystal Load Capacitance		14		pF
C0/C1			240		
ESR	Equivalent Series Resistance		35		Ω
T_o	Operating Temperature	0		70	°C
Crystal Accuracy	Crystal Accuracy			± 20	ppm
TT_S	Stability over temperature and aging			± 50	ppm

Absolute Maximum Conditions

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	–0.5	7.0	V
V_{DDL}	I/O Supply Voltage	–0.5	7.0	V
T_S	Storage Temperature[2]	–65	100	°C
T_J	Junction Temperature		125	°C
	Digital Inputs	AV_{SS} – 0.3	AV_{DD} + 0.3	V
	Digital Outputs referred to V_{DD}	V_{SS} – 0.3	V_{DD} + 0.3	V
	Digital Outputs referred to V_{DDL}	V_{SSL} – 0.3	V_{DDL} +0.3	V
	Analog Input referred to AV_{DD}	AV_{SS} – 0.3	AV_{DD} + 0.3	V
	Electro-Static Discharge	2		kV
	Soldering Temperature 10 sec		235°	°C

Note:
2. Rated for 10 years.

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	3.0	3.3	3.6	V
V_{DDL}	Operating Voltage	2.375	2.5	2.625	V
AV_{DD}	Analog Operating Voltage	3.0	3.3	3.6	V
T_A	Ambient Temperature	0		70	°C
C_{LOAD}	Max. Load Capacitance V_{DD}/V_{DDL}=3.3V			15	pF
C_{LOAD}	Max. Load Capacitance V_{DDL}=2.5V			15	pF
f_{REF}	Reference Frequency		13.5		MHz
P_{max}	Max. Output Power Dissipation			115	°C/W
t_{PU}	Power-up time for all VDD's to reach minimum specified voltage (power ramps must be monotonic)	0.05		500	ms

DC Electrical Characteristics

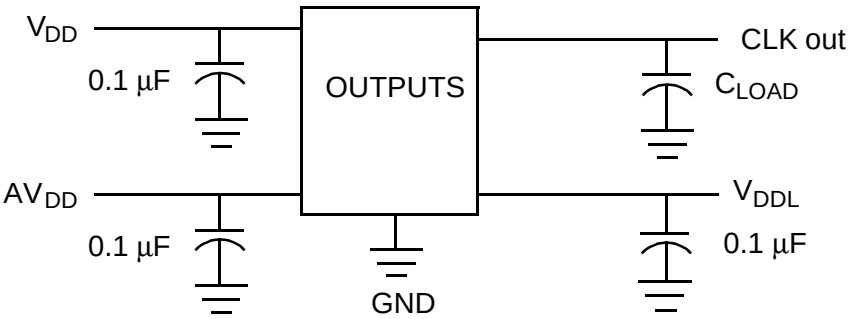
Parameter[3]	Name	Description	Min.	Typ.	Max.	Unit
I_{OH}	Output High Current	$V_{OH} = V_{DD} – 0.5$, V_{DD}/V_{DDL} = 3.3V	12	24		mA
I_{OL}	Output Low Current	V_{OL} = 0.5, V_{DD}/V_{DDL} = 3.3V	12	24		mA
I_{OH}	Output High Current	$V_{OH} = V_{DDL} – 0.5$, V_{DDL} = 2.5V	8	16		mA
I_{OL}	Output Low Current	V_{OL} = 0.5, V_{DDL} = 2.5V	8	16		mA
V_{IH}	Input High Voltage	CMOS levels, 70% of V_{DD}	0.7			VDD
V_{IL}	Input Low Voltage	CMOS levels, 30% of V_{DD}			0.3	VDD
C_{IN}	Input Capacitance	Frequency Select and OE Pins			7	pF
I_{IZ}	Input Leakage Current	Frequency Select and OE Pins		5		µA
$f_{\Delta XO}$	VCXO pullability range		–150		+150	ppm
V_{VCXO}	VCXO input range		0		AV_{DD}	V
f_{VBW}	VCXO input bandwidth			DC to 200		kHz
I_{VDD}	Supply Current	AV_{DD}/V_{DD} Current	10		35	mA
I_{VDDL3}	Supply Current	V_{DDL} Current (V_{DDL}=3.6V)	5		15	mA
I_{VDDL2}	Supply Current	V_{DDL} Current (V_{DDL}=2.625V)	5		12	mA

AC Electrical Characteristics

Parameter[3]	Name	Description	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	Duty Cycle is defined in *Figure 2*, 50% of V_{DD}	45	50	55	%
t_3	Rising Edge Rate	Output Clock Rise Time, 80% – 20% of V_{DD}/V_{DDL}, V_{DDL} = 3.3V	0.8	1.4		V/ns
t_3	Rising Edge Rate	Output Clock Rise Time, 80% – 20% of V_{DDL} = 2.5V	0.6	1.2		V/ns
t_4	Falling Edge Rate	Output Clock Fall Time, 80% – 20% of V_{DD}/V_{DDL}, V_{DDL} = 3.3V	0.8	1.4		V/ns
t_4	Falling Edge Rate	Output Clock Fall Time, 80% – 20% of V_{DDL} = 2.5V	0.6	1.2		V/ns
t_9	Clock Jitter	Peak to Peak period jitter		250	450	ps
t_{10}	PLL Lock Time	Measured from V_{DD} = 3.0V			3	ms

Note:
3. Not 100% tested

Test Circuit



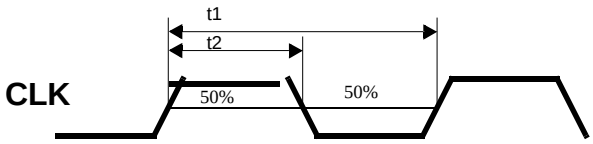


Figure 1. Duty Cycle Definition; DC = t2/t1

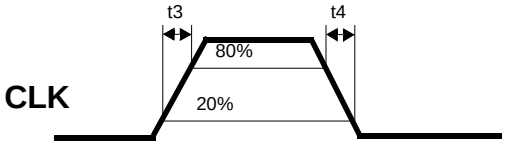


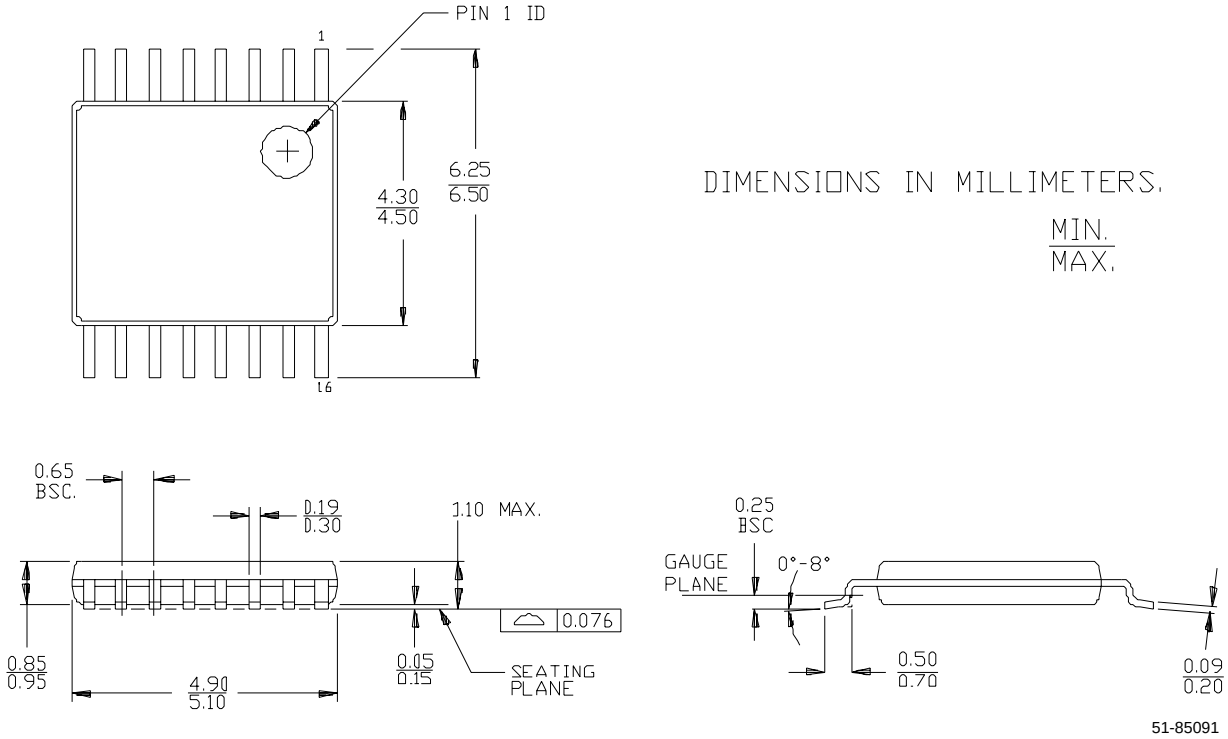
Figure 2. Rise and Fall Time Definitions

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage
CY2413ZC-1	Z16	16-Pin TSSOP	Commercial	3.3V
CY2413ZC-2	Z16	16-Pin TSSOP	Commercial	3.3V

Package Diagram

16-Lead Thin Shrunk Small Outline Package (4.40 MM Body) Z16



Document Title: CY2413 Set Top Box Clock Generator with VCXO Document Number: 38-07226				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110491	10/21/01	SZV	Change from Spec number: 38-00895 to 38-07226
*B	121878	12/14/02	RBI	Power up requirements added to Operating Conditions Information