TDA8593J; TDA8593Q

I²C-bus controlled 4 × 45 W power amplifier

Rev. 01 — 9 June 2004 Preliminary data sheet

1. General description

The TDA8593J; TDA8593Q is a complementary quad BTL audio power amplifier made in the BCDMOS technology. It contains four independent amplifiers in Bridge Tied Load (BTL) configuration. Through the I²C-bus the diagnostic information of each amplifier and speaker can be read separately.

Both front and both rear channel amplifiers can be configured independently in line driver mode with a gain of 20 dB.

2. Features

- I²C-bus control
- Hardware programmable I²C-bus address
- Can drive a 2 Ω load with a battery voltage of up to 16 V and a 4 Ω load with a battery voltage of up to 18 V
- DC-load detection: open, short and present
- AC-load (tweeter) detection
- Programmable clip detection: 1 % or 3 %
- Programmable thermal protection pre-warning
- Independent short-circuit protection per channel
- Low gain line driver mode (20 dB)
- Loss-of-ground and open V_P safe
- All outputs protected from short-circuit to ground, to V_P, or across the load
- All pins protected from short-circuit to ground
- Soft thermal clipping to prevent audio holes
- Low battery detection.

3. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{P1}, V_{P2}	operating supply voltage		8	14.4	18	V
I_q	quiescent current		-	280	400	mA

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Table 1: Quick reference data *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{o(max)}$	maximum output power	R_L = 4 Ω; V_P = 14.4 V; V_{IN} = 2 V (RMS) square wave	39	41	-	W
		R_L = 4 Ω; V_P = 15.2 V; V_{IN} = 2 V (RMS) square wave	44	46	-	W
		R_L = 2 Ω; V_P = 14.4 V; V_{IN} = 2 V (RMS) square wave	64	69	-	W
THD	total harmonic distortion		-	0.01	0.1	%
$V_{n(o)(amp)}$	noise output voltage in amplifier mode		-	50	70	μV
$V_{n(o)(LN)}$	noise output voltage in line driver mode		-	25	35	μV

4. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
TDA8593J	DBS27P	plastic DIL-bent-SIL (special bent) power package; 27 leads (lead length 7.7 mm)	SOT767-1
TDA8593Q	DBS27P	plastic DIL-bent-SIL (special bent) power package; 27 leads (lead length 6.8 mm)	SOT827-1

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5. Block diagram

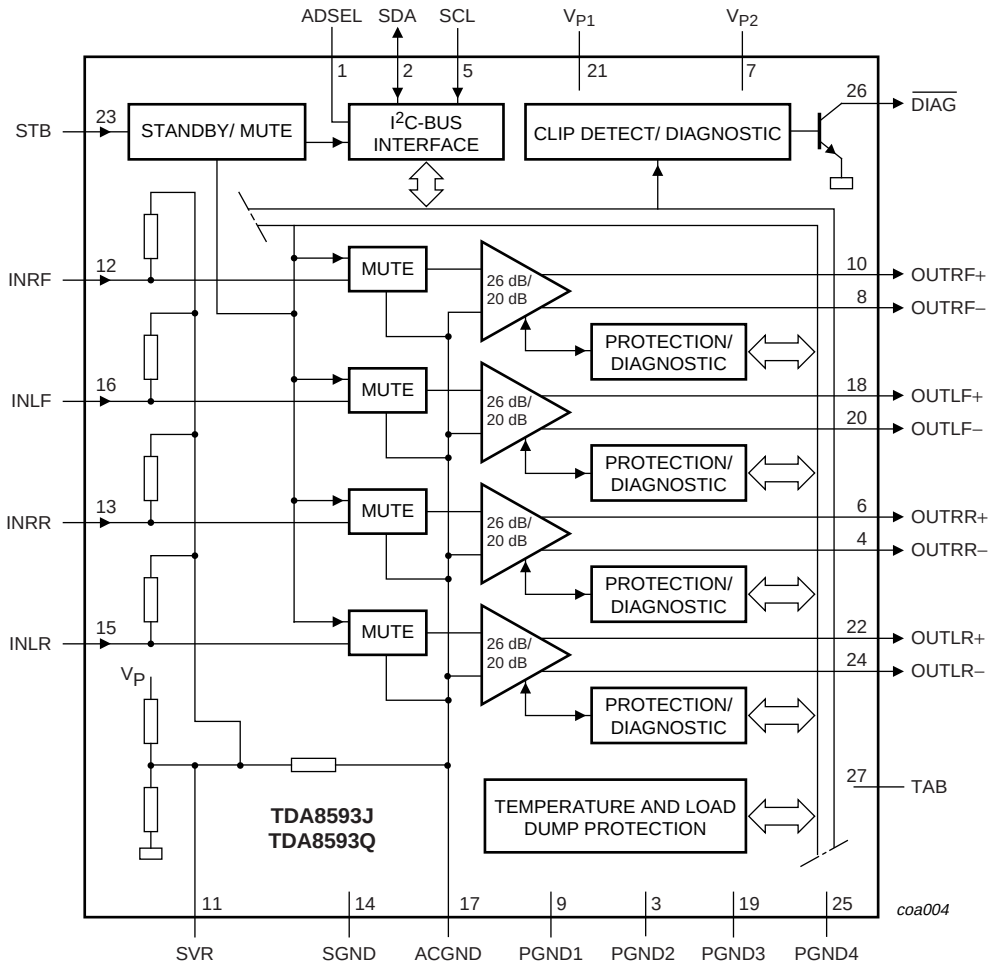

Fig 1. Block diagram.

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6. Pinning information

6.1 Pinning

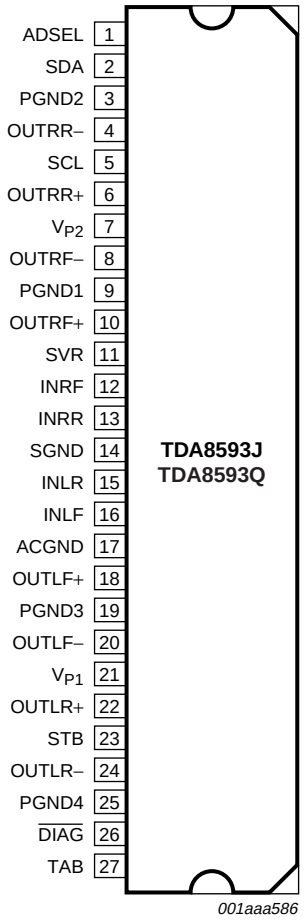

Fig 2. Pin configuration.

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
ADSEL	1	I²C-bus address selection
SDA	2	I²C-bus data input and output
PGND2	3	power ground 2
OUTRR–	4	channel right rear negative output
SCL	5	I²C-bus clock input
OUTRR+	6	channel right rear positive output
V_{P2}	7	power supply voltage 2
OUTRF–	8	channel right front negative output
PGND1	9	power ground 1

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Table 3: Pin description *…continued*

Symbol	Pin	Description
OUTRF+	10	channel right front positive output
SVR	11	half supply voltage filter capacitor
INRF	12	channel right front input
INRR	13	channel right rear input
SGND	14	signal ground
INLR	15	channel left rear input
INLF	16	channel left front input
ACGND	17	AC ground
OUTLF+	18	channel left front positive output
PGND3	19	power ground 3
OUTLF–	20	channel left front negative output
V_{P1}	21	power supply voltage 1
OUTLR+	22	channel left rear positive output
STB	23	standby or operating mute mode select input
OUTLR–	24	channel left rear negative output
PGND4	25	power ground 4
$\overline{DIAG}$	26	diagnose and clip detection output; active LOW
TAB	27	heatsink connection, must be connected to ground

To keep the output pins on the front side, shift bending is applied.

7. Functional description

The TDA8593J; TDA8593Q is an audio power amplifier with four independent amplifiers configured in Bridge Tied Load (BTL) with diagnostic capability. The amplifier diagnostic functions give information about output offset, load, or short-circuit. Diagnostic functions are controlled via the I²C-bus. The TDA8593J; TDA8593Q is protected against short-circuit, over-temperature, open ground and open V_P connections. If a short-circuit occurs at the input or output of a single amplifier, that channel shuts down, and the other channels continue to operate normally. The channel that has a short-circuit can be disabled by the microcontroller via the appropriate enable bit of the I²C-bus to prevent any noise generated by the fault condition from being heard.

7.1 Start-up

When pin STB is LOW, the total quiescent current is low, and the I²C-bus lines are high-impedance.

When pin STB is HIGH, the I²C-bus is biased and then the TDA8593J; TDA8593Q performs a power-on reset. When bit D0 of instruction byte IB1 is set, the amplifier is activated, bit D7 of data byte 2 (power-on reset occurred) is reset, and pin $\overline{DIAG}$ is no longer held LOW.

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7.2 Start-up and shut-down timing

A capacitor connected to pin SVR enables smooth start-up and shut-down, preventing the amplifier from producing audible clicks at switch-on or switch-off. The start-up and shut-down times can be extended by increasing the capacitor value.

If the amplifier is shut-down using pin STB, the amplifier is muted, and the capacitor connected to pin SVR discharges. The low current standby mode is activated 2 seconds after pin STB goes LOW; see Figure 8.

7.3 Power-on reset and supply voltage spikes

If the supply voltage drops too low to guarantee the integrity of the data in the I²C-bus latches, the power-on reset cycle will start. All latches will be set to a pre-defined state, pin $\overline{\text{DIAG}}$ will be pulled LOW to indicate that a power-on reset has occurred, and bit D7 of data byte 2 is also set for the same reason. When D0 of instruction byte 1 is set, the power-on flag resets, pin $\overline{\text{DIAG}}$ is released and the amplifier will then enter its start-up cycle; see Figure 9 and Figure 10.

7.4 Diagnostic output

Pin $\overline{\text{DIAG}}$ indicates clipping, thermal protection pre-warning, short-circuit protection, low and high battery voltage. Pin $\overline{\text{DIAG}}$ is an open-drain output, is active LOW, and must be connected to an external voltage via an external pull-up resistor. If a failure occurs, pin $\overline{\text{DIAG}}$ remains LOW during the failure and no clipping information is available. The microcontroller can read the failure information via the I²C-bus.

7.5 Muting

A hard mute and a soft mute can both be performed via the I²C-bus. A hard mute mutes the amplifier within 0.5 ms. A soft mute mutes the amplifier within 20 ms and is less audible. A hard mute is also activated if a voltage of 8 V is applied to pin STB.

7.6 Temperature protection

If the average junction temperature rises to a temperature value that has been set via the I²C-bus, a thermal protection pre-warning is activated making pin $\overline{\text{DIAG}}$ LOW. If the temperature continues to rise, all four channels will be muted to reduce the output power (soft thermal clipping). The value at which the temperature mute control activates is fixed: only the temperature at which the thermal protection pre-warning signal occurs can be specified by bit D4 in instruction byte 3. If the temperature mute control does not reduce the average junction temperature, all the power stages will be switched off (muted) at the absolute maximum temperature $T_{j(max)}$.

7.7 Offset detection

Offset detection can only be performed when there is no input signal to the amplifiers, for instance when the external digital signal processor is muted after a start-up. The output voltage of each channel is measured and compared with a reference voltage. If the output voltage of a channel is greater than the reference voltage, bit D2 of the associated data byte is set and read by the microcontroller during a read instruction. Note that the value of this bit is only meaningful when there is no input signal and the amplifier is not muted. Offset detection is always enabled.

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7.8 Speaker protection

If one side of a speaker is connected to ground, a missing current protection is implemented to prevent damage to the speaker. A fault condition is detected in a channel when there is a mismatch between the power current in the high side and the power current in the low side; during a fault condition the channel will be switched off.

The load status of each channel can be read via the I²C-bus: short to ground (one side of the speaker connected to ground), short to V_P (one side of the speaker connected to V_P), and shorted load.

7.9 Line driver mode

An amplifier can be used as a line driver by switching it to low gain mode. In normal mode, the gain between single-ended input and differential output (across the load) is 26 dB. In low gain mode the gain between single-ended input and differential output is 20 dB.

7.10 Input and AC ground capacitor values

The negative inputs to all four amplifier channels are combined at pin ACGND. To obtain the best performance for supply voltage ripple rejection and unwanted audible noise, the value of the capacitor connected to pin ACGND must be as close as possible to 4 times the value of the input capacitor connected to the positive input of each channel.

7.11 DC-load detection

When DC-load detection is enabled, during the start-up cycle, a DC offset is applied slowly to the amplifier outputs, and the output currents are measured. If the output current of an amplifier rises above a certain level, it is assumed that there is a load of less than 6 Ω and bit D5 is reset in the associated data byte register to indicate that a load is detected.

Because the offset is measured during the amplifier start-up cycle, detection is inaudible and can be performed every time the amplifier is switched on.

7.12 I²C-bus address selection

If in the application more amplifiers are used, the I²C-bus address of the TDA8593J; TDA8593Q can be changed with an external resistor; see Section 8.

7.13 AC-load detection

AC-load detection can be used to detect that AC-coupled speakers are connected correctly during assembly. This requires at least 3 periods of a 19 kHz sine wave to be applied to the amplifier inputs. The amplifier produces a peak output voltage which also generates a peak output current through the AC-coupled speaker. The 19 kHz sine wave is also audible during the test. If the amplifier detects three current peaks that are greater than 550 mA, the AC-load detection bit D1 of instruction byte IB1 is set to logic 1. Three current peaks are counted to avoid false AC-load detection which can occur if the input signal is switched on and off. The peak current counter can be reset by setting bit D1 of instruction byte IB1 to logic 0. To guarantee AC-load detection, an amplifier current of more than 550 mA is required. AC-load detection will never occur with a current of less

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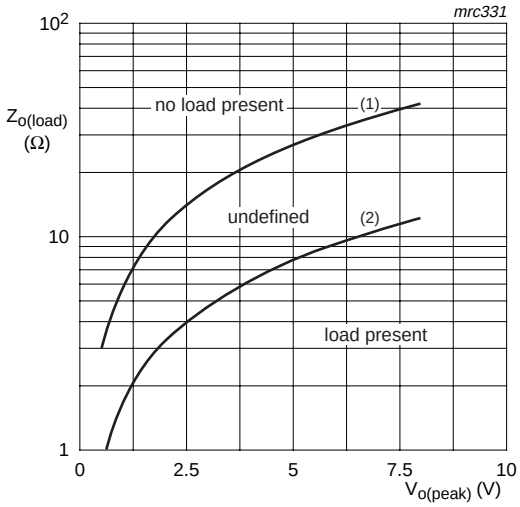
than 150 mA. Figure 3 shows which AC-loads are detected at different output voltages. For example, if a load is detected at an output voltage of 2.5 V (peak), the load is less than 4 Ω. If no load is detected, the output impedance is more than 14 Ω.



(1) $I_{o(peak)}$ < 150 mA.

(2) $I_{o(peak)}$ > 550 mA.

Fig 3. Tolerance of AC detected load as function of the output voltage.

7.14 Load detection procedure

Procedure:

1. At start-up, enable the AC or DC-load detection by setting D1 of instruction byte IB1 to logic 1.
2. After 250 ms the DC-load is detected and the mute is released. This is inaudible and can be implemented each time the IC is powered on.
3. When the amplifier start-up cycle is completed (after 1.5 s), apply an AC signal to the input, and DC-load bits D5 of each data byte should be read and stored by the microcontroller.
4. After at least 3 periods of the input signal, the load status can be checked by reading AC-detect bits D4 of each data byte.

The AC-load peak current counter can be reset by setting bit D1 of instruction byte IB1 to logic 0 and then to logic 1. Note that this will also reset the DC-load detection bits D5 in each data byte.

7.15 Low headroom protection

The normal DC output voltage of the amplifier is set to half the supply voltage and is related to the voltage on pin SVR. An external capacitor is connected to pin SVR to suppress power supply ripple. If the supply voltage drops (at vehicle engine start), the DC output voltage will follow slowly due to the affect of the SVR capacitor.

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The headroom voltage is the voltage required for correct operation of the amplifier and is defined as the voltage difference between the level of the DC output voltage before the V_P voltage drop and the level of V_P after the voltage drop; see Figure 4.

At a certain supply voltage drop, the headroom voltage will be insufficient for correct operation of the amplifier. To prevent unwanted audible noises at the output, the headroom protection mode will be activated; see Figure 9. This protection discharges the capacitors connected to pins SVR and ACGND to increase the headroom voltage.

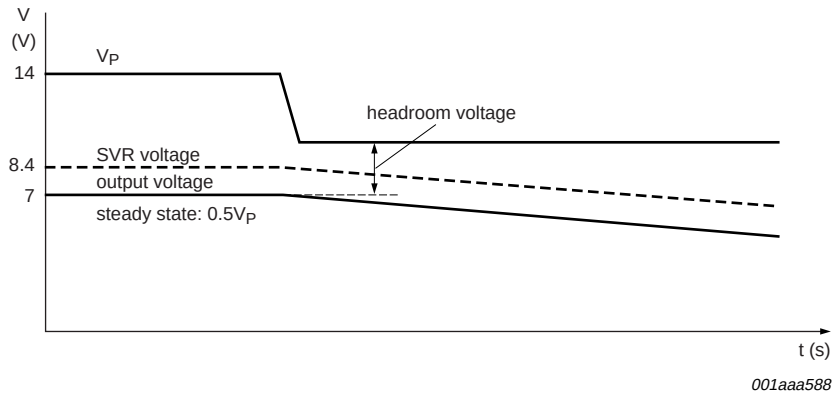

Fig 4. Amplifier output during supply voltage.

8. I²C-bus specification

Table 4: Device address with hardware address selection; see Figure 24.

R_{ADSEL}	A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
300 kΩ	1	1	0	1	1	0	0	0 = write to device
								1 = read from device
27 kΩ	1	1	0	1	1	0	1	0 = write to device
								1 = read from device
1 kΩ	1	1	0	1	1	1	1	0 = write to device
								1 = read from device

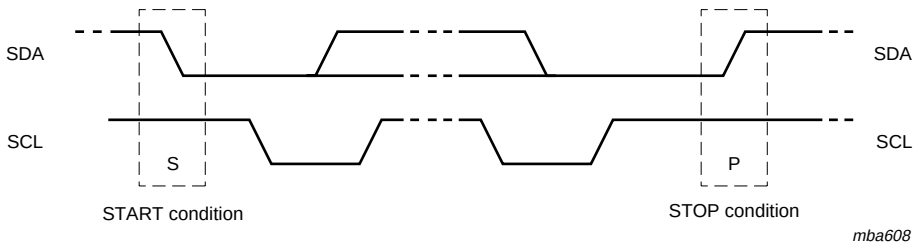

Fig 5. Definition of start and stop conditions.

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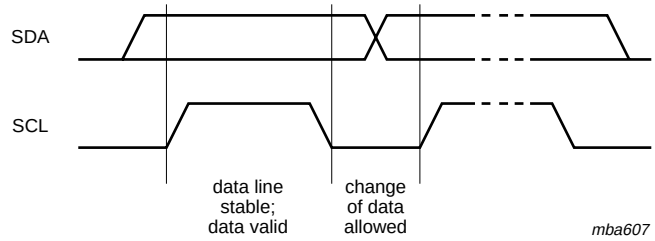

Fig 6. Bit transfer.

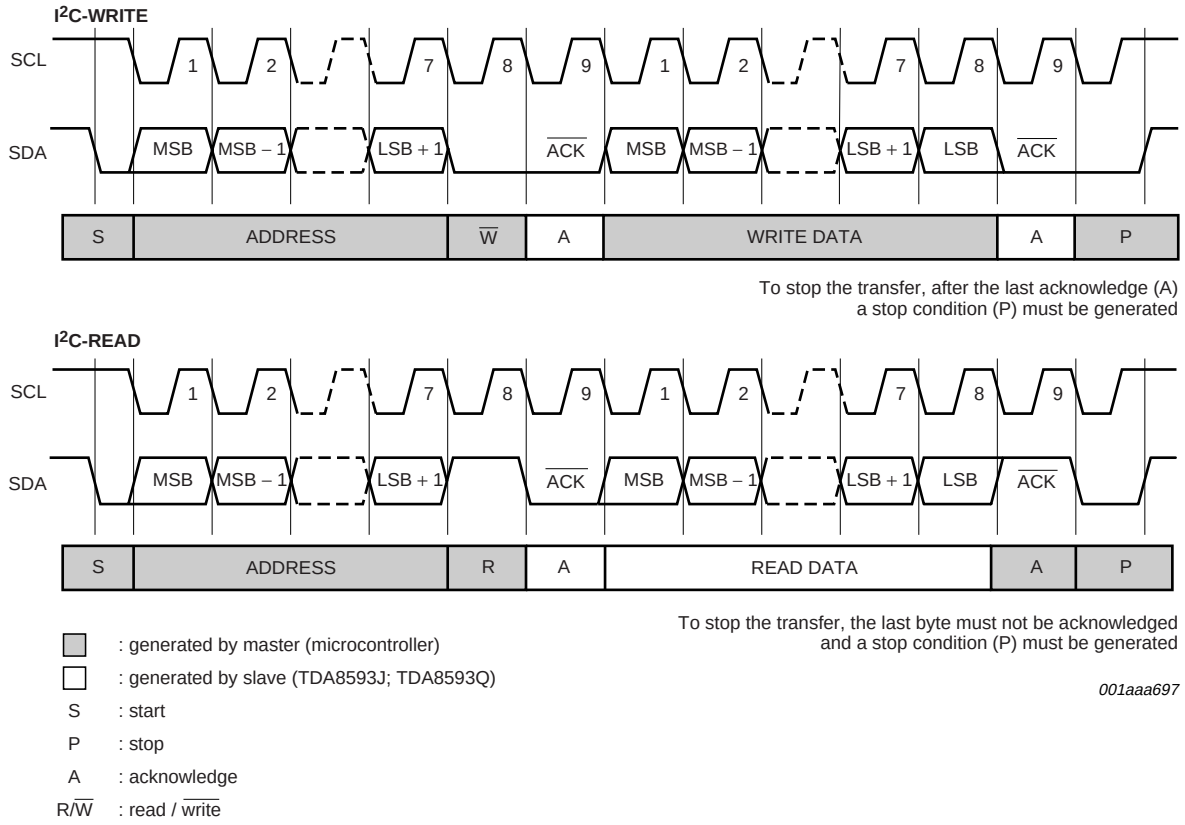

Fig 7. I²C-bus read and write modes.

8.1 Instruction bytes

If bit R/$\overline{W}$ = 0, the TDA8593J; TDA8593Q expects 3 instruction bytes: IB1, IB2 and IB3.

After a power-on reset, all instruction bits are set to zero.

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Table 5: Instruction byte IB1

Bit	Description
D7 to D2	-
D1	AC or DC-load detection switch
	0 = AC or DC-load detection off; resets DC-load detection bits and AC-load detection peak current counter
	1 = AC or DC-load detection on
D0	amplifier start enable (clear power-on reset flag, D7 of DB2)
	0 = amplifier off; pin $\overline{\text{DIAG}}$ remains LOW
	1 = amplifier on; when power-on occurs, bit D7 of DB2 is reset and pin $\overline{\text{DIAG}}$ is released

Table 6: Instruction byte IB2

Bit	Description
D7 to D2	-
D1	soft mute all amplifier channels (mute delay 20 ms)
	0 = no mute
	1 = mute
D0	hard mute all amplifier channels (mute delay 0.4 ms)
	0 = no mute
	1 = mute

Table 7: Instruction byte IB3

Bit	Description
D7	clip detection level
	0 = 3 % detection level
	1 = 1 % detection level
D6	amplifier front channels gain select
	0 = 26 dB (normal mode)
	1 = 20 dB (line driver mode)
D5	amplifier rear channels gain select
	0 = 26 dB (normal mode)
	1 = 20 dB (line driver mode)
D4	amplifier thermal protection pre-warning
	0 = warning level on 145 °C
	1 = warning level on 122 °C
D3	disable RF channel
	0 = RF channel enabled
	1 = RF channel disabled
D2	disable LF channel
	0 = LF channel enabled
	1 = LF channel disabled

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Table 7: Instruction byte IB3 *…continued*

Bit	Description
D1	disable RR channel
	0 = RR channel enabled
	1 = RR channel disabled
D0	disable LR channel
	0 = LR channel enabled
	1 = LR channel disabled

8.2 Data bytes

If bit R/$\overline{W}$ = 1, the TDA8593J; TDA8593Q will sent 4 data bytes to the microcontroller: DB1, DB2, DB3 and DB4.

Table 8: Data byte DB1

Bit	Description
D7	amplifier thermal protection pre-warning
	0 = no warning
	1 = junction temperature above pre-warning level
D6	amplifier maximum thermal protection
	0 = junction temperature below 175 °C
	1 = junction temperature above 175 °C
D5	channel LR DC-load detection
	0 = DC-load detected
	1 = no DC-load detected
D4	channel LR AC-load detection
	0 = no AC-load detected
	1 = AC-load detected
D3	channel LR load short-circuit
	0 = normal load
	1 = short-circuit load
D2	channel LR output offset
	0 = no output offset
	1 = output offset
D1	channel LR V_P short-circuit
	0 = no short-circuit to V_P
	1 = short-circuit to V_P
D0	channel LR ground short-circuit
	0 = no short-circuit to ground
	1 = short-circuit to ground

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Table 9: Data byte DB2

Bit	Description
D7	power-on reset occurred or amplifier status
	0 = amplifier on
	1 = POR has occurred; amplifier off
D6	-
D5	channel RR DC-load detection
	0 = DC-load detected
	1 = no DC-load detected
D4	channel RR AC-load detection
	0 = no AC-load detected
	1 = AC-load detected
D3	channel RR load short-circuit
	0 = normal load
	1 = short-circuit load
D2	channel RR output offset
	0 = no output offset
	1 = output offset
D1	channel RR V_P short-circuit
	0 = no short-circuit to V_P
	1 = short-circuit to V_P
D0	channel RR ground short-circuit
	0 = no short-circuit to ground
	1 = short-circuit to ground

Table 10: Data byte DB3

Bit	Description
D7 to D6	-
D5	channel LF DC-load detection
	0 = DC-load detected
	1 = no DC-load detected
D4	channel LF AC-load detection
	0 = no AC-load detected
	1 = AC-load detected
D3	channel LF load short-circuit
	0 = normal load
	1 = short-circuit load
D2	channel LF output offset
	0 = no output offset
	1 = output offset
D1	channel LF V_P short-circuit
	0 = no short-circuit to V_P
	1 = short-circuit to V_P

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Table 10: Data byte DB3 *…continued*

Bit	Description
D0	channel LF ground short-circuit
	0 = no short-circuit to ground
	1 = short-circuit to ground

Table 11: Data byte DB4

Bit	Description
D7 to D6	-
D5	channel RF DC-load detection
	0 = DC-load detected
	1 = no DC-load detected
D4	channel RF AC-load detection
	0 = no AC-load detected
	1 = AC-load detected
D3	channel RF load short-circuit
	0 = normal load
	1 = short-circuit load
D2	channel RF output offset
	0 = no output offset
	1 = output offset
D1	channel RF V_P short-circuit
	0 = no short-circuit to V_P
	1 = short-circuit to V_P
D0	channel RF ground short-circuit
	0 = no short-circuit to ground
	1 = short-circuit to ground

9. Limiting values

Table 12: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_P	supply voltage	operating	-	18	V
		non operating	–1	+50	V
		load dump protection	0	50	V
V_{SDA}, V_{SCL}	voltage on pins SDA and SCL	operating	0	7	V
V_{INn}, V_{SVR}, V_{ACGND}, $V_{\overline{DIAG}}$	voltage on pins INLF, INLR, INRF, INRR, SVR, ACGND and $\overline{DIAG}$	operating	0	13	V
V_{STB}	voltage on pin STB	operating	0	24	V
I_{OSM}	non-repetitive peak output current		-	10	A
I_{ORM}	repetitive peak output current		-	6	A

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Table 12: Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
T_j	junction temperature			-	150	°C
T_{stg}	storage temperature			–55	+150	°C
T_{amb}	ambient temperature			–40	+85	°C
$V_{P(prot)}$	supply voltage for protections	AC and DC short-circuit voltage of output pins and across the load		-	18	V
P_{tot}	total power dissipation	T_{case} = 70 °C		-	80	W
V_{esd}	electrostatic discharge voltage	HBM	[1]	-	2000	V
		MM	[2]	-	200	V

[1] Human body model: R_s = 1.5 kΩ; C = 100 pF; all pins have passed all tests to 2500 V to guarantee 2000 V, according to class II.

[2] Machine model: R_s = 10 Ω; C = 200 pF; L = 0.75 mH; all pins have passed all tests to 250 V to guarantee 200 V, according to class II.

10. Thermal characteristics

Table 13: Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case		1	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	40	K/W

11. Characteristics

Table 14: Characteristics

T_{amb} = 25 °C; V_P = 14.4 V, R_L = 4 Ω; measured in test circuit Figure 24; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage behavior						
V_{P1}, V_{P2}	operating supply voltage	R_L = 4 Ω	8	14.4	18	V
		R_L = 2 Ω	8	14.4	16	V
I_q	quiescent current	no load	-	280	400	mA
I_{stb}	standby current		-	10	50	µA
V_O	DC output voltage		-	7.2	-	V
$V_{P(mute)}$	low supply voltage mute		6.5	7	8	V
V_{hr}	headroom voltage	when headroom protection activated; see Figure 4	-	1.4	-	V
V_{POR}	power-on reset voltage	see Figure 10	-	5.5	-	V
V_{OO}	output offset voltage	mute mode and power on	–100	0	+100	mV
Mode select (pin STB)						
V_{stb}	standby mode voltage		-	-	1.3	V
V_{oper}	operating mode voltage		2.5	-	5.5	V

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Table 14: Characteristics *...continued*

T_{amb} = 25 °C; V_P = 14.4 V, R_L = 4 Ω; measured in test circuit Figure 24; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{mute}	mute mode voltage		8	-	V_P	V
I_I	input current	V_{STB} = 5 V	-	4	25	µA
Start-up, shut-down and mute timing						
t_{wake}	wake-up time from standby before first I²C-bus transmission is recognized	via pin STB; see Figure 8	-	300	500	µs
$t_{mute(off)}$	time from amplifier switch-on to mute release	via I²C-bus D0(IB1) = 1; C_{SVR} = 22 µF; see Figure 8	-	250	-	ms
$t_{d(mute-on)}$	delay from mute to on (soft mute)	D1(IB2) = 1 → 0	10	25	40	ms
	delay from mute to on (fast mute)	D0(IB2) = 1 → 0	10	25	40	ms
	delay from mute to on via pin STB	V_{STB} from 8 V to 4 V	10	25	40	ms
$t_{d(on-mute)}$	delay from on to mute (soft mute)	D1(IB2) = 0 → 1	10	25	40	ms
	delay from on to mute (fast mute)	D0(IB2) = 0 → 1	-	0.4	1	ms
	delay from on to mute via pin STB	V_{STB} from 4 V to 8 V	-	0.4	1	ms
I²C-bus interface						
V_{IL}	LOW-level input voltage on pins SCL and SDA		-	-	1.5	V
V_{IH}	HIGH-level input voltage on pins SCL and SDA		2.3	-	5.5	V
V_{OL}	LOW-level output voltage on pin SDA	I_L = 3 mA	-	-	0.4	V
f_{SCL}	clock frequency		-	-	400	kHz
R_{ADSEL}	resistor value for address selection	I²C-bus address D8/D9h	200	300	∞	kΩ
		I²C-bus address DA/DBh	15	27	36	kΩ
		I²C-bus address DE/DFh	0	1	1.6	kΩ
Diagnostic						
$V_{DIAG(L)}$	LOW-level output voltage on pin DIAG	fault condition; I_{DIAG} = 200 µA	-	-	0.8	V
$V_{o(offset)}$	output voltage when offset is detected		±1.5	±2	±2.5	V
THD_{clip}	THD clip detection level	D7(IB3) = 0	-	3	-	%
		D7(IB3) = 1	-	1	-	%
$T_{j(warn1)}$	average junction temperature for pre-warning 1	D4(IB3) = 0	135	145	155	°C
$T_{j(warn2)}$	average junction temperature for pre-warning 2	D4(IB3) = 1	112	122	132	°C

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Table 14: Characteristics *...continued*

T_{amb} = 25 °C; V_P = 14.4 V, R_L = 4 Ω; measured in test circuit Figure 24; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{j(mute)}$	average junction temperature for 3 dB muting	V_{IN} = 0.05 V	150	160	170	°C
$T_{j(off)}$	average junction temperature when all outputs are switched off		165	175	185	°C
$Z_{o(load)}$	impedance when a DC-load is detected		-	-	6	Ω
$Z_{o(open)}$	impedance when an open DC-load is detected		500	-	-	Ω
$I_{o(load)}$	amplifier current when the AC-load bit is set		550	-	-	mA
$I_{o(open)}$	amplifier current when the AC-load bit is not set		-	-	150	mA
Amplifier						
P_o	output power	R_L = 4 Ω; V_P = 14.4 V; THD = 0.5 %	18	19	-	W
		R_L = 4 Ω; V_P = 14.4 V; THD = 10 %	25	26	-	W
		R_L = 4 Ω; V_P = 14.4 V; V_{IN} = 2 V (RMS) square wave (maximum power)	39	41	-	W
		R_L = 4 Ω; V_P = 15.2 V; V_{IN} = 2 V (RMS) square wave (maximum power)	44	46	-	W
		R_L = 2 Ω; V_P = 14.4 V; THD = 0.5 %	27	31	-	W
		R_L = 2 Ω; V_P = 14.4 V; THD = 10 %	40	44	-	W
		R_L = 2 Ω; V_P = 14.4 V; V_{IN} = 2 V (RMS) square wave (maximum power)	64	69	-	W
THD	total harmonic distortion	P_o = 1 W to 12 W; f = 1 kHz; R_L = 4 Ω	-	0.01	0.1	%
		P_o = 1 W to 12 W; f = 10 kHz	-	0.2	0.5	%
		P_o = 4 W; f = 1 kHz	-	0.01	0.03	%
		line driver mode; V_o = 2 V (RMS); f = 1 kHz; R_L = 600 Ω	-	0.01	0.03	%
α_{CS}	channel separation (crosstalk)	1 kHz to 10 kHz; R_{source} = 600 Ω	50	60	-	dB
		P_o = 4 W; f = 1 kHz	-	80	-	dB
SVRR	supply voltage ripple rejection	100 Hz to 10 kHz; R_{source} = 600 Ω	55	70	-	dB

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Table 14: Characteristics *...continued*

T_{amb} = 25 °C; V_P = 14.4 V, R_L = 4 Ω; measured in test circuit Figure 24; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CMRR	common mode ripple rejection	amplifier mode; V_{cm} = 0.3 V (p-p); f = 1 kHz to 3 kHz; R_{source} = 0 Ω	40	70	-	dB
$V_{cm(max)(rms)}$	maximum common mode voltage level (RMS value)	f = 1 kHz	-	-	0.6	V
$V_{n(o)(LN)}$	noise output voltage in line driver mode	filter: 20 Hz to 22 kHz; R_{source} = 600 Ω	-	25	35	μV
$V_{n(o)(amp)}$	noise output voltage in amplifier mode	filter: 20 Hz to 22 kHz; R_{source} = 600 Ω	-	50	70	μV
$G_{v(amp)}$	voltage gain in amplifier mode	single-ended input to differential output	25	26	27	dB
$G_{v(LN)}$	voltage gain in line driver mode	single-ended input to differential output	19	20	21	dB
Z_i	input impedance	C_{IN} = 220 nF	55	70	-	kΩ
α_{mute}	mute attenuation	$V_{o(on)}/V_{o(mute)}$	80	90	-	dB
$V_{o(mute)}$	mute output voltage	V_{IN} = 1 V (RMS)	-	70	-	μV
B_p	power bandwidth	−1 dB; THD = 1 %	-	20	-	kHz

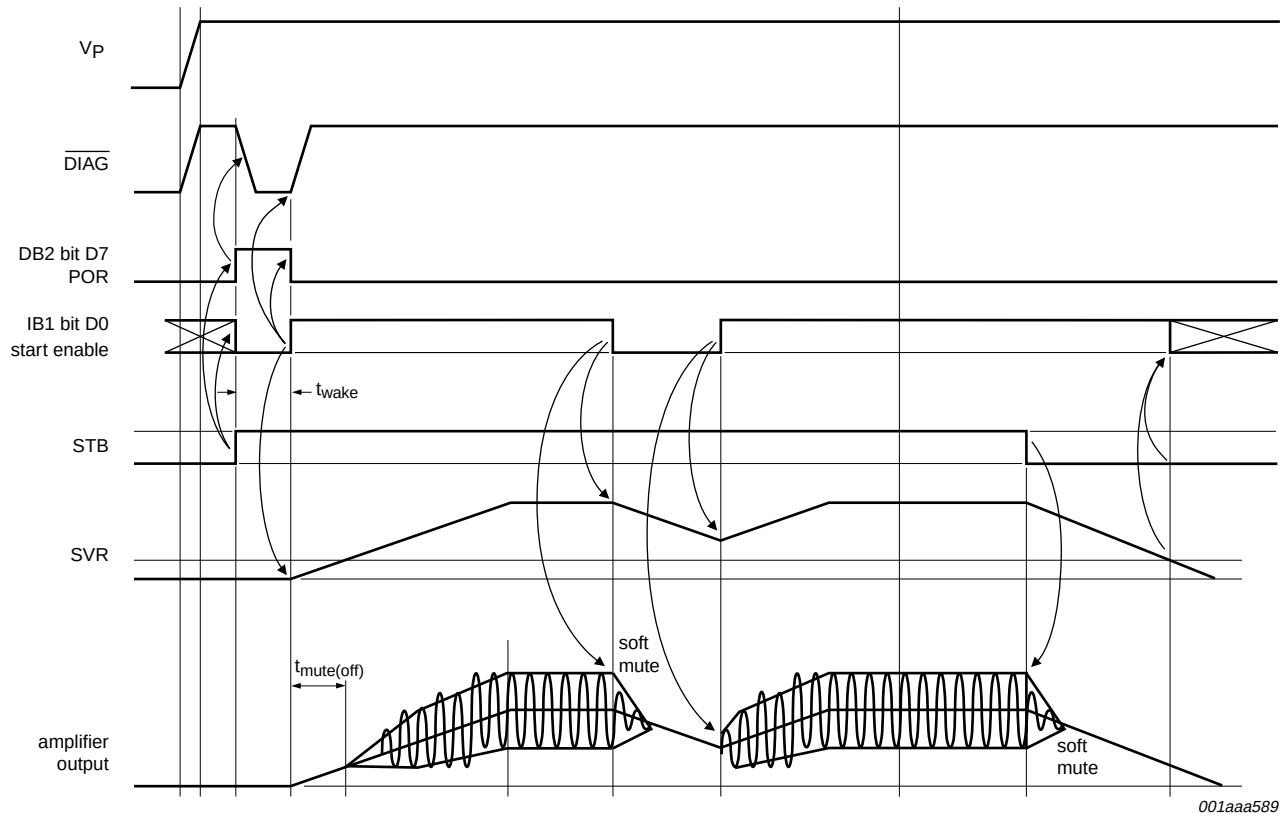

Fig 8. Start-up and shut-down timing.

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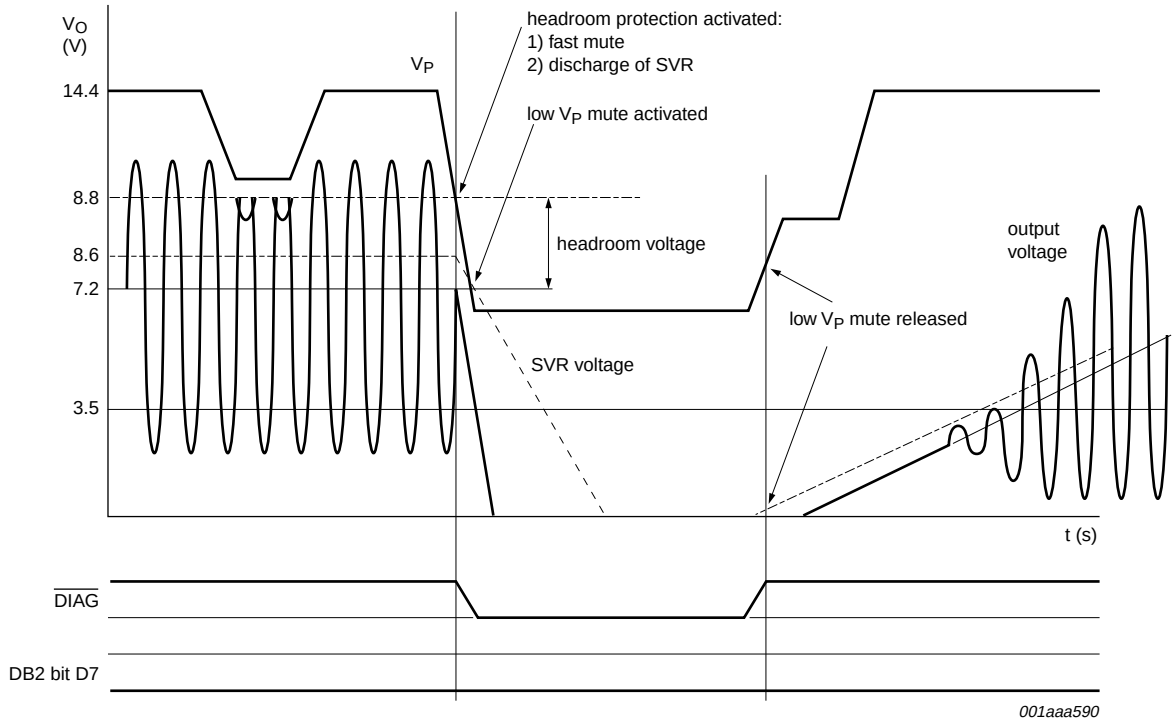

Fig 9. Low V_P behavior (V_P > 5.5 V).

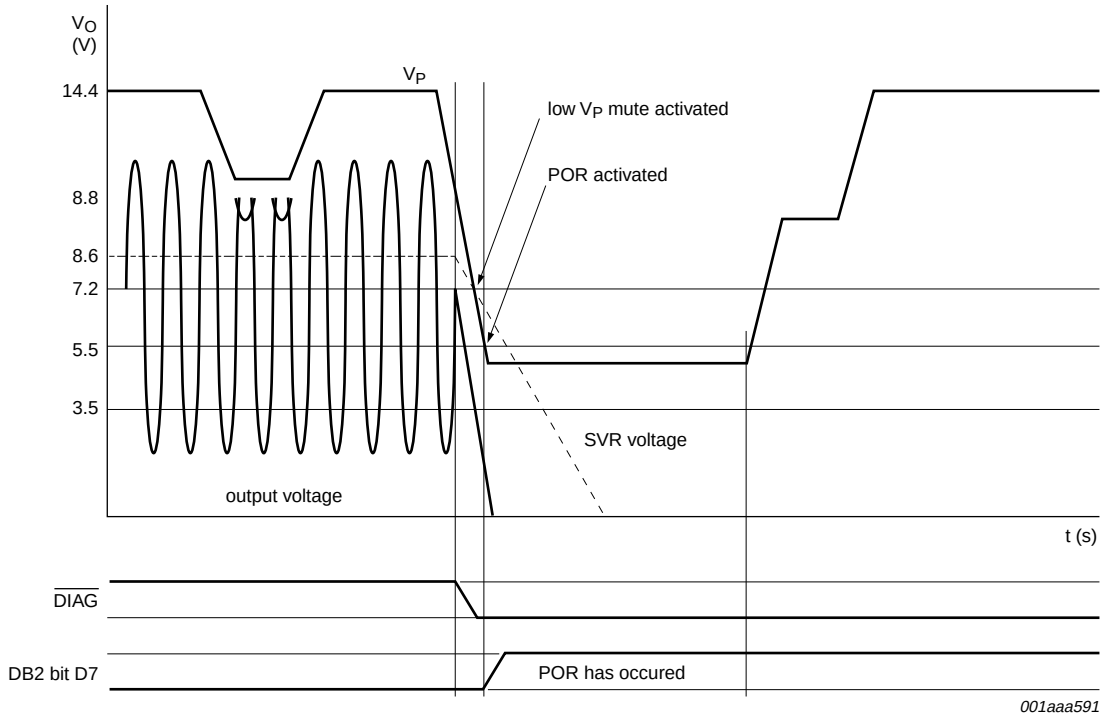

Fig 10. Low V_P behavior (V_P < 5.5 V).

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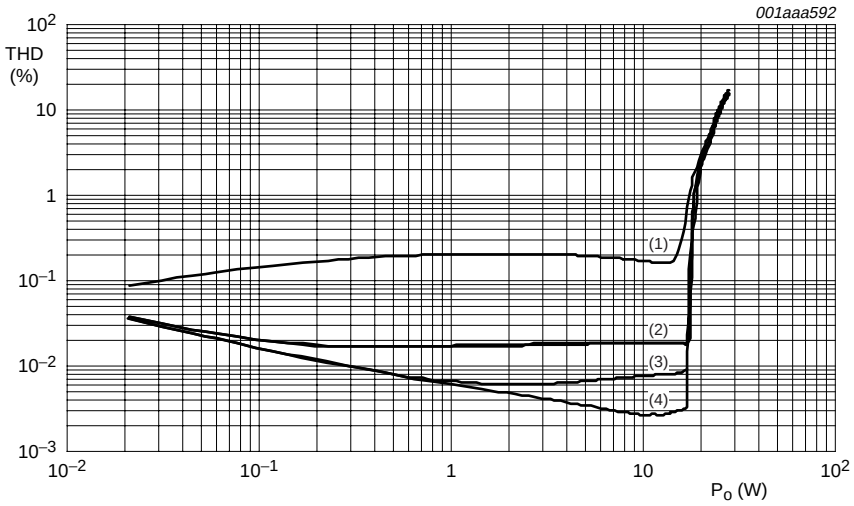
11.1 Performance diagrams

11.1.1 THD as function of output power P_o for different frequencies



(1) V_P = 14.4 V; R_L = 4 Ω; all channels 10 kHz.

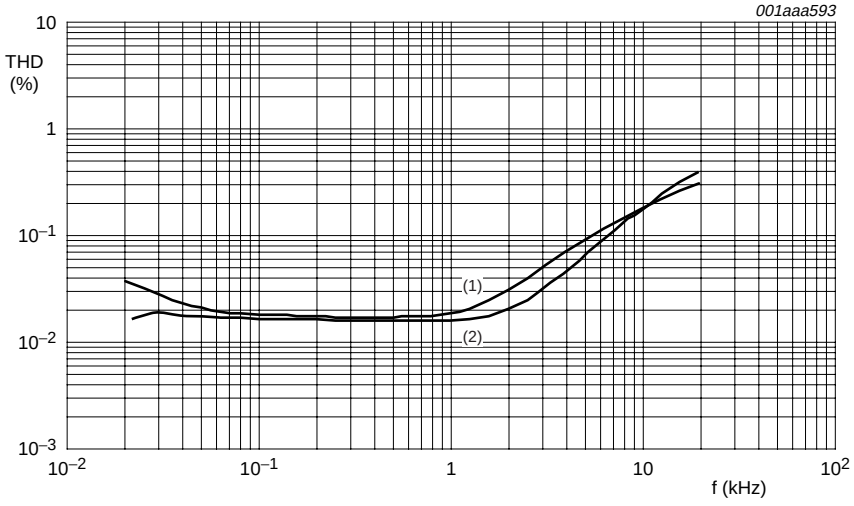
(2) V_P = 14.4 V; R_L = 4 Ω; front channels 100 Hz and 1 kHz.

(3) V_P = 14.4 V; R_L = 4 Ω; rear channels 1 kHz.

(4) V_P = 14.4 V; R_L = 4 Ω; rear channels 100 Hz.

Fig 11. THD as function of P_o.

11.1.2 THD as function of frequency for different output powers



(1) V_P = 14.4 V; R_L = 4 Ω; front channels; P_o = 1 W.

(2) V_P = 14.4 V; R_L = 4 Ω; front channels; P_o = 10 W.

Fig 12. THD as function of frequency for front channels.

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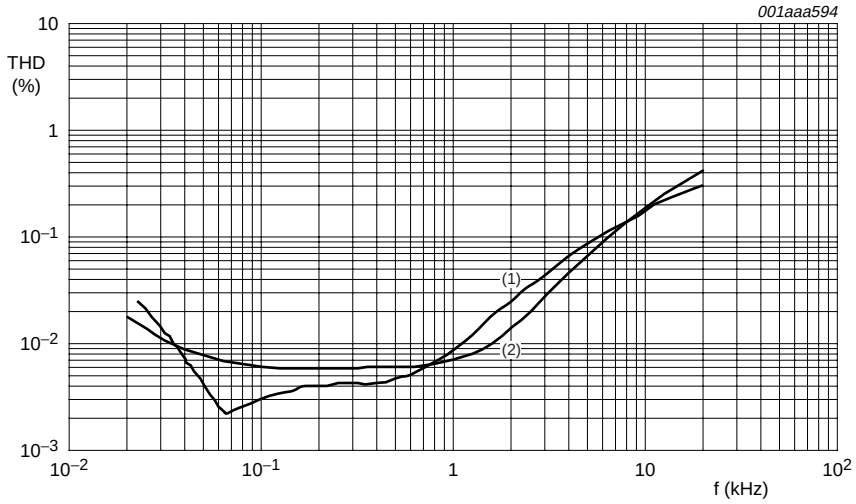
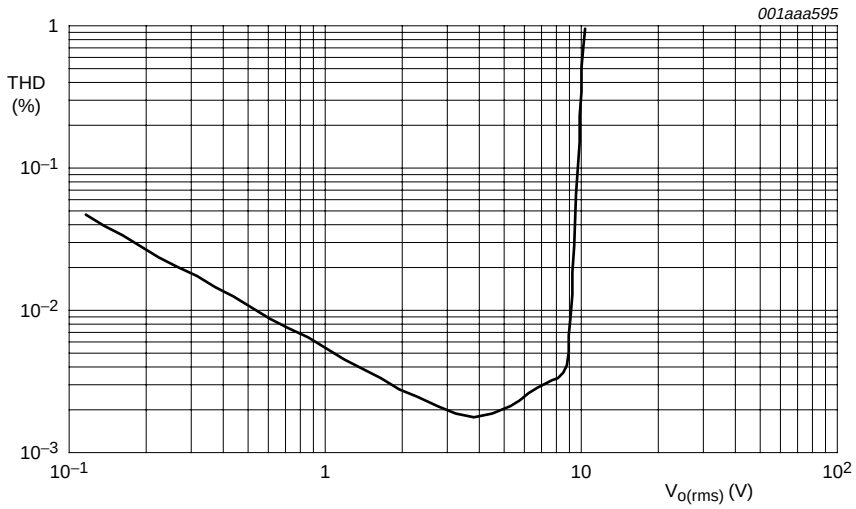


(1) V_P = 14.4 V; R_L = 4 Ω; rear channels; P_o = 10 W.

(2) V_P = 14.4 V; R_L = 4 Ω; rear channels; P_o = 1 W.

Fig 13. THD as function of frequency for rear channels.

11.1.3 Line driver mode



V_P = 14.4 V; R_L = 600 Ω; f = 1 kHz.

Fig 14. THD as function of V_o in balanced line driver mode.

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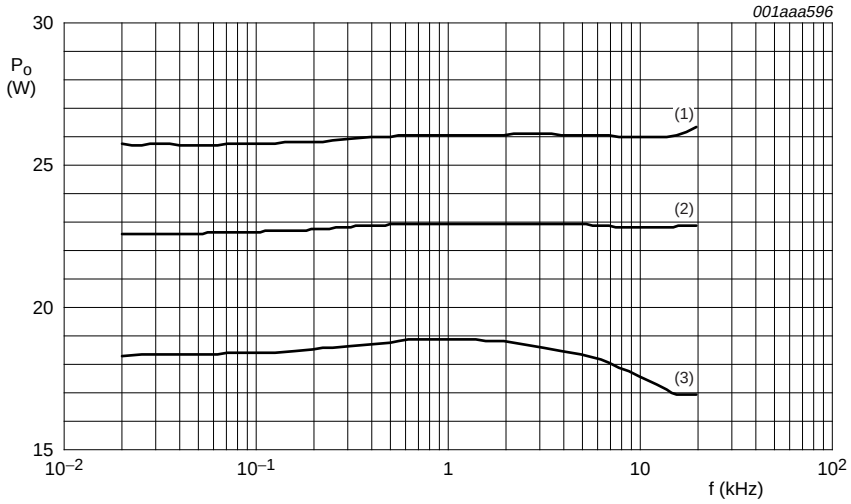
11.1.4 Output power as function of frequency for different THD levels

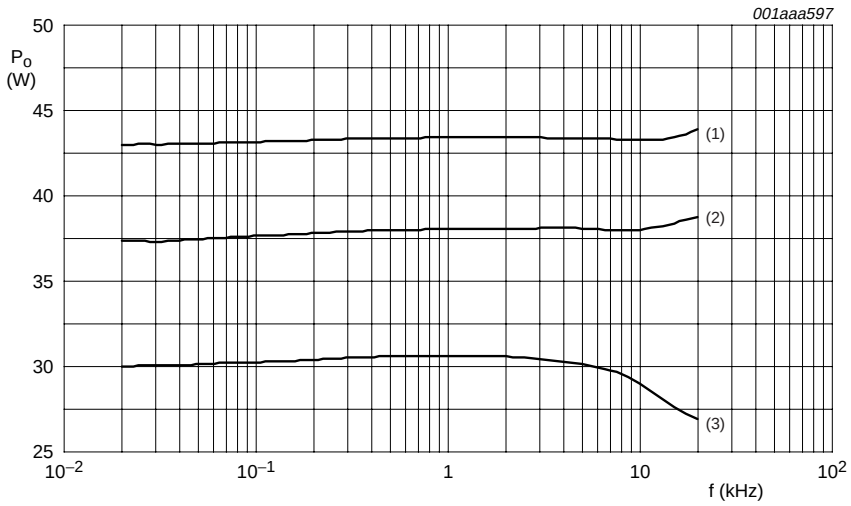


(1) V_P = 14.4 V; R_L = 4 Ω; THD = 10 %.

(2) V_P = 14.4 V; R_L = 4 Ω; THD = 5 %.

(3) V_P = 14.4 V; R_L = 4 Ω; THD = 0.5 %.

Fig 15. P_o as function of frequency at 4 Ω load.



(1) V_P = 14.4 V; R_L = 2 Ω; THD = 10 %.

(2) V_P = 14.4 V; R_L = 2 Ω; THD = 5 %.

(3) V_P = 14.4 V; R_L = 2 Ω; THD = 0.5 %.

Fig 16. P_o as function of frequency at 2 Ω load.

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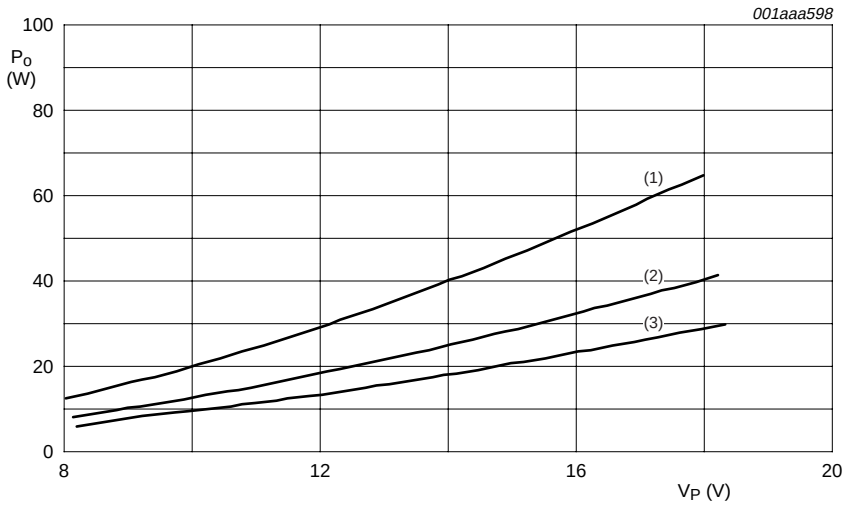
11.1.5 Output power as function of supply voltage

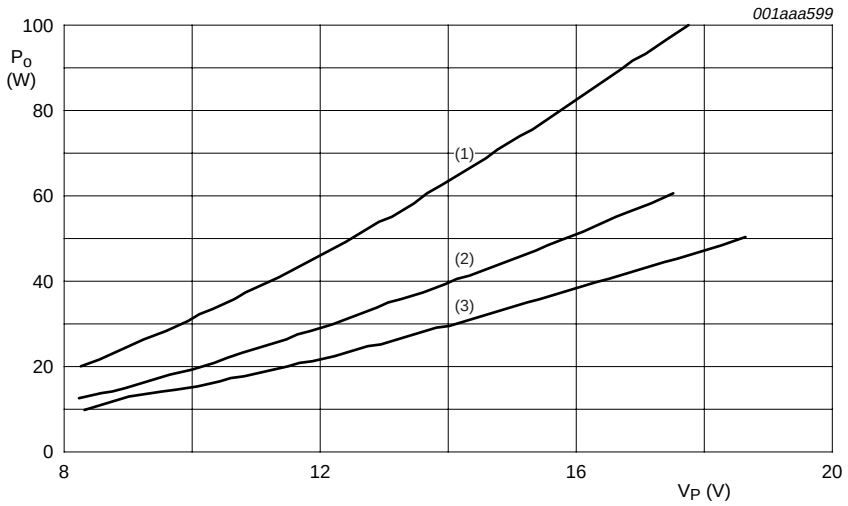


(1) f = 1 kHz; R_L = 4 Ω; maximum P_o.

(2) f = 1 kHz; R_L = 4 Ω; THD = 10 %.

(3) f = 1 kHz; R_L = 4 Ω; THD = 0.5 %.

Fig 17. P_o as function of supply voltage at 4 Ω load.



(1) f = 1 kHz; R_L = 2 Ω; maximum P_o.

(2) f = 1 kHz; R_L = 2 Ω; THD = 10 %.

(3) f = 1 kHz; R_L = 2 Ω; THD = 0.5 %.

Fig 18. P_o as function of supply voltage at 2 Ω load.

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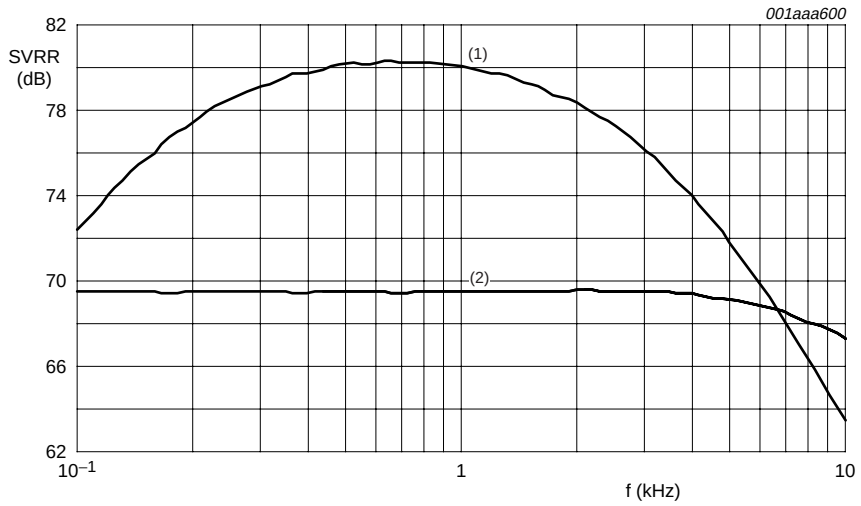
11.1.6 Supply voltage ripple rejection in operating and mute mode

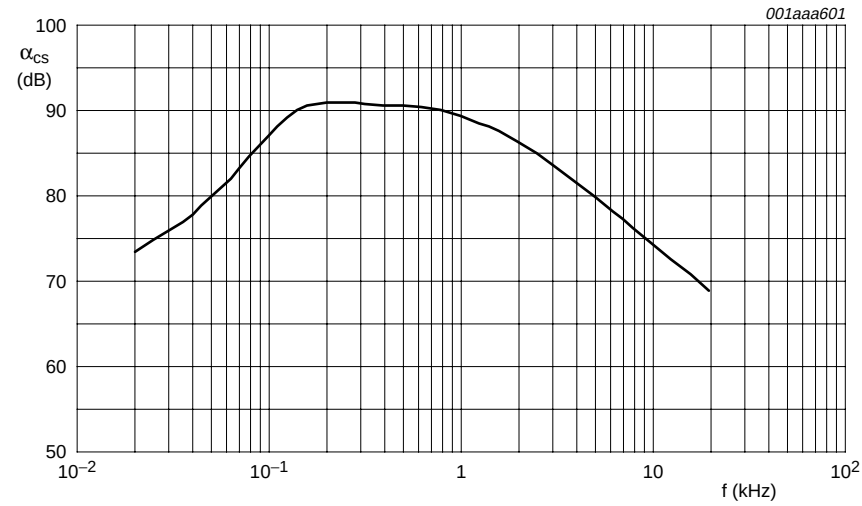


(1) V_P = 14.4 V; R_L = 4 Ω; V_{ripple} = 2 V (p-p); R_{in} = 600 Ω; operating.

(2) V_P = 14.4 V; R_L = 4 Ω; V_{ripple} = 2 V (p-p); R_{in} = 600 Ω; mute.

Fig 19. SVRR as function of frequency, in operating and mute.

11.1.7 Channel separation as function of frequency



V_P = 14.4 V; R_L = 4 Ω; P_o = 4 W; R_{in} = 600 Ω.

Fig 20. Channel separation as function of frequency.

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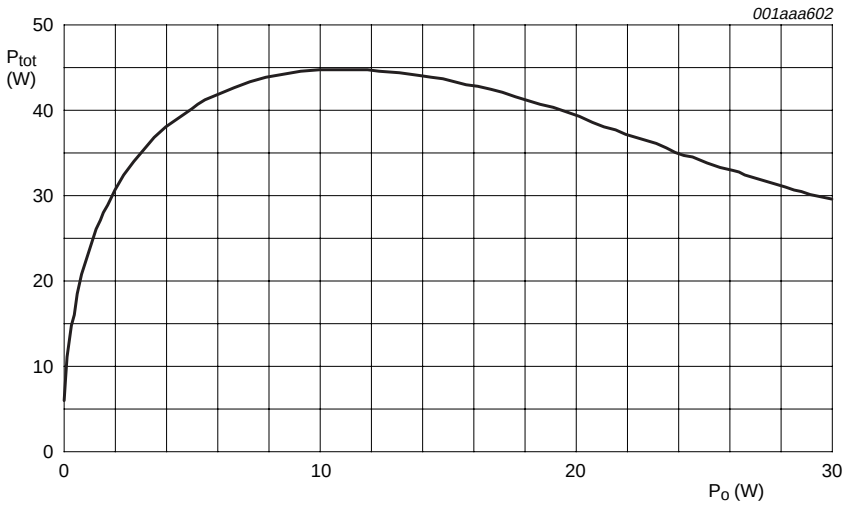
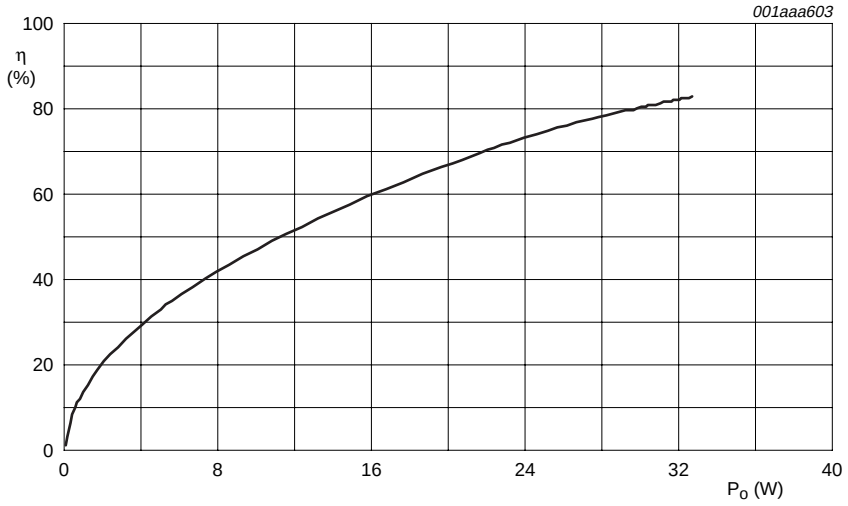
11.1.8 Power dissipation and efficiency



V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz.

Fig 21. Power dissipation as function of output power per channel (4 channels driven).



V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz.

Fig 22. Efficiency as function of output power per channel (4 channels driven).

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12. Application information

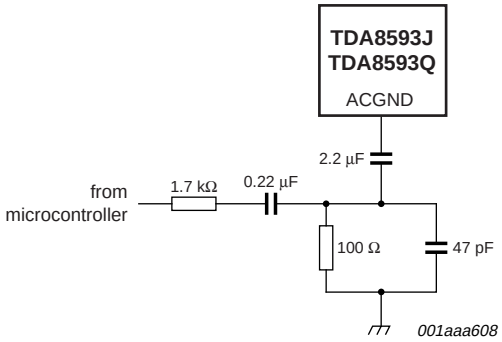

Fig 23. Beep input application diagram.

The beep input circuit is to amplify the beep signal from the microcontroller to all 4 amplifiers (gain = 0 dB).

Remark: This circuit will not effect the amplifier performance.

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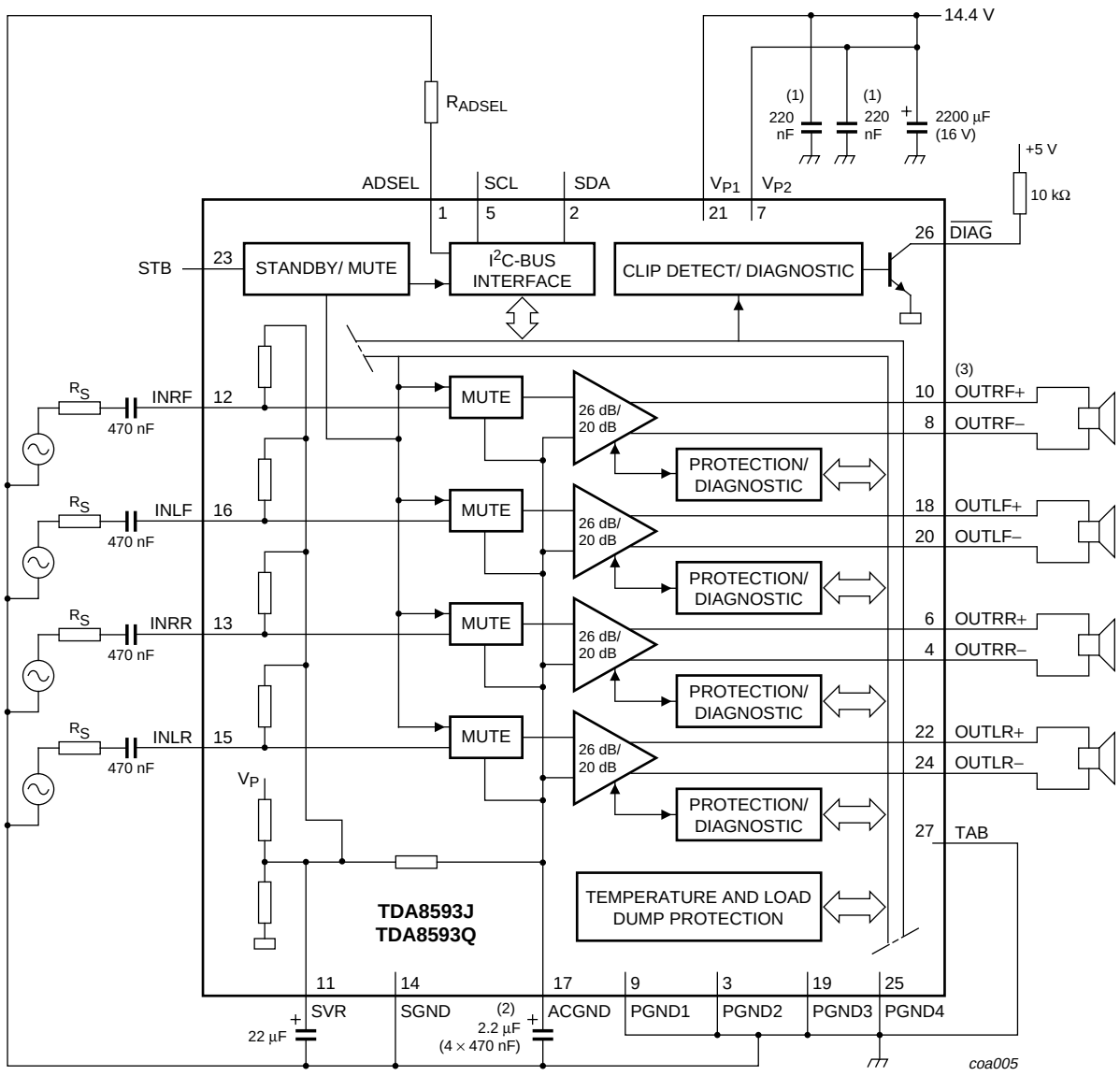
12.1 Test and application information



(1) Supply decoupling:
The high frequency decoupling capacitors (220 nF) should be connected as close as possible to the supply pins.
It is important that these capacitors are of a good quality. When several channels are shorted to the supply simultaneously, high peak voltages can occur at the supply line due to the activation of the protections. The high frequency decoupling capacitors should suppress these voltage peaks.
Good results have been achieved with 0805 case size capacitors (X7R material, 220 nF) connected close to each of the supply pins.

(2) The ACGND capacitor value must be close to four times the input capacitor value.

(3) A capacitor of 10 nF may be added from every amplifier output to ground for EMC reasons.

Fig 24. Test and application diagram.

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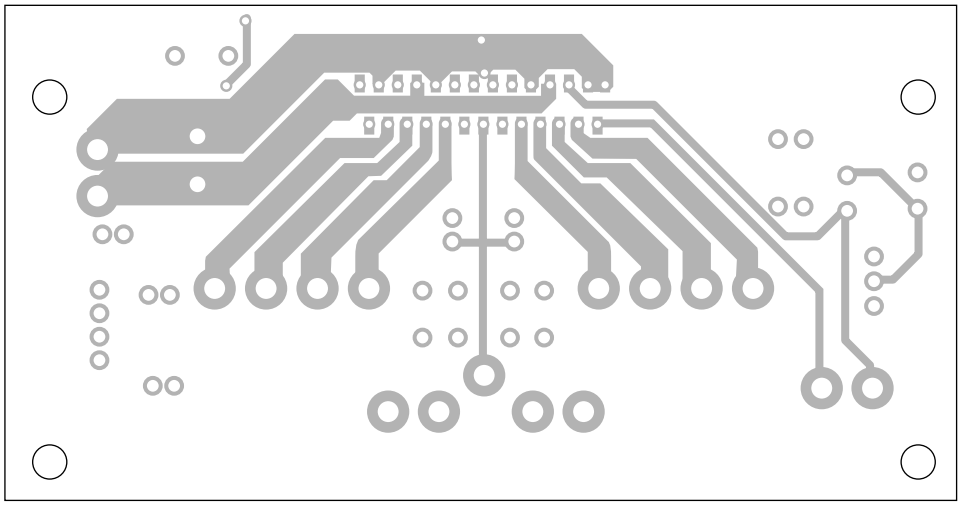
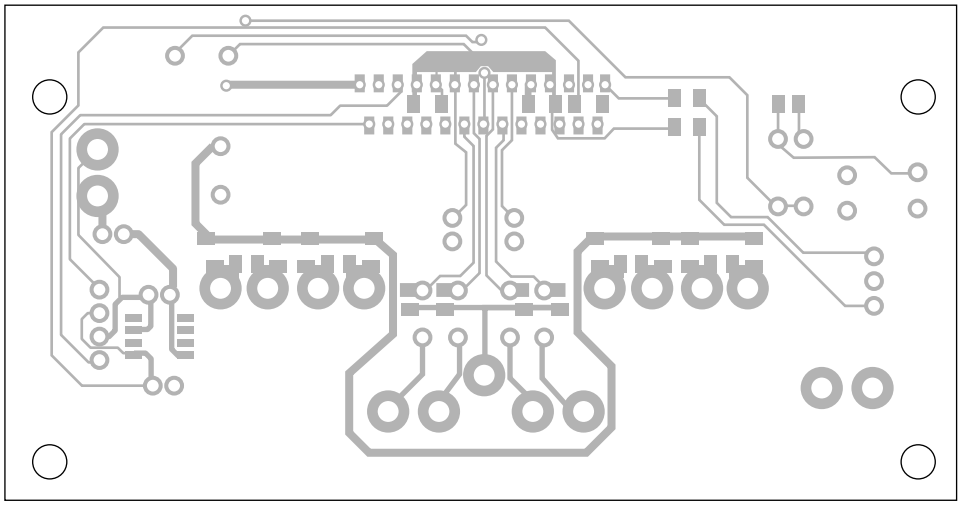
12.2 PCB layout



001aaa604

Fig 25. PCB layout of test and application circuit; copper layer top.



001aaa605

Fig 26. PCB layout of test and application circuit; copper layer bottom.

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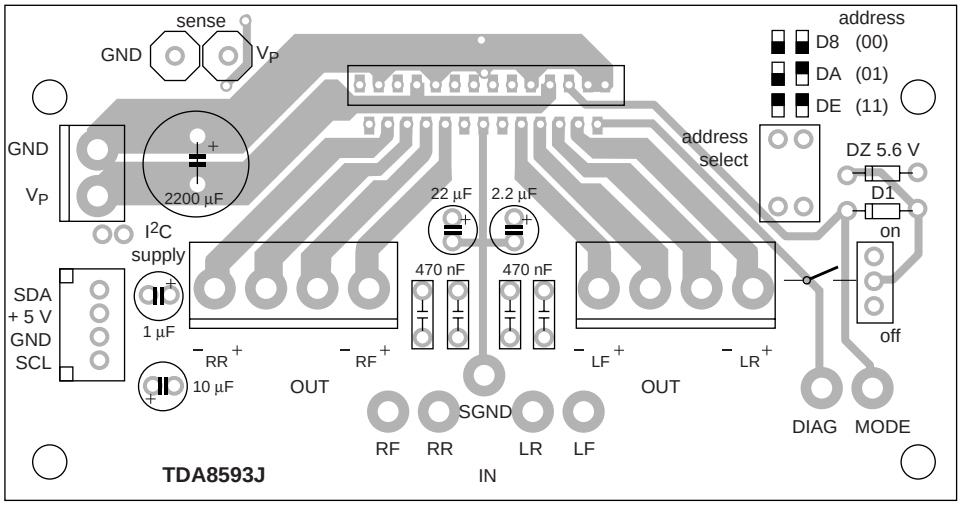
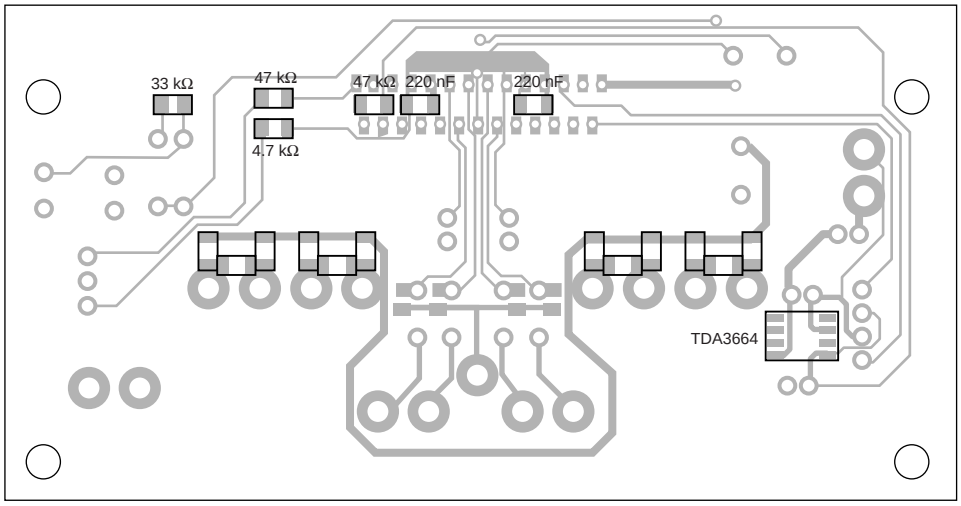


001aaa606

Fig 27. PCB layout of test and application circuit; components top.



001aaa607

Fig 28. PCB layout of test and application circuit; components bottom.

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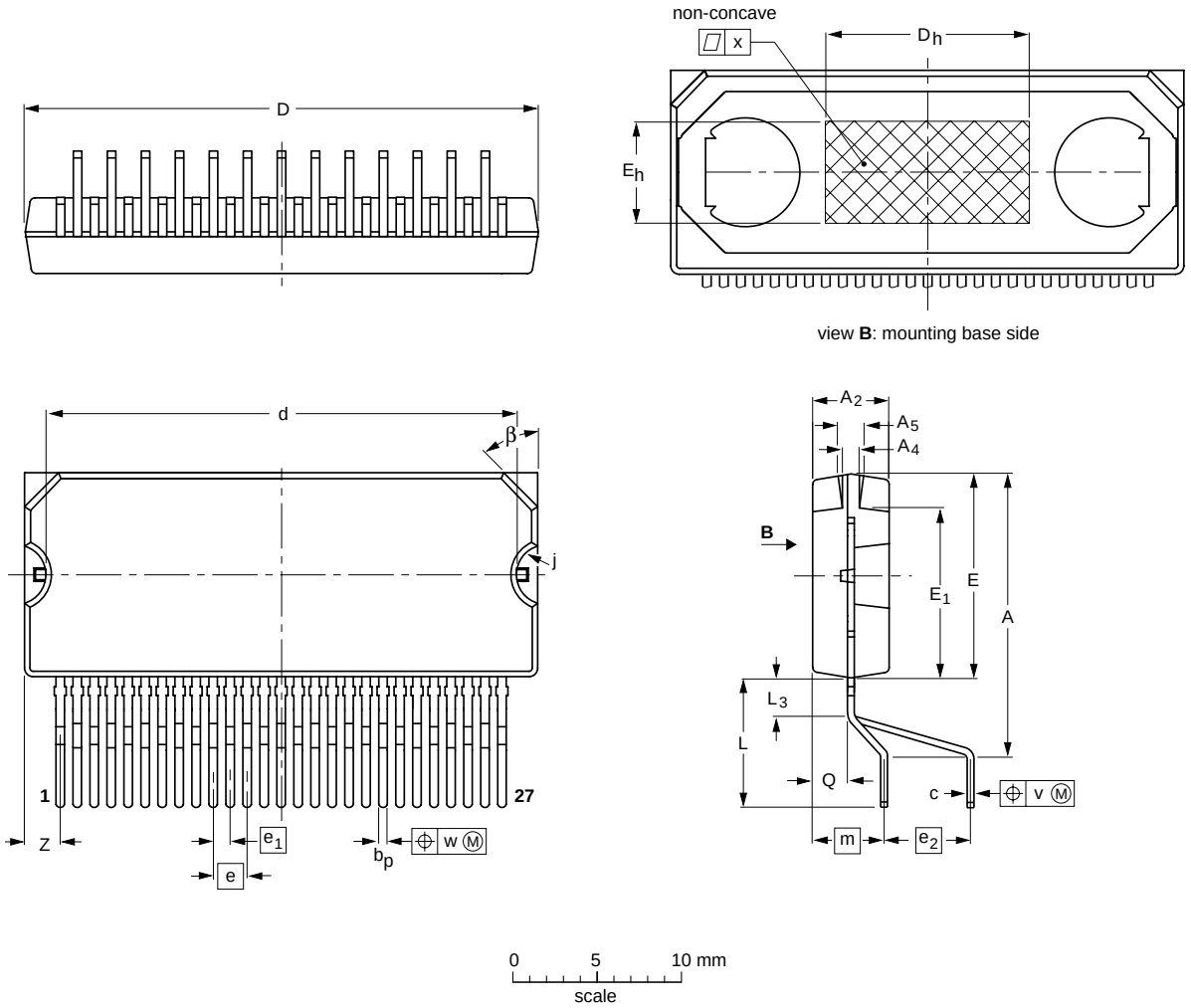
13. Package outline

DBS27P: plastic DIL-bent-SIL (special bent) power package; 27 leads (lead length 7.7 mm) **SOT767-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	A_4	A_5	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	E_1	j	L	L_3	m	Q	v	w	x	β	$Z^{(1)}$
mm	17.0 15.5	4.6 4.3	1.15 0.85	1.65 1.35	0.60 0.45	0.5 0.3	30.4 29.9	28.0 27.5	12	12.2 11.8	2	1	4	6	10.15 9.85	1.85 1.65	8.4 7.0	2.4 1.6	4.3	2.1 1.8	0.6	0.25	0.03	45°	2.4 1.8

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT767-1						02-05-02

Fig 29. Package outline SOT767-1.

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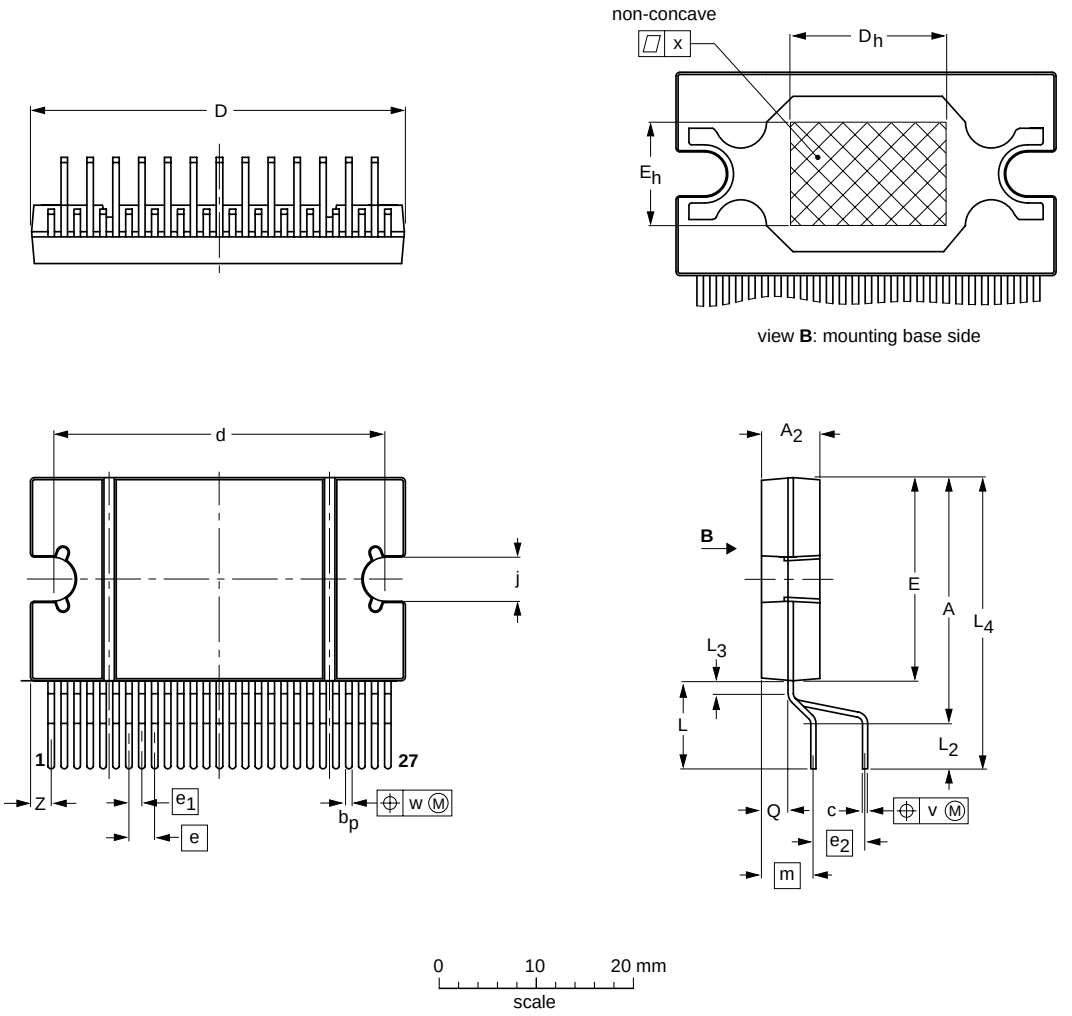
DBS27P: plastic DIL-bent-SIL (special bent) power package; 27 leads (lead length 6.8 mm) **SOT827-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	j	L	L_2	L_3	L_4	m	Q	v	w	x	$Z^{(1)}$
mm	19	4.65 4.35	0.60 0.45	0.5 0.3	29.2 28.8	25.8 25.4	12	15.9 15.5	2	1	4	8	3.4 3.1	6.8	3.9 3.1	1.15 0.85	22.9 22.1	4	2.1 1.8	0.6	0.25	0.03	1.8 1.2

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT827-1	- - -	- - -	- - -			03-07-29

Fig 30. Package outline SOT827-1.

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14. Revision history

Table 15: Revision history

Document ID	Release date	Data sheet status	Change notice	Order number	Supersedes
TDA8593_1	20040609	Preliminary data sheet	-	9397 750 13008	-

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15. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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For additional information, please visit: **http://www.semiconductors.philips.com**

For sales office addresses, send an email to: **sales.addresses@www.semiconductors.philips.com**

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20. Contents

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