# TDA8757C

Triple 8-bit ADC 205 Msps

**Rev. 01 — 14 August 2002** **Preliminary data**

## 1. General description

The TDA8757C is a triple 8-bit ADC for the digitizing of large bandwidth RGB/YUV signals at a sampling rate up to 205 Msps.

The IC supports display resolutions up to $1600 \times 1200$ (UXGA) at 75 Hz.

The IC also includes a PLL that can be locked to the horizontal line frequency and generates the ADC clock. The PLL jitter is minimized for high resolution PC graphics applications. An external clock signal can also be used to clock the ADC.

The outputs are available either on one port up to 110 Msps or on two ports up to 205 Msps. The operating mode is selectable via the serial interface for either I$^2$C-bus or 3-wire serial bus (3W-bus) operation.

The clamp level, the gain and the other settings are controllable through the serial interface.

## 2. Features

- Triple 8-bit ADC
- Sampling rate up to 205 Msps
- IC controllable by a serial interface which can be I$^2$C-bus or 3W-bus, selected by a TTL input pin
- Three clamps for programming a clamping code from −63.5 to +64 in steps of ½ LSB (RGB) and from +120 to +136 in steps of ½ LSB (YUV)
- Three controllable amplifiers: gain controlled through the serial interface to produce a full-scale resolution of ½ LSB peak-to-peak
- Amplifier bandwidth of 250 MHz
- Low gain variation with temperature
- PLL controllable with the serial interface to generate the ADC clock which can be locked to any line frequency of 15 to 150 kHz
- Integrated PLL divider
- Programmable phase clock adjustment cells
- Internal voltage regulators
- TTL compatible digital inputs and outputs
- Outputs on one port or demultiplexed on two ports; selectable with the serial interface
- Chip enable high-impedance ADC output via the I$^2$C-bus
- Power-down mode via the I$^2$C-bus
- 1.7 W power dissipation

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- Sync on green extractor.

## 3. Applications

- RGB/YUV high-speed digitizing
- LCD panels driver
- LCD projection systems
- VGA to UXGA (1600 × 1200 at 75 Hz) modes.

## 4. Quick reference data

**Table 1: Quick reference data**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CCA}$ | analog supply voltage for PLL and the RGB channels | | 4.75 | 5.0 | 5.25 | V |
| $V_{DDD}$ | logic supply voltage for $I^2C$-bus and 3W-bus | | 4.75 | 5.0 | 5.25 | V |
| $V_{CCD}$ | digital supply voltage | | 4.75 | 5.0 | 5.25 | V |
| $V_{CCO}$ | output stages supply voltage for PLL and the RGB channels | | 3.0 | 3.3 | 3.6 | V |
| $V_{CCA(PLL)}$ | analog PLL supply voltage | | 4.75 | 5.0 | 5.25 | V |
| $V_{CCO(PLL)}$ | output PLL supply voltage | | 3.0 | 3.3 | 3.6 | V |
| $I_{CCA}$ | analog supply current for the RGB channels | | – | 135 | – | mA |
| $I_{DDD}$ | logic supply current for $I^2C$-bus and 3W-bus | | – | 1 | – | mA |
| $I_{CCD}$ | digital supply current | | – | 95 | – | mA |
| $I_{CCO}$ | output stages supply current | | – | 80 | – | mA |
| $I_{CCA(PLL)}$ | analog PLL supply current | | – | 34 | – | mA |
| $f_{clk}$ | clock frequency | normal (Dmx = 0) | – | – | 110 | MHz |
| | | demultiplexed (Dmx = 1) | – | – | 205 | MHz |
| $f_{ref(PLL)}$ | PLL reference clock frequency | | 15 | – | 150 | kHz |
| $f_{PLL}$ | output clock frequency range | | 12 | – | 205 | MHz |
| INL | DC integral non-linearity | from analog input to digital output; full-scale; sine wave input; $f_{clk}$ = 205 MHz | – | ±0.5 | ±1.5 | LSB |
| DNL | DC differential non-linearity | from analog input to digital output; full-scale; sine wave input; $f_{clk}$ = 205 MHz | – | ±0.4 | ±1 | LSB |
| $\Delta G_{amp}/\Delta T$ | amplifier gain stability variation with temperature | $V_{ref}$ = 2.5 V with 100 ppm/°C maximum | – | 325 | – | ppm/°C |
| B | amplifier bandwidth | –3 dB; $T_{amb}$ = 25 °C | 250 | – | – | MHz |

**Table 1: Quick reference data**...*continued*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{set(ADC+AGC)}$ | settling time of the block ADC + AGC | input signal settling time <1 ns; settling to 1%; $f_i$ = 85 MHz | – | 4 | – | ns |
| $DR_{PLL}$ | PLL divider ratio | | 100 | – | 4095 | |
| $P_{tot}$ | total power dissipation | $f_{clk}$ = 205 MHz; sine wave input | – | 1.7 | – | W |
| $j_{PLL(max)(p-p)}$ | maximum PLL phase jitter (peak-to-peak value) | $f_{clk}$ = 205 MHz | – | 336 | – | ps |

# 5. Ordering information

**Table 2: Ordering information**

| Type number | Package | | | Sampling frequency (MHz) |
|---|---|---|---|---|
| | Name | Description | Version | |
| TDA8757CHV/17 | HLQFP144 | plastic thermal enhanced low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm; exposed die pad | SOT612-1 | 170 |
| TDA8757CHV/21 | | | | 205 |

## 6. Block diagram

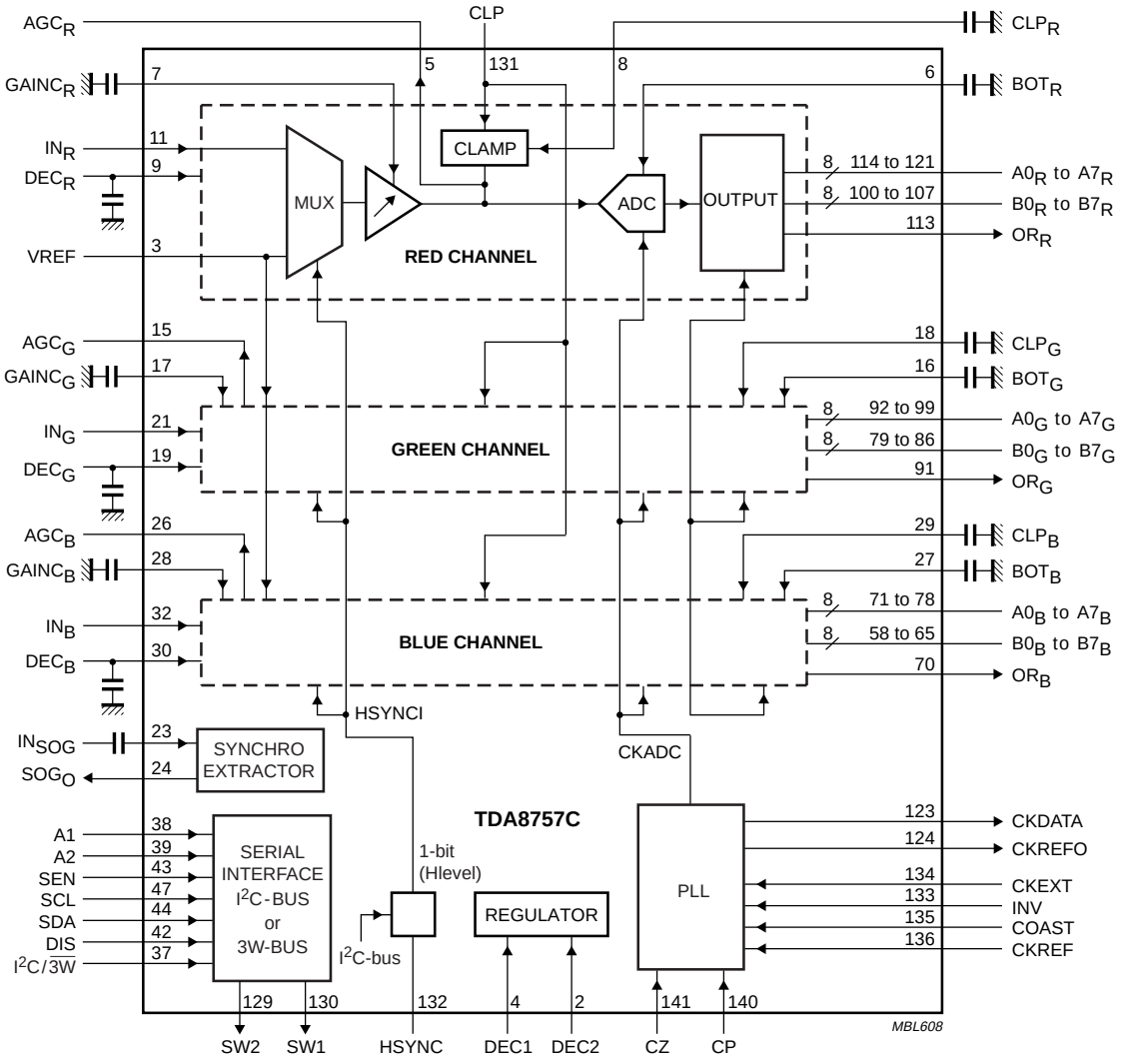



**Fig 1. Block diagram.**

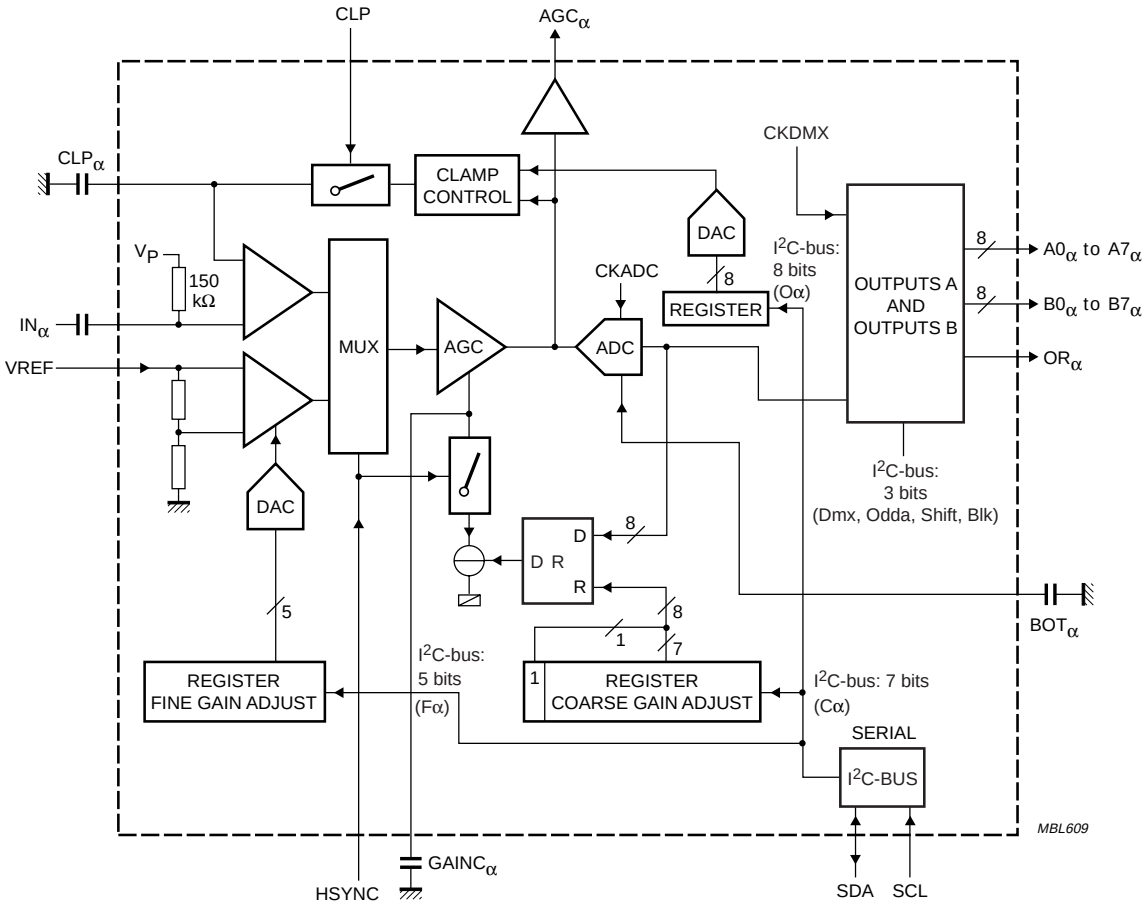



**Fig 2. Channel diagram (where α stands for R, G or B).**

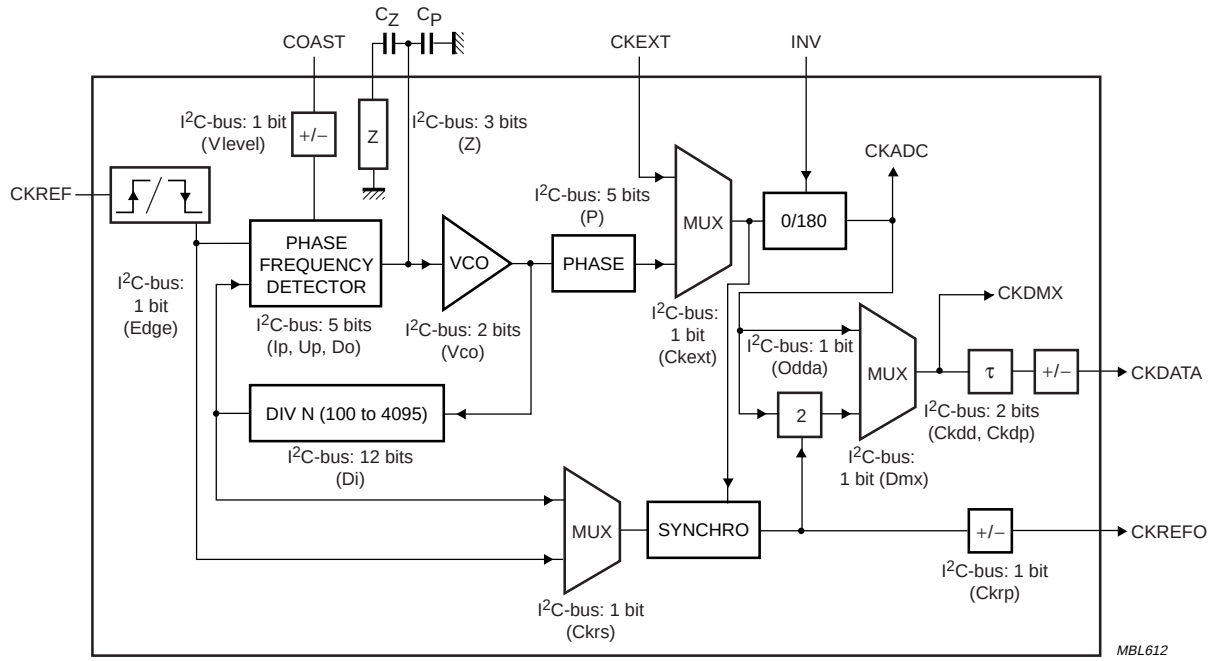



**Fig 3. PLL diagram.**

# 7. Pinning information

## 7.1 Pinning

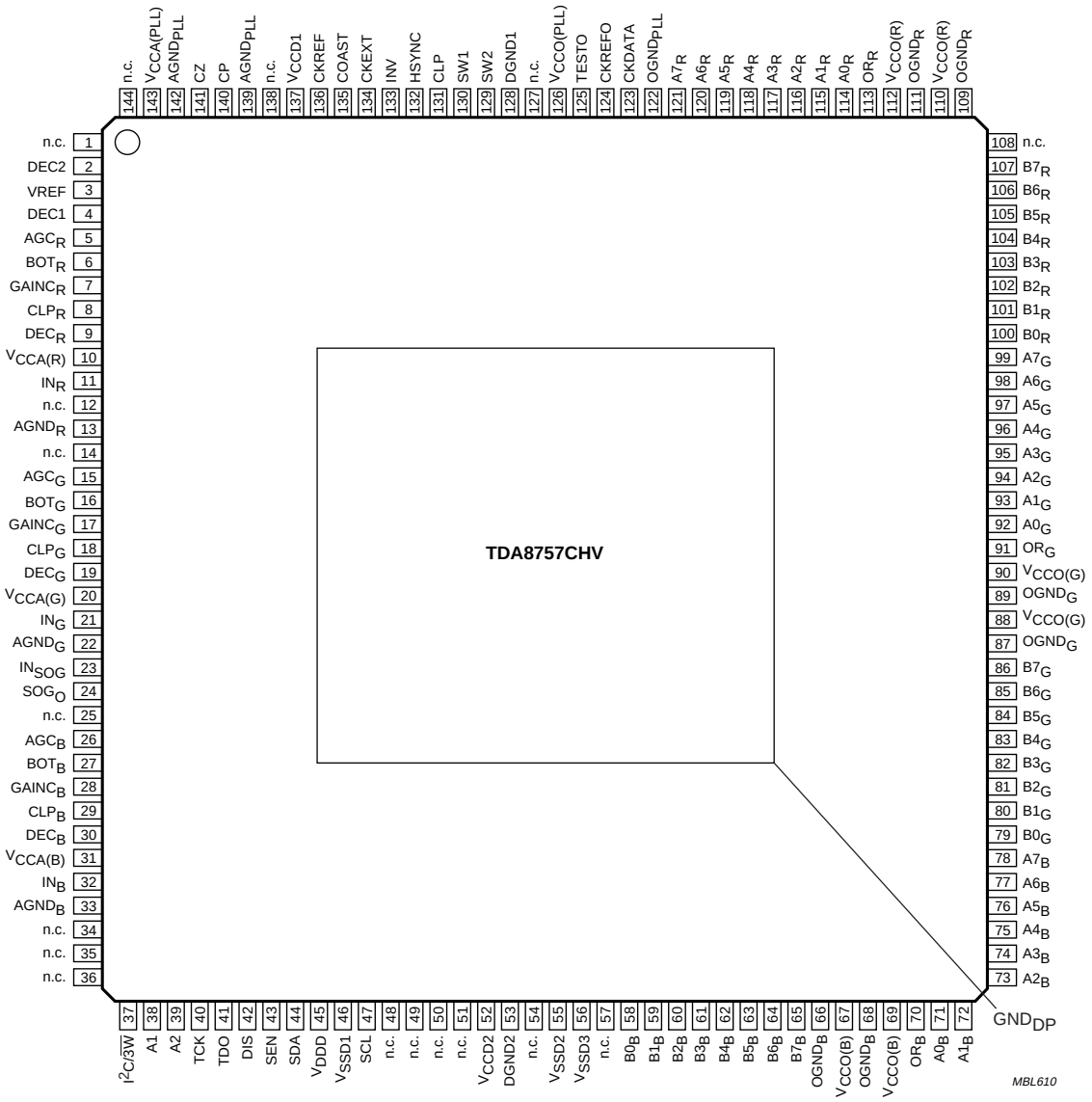



**Fig 4. Pin configuration.**

## 7.2 Pin description

**Table 3: Pin description**

| Symbol | Pin | Description |
|---|---|---|
| n.c. | 1 | not connected |
| DEC2 | 2 | main regulator decoupling input 2 |
| VREF | 3 | gain stabilizer voltage reference input |
| DEC1 | 4 | main regulator decoupling input 1 |
| $AGC_R$ | 5 | red channel AGC output |
| $BOT_R$ | 6 | red channel ladder decoupling input (BOT) |
| $GAINC_R$ | 7 | red channel gain capacitor input |
| $CLP_R$ | 8 | red channel clamp capacitor input |
| $DEC_R$ | 9 | red channel regulator decoupling input |
| $V_{CCA(R)}$ | 10 | red channel analog supply voltage |
| $IN_R$ | 11 | red channel analog input |
| n.c. | 12 | not connected |
| $AGND_R$ | 13 | red channel gain analog ground |
| n.c. | 14 | not connected |
| $AGC_G$ | 15 | green channel AGC output |
| $BOT_G$ | 16 | green channel ladder decoupling input (BOT) |
| $GAINC_G$ | 17 | green channel gain capacitor input |
| $CLP_G$ | 18 | green channel clamp capacitor input |
| $DEC_G$ | 19 | green channel regulator decoupling input |
| $V_{CCA(G)}$ | 20 | green channel analog supply voltage |
| $IN_G$ | 21 | green channel analog input |
| $AGND_G$ | 22 | green channel gain analog ground |
| $IN_{SOG}$ | 23 | sync on green channel input |
| $SOG_O$ | 24 | composite sync output |
| n.c. | 25 | not connected |
| $AGC_B$ | 26 | blue channel AGC output |
| $BOT_B$ | 27 | blue channel ladder decoupling input (BOT) |
| $GAINC_B$ | 28 | blue channel gain capacitor input |
| $CLP_B$ | 29 | blue channel clamp capacitor input |
| $DEC_B$ | 30 | blue channel regulator decoupling input |
| $V_{CCA(B)}$ | 31 | blue channel analog supply voltage |
| $IN_B$ | 32 | blue channel analog input |
| $AGND_B$ | 33 | blue channel gain analog ground |
| n.c. | 34 | not connected |
| n.c. | 35 | not connected |
| n.c. | 36 | not connected |
| $I^2C/\overline{3W}$ | 37 | selection input between $I^2C$-bus (active HIGH) and 3W-bus (active LOW) |
| A1 | 38 | $I^2C$-bus address control input 1 |

**Table 3: Pin description** *...continued*

| Symbol | Pin | Description |
|---|---|---|
| A2 | 39 | $I^2C$-bus address control input 2 |
| TCK | 40 | scan test mode input (active HIGH) |
| TDO | 41 | scan test output |
| DIS | 42 | $I^2C$-bus and 3W-bus disable control input (disable at HIGH level) |
| SEN | 43 | select enable input for 3W-bus |
| SDA | 44 | $I^2C$-bus/3W-bus serial data input |
| $V_{DDD}$ | 45 | logic $I^2C$-bus/3W-bus digital supply voltage |
| $V_{SSD1}$ | 46 | logic $I^2C$-bus/3W-bus digital ground 1 |
| SCL | 47 | $I^2C$-bus/3W-bus serial clock input |
| n.c. | 48 | not connected |
| n.c. | 49 | not connected |
| n.c. | 50 | not connected |
| n.c. | 51 | not connected |
| $V_{CCD2}$ | 52 | digital supply voltage 2 |
| DGND2 | 53 | digital ground 2 |
| n.c. | 54 | not connected |
| $V_{SSD2}$ | 55 | logic $I^2C$-bus/3W-bus digital ground 2 |
| $V_{SSD3}$ | 56 | logic $I^2C$-bus/3W-bus digital ground 3 |
| n.c. | 57 | not connected |
| $B0_B$ | 58 | blue channel ADC output B bit 0 (LSB) |
| $B1_B$ | 59 | blue channel ADC output B bit 1 |
| $B2_B$ | 60 | blue channel ADC output B bit 2 |
| $B3_B$ | 61 | blue channel ADC output B bit 3 |
| $B4_B$ | 62 | blue channel ADC output B bit 4 |
| $B5_B$ | 63 | blue channel ADC output B bit 5 |
| $B6_B$ | 64 | blue channel ADC output B bit 6 |
| $B7_B$ | 65 | blue channel ADC output B bit 7 (MSB) |
| $OGND_B$ | 66 | blue channel ADC output B ground |
| $V_{CCO(B)}$ | 67 | blue channel ADC output B supply voltage |
| $OGND_B$ | 68 | blue channel ADC output A ground |
| $V_{CCO(B)}$ | 69 | blue channel ADC output A supply voltage |
| $OR_B$ | 70 | blue channel ADC output bit out of range |
| $A0_B$ | 71 | blue channel ADC output A bit 0 (LSB) |
| $A1_B$ | 72 | blue channel ADC output A bit 1 |
| $A2_B$ | 73 | blue channel ADC output A bit 2 |
| $A3_B$ | 74 | blue channel ADC output A bit 3 |
| $A4_B$ | 75 | blue channel ADC output A bit 4 |
| $A5_B$ | 76 | blue channel ADC output A bit 5 |
| $A6_B$ | 77 | blue channel ADC output A bit 6 |
| $A7_B$ | 78 | blue channel ADC output A bit 7 (MSB) |

**Table 3: Pin description** *...continued*

| Symbol | Pin | Description |
|---|---|---|
| $B0_G$ | 79 | green channel ADC output B bit 0 (LSB) |
| $B1_G$ | 80 | green channel ADC output B bit 1 |
| $B2_G$ | 81 | green channel ADC output B bit 2 |
| $B3_G$ | 82 | green channel ADC output B bit 3 |
| $B4_G$ | 83 | green channel ADC output B bit 4 |
| $B5_G$ | 84 | green channel ADC output B bit 5 |
| $B6_G$ | 85 | green channel ADC output B bit 6 |
| $B7_G$ | 86 | green channel ADC output B bit 7 (MSB) |
| $OGND_G$ | 87 | green channel ADC output B ground |
| $V_{CCO(G)}$ | 88 | green channel ADC output B supply voltage |
| $OGND_G$ | 89 | green channel ADC output A ground |
| $V_{CCO(G)}$ | 90 | green channel ADC output A supply voltage |
| $OR_G$ | 91 | green channel ADC output bit out of range |
| $A0_G$ | 92 | green channel ADC output A bit 0 (LSB) |
| $A1_G$ | 93 | green channel ADC output A bit 1 |
| $A2_G$ | 94 | green channel ADC output A bit 2 |
| $A3_G$ | 95 | green channel ADC output A bit 3 |
| $A4_G$ | 96 | green channel ADC output A bit 4 |
| $A5_G$ | 97 | green channel ADC output A bit 5 |
| $A6_G$ | 98 | green channel ADC output A bit 6 |
| $A7_G$ | 99 | green channel ADC output A bit 7 (MSB) |
| $B0_R$ | 100 | red channel ADC output B bit 0 (LSB) |
| $B1_R$ | 101 | red channel ADC output B bit 1 |
| $B2_R$ | 102 | red channel ADC output B bit 2 |
| $B3_R$ | 103 | red channel ADC output B bit 3 |
| $B4_R$ | 104 | red channel ADC output B bit 4 |
| $B5_R$ | 105 | red channel ADC output B bit 5 |
| $B6_R$ | 106 | red channel ADC output B bit 6 |
| $B7_R$ | 107 | red channel ADC output B bit 7 (MSB) |
| n.c. | 108 | not connected |
| $OGND_R$ | 109 | red channel ADC output B ground |
| $V_{CCO(R)}$ | 110 | red channel ADC output B supply voltage |
| $OGND_R$ | 111 | red channel ADC output A ground |
| $V_{CCO(R)}$ | 112 | red channel ADC output A supply voltage |
| $OR_R$ | 113 | red channel ADC output A bit out of range |
| $A0_R$ | 114 | red channel ADC output A bit 0 (LSB) |
| $A1_R$ | 115 | red channel ADC output A bit 1 |
| $A2_R$ | 116 | red channel ADC output A bit 2 |
| $A3_R$ | 117 | red channel ADC output A bit 3 |
| $A4_R$ | 118 | red channel ADC output A bit 4 |
| $A5_R$ | 119 | red channel ADC output A bit 5 |

**Table 3: Pin description** *...continued*

| Symbol | Pin | Description |
|---|---|---|
| $A6_R$ | 120 | red channel ADC output A bit 6 |
| $A7_R$ | 121 | red channel ADC output A bit 7 (MSB) |
| $OGND_{PLL}$ | 122 | PLL digital ground |
| CKDATA | 123 | output data clock |
| CKREFO | 124 | output horizontal pulse synchronized to pixel clock |
| TESTO | 125 | output reserved for test |
| $V_{CCO(PLL)}$ | 126 | PLL output supply voltage |
| n.c. | 127 | not connected |
| DGND1 | 128 | digital ground 1 |
| SW2 | 129 | output pin SW2 is controlled by the $I^2C$-bus |
| SW1 | 130 | output pin SW1 is controlled by the $I^2C$-bus |
| CLP | 131 | clamp pulse input (clamp active HIGH) |
| HSYNC | 132 | horizontal synchronization pulse input |
| INV | 133 | PLL clock output inverter control input (invert when HIGH) |
| CKEXT | 134 | external clock input |
| COAST | 135 | PLL coast control input |
| CKREF | 136 | PLL reference clock input |
| $V_{CCD1}$ | 137 | digital supply voltage 1 |
| n.c. | 138 | not connected |
| $AGND_{PLL}$ | 139 | PLL analog ground |
| CP | 140 | PLL filter input |
| CZ | 141 | PLL filter input |
| $AGND_{PLL}$ | 142 | PLL analog ground |
| $V_{CCA(PLL)}$ | 143 | PLL analog supply voltage |
| n.c. | 144 | not connected |
| $GND_{DP}$ | exposed die pad connection | |

# 8. Functional description

This triple high-speed 8-bit ADC is designed to convert RGB/YUV signals, coming from an analog source, into digital data used by a LCD driver (pixel clock up to 205 MHz).

## 8.1 Analog video inputs

The RGB/YUV video inputs are externally AC-coupled and are internally DC polarized.

The synchronization signals are also used by the device for the internal PLL and the gain calibration.

If the green video signal has composite sync (sync on green) it is possible to extract this composite sync by connecting the green signal to pin $IN_{SOG}$ (AC-coupled). When the sync pulse amplitude is below 300 mV, the $I^2C$-bus bit 'Slevel' has to be set to logic 1 (see Figure 5). The maximum amplitude for the sync pulse is 600 mV typical.

The composite sync is available at pin $SOG_O$ (TTL level compatible signal).

If this function is not used, pin $IN_{SOG}$ should be connected to the analog power supply. In this event pin $SOG_O$ is at LOW-level TTL.

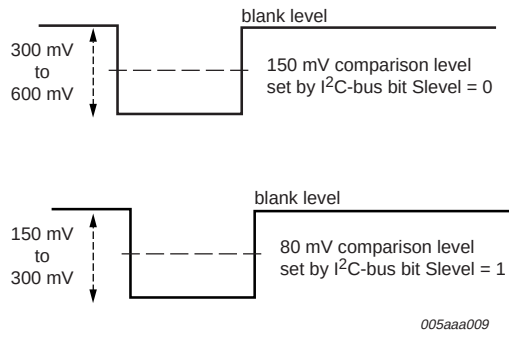



**Fig 5. Sync level diagram.**

## 8.2 Clamps

Three independent parallel clamping circuits are used to clamp the video input signals on several black levels. The clamping levels may be set from −63.5 to +64 LSBs (RGB) and from +120 to +136 LSBs in steps of ½ LSB (YUV). They are controlled by changing the values in three 9-bit registers: OFFSETR, OFFSETG and OFFSETB (see Table 5). Each clamp must be able to correct an offset from ±100 mV to ±10 mV within 300 ns, and correct the total offset in 10 lines.

The clamping is done using the following principle: When a TTL positive going input pulse is applied to pin CLP, three external capacitors are loaded independently by the device in order to change the voltage level of each analog RGB input. The capacitors are connected to pins $CLP_R$, $CLP_G$ and $CLP_B$.

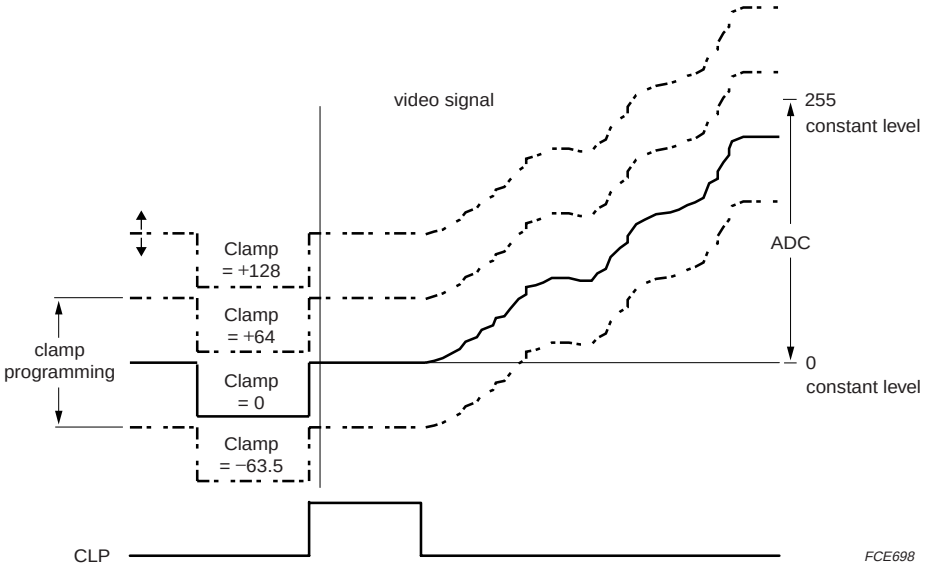



**Fig 6. Clamp definition.**

### 8.2.1 Variable gain amplifiers

Three independent variable gain amplifiers are used to provide, for each channel, a full-scale input signal to the 8-bit ADC. The gain adjustment range is designed so that for an input range varying from 0.4 to 1.2 V (p-p), the output signal corresponds to the ADC full-scale input of 1 V (p-p).

To ensure that the gain does not vary over the whole operating temperature range a reference voltage $V_{ref}$ = 2.5 V (DC), with a maximum variation of 100 ppm/°C, is supplied externally on pin VREF.

The calibration of the gains is done using the following principle. When an input pulse is applied to pin HSYNC, an internal multiplexer switches from the RGB video signals to a reference voltage ($^1/_{16}V_{ref}$). The ADCs inputs become this reference signal and the three corresponding outputs are compared to pre-set values loaded in three 7-bit registers: COARSER, COARSEG and COARSEB. Depending on the result of the comparisons, the three gains are adjusted such that the ADC outputs become equal to the pre-set values in the registers. The three gains are controlled by changing the values in the COARSE registers.

The signal supplied on pin HSYNC, may be selected active HIGH or active LOW. The choice is done through the serial interface by setting bit ‘Hlevel’ in the control register (active HIGH when bit Hlevel = 0).

This active part of the signal has to occur during the blanking period of the signal in order not to interrupt the active video. Normally the horizontal synchronization signal, provided by the video source, is connected to pin HSYNC.

The values loaded in the gain registers (COARSER, COARSEG, COARSEB) are chosen from 68 values (see Table 6).

A fine correction is also used to finely tune the gain on the three channels and to compensate the channel-to-channel gain mismatch. The fine correction is done using the following principle: the three binary codes, stored in the three 5-bit registers (FINER, FINEG and FINEB) are converted into three analog voltages (with three DACs) and are independently added to the reference voltage ($^1/_{16}V_{ref}$). Thus, three different reference voltages are used for the gain calibration of the three channels.

When the COARSE registers are set at full-scale, the resolution of the fine registers corresponds to $^1/_2$ LSB peak-to-peak (see Equation 3).

### 8.2.2 Important recommendations

The clamping and the gain calibration requires two external signals (pulses). One signal is connected to pin CLP and the other is connected to pin HSYNC. It is very important that:

- The active part of these two signals occur during the blanking of the video signal, in order not to interrupt or disturb the active video.
- The active part of these two signals do not overlap each other, in order to perform correctly the gain calibration and the clamping. Normally the clamp pulse is sent after the end of the horizontal synchronization pulse.

### 8.2.3 ADCs

Three ADCs convert analog signals into three series of 8-bit codes, with a maximum clock frequency of 205 Msps. The ADCs input range is 1 V (p-p) full-scale and the pipeline delay is 1 clock cycle from the sampling to the data output. The reference ladders regulators are integrated.

### 8.2.4 Data outputs

The ADC outputs are straight binary. It is possible to switch the data and clock outputs to high-impedance by setting bit PWD in register FINER (PWD = 1 when the data and clock outputs are in high-impedance). The data and clock outputs can drive a maximum 10 pF load. The timing must be checked very carefully if the capacitive load exceeds 10 pF.

It is possible to force the outputs to logic 0 during the gain calibration (during HSYNC pulse) and during the clamping (CLP pulse). This mode is activated through the serial interface by setting bit ‘Blk’ to logic 1 in register DEMUX.

The TDA8757C provides outputs either on one port (port A) or on two ports (ports A and B). The selection is made with the serial interface by setting bit ‘Dmx’ to logic 0 or logic 1 in register DEMUX. When just one port is used (Dmx = 0), the unused ports are forced to LOW level. When two ports are used (Dmx = 1), it is possible to select the port that would provide the odd pixel by setting bit ‘Odda’ to logic 1 or logic 0 in register DEMUX; when this bit is logic 1, odd pixel on output of port A.

One out-of-range bit exists per channel ($OR_R$, $OR_G$ and $OR_B$). It will be at logic 1 when the signal is out-of-range of the ADC voltage ladder.

Finally, two configurations are possible: either the port A outputs and the port B outputs are both synchronous or they are interleaved. The selection is done by setting bit ‘Shift’ to logic 0 or logic 1 in register DEMUX.

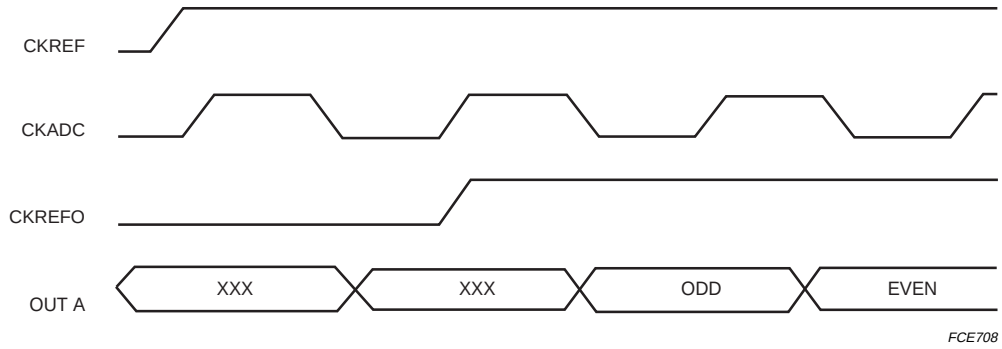



**Fig 7. Definition of odd and even pixels; Edge = 0, Dmx = 0 and Ckrp = 1.**

### 8.2.5 PLL

The ADCs are clocked by either the internal PLL locked to the reference clock CKREF or an external clock connected to pin CKEXT. All parts of the PLL are on-chip except the loop filter capacitors. The selection is performed via the serial interface by setting bit 'Ckext' in register PHASE (Ckext = 1 when the external clock is used).

The reference clock (CKREF) range is between 15 and 150 kHz. Consequently, the VCO minimum frequency is 12 MHz and the maximum frequency is 205 MHz. The gain of the VCO part can be controlled through the serial interface, depending on the frequency range to which the PLL is locked.

Moreover, the PLL may be locked either on the rising or on the falling edge of the CKREF signal pulses. This choice is made via the serial interface by setting bit 'Edge' in register CONTROL (rising edge when bit 'Edge' = 0).

The charge pump current ($I_{cp}$) can increase the PLL bandwidth. It is programmable through the serial interface by setting bits 'Ip2', 'Ip1' and 'Ip0' in the control register (see Table 8).

Different resistance values (R) for the filter can also be programmed through the serial interface by setting the bits 'Z2', 'Z1' and 'Z0' in register VCO (see Table 9).

To have optimal PLL performance, R and $I_{cp}$ must be chosen so that:

- The result of the product '$R \times I_{cp}$' is smaller than a determined limit (Lim)
- The result of the product '$R \times I_{cp}$' is as close as possible to this limit (Lim).

$$Lim = \frac{0.3\pi \times DR_{PLL} \times f_{ref}}{K_0} \quad (1)$$

where:

- $DR_{PLL}$ = the divider ratio, which is the ratio between the pixel frequency and the horizontal line frequency of the incoming signal. The setting of this parameter is performed through the serial interface with bits Di0 to Di11. These bits are present in the VCO-, divider- and phase registers.
- $f_{ref}$ = the frequency of the signal.
- $K_0$ = the VCO gain, which depends on the pixel frequency ranges given in Table 10.

In the event that several combinations of R and $I_{cp}$ give the same result, a calculating of the damping factor ($\xi$) for each couple becomes necessary.

The combination of R and $I_{cp}$ whose damping factor is the closest to 1.5, generates the optimum PLL performance.

$$\xi = \frac{R \cdot C_Z}{2} \cdot \sqrt{\frac{K_0 \cdot I_{cp}}{DR_{PLL} \cdot (C_Z + C_P)}} \quad (2)$$

where $C_Z$ and $C_P$ are the external capacitors of the PLL loop filter. The recommended values are: $C_Z$ = 68 nF and $C_P$ = 150 pF.

Pin COAST is used to disconnect the PLL phase frequency detector during the frame flyback (vertical blanking) or the unavailability of the CKREF signal. This signal can normally be derived from the VSYNC signal.

The COAST signal may be active either HIGH or LOW by setting bit ‘Vlevel’ in the control register, through the serial interface (Vlevel = 0 when HIGH).

It is possible to control the phase of the ADC clock (CKADC), through the serial interface, with the included digital phase-shift controller. The phase register (5 bits) enables to shift the phase by steps of 11.25 deg.

The CKREF signal is resynchronized by the synchro-block on the CKADC clock. The new reference is available on pin CKREFO. This synchronization may be done either with the CKREF signal directly, or with the output of the divider in the PLL (see Figure 3).

The selection is done via the serial interface by setting bit ‘Ckrs’ in the phase register (Ckrs = 1 when the CKREF signal is used). The polarity of the signal on pin CKREFO is controlled through the serial interface by setting bit ‘Ckrp’ in register DEMUX (positive polarity if Ckrp = 0). The width of this signal is fixed to 8 clock cycles.

The PLL also provides a CKDATA clock. This clock is synchronized on the data outputs regardless of the mode.

It is possible to delay the CKDATA clock with a constant time ($\tau = 3$ ns, compared to the outputs) by setting bit ‘Ckdd’ to logic 1 in register DEMUX. Moreover, it is possible to invert the CKDATA clock, referenced to the outputs, by setting bit ‘Ckdp’ in register DEMUX.

The maximum capacitive load for each clock output is 10 pF.

If an external clock is used, it has to be connected to pin CKEXT. Bit ‘Ckext’ and bit ‘Ckrs’ in the phase register have to be set at logic 1. It is also important to disconnect the internal PLL by using the following settings:

- Set bit ‘Do’ in the control register to logic 1.
- Set bits ‘Vco1’ and ‘Vco0’ in register VCO to logic 0.

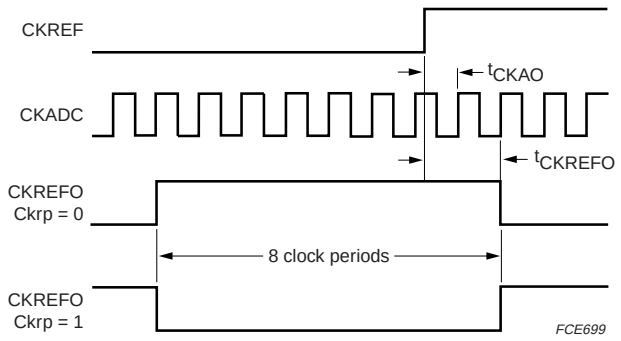



**Fig 8. Timing diagram; CKREFO; Dmx = 0.**

There is a delay ($t_{CKREFO}$) between the input signal on pin CKREF and the corresponding output on pin CKREFO; see Figure 8.

$t_{CKREFO}$ = either $t_{CKAO}$ (if clock phase >01000) or $t_{CKAO}$ + $T_{CLK(pixel)}$ (if phase <01000)

$t_{CKAO} = t_{CLK(buffer)} + t_{phase\ selector}$

$t_{CLK(buffer)}$ = tbf and $t_{phase\ selector} = \left(\frac{phase}{2\pi}\right) \cdot T_{CLK(pixel)}$

# 9. I²C-bus and 3W-bus interfaces

## 9.1 Register definitions

The configuration of the registers is given in Table 4.

**Table 4: I²C-bus and 3W-bus registers**

| Function name | Subaddress | | | | | | | | Bit definition | | | | | | | | Default value |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | MSB | | | | | | | LSB | |
| SUBADDR | | | | | | | | | X | X | X | Mode | Sa3 | Sa2 | Sa1 | Sa0 | XXX1 0000 |
| OFFSETR | X | X | X | X | 0 | 0 | 0 | 0 | Or7 | Or6 | Or5 | Or4 | Or3 | Or2 | Or1 | Or0 | 0111 1111 |
| COARSER | X | X | X | X | 0 | 0 | 0 | 1 | Or8 | Cr6 | Cr5 | Cr4 | Cr3 | Cr2 | Cr1 | Cr0 | 0010 0000 |
| FINER | X | X | X | X | 0 | 0 | 1 | 0 | PWD | Testvol | Testvoh | Fr4 | Fr3 | Fr2 | Fr1 | Fr0 | 0000 0000 |
| OFFSETG | X | X | X | X | 0 | 0 | 1 | 1 | Og7 | Og6 | Og5 | Og4 | Og3 | Og2 | Og1 | Og0 | 0111 1111 |
| COARSEG | X | X | X | X | 0 | 1 | 0 | 0 | Og8 | Cg6 | Cg5 | Cg4 | Cg3 | Cg2 | Cg1 | Cg0 | 0010 0000 |
| FINEG | X | X | X | X | 0 | 1 | 0 | 1 | SW2 | SW1 | Slevel | Fg4 | Fg3 | Fg2 | Fg1 | Fg0 | 0000 0000 |
| OFFSETB | X | X | X | X | 0 | 1 | 1 | 0 | Ob7 | Ob6 | Ob5 | Ob4 | Ob3 | Ob2 | Ob1 | Ob0 | 0111 1111 |
| COARSEB | X | X | X | X | 0 | 1 | 1 | 1 | Ob8 | Cb6 | Cb5 | Cb4 | Cb3 | Cb2 | Cb1 | Cb0 | 0010 0000 |

**Table 4: $I^2C$-bus and 3W-bus registers**...*continued*

| Function name | Subaddress | | | | | | | | Bit definition | | | | | | | | Default value |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | MSB | | | | | | | LSB | |
| FINEB | X | X | X | X | 1 | 0 | 0 | 0 | X | X | Cken | Fb4 | Fb3 | Fb2 | Fb1 | Fb0 | XX00 0000 |
| CONTROL | X | X | X | X | 1 | 0 | 0 | 1 | Vlevel | Hlevel | Edge | Up | Do | Ip2 | Ip1 | Ip0 | 0000 0111 |
| VCO | X | X | X | X | 1 | 0 | 1 | 0 | Z2 | Z1 | Z0 | Vco1 | Vco0 | Di11 | Di10 | Di9 | 1011 1011 |
| DIVIDER (LSB) | X | X | X | X | 1 | 0 | 1 | 1 | Di8 | Di7 | Di6 | Di5 | Di4 | Di3 | Di2 | Di1 | 0100 1100 |
| PHASE | X | X | X | X | 1 | 1 | 0 | 0 | Di0 | Ckrs | Ckext | P4 | P3 | P2 | P1 | P0 | 0000 0000 |
| DEMUX | X | X | X | X | 1 | 1 | 0 | 1 | Blk | Shpixel | Ckrp | Ckdp | Ckdd | Shift | Odda | Dmx | 1000 0111 |

### 9.1.1 Subaddress

All the registers are defined by a subaddress of 7 bits: bit Mode refers to the mode which is used with the $I^2C$-bus interface, bits 'Sa3' to 'Sa0' give the subaddress of each register.

Bit Mode, used only with the $I^2C$-bus, allows two modes for the programming:

Mode 0 — Each register is programmed independently, by giving its subaddress and its content.

Mode 1 — All the registers are programmed one after the other, by giving this initial condition (XXX1 1111) as the subaddress state; thus, the registers are changed following the predefined sequence of 16 bytes (from subaddress 0000 to 1101).

The default values correspond to a VESA 1280 × 1024 at 75 Hz graphic mode.

### 9.1.2 Offset register

This register controls the clamp level for the RGB channels. The relationship between the programming code and the level of the clamp code is given in Table 5.

**Table 5: Coding**

| Programmed code | Clamp code | ADC output |
|---|---|---|
| 0 | –63.5 | underflow |
| 1 | –63 | |
| 2 | –62.5 | |
| ... | ... | |
| 127 | 0 | 0 |
| ... | ... | ... |
| 254 | 63.5 | 63 or 64 |
| 255 | 64 | 64 |
| 256 | 120 | 120 |
| ... | ... | ... |
| 287 | 136 | 136 |

The default programmed value is:

- Programmed code = 127
- Clamp code = 0
- ADC output = 0.

### 9.1.3 Coarse and Fine registers

The coarse register enables the gain control and the AGC gain. The fine register controls the reference voltage, control pins SW1 and SW2, and the power-down mode.

The coarse register programming equation is as follows:

$$GAIN = \left(\frac{N_{COARSE} + 1}{V_{ref} \cdot \left(1 - \frac{N_{FINE}}{32 \times 16}\right)}\right) \times \frac{1}{16} = \left(\frac{N_{COARSE} + 1}{V_{ref} \cdot (512 - N_{FINE})}\right) \times 32 \quad (3)$$

Where: $V_{ref}$ = 2.5 V.

The gain correspondence is given in Table 6. The gain is linear with reference to the programming code ($N_{FINE}$ = 0).

**Table 6: Typical gain correspondence (COARSE)**

| $N_{COARSE}$ | Gain | $V_i$ to be full-scale (V) |
|---|---|---|
| 32 | 0.825 | 1.212 |
| 99 | 2.5 | 0.4 |

The default programmed value is as follows:

- $N_{COARSE}$ = 32
- Gain = 0.825
- $V_i$ to be full-scale = 1.212.

To modulate this gain, the fine register is programmed using the above equation. With a full-scale ADC input, the fine register resolution is a ½ LSB peak-to-peak (see Table 7 for $N_{COARSE}$ = 32).

**Table 7: Typical gain correspondence (FINE)**

| $N_{FINE}$ | Gain | $V_i$ to be full-scale (V) |
|---|---|---|
| 0 | 0.825 | 1.212 |
| 31 | 0.878 | 1.139 |

The default programmed value is: $N_{FINE}$ = 0.

In addition bit PWD (in register FINER) sets the device into power-down mode as well as the data and clock outputs into high-impedance:

PWD = 0: chip active

PWD = 1: chip in power-down mode and data and clock outputs in high-impedance.

Pins SW1 (pin 130) and SW2 (pin 129) are controlled by the I$^2$C-bus and command external devices such as Video Switch by setting bits SW1 and SW2 respectively in register FINEG.

### 9.1.4 Control register

COAST and HSYNC signals can be derived by setting the I$^2$C-bus control bits 'Vlevel' and 'Hlevel' respectively. When bits 'Vlevel' and 'Hlevel' are set to zero, COAST and HSYNC are active HIGH.

Bit 'Edge' defines the rising or falling edge of CKREF to synchronize the PLL. It will be on the rising edge if the bit is a logic 0 and on the falling edge if the bit is at logic 1.

Bits 'Up' and 'Do' are used for the test, to force the charge pump current. These bits have to be logic 0 during normal use.

Bit 'Cken' is used for the test to check the CKADC internal signal. This bit has to be logic 0 during normal use.

Bits 'Ip0', 'Ip1' and 'Ip2' control the charge pump current, to increase the bandwidth of the PLL, as shown in Table 8.

**Table 8: Charge pump current control**

| Ip2 | Ip1 | Ip0 | Current (μA) |
|---|---|---|---|
| 0 | 0 | 0 | 6.25 |
| 0 | 0 | 1 | 12.5 |
| 0 | 1 | 0 | 25 |
| 0 | 1 | 1 | 50 |
| 1 | 0 | 0 | 100 |
| 1 | 0 | 1 | 200 |
| 1 | 1 | 0 | 400 |
| 1 | 1 | 1 | 700 |

The default programmed value is as follows:

- Charge pump current = 700 μA
- Bits 'Up' and 'Do' are used for testing, normally they are set to logic 0
- Rising edge of CKREF: bit 'Edge' at logic 0
- COAST and HSYNC inputs are active HIGH: bits 'Vlevel' and 'Hlevel' at logic 0.

### 9.1.5 VCO register

Bits ‘Z2’, ‘Z1’ and ‘Z0’ enable the internal resistance for the VCO filter to be selected.

**Table 9: VCO register bits**

| Z2 | Z1 | Z0 | Resistance (kΩ) |
|---|---|---|---|
| 0 | 0 | 0 | high-impedance |
| 0 | 0 | 1 | 9 |
| 0 | 1 | 0 | 6.4 |
| 0 | 1 | 1 | 4.5 |
| 1 | 0 | 0 | 3.2 |
| 1 | 0 | 1 | 2.25 |
| 1 | 1 | 0 | 1.6 |
| 1 | 1 | 1 | 1.1 |

Bits ‘Vco1’ and ‘Vco0’ control the VCO gain.

**Table 10: VCO gain control**

| Vco1 | Vco0 | VCO gain (MHz/V) | Pixel clock frequency range (MHz) |
|---|---|---|---|
| 0 | 0 | 20 | 12 to 28 |
| 0 | 1 | 30 | 28 to 55 |
| 1 | 0 | 60 | 55 to 115 |
| 1 | 1 | 115 | 115 to 205 |

The default programmed value is as follows:

- Internal resistance = 2.25 kΩ
- VCO gain = 115 MHz/V.

### 9.1.6 Divider register

This register controls the PLL frequency. Bits ‘Di8’ to ‘Di0’ are the LSB bits. The default programmed value is 0110 1001 1000 = 1688.

The MSB bits (‘Di11’, ‘Di10’ and ‘Di9’) and the LSB bit ‘Di0’ have to be programmed before bits ‘Di8’ to ‘Di1’ in order to have the required divider ratio. Bit ‘Di0’ is used for the parity divider number (Di0 = 0: even number; Di0 = 1: odd number). It should be noted that if the $I^2C$-bus programming is done in mode 1 and the bit ‘Di0’ has to be toggled, then the registers have to be loaded twice to have the updated divider ratio.

### 9.1.7 Phase register

Bit ‘Ckext’ is logic 0 when the PLL clock is used and logic 1 when the external clock is used.

Bit ‘Ckrs’ is logic 1 when the synchronization is done with CKREF (see Figure 3).

Bits ‘P4’ to ‘P0’ are used to program the phase shift for clock CKDATA.

**Table 11: Phase registers bits**

| P4 | P3 | P2 | P1 | P0 | Phase shift (deg) |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 11.25 |
| ... | ... | ... | ... | ... | ... |
| 1 | 1 | 1 | 1 | 0 | 337.5 |
| 1 | 1 | 1 | 1 | 1 | 348.75 |

The default programmed value is as follows:

- No external clock: bit ‘Ckext’ is logic 0
- Phase shift for CKDATA is 0 deg.

### 9.1.8 DEMUX register

The default programming is:

- Outputs forced to logic 0 during CLP and HSYNC pulses: bit ‘Blk’ = 1
- First pixel not shifted: bit ‘Shpixel’ = 0
- CKREFO with positive polarity: bit ‘Ckrp’ = 0
- CKDATA not reversed: bit ‘Ckdp’ = 0
- CKDATA not delayed: bit ‘Ckdd’ = 0
- Interleaved outputs: bit ‘Shift’ = 1
- Odd pixels on port A: bit ‘Odda’ = 1.
- Demultiplexed outputs: bit ‘Dmx’ = 1

For timing diagrams concerning various settings of this register, see Figure 11 - 13.

### 9.1.9 Power-down mode

- When the supply is disconnected, the registers are reset to their default values; they require reprogramming if the settings are different (e.g. through an EEPROM)
- When the device is in Power-down mode (bit PWD = 1), all data and clock outputs are in high-impedance.

## 9.2 I²C-bus protocol

**Table 12: Register format**

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | RW |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 1 | A2 | A1 | 0 |

The address of the circuit for the I²C-bus is 1001 1XX0.

Bits ‘A1’ and ‘A0’ are fixed by the potential on pins A2 and A1. Bit ‘RW’ must always be equal to logic 0 because it is not possible to read the data in the register. The timing and protocol for the I²C-bus are standard. Two sequences are available; see Table 13 and 14.

**Table 13: Address sequence for mode 0**

*S = START condition, A = acknowledge bit (generated by the device) and P = STOP condition.*

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| S | IC ADDRESS | A | SUBADDRESS REGISTER1 | A | DATA REGISTER1 (see Table 4) | A | SUBADDRESS REGISTER2 | A | ... | P |

**Table 14: Address sequence for mode 1**

*S = START condition, A = acknowledge bit (generated by the device) and P = STOP condition.*

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| S | IC ADDRESS | A | SUBADDRESS XX11 1111 | A | DATA REGISTER1 (see Table 4) | A | DATA REGISTER2 | A | ... | P |

## 9.3 3W-bus protocol

For the 3W-bus, the first byte refers to the register address which is programmed. The second byte refers to the data to be sent to the chosen register (see Table 4).

Using a 3W-bus interface, an indefinite number of ICs can operate on the same system. Pin SEN is used to validate the circuits.

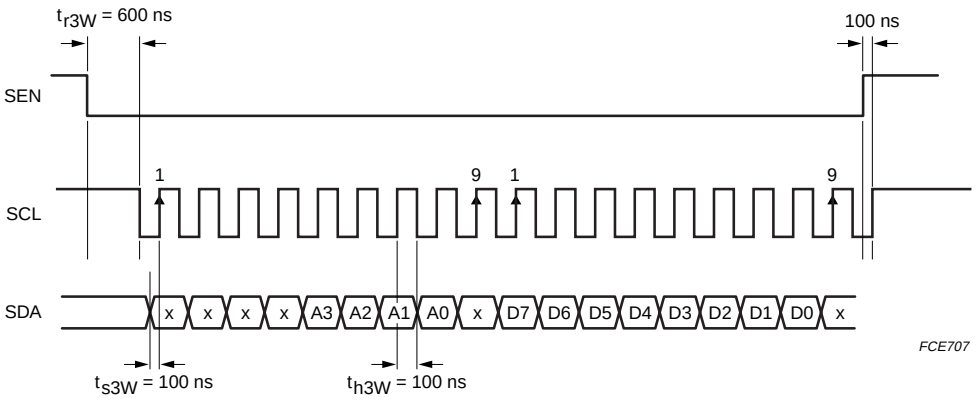



**Fig 9. 3W-bus protocol.**

# 10. Limiting values

**Table 15: Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCA}$ | analog supply voltage | | –0.3 | +7.0 | V |
| $V_{DDD}$ | logic supply voltage | | –0.3 | +7.0 | V |
| $V_{CCD}$ | digital supply voltage | | –0.3 | +7.0 | V |
| $V_{CCO}$ | output stages supply voltage | | –0.3 | +7.0 | V |
| $\Delta V_{CC}$ | supply voltage differences | | | | |
| | $V_{CCA} - V_{CCD}$ | | –1.0 | +1.0 | V |
| | $V_{CCA} - V_{DDD}$ | | –1.0 | +1.0 | V |
| | $V_{CCD} - V_{DDD}$ | | –1.0 | +1.0 | V |
| $V_{i(RGB)}$ | RGB input voltage range | referenced to AGND | –0.3 | +7.0 | V |
| $I_o$ | output current | | – | 10 | mA |
| $T_{stg}$ | storage temperature | | –55 | +150 | °C |
| $T_{amb}$ | ambient temperature | | 0 | 70 | °C |
| $T_j$ | junction temperature | | – | 150 | °C |

# 11. Thermal characteristics

**Table 16: Typical thermal characteristics**

| Symbol | Parameter | Conditions | Value | Unit |
|---|---|---|---|---|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | 30 | K/W |

# 12. Characteristics

**Table 17: Characteristics**

*$V_{CCA}$ = 4.75 V to 5.25 V (referenced to AGND); $V_{CCD}$ = 4.75 V to 5.25 V (referenced to DGND); $V_{DDD}$ = 4.75 V to 5.25 V (referenced to $V_{SSD}$); $V_{CCO}$ = 3.0 V to 3.6 V (referenced to OGND); AGND, DGND, OGND and $V_{SS}$ connected together; $T_{amb}$ = 0 to 70 °C; typical values measured at $V_{CCA}$ = $V_{DDD}$ = $V_{CCD}$ = 5 V; $V_{CCO}$ = 3.3 V and $T_{amb}$ = 25 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supplies** | | | | | | |
| $V_{CCA(PLL)}$, $V_{CCA(R)}$, $V_{CCA(G)}$, $V_{CCA(B)}$ | analog supply voltage for the PLL and the RGB channels | | 4.75 | 5.0 | 5.25 | V |
| $V_{DDD}$ | logic supply voltage for I²C-bus and 3W-bus | | 4.75 | 5.0 | 5.25 | V |
| $V_{CCD}$ | digital supply voltage | | 4.75 | 5.0 | 5.25 | V |
| $V_{CCO(PLL)}$, $V_{CCO(R)}$, $V_{CCO(G)}$, $V_{CCO(B)}$ | output stages supply voltage for PLL and the RGB channels | | 3.0 | 3.3 | 3.6 | V |
| $I_{CCA(PLL)}$ | analog PLL supply current | | – | 34 | – | mA |
| $I_{CCA(R)}$, $I_{CCA(G)}$, $I_{CCA(B)}$ | analog supply current for the RGB channels | | – | 135 | – | mA |
| $I_{DDD}$ | logic supply current for I²C-bus and 3W-bus | | – | 1 | – | mA |
| $I_{CCD}$ | digital supply current | | – | 95 | – | mA |
| $I_{CCO(R)}$, $I_{CCO(G)}$, $I_{CCO(B)}$, $I_{CCO(PLL)}$ | output stages supply current for the PLL and the RGB channels | sine wave input | – | 80 | – | mA |
| $\Delta V_{CC}$ | supply voltage difference | | | | | |
| | $V_{CCA} - V_{CCD}$ | | –0.25 | – | +0.25 | V |
| | $V_{CCA} - V_{DDD}$ | | –0.25 | – | +0.25 | V |
| | $V_{CCD} - V_{DDD}$ | | –0.25 | – | +0.25 | V |
| $P_{tot}$ | total power dissipation | sine wave input | – | 1.7 | – | W |
| $P_{pd}$ | power dissipation in Power-down mode | | – | 55 | – | mW |
| **R, G and B amplifiers** | | | | | | |
| B | bandwidth | –3 dB; $T_{amb}$ = 25 °C | 250 | – | – | MHz |
| $t_{set(ADC+AGC)}$ | settling time of the block ADC + AGC | full-scale (black-to-white) transition; input signal settling time <1 ns; settling to within 2 LSB | – | 4 | – | ns |
| $G_{COARSE}$ | coarse gain range | minimum coarse gain; code = 32 | – | –1.67 | – | dB |
| | | maximum coarse gain; code = 99 | – | 8 | – | dB |

**Table 17: Characteristics**...*continued*

*$V_{CCA}$ = 4.75 V to 5.25 V (referenced to AGND); $V_{CCD}$ = 4.75 V to 5.25 V (referenced to DGND); $V_{DDD}$ = 4.75 V to 5.25 V (referenced to $V_{SSD}$); $V_{CCO}$ = 3.0 V to 3.6 V (referenced to OGND); AGND, DGND, OGND and $V_{SS}$ connected together; $T_{amb}$ = 0 to 70 °C; typical values measured at $V_{CCA}$ = $V_{DDD}$ = $V_{CCD}$ = 5 V; $V_{CCO}$ = 3.3 V and $T_{amb}$ = 25 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $G_{FINE}$ | fine gain correction range | minimum fine input code = 0 | – | 0 | – | dB |
| | | maximum fine input code = 31 | – | –0.5 | – | dB |
| $\Delta G_{amp}/\Delta T$ | amplifier gain stability variation with temperature | $V_{ref}$ with 100 ppm/°C maximum variation | – | 325 | – | ppm/°C |
| $I_{GC}$ | gain current | | – | ±20 | – | µA |
| $t_{stab}$ | amplifier gain adjustment speed from minimum to maximum gain | HSYNC active; capacitors on pins 8, 16 and 24 are 22 nF | – | 25 | – | mdB/µs |
| $V_{ref}$ | amplifier reference voltage | | – | 2.5 | – | V |
| $I_{ref}$ | amplifier reference voltage current | | – | 50 | – | µA |
| $V_{i(p-p)}$ | input voltage (peak-to-peak value) | corresponding to full-scale input at high gain | – | 0.4 | – | V |
| | | corresponding to full-scale output at low gain | – | – | 1.212 | V |
| $C_i$ | input capacitance | | – | 10 | – | pF |
| $G_{E(rms)}$ | channel-to-channel gain matching (RMS value) | maximum coarse gain; $T_{amb}$ = 25 °C | – | 1 | – | % |
| | | minimum coarse gain; $T_{amb}$ = 25 °C | – | 5 | – | % |
| **Clamps** | | | | | | |
| $P_{CLP}$ | precision | maximum black level noise on RGB channels = 10 mV; $T_{amb}$ = 25 °C | – | 0.5 | – | LSB |
| $t_{W(CLP)}$ | clamp pulse width | | 500 | – | 2000 | ns |
| $CLP_E$ | channel-to-channel clamp matching | | – | 0.5 | – | LSB |
| $A_{off}$ | code clamp reference | clamp register input code = 0 | – | –63.5 | – | LSB |
| | | clamp register input code = 255 | – | +64 | – | LSB |
| | | clamp register input code = 256 | – | +120 | – | LSB |
| | | clamp register input code = 287 | – | +135.5 | – | LSB |
| **Phase-locked loop (PLL)** | | | | | | |
| $j_{PLL(max)(p-p)}$ | long term PLL phase jitter (peak-to-peak value) | $f_{clk}$ = 205 MHz | – | 336 | – | ps |
| DR | divider ratio | | 100 | – | 4095 | – |
| $f_{ref}$ | reference clock frequency | | 15 | – | 150 | kHz |

**Table 17: Characteristics** *...continued*

*$V_{CCA}$ = 4.75 V to 5.25 V (referenced to AGND); $V_{CCD}$ = 4.75 V to 5.25 V (referenced to DGND); $V_{DDD}$ = 4.75 V to 5.25 V (referenced to $V_{SSD}$); $V_{CCO}$ = 3.0 V to 3.6 V (referenced to OGND); AGND, DGND, OGND and $V_{SS}$ connected together; $T_{amb}$ = 0 to 70 °C; typical values measured at $V_{CCA}$ = $V_{DDD}$ = $V_{CCD}$ = 5 V; $V_{CCO}$ = 3.3 V and $T_{amb}$ = 25 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{PLL}$ | output clock frequency | | 12 | – | 205 | MHz |
| $\Delta\Phi_{step}$ | phase drift[1] | standard at 160 Msps | – | – | 2 | step |
| $\Phi_{step}$ | phase shift step | $T_{amb}$ = 25 °C | – | 11.25 | – | deg |
| **ADCs** | | | | | | |
| $f_s$ | maximum sampling frequency | | 205 | – | – | MHz |
| INL | DC integral non-linearity | from IC analog input to digital output; sine wave input; $f_{clk}$ = 205 MHz | – | ±0.5 | ±1.5 | LSB |
| DNL | DC differential non-linearity | from IC analog input to digital output; sine wave input; $f_{clk}$ = 205 MHz | – | ±0.4 | ±1 | LSB |
| ENOB[2] | effective number of bits | | – | 7.4 | – | bits |
| **Signal-to-noise ratio** | | | | | | |
| S/N | signal-to-noise ratio | $f_{clk}$ = 205 MHz | – | 46 | – | dB |
| **Spurious free dynamic range** | | | | | | |
| SFDR | spurious free dynamic range | $f_{clk}$ = 205 MHz | – | 57 | – | dB |
| **Clock timing output (CKDATA)** | | | | | | |
| $\eta_{ext}$ | ADC clock duty factor | | 45 | 50 | 55 | % |
| $f_{clk(max)}$ | maximum clock frequency | | – | – | 205 | MHz |
| **Clock timing input (CKEXT)** | | | | | | |
| $f_{clk(max)}$ | maximum clock frequency | | – | – | 205 | MHz |
| $t_{CPH}$ | clock pulse width HIGH | | 2.5 | – | – | ns |
| $t_{CPL}$ | clock pulse width LOW | | 2.5 | – | – | ns |
| **Data timing[3]** | | | | | | |
| $t_{d(s)}$ | sampling delay time | referenced to CKDATA | – | –7.5 | – | ns |
| $t_{su(d)(o)}$ | output data set-up time | | – | –7 | – | ns |
| $t_{h(o)}$ | output hold time | | – | 1 | – | ns |
| **3-state output delay time** | | | | | | |
| $t_{dZH}$ | output enable HIGH | | – | 15 | – | ns |
| $t_{dZL}$ | output enable LOW | | – | 18 | – | ns |
| $t_{dHZ}$ | output disable HIGH | | – | 13 | – | ns |
| $t_{dLZ}$ | output disable LOW | | – | 10 | – | ns |
| **Data, sync, SW1 and SW2 outputs** | | | | | | |
| $V_{OL}$ | LOW-level output voltage | $I_o$ = 1 mA | – | – | 0.4 | V |
| $V_{OH}$ | HIGH-level output voltage | $I_o$ = 1 mA | 2.4 | – | – | V |
| $I_{OL}$ | LOW-level output current | | – | 0.2 | – | mA |
| $I_{OH}$ | HIGH-level output current | | – | 0.3 | – | mA |
| $C_L$ | load capacitance | | – | 10 | – | pF |

**Table 17: Characteristics** *...continued*

*$V_{CCA}$ = 4.75 V to 5.25 V (referenced to AGND); $V_{CCD}$ = 4.75 V to 5.25 V (referenced to DGND); $V_{DDD}$ = 4.75 V to 5.25 V (referenced to $V_{SSD}$); $V_{CCO}$ = 3.0 V to 3.6 V (referenced to OGND); AGND, DGND, OGND and $V_{SS}$ connected together; $T_{amb}$ = 0 to 70 °C; typical values measured at $V_{CCA}$ = $V_{DDD}$ = $V_{CCD}$ = 5 V; $V_{CCO}$ = 3.3 V and $T_{amb}$ = 25 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **TTL digital input level (CKREF, COAST, INV, HSYNC, CLP, DIS, I²C/$\overline{3W}$ and CKEXT)** | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | – | – | 0.8 | V |
| $V_{IH}$ | HIGH-level input voltage | | 2.0 | – | – | V |
| $I_{IL}$ | LOW-level input current | | – | 400 | – | µA |
| $I_{IH}$ | HIGH-level input current | | – | 35 | – | µA |
| **TTL digital input impedance (CKREF, COAST, INV, HSYNC, CLP and CKEXT)** | | | | | | |
| $Z_i$ | input impedance | | – | 4 | – | kΩ |
| $C_i$ | input capacitance | | – | 4 | – | pF |
| **TTL digital input impedance (DIS and I²C/$\overline{3W}$)** | | | | | | |
| $Z_i$ | input impedance | | – | 100 | – | kΩ |
| $C_i$ | input capacitance | | – | – | 10 | pF |
| **Sync on green input** | | | | | | |
| $V_{sync(G)}$ | sync on green pulse amplitude[4] | Slevel = 0; see Figure 5 | 300 | – | 600 | mV |
| | | Slevel = 1; see Figure 5 | 150 | – | 300 | mV |
| **3W-bus** | | | | | | |
| $t_{rst}$ | reset time of the chip before 3-wire communication | | – | 600 | – | ns |
| $t_{su}$ | data set-up time for 3-wire communication | | – | 100 | – | ns |
| $t_h$ | data hold time for 3-wire communication | | – | 100 | – | ns |
| **I²C-bus**[5] | | | | | | |
| $V_{IL}$ | LOW-level input voltage | for SCL and SDA | – | – | $0.3V_{DD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | for SCL and SDA; $V_{PU}$ = 5 V | 3 | – | – | V |
| | | for SCL and SDA; $V_{PU}$ = 3 V | $0.7V_{DD}$ | – | – | |
| $f_{SCL}$ | clock frequency | | 0 | – | 100 | kHz |
| $t_{BUF}$ | time the bus must be free before new transmission can start | | 4.7 | – | – | µs |
| $t_{HD;STA}$ | start condition hold time | | 4.0 | – | – | µs |
| $t_{SU;STA}$ | start condition set-up time | repeated start | 4.7 | – | – | µs |
| $t_{LOW}$ | LOW-level clock period | | 4.7 | – | – | µs |
| $t_{HIGH}$ | HIGH-level clock period | | 4.0 | – | – | µs |
| $t_{SU;DAT}$ | data set-up time | | 250 | – | – | ns |
| $t_{HD;DAT}$ | data hold time | | 0 | – | – | ns |
| $t_r$ | SDA and SCL rise time | $f_{SCL}$ = 100 kHz | – | – | 1.0 | µs |

**Table 17: Characteristics** *...continued*

*$V_{CCA}$ = 4.75 V to 5.25 V (referenced to AGND); $V_{CCD}$ = 4.75 V to 5.25 V (referenced to DGND); $V_{DDD}$ = 4.75 V to 5.25 V (referenced to $V_{SSD}$); $V_{CCO}$ = 3.0 V to 3.6 V (referenced to OGND); AGND, DGND, OGND and $V_{SS}$ connected together; $T_{amb}$ = 0 to 70 °C; typical values measured at $V_{CCA}$ = $V_{DDD}$ = $V_{CCD}$ = 5 V; $V_{CCO}$ = 3.3 V and $T_{amb}$ = 25 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_f$ | SDA and SCL fall time | $f_{SCL}$ = 100 kHz | – | – | 300 | ns |
| $t_{SU;STO}$ | stop condition set-up time | | 4.0 | – | – | µs |
| $C_b$ | bus line capacitive loading | | – | – | 400 | pF |

[1] From 25 to 70 °C, the edge of the clock CKDATA has a shift of 1 phase compared to CKREF.

[2] Effective bits are obtained from a Fast Fourier Transform (FFT) treatment taking 8000 acquisition points per equivalent fundamental period. The calculation takes into account all harmonics and noise up to half clock frequency (NYQUIST frequency). Conversion-to-noise ratio: S/N = EB × 6.02 + 1.76 dB.

[3] Output data acquisition: the output data is available after the maximum sampling delay time $t_{d(s)}$. All the timings are given for a 10 pF capacitive load.

[4] Pulse relative to the blank level.

[5] The $I^2C$-bus timings are given for use of the bus at a frequency of 100 kbit/s (100 kHz). This bus could be used at a frequency of 400 kbit/s (400 kHz).

**Table 18: Examples of PLL settings and performance**

*$V_{CCA}$ = $V_{DDD}$ = $V_{CCD}$ = 5 V; $V_{CCO}$ = 3.3 V; $T_{amb}$ = 25 °C.*

| Video standards | $f_{ref}$ (kHz) | $f_{clk}$ (MHz) | N | $K_O$ (MHz/V) | $C_Z$ (nF) | $C_P$ (nF) | $I_P$ (µA) | Z (kΩ) | Long-term time jitter[1] | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | RMS-value (ps) | peak-to-peak value (ps) |
| VESA: 640 × 480 (VGA 60 Hz) | 31.469 | 25.175 | 800 | 20 | 68 | 0.15 | 700 | 1.6 | tbf | tbf |
| VESA: 800 × 600 (SVGA 72 Hz) | 48.08 | 50 | 1040 | 30 | 68 | 0.15 | 400 | 3.2 | tbf | tbf |
| VESA: 1024 × 768 (XGA 75 Hz) | 60.02 | 78.75 | 1312 | 60 | 68 | 0.15 | 700 | 1.6 | tbf | tbf |
| VESA: 1280 × 1024 (SXGA 60 Hz) | 63.98 | 108 | 1688 | 60 | 68 | 0.15 | 700 | 2.25 | tbf | tbf |
| VESA: 1280 × 1024 (SXGA 75 Hz) | 80.00 | 135 | 1688 | 115 | 68 | 0.15 | 400 | 2.25 | tbf | tbf |
| VESA: 1600 × 1200 (UXGA 60 Hz) | 75.00 | 162 | 2160 | 115 | 68 | 0.15 | 400 | 3.2 | tbf | tbf |
| VESA: 1600 × 1200 (UXGA 75 Hz) | 93.75 | 202.5 | 2160 | 115 | 68 | 0.15 | 700 | 2.25 | tbf | tbf |

[1] PLL long-term time jitter is measured at the end of the video line, where it is at its maximum.

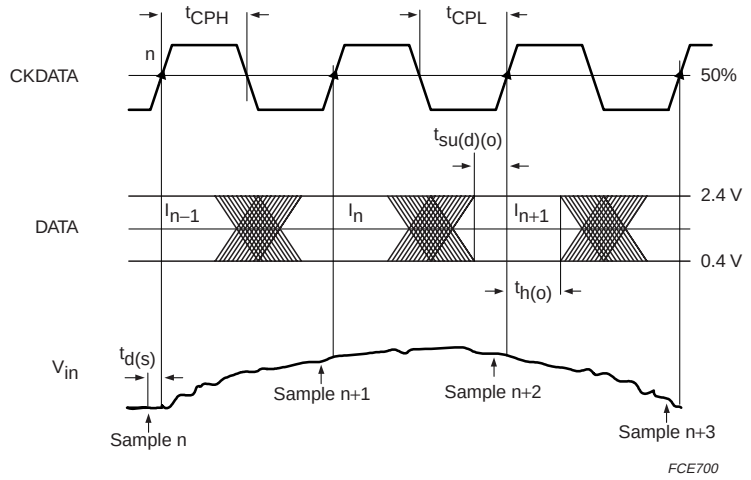



**Fig 10. Data timing; Dmx = 0; n = even pixel.**

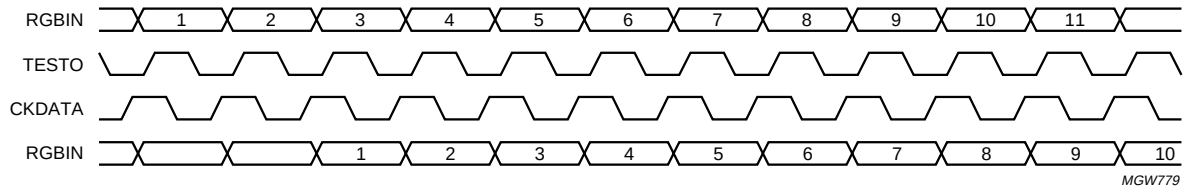



**Fig 11. Timing diagram; single port mode (Dmx = 0).**

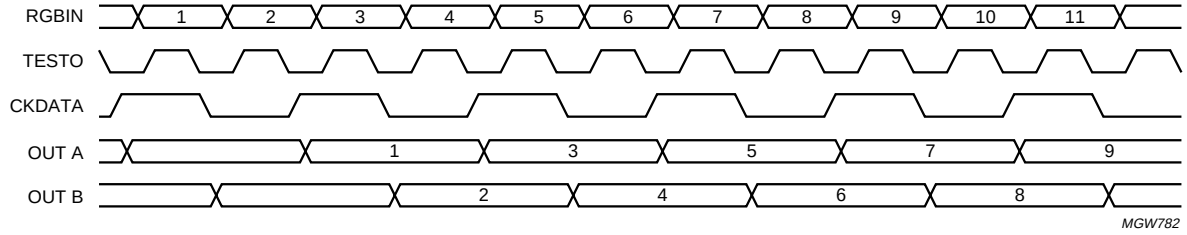



**Fig 12. Timing diagram; dual port mode (Dmx = 1), interleaved output (Shift = 1), odd pixel on port A (Odda = 1), don't care (Shpixel = x).**

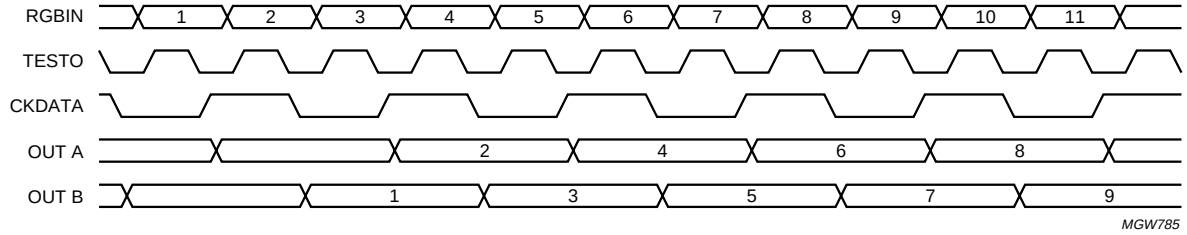



**Fig 13. Timing diagram; dual port mode (Dmx = 1), interleaved output (Shift = 1), even pixel on port A (Odda = 0), don't care (Shpixel = x).**

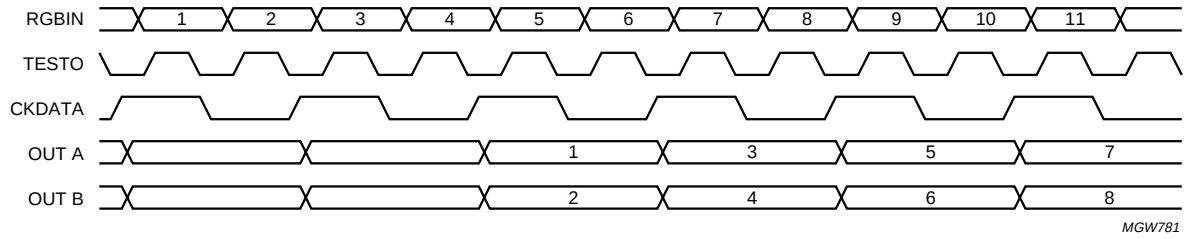



**Fig 14. Timing diagram; dual port mode (Dmx = 1), synchronized output (Shift = 0), odd pixel on port A (Odda = 1), pixel not shifted (Shpixel = 0).**

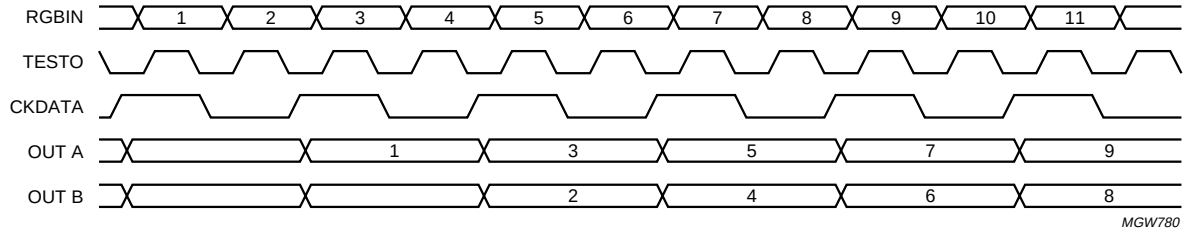



**Fig 15. Timing diagram; dual port mode (Dmx = 1), synchronized output (Shift = 0), odd pixel on port A (Odda = 1), pixel shifted (Shpixel = 1).**

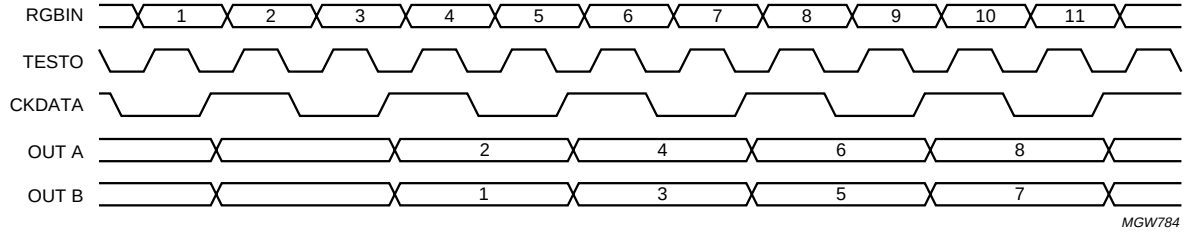



**Fig 16. Timing diagram; dual port mode (Dmx = 1), synchronized output (Shift = 0), even pixel on port A (Odda = 0), pixel not shifted (Shpixel = 0).**

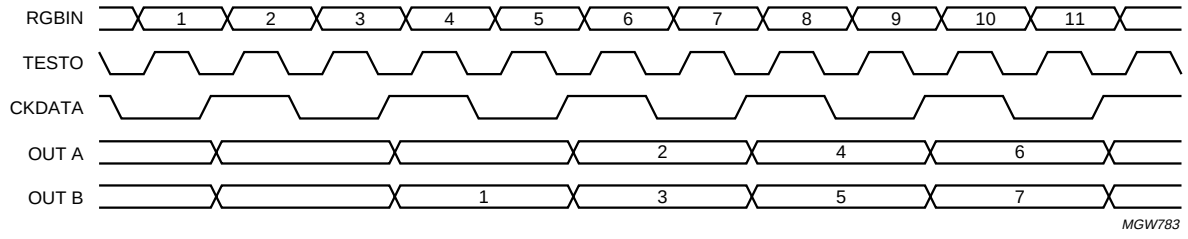



**Fig 17. Timing diagram; dual port mode (Dmx = 1), synchronized output (Shift = 0), even pixel on port A (Odda = 0), pixel shifted (Shpixel = 1).**

# 13. Application information

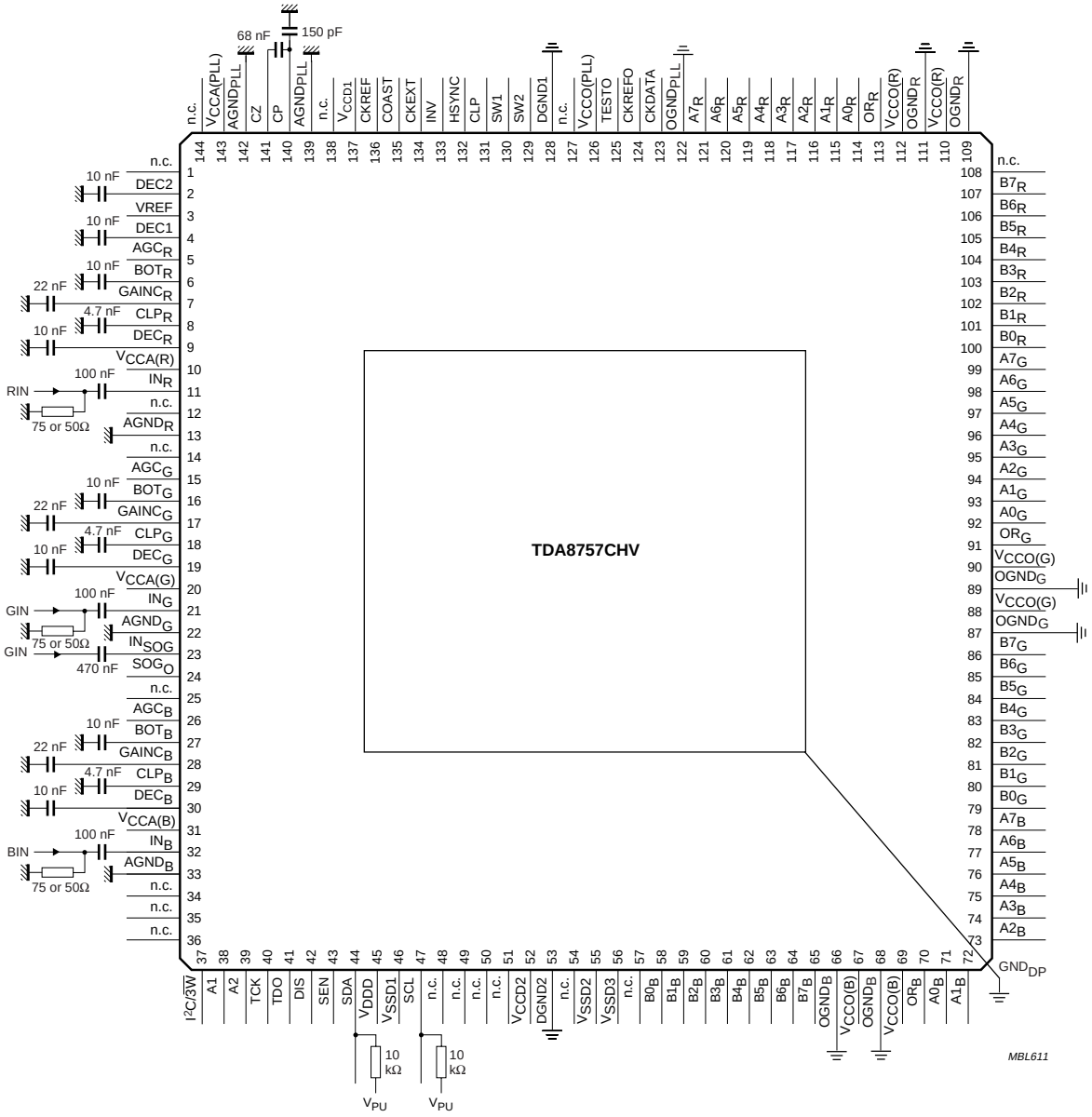
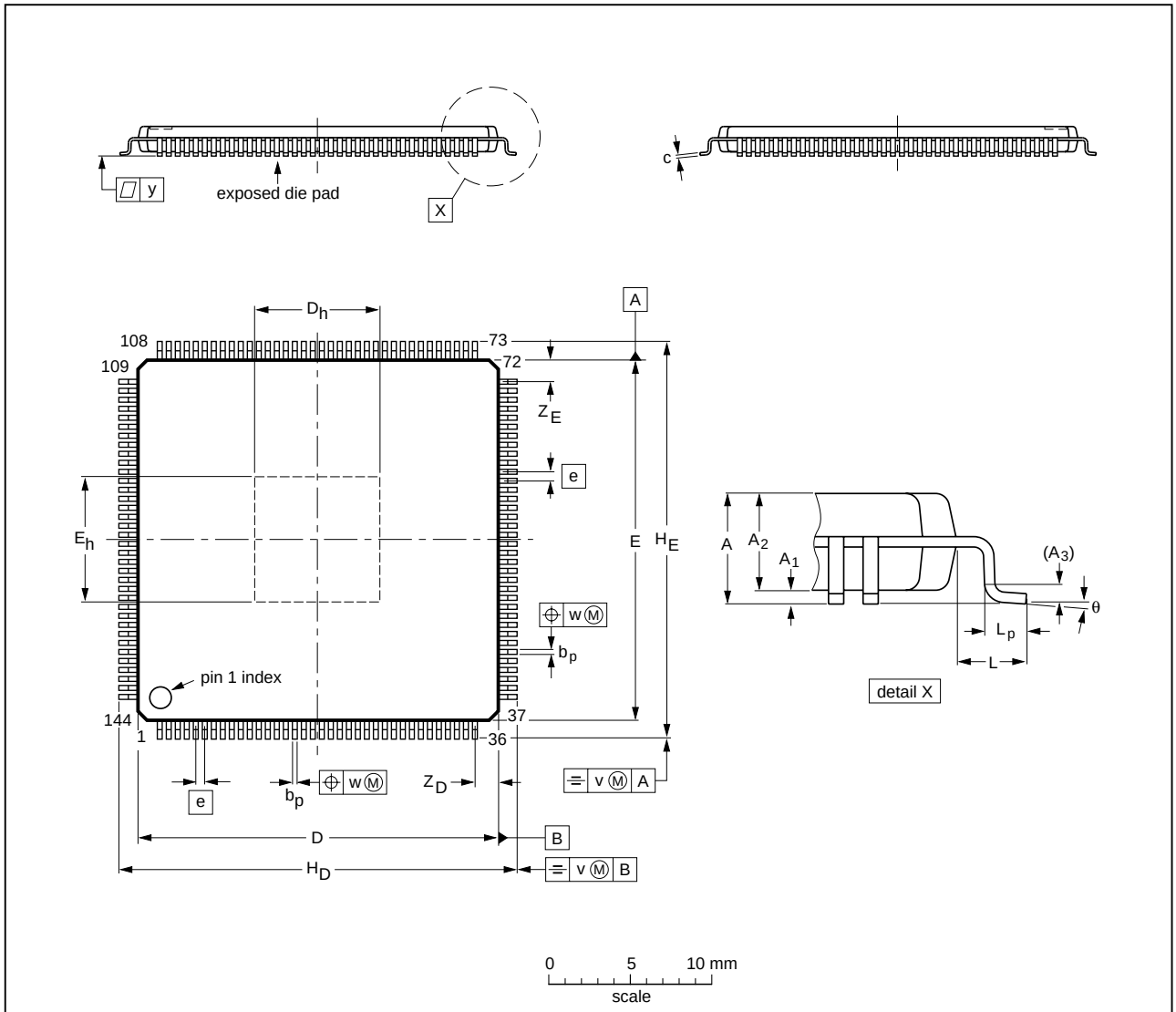



Fig 18. Application diagram.

## 14. Package outline

**HLQFP144: plastic thermal enhanced low profile quad flat package; 144 leads; body 20 x 20 x 1.4 mm; exposed die pad** **SOT612-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $D_h$ | $E^{(1)}$ | $E_h$ | e | $H_D$ | $H_E$ | L | $L_p$ | v | w | y | $Z_D^{(1)}$ | $Z_E^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.6 | 0.15<br>0.05 | 1.45<br>1.35 | 0.25 | 0.27<br>0.17 | 0.20<br>0.09 | 20.1<br>19.9 | 7.1<br>6.9 | 20.1<br>19.9 | 7.1<br>6.9 | 0.5 | 22.15<br>21.85 | 22.15<br>21.85 | 1 | 0.75<br>0.45 | 0.2 | 0.08 | 0.08 | 1.4<br>1.1 | 1.4<br>1.1 | $7^o$<br>$0^o$ |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT612-1 | | MS-026 | | | | ~~02-01-25~~<br>02-04-24 |

**Fig 19. Package outline.**

# 15. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

# 16. Soldering

## 16.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

## 16.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C small/thin packages.

## 16.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

## 16.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

## 16.5 Package related soldering information

**Table 19: Suitability of surface mount IC packages for wave and reflow soldering methods**

| Package[1] | Soldering method | |
|---|---|---|
| | Wave | Reflow[2] |
| BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA | not suitable | suitable |
| HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS | not suitable[3] | suitable |
| PLCC[4], SO, SOJ | suitable | suitable |
| LQFP, QFP, TQFP | not recommended[4][5] | suitable |
| SSOP, TSSOP, VSO | not recommended[6] | suitable |

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[4] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[5] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[6] Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

# 17. Revision history

**Table 20: Revision history**

| Rev | Date | CPCN | Description |
|---|---|---|---|
| 01 | 20020814 | - | Preliminary data (9397 750 10111). |

## 18. Data sheet status

| Data sheet status[1] | Product status[2] | Definition |
|---|---|---|
| Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| Preliminary data | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
| Product data | Production | This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A. |

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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**Limiting values definition —** Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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## Contents





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