# ADC1610S series

## Single 16-bit ADC; 65 Msps, 80 Msps, 105 Msps or 125 Msps; CMOS or LVDS DDR digital outputs

Rev. 02 — 12 April 2010 Objective data sheet

## 1. General description

The ADC1610S is a single-channel 16-bit Analog-to-Digital Converter (ADC) optimized for high dynamic performances and low power consumption at sample rates up to 125 Msps. Pipelined architecture and output error correction ensure the ADC1610S is accurate enough to guarantee zero missing codes over the entire operating range. Supplied from a single 3 V source, it can handle output logic levels from 1.8 V to 3.3 V in CMOS mode, because of a separate digital output supply. It supports the Low Voltage Differential Signalling (LVDS) Double Data Rate (DDR) output standard. An integrated Serial Peripheral Interface (SPI) allows the user to easily configure the ADC. The device also includes a SPI programmable full-scale to allow flexible input voltage range from 1 V to 2 V (peak-to-peak). With excellent dynamic performance from the baseband to input frequencies of 170 MHz or more, the ADC1610S is ideal for use in communications, imaging and medical applications.

## 2. Features and benefits

- SNR, 72.5 dBFS; SFDR, 88 dBc
- Sample rate up to 125 Msps
- 16-bit pipelined ADC core
- Clock input divider by 2 for less jitter contribution
- Single 3 V supply
- Flexible input voltage range: 1 V to 2 V (peak-to-peak).
- CMOS or LVDS DDR digital outputs
- Power-down and Sleep modes
- Input bandwidth, 600 MHz
- Power dissipation, 430 mW at 80 Msps
- Serial Peripheral Interface (SPI)
- Duty cycle stabilizer
- Fast OuT of Range (OTR) detection
- INL ±1 LSB, DNL ±0.5 LSB
- Offset binary, two's complement, gray code
- HVQFN40 package

## 3. Applications

- Wireless and wired broadband communications
- Spectral analysis
- Ultrasound equipment
- Portable instrumentation
- Imaging systems
- Software define radio

## 4. Ordering information

**Table 1. Ordering information**

| Type number | $f_s$ (Msps) | Package | | |
|---|---|---|---|---|
| | | Name | Description | Version |
| ADC1610S125HN/C1 | 125 | HVQFN40 | plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 × 6 × 0.85 mm | SOT618-6 |
| ADC1610S105HN/C1 | 105 | HVQFN40 | plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 × 6 × 0.85 mm | SOT618-6 |
| ADC1610S080HN/C1 | 80 | HVQFN40 | plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 × 6 × 0.85 mm | SOT618-6 |
| ADC1610S065HN/C1 | 65 | HVQFN40 | plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 × 6 × 0.85 mm | SOT618-6 |

## 5. Block diagram

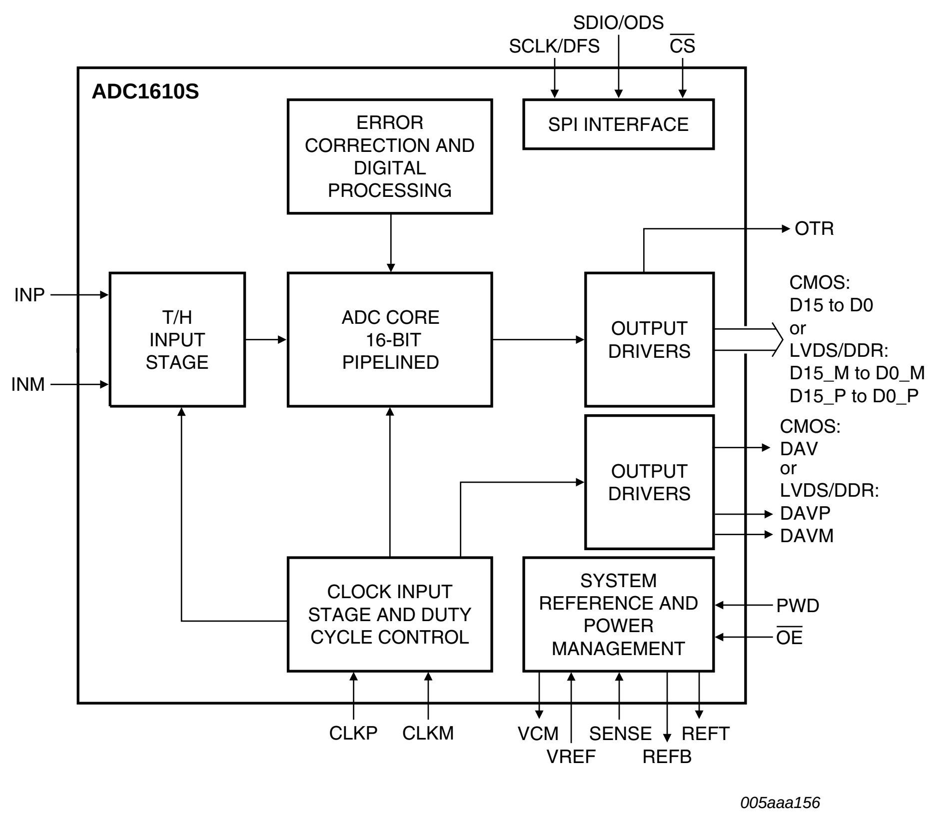



**Fig 1. Block diagram**

# 6. Pinning information

## 6.1 Pinning

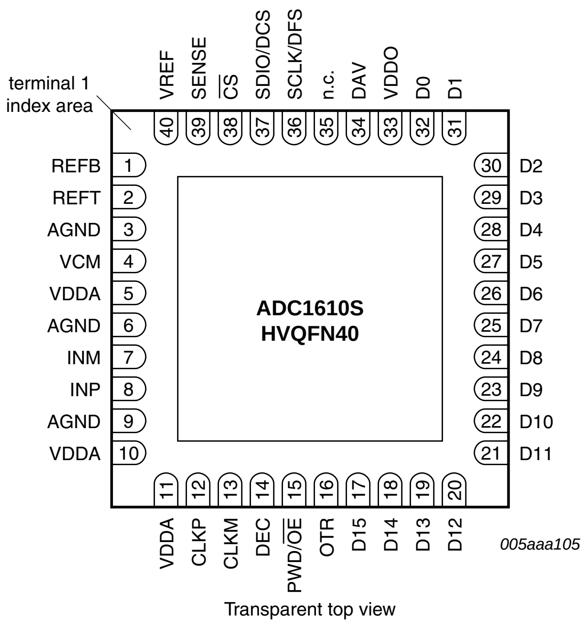



Fig 2. Pin configuration with CMOS digital outputs selected

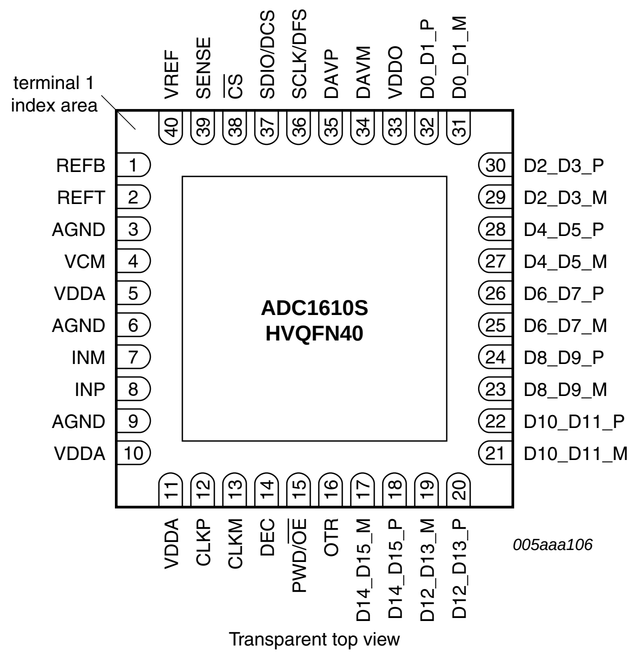



Fig 3. Pin configuration with LVDS/DDR digital outputs selected

## 6.2 Pin description

Table 2. Pin description (CMOS digital outputs)

| Symbol | Pin | Type[1] | Description |
|---|---|---|---|
| REFB | 1 | O | bottom reference |
| REFT | 2 | O | top reference |
| AGND | 3 | G | analog ground |
| VCM | 4 | O | common-mode output voltage |
| VDDA | 5 | P | analog power supply |
| AGND | 6 | G | analog ground |
| INM | 7 | I | complementary analog input |
| INP | 8 | I | analog input |
| AGND | 9 | G | analog ground |
| VDDA | 10 | P | analog power supply |
| VDDA | 11 | P | analog power supply |
| CLKP | 12 | I | clock input |
| CLKM | 13 | I | complementary clock input |
| DEC | 14 | O | regulator decoupling node |
| PWD/$\overline{OE}$ | 15 | I | power down, active HIGH; output enable, active LOW |
| OTR | 16 | O | out of range |

Table 2. Pin description (CMOS digital outputs)

| Symbol | Pin | Type[1] | Description |
|---|---|---|---|
| D15 | 17 | O | data output bit 15 (MSB) |
| D14 | 18 | O | data output bit 14 |
| D13 | 19 | O | data output bit 13 |
| D12 | 20 | O | data output bit 12 |
| D11 | 21 | O | data output bit 11 |
| D10 | 22 | O | data output bit10 |
| D9 | 23 | O | data output bit 9 |
| D8 | 24 | O | data output bit 8 |
| D7 | 25 | O | data output bit 7 |
| D6 | 26 | O | data output bit 6 |
| D5 | 27 | O | data output bit 5 |
| D4 | 28 | O | data output bit 4 |
| D3 | 29 | O | data output bit 3 |
| D2 | 30 | O | data output bit 2 |
| D1 | 31 | O | data output bit 1 |
| D0 | 32 | O | data output bit 0 (LSB) |
| VDDO | 33 | P | output power supply |
| DAV | 34 | O | data valid output clock |
| n.c. | 35 | - | not connected |
| SCLK/DFS | 36 | I | SPI clock / data format select |
| SDIO/ODS | 37 | I/O | SPI data IO / output data standard |
| $\overline{CS}$ | 38 | I | SPI chip select |
| SENSE | 39 | I | reference programming pin |
| VREF | 40 | I/O | voltage reference input/output |

[1] P: power supply; G: ground; I: input; O: output; I/O: input/output.

Table 3. Pin description (LVDS/DDR) digital outputs)

| Symbol | Pin[1] | Type[2] | Description |
|---|---|---|---|
| D14_D15_M | 17 | O | differential output data D14 and D15 multiplexed, complement |
| D14_D15_P | 18 | O | differential output data D14 and D15 multiplexed, true |
| D12_D13_M | 19 | O | differential output data D12 and D13 multiplexed, complement |
| D12_D13_P | 20 | O | differential output data D12 and D13 multiplexed, true |
| D10_D11_M | 21 | O | differential output data D10 and D11multiplexed, complement |
| D10_D11_P | 22 | O | differential output data D10 and D11 multiplexed, true |
| D8_D9_M | 23 | O | differential output data D8 and D9 multiplexed, complement |
| D8_D9_P | 24 | O | differential output data D8 and D9 multiplexed, true |
| D6_D7_M | 25 | O | differential output data D6 and D7 multiplexed, complement |
| D6_D7_P | 26 | O | differential output data D6 and D7 multiplexed, true |
| D4_D5_M | 27 | O | differential output data D4 and D5 multiplexed, complement |
| D4_D5_P | 28 | O | differential output data D4 and D5 multiplexed, true |
| D2_D3_M | 29 | O | differential output data D2 and D3 multiplexed, complement |
| D2_D3_P | 30 | O | differential output data D2 and D3 multiplexed, true |
| D0_D1_M | 31 | O | differential output data D0 and D1 multiplexed, complement |
| D0_D1_P | 32 | O | differential output data D0 and D1 multiplexed, true |
| DAVM | 34 | O | data valid output clock, complement |
| DAVP | 35 | O | data valid output clock, true |

[1] Pins 1 to 16 and pins 36 to 40 are the same for both CMOS and LVDS DDR outputs (see Table 2)

[2] P: power supply; G: ground; I: input; O: output; I/O: input/output.

## 7. Limiting values

Table 4. Limiting values

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_O$ | output voltage | pins D15 to D0; pins D15P to D0P; pins D15M to D0M | –0.4 | +3.9 | V |
| $V_{DDA}$ | analog supply voltage | | –0.4 | +3.9 | V |
| $V_{DDO}$ | output supply voltage | | –0.4 | +3.9 | V |
| $T_{stg}$ | storage temperature | | –55 | +125 | °C |
| $T_{amb}$ | ambient temperature | | –40 | +85 | °C |
| $T_j$ | junction temperature | | - | 125 | °C |

## 8. Thermal characteristics

Table 5. Thermal characteristics

| Symbol | Parameter | Conditions | Typ | Unit |
|---|---|---|---|---|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | [1] | 22.5 | K/W |
| $R_{th(j-c)}$ | thermal resistance from junction to case | [1] | 11.7 | K/W |

[1] Value for six layers board in still air with a minimum of 25 thermal vias.

## 9. Static characteristics

Table 6. Static characteristics[1]

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supplies** | | | | | | |
| $V_{DDA}$ | analog supply voltage | | 2.85 | 3.0 | 3.4 | V |
| $V_{DDO}$ | output supply voltage | CMOS mode | 1.65 | 1.8 | 3.6 | V |
| | | LVDS DDR mode | 2.85 | 3.0 | 3.6 | V |
| $I_{DDA}$ | analog supply current | $f_{clk}$ = 125 Msps; $f_i$ =70 MHz | - | 210 | - | mA |
| $I_{DDO}$ | output supply current | CMOS mode; $f_{clk}$ = 125 Msps; $f_i$ =70 MHz | - | 14 | - | mA |
| | | LVDS DDR mode: $f_{clk}$ = 125 Msps; $f_i$ =70 MHz | - | 43 | - | mA |
| P | power dissipation | ADC1610S125; analog supply only | - | 630 | - | mW |
| | | ADC1610S105; analog supply only | - | 550 | - | mW |
| | | ADC1610S080; analog supply only | - | 430 | - | mW |
| | | ADC1610S065; analog supply only | - | 380 | - | mW |
| | | power-down mode | - | 2 | - | mW |
| | | sleep mode | - | 40 | - | mW |
| **Clock inputs: pins CLKP and CLKM** | | | | | | |
| LVPECL | | | | | | |
| $V_{i(clk)dif}$ | differential clock input voltage | peak-to-peak | - | ±0.8 | - | V |
| LVDS | | | | | | |
| $V_{i(clk)dif}$ | differential clock input voltage | peak-to-peak | - | ±0.70 | - | V |
| SINE wave | | | | | | |
| $V_{i(clk)dif}$ | differential clock input voltage | peak-to-peak | ±0.8 | ±3.0 | - | V |
| LVCMOS | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | - | - | $0.3V_{DDA}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | $0.7V_{DDA}$ | - | - | V |
| **Logic inputs, Power-down: pin PWD/OEB** | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | - | 0 | - | V |
| | | LOW-medium level | - | $0.3V_{DDA}$ | - | V |
| | | Medium-HIGH level | - | $0.6V_{DDA}$ | - | V |
| $V_{IH}$ | HIGH-level input voltage | | - | $V_{DDA}$ | - | V |
| $I_{IL}$ | LOW-level input current | | <tbd> | - | <tbd> | µA |
| $I_{IH}$ | HIGH-level input current | | −10 | - | +10 | µA |
| **Serial peripheral interface: pins $\overline{CS}$, SDIO/ODS, SCLK/DFS** | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | 0 | - | $0.3V_{DDA}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | $0.7V_{DDA}$ | - | $V_{DDA}$ | V |
| $I_{IL}$ | LOW-level input current | | −10 | - | +10 | µA |

**Table 6. Static characteristics[1]** *…continued*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IH}$ | HIGH-level input current | | –50 | - | +50 | µA |
| $C_I$ | input capacitance | | - | 4 | - | pF |
| **Digital outputs, CMOS mode: pins D15 to D0, OTR, DAV** | | | | | | |
| Output levels, $V_{DDO}$ = 3 V | | | | | | |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = <tbd> | OGND | - | 0.2$V_{DDO}$ | V |
| $V_{OH}$ | HIGH-level output voltage | $I_{OH}$ = <tbd> | 0.8$V_{DDO}$ | - | $V_{DDO}$ | V |
| $I_{OL}$ | LOW-level output current | 3-state; output level = 0 V | - | <tbd> | - | µA |
| $I_{OH}$ | HIGH-level output current | 3-state; output level = $V_{DDA}$ | - | <tbd> | - | µA |
| $C_O$ | output capacitance | high impedance; $\overline{OE}$ = HIGH | - | 3 | - | pF |
| Output levels, $V_{DDO}$ = 1.8 V | | | | | | |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = <tbd> | OGND | - | 0.2$V_{DDO}$ | V |
| $V_{OH}$ | HIGH-level output voltage | $I_{OH}$ = <tbd> | 0.8$V_{DDO}$ | - | $V_{DDO}$ | V |
| **Digital outputs, LVDS mode: pins D15P to D0P, D15M to D0M, DAVP and DAVM** | | | | | | |
| Output levels, $V_{DDO}$ = 3 V only, $R_L$ = 100 Ω | | | | | | |
| $V_{O(offset)}$ | output offset voltage | output buffer current set to 3.5 mA | - | 1.2 | - | V |
| $V_{O(dif)}$ | differential output voltage | output buffer current set to 3.5 mA | - | 350 | - | mV |
| $C_O$ | output capacitance | | - | <tbd> | - | pF |
| **Analog inputs: pins INP and INM** | | | | | | |
| $I_I$ | input current | | –5 | - | +5 | µA |
| $R_I$ | input resistance | | - | <tbd> | - | Ω |
| $C_I$ | input capacitance | | - | 5 | - | pF |
| $V_{I(cm)}$ | common mode input voltage | $V_{INP} = V_{INM}$ | 0.9 | 1.5 | 2 | V |
| $B_i$ | input bandwidth | | - | 600 | - | MHz |
| $V_{I(dif)}$ | differential input voltage | peak-to-peak | 1 | | 2 | V |
| **Common mode output voltage: pin VCM** | | | | | | |
| $V_{O(cm)}$ | common-mode output voltage | | - | $V_{DDA}$ / 2 | - | V |
| $I_{O(cm)}$ | common-mode output current | | - | <tbd> | - | µA |
| **I/O reference voltage: pin VREF** | | | | | | |
| $V_{VREF}$ | voltage on pin VREF | output | 0.5 | - | 1 | V |
| | | input | 0.5 | - | 1 | V |
| **Accuracy** | | | | | | |
| INL | integral non-linearity | | - | ±4 | - | LSB |
| DNL | differential non-linearity | guaranteed no missing codes | -0.95 | ±0.5 | +0.95 | LSB |
| $E_{offset}$ | offset error | | - | ±2 | - | mV |
| $E_G$ | gain error | full-scale | | ±0.5 | | % |

**Table 6. Static characteristics**[1] *…continued*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supply** | | | | | | |
| PSRR | power supply rejection ratio | 100 mV (p-p) on $V_{DDA}$ | - | 35 | - | dBc |

[1] Typical values measured at $V_{DDA}$ = 3 V, $V_{DDO}$ = 1.8 V, $T_{amb}$ = 25 °C and $C_L$ = 5 pF; minimum and maximum values are across the full temperature range $T_{amb}$ = −40 °C to +85 °C at $V_{DDA}$ = 3 V, $V_{DDO}$ = 1.8 V; $V_{INP} - V_{INM}$ = −1 dBFS; internal reference mode; applied to CMOS and LVDS interface; unless otherwise specified.

# 10. Dynamic characteristics

## 10.1 Dynamic characteristics

**Table 7. Dynamic characteristics**

| Symbol | Parameter | Conditions | | ADC1610S065 | | | ADC1610S080 | | | ADC1610S105 | | | ADC1610S125 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| **Analog signal processing** | | | | | | | | | | | | | | | | |
| $\alpha_{2H}$ | second harmonic level | $f_i$ = 3 MHz | | - | 89 | - | - | 89 | - | - | 88 | - | - | 90 | - | dBc |
| | | $f_i$ = 30 MHz | | - | 88 | - | - | 88 | - | - | 88 | - | - | 89 | - | dBc |
| | | $f_i$ = 70 MHz | | - | 87 | - | - | 87 | - | - | 86 | - | - | 87 | - | dBc |
| | | $f_i$ = 170 MHz | | - | 84 | - | - | 84 | - | - | 83 | - | - | 85 | - | dBc |
| $\alpha_{3H}$ | third harmonic level | $f_i$ = 3 MHz | | - | 88 | - | - | 88 | - | - | 87 | - | - | 89 | - | dBc |
| | | $f_i$ = 30 MHz | | - | 87 | - | - | 87 | - | - | 87 | - | - | 88 | - | dBc |
| | | $f_i$ = 70 MHz | | - | 86 | - | - | 86 | - | - | 85 | - | - | 86 | - | dBc |
| | | $f_i$ = 170 MHz | | - | 83 | - | - | 83 | - | - | 82 | - | - | 84 | - | dBc |
| THD | total harmonic distortion | $f_i$ = 3 MHz | | - | 87 | - | - | 87 | - | - | 86 | - | - | 88 | - | dBc |
| | | $f_i$ = 30 MHz | | - | 86 | - | - | 86 | - | - | 86 | - | - | 87 | - | dBc |
| | | $f_i$ = 70 MHz | | - | 85 | - | - | 85 | - | - | 84 | - | - | 85 | - | dBc |
| | | $f_i$ = 170 MHz | | - | 82 | - | - | 82 | - | - | 81 | - | - | 83 | - | dBc |
| ENOB | effective number of bits | $f_i$ = 3 MHz | | - | 11.7 | - | - | 11.7 | - | - | 11.7 | - | - | 11.6 | - | bits |
| | | $f_i$ = 30 MHz | | - | 11.6 | - | - | 11.6 | - | - | 11.6 | - | - | 11.6 | - | bits |
| | | $f_i$ = 70 MHz | | - | 11.5 | - | - | 11.5 | - | - | 11.5 | - | - | 11.5 | - | bits |
| | | $f_i$ = 170 MHz | | - | 11.4 | - | - | 11.4 | - | - | 11.4 | - | - | 11.4 | - | bits |
| SNR | signal-to-noise ratio | $f_i$ = 3 MHz | | - | 72.3 | - | - | 72.2 | - | - | 72.0 | - | - | 71.6 | - | dBFS |
| | | $f_i$ = 30 MHz | | - | 71.5 | - | - | 71.4 | - | - | 71.4 | - | - | 71.3 | - | dBFS |
| | | $f_i$ = 70 MHz | | - | 70.9 | - | - | 70.9 | - | - | 70.8 | - | - | 70.7 | - | dBFS |
| | | $f_i$ = 170 MHz | | - | 70.4 | - | - | 70.3 | - | - | 70.2 | - | - | 70.1 | - | dBFS |
| SFDR | spurious-free dynamic range | $f_i$ = 3 MHz | | - | 88 | - | - | 88 | - | - | 87 | - | - | 89 | - | dBc |
| | | $f_i$ = 30 MHz | | - | 87 | - | - | 87 | - | - | 87 | - | - | 88 | - | dBc |
| | | $f_i$ = 70 MHz | | - | 86 | - | - | 86 | - | - | 85 | - | - | 86 | - | dBc |
| | | $f_i$ = 170 MHz | | - | 83 | - | - | 83 | - | - | 82 | - | - | 84 | - | dBc |

**Table 7. Dynamic characteristics** *…continued*

| Symbol | Parameter | Conditions | | ADC1610S065 | | | ADC1610S080 | | | ADC1610S105 | | | ADC1610S125 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| IMD | intermodulation distortion | $f_i$ = 3 MHz | | - | 89 | - | - | 89 | - | - | 88 | - | - | 89 | - | dBc |
| | | $f_i$ = 30 MHz | | - | 88 | - | - | 88 | - | - | 88 | - | - | 88 | - | dBc |
| | | $f_i$ = 70 MHz | | - | 87 | - | - | 87 | - | - | 86 | - | - | 86 | - | dBc |
| | | $f_i$ = 170 MHz | | - | 84 | - | - | 85 | - | - | 83 | - | - | 84 | - | dBc |

[1] Typical values measured at $V_{DDA}$ = 3 V, $V_{DDO}$ = 1.8 V, $T_{amb}$ = 25 °C and $C_L$ = 5 pF; minimum and maximum values are across the full temperature range $T_{amb}$ = −40 °C to +85 °C at $V_{DDA}$ = 3 V, $V_{DDO}$ = 1.8 V; $V_{INP} - V_{INM}$ = −1 dBFS; internal reference mode; applied to CMOS and LVDS interface; unless otherwise specified.

## 10.2 Clock and digital output timing

**Table 8. Clock and digital output timing characteristics[1]**

| Symbol | Parameter | Conditions | ADC1610S065 | | | ADC1610S080 | | | ADC1610S105 | | | ADC1610S125 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| **Clock timing input: pins CLKP and CLKM** | | | | | | | | | | | | | | | |
| $f_{clk}$ | clock frequency | | 20 | - | 65 | 60 | - | 80 | 75 | - | 105 | 100 | - | 125 | MHz |
| $t_{lat(data)}$ | data latency time | clock cycles | - | 14 | - | - | 14 | - | - | 14 | - | - | 14 | - | clock cycle |
| $\delta_{clk}$ | clock duty cycle | DCS_EN = 1 | 30 | 50 | 70 | 30 | 50 | 70 | 30 | 50 | 70 | 30 | 50 | 70 | % |
| | | DCS_EN = 0 | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | % |
| $t_{d(s)}$ | sampling delay time | | - | 0.8 | - | - | 0.8 | - | - | 0.8 | - | - | 0.8 | - | ns |
| $t_{wake}$ | wake-up time | | - | <tbd> | - | - | <tbd> | - | - | <tbd> | - | - | <tbd> | - | ns |
| **CMOS Mode Timing output: pins D15 to D0 and DAV** | | | | | | | | | | | | | | | |
| $t_{PD}$ | propagation delay | DATA | - | 3.9 | - | - | 3.9 | - | - | 3.9 | - | - | 3.9 | - | ns |
| | | DAV | - | 4.2 | - | - | 4.2 | - | - | 4.2 | - | - | 4.2 | - | ns |
| $t_{su}$ | set-up time | | - | 7.7 | - | - | 6.5 | - | - | 4.7 | - | - | 4.3 | - | ns |
| $t_h$ | hold time | | - | 6.7 | - | - | 5.5 | - | - | 3.8 | - | - | 3.5 | - | ns |
| $t_r$ | rise time[2] | DATA | 0.5 | - | 2.4 | 0.5 | - | 2.4 | 0.5 | - | 2.4 | 0.5 | - | 2.4 | ns |
| | | DAV | 0.5 | - | 2.4 | 0.5 | - | 2.4 | 0.5 | - | 2.4 | 0.5 | - | 2.4 | ns |
| $t_f$ | fall time[2] | DATA | 0.5 | - | 2.4 | 0.5 | - | 2.4 | 0.5 | - | 2.4 | 0.5 | - | 2.4 | ns |
| **LVDS DDR mode timing output: pins D15P to D0P, D15M to D0M, DAVP and DAVM** | | | | | | | | | | | | | | | |
| $t_{PD}$ | propagation delay | DATA | - | 3.9 | - | - | 3.9 | - | - | 3.9 | - | - | 3.9 | - | ns |
| | | DAV | - | 4.2 | - | - | 4.2 | - | - | 4.2 | - | - | 4.2 | - | ns |
| $t_{su}$ | set-up time | | - | 5.1 | - | - | 3.5 | - | - | 2.1 | - | - | 1.4 | - | ns |
| $t_h$ | hold time | | - | 2.0 | - | - | 2.0 | - | - | 2.0 | - | - | 2.0 | - | ns |
| $t_r$ | rise time[3] | DATA | 50 | 100 | 200 | 50 | 100 | 200 | 50 | 100 | 200 | 50 | 100 | 200 | ps |
| | | DAV | 50 | 100 | 200 | 50 | 100 | 200 | 50 | 100 | 200 | 50 | 100 | 200 | ps |
| $t_f$ | fall time[3] | DATA | 50 | 100 | 200 | 50 | 100 | 200 | 50 | 100 | 200 | 50 | 100 | 200 | ps |
| | | DAV | 50 | 100 | 200 | 50 | 100 | 200 | 50 | 100 | 200 | 50 | 100 | 200 | ps |

[1] Typical values measured at $V_{DDA}$ = 3 V, $V_{DDO}$ = 1.8 V, $T_{amb}$ = 25 °C and $C_L$ = 5 pF; minimum and maximum values are across the full temperature range $T_{amb}$ = −40 °C to +85 °C at $V_{DDA}$ = 3 V, $V_{DDO}$ = 1.8 V; $V_{INP} - V_{INM}$ = −1 dBFS; internal reference mode; applied to CMOS and LVDS interface; unless otherwise specified.

[2] Measured between 20 % to 80 % of $V_{DDO}$.

[3] Rise time measured from −50 mV to +50 mV; fall time measured from +50 mV to −50 mV.

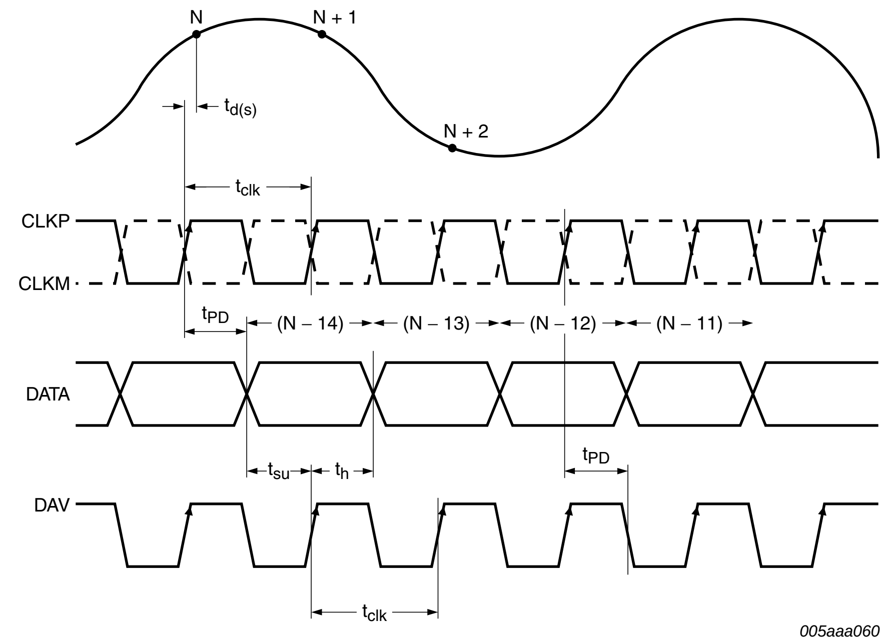



**Fig 4. CMOS mode timing**

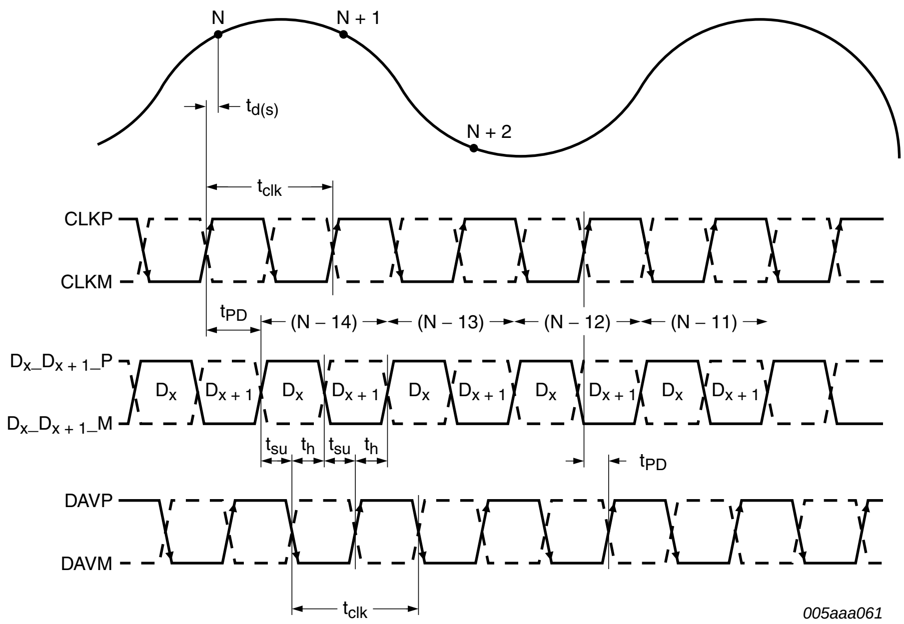



**Fig 5. LDVS DDR mode timing**

## 10.3 SPI timings

**Table 9. SPI timings characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{w(SCLK)}$ | SCLK pulse width | | 40 | - | - | ns |
| $t_{w(SCLKH)}$ | SCLK HIGH pulse width | | 16 | - | - | ns |
| $t_{w(SCLKL)}$ | SCLK LOW pulse width | | 16 | - | - | ns |
| $t_{su}$ | set-up time | data to SCLK HIGH | 5 | - | - | ns |
| | | $\overline{CS}$ to SCLK HIGH | 5 | - | - | ns |
| $t_h$ | hold time | data to SCLK HIGH | 2 | - | - | ns |
| | | $\overline{CS}$ to SCLK HIGH | 2 | - | - | ns |
| $f_{clk(max)}$ | maximum clock frequency | | - | - | 25 | MHz |

[1] Typical values measured at $V_{DDA}$ = 3 V, $V_{DDO}$ = 1.8 V, $T_{amb}$ = 25 °C and $C_L$ = 5 pF; minimum and maximum values are across the full temperature range $T_{amb}$ = −40 °C to +85 °C at $V_{DDA}$ = 3 V, $V_{DDO}$ = 1.8 V

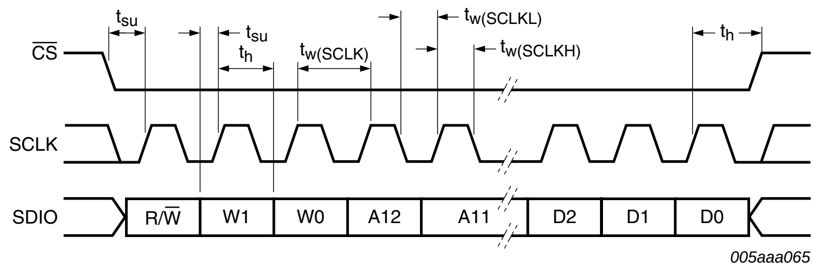



**Fig 6. SPI timing**

# 11. Application information

## 11.1 Device control

The ADC1610S can be controlled via SPI or directly via the I/O pins (Pin control mode).

### 11.1.1 SPI and Pin control modes

The device enters Pin control mode at power-up, and remains in this mode as long as pin $\overline{CS}$ is held HIGH. In Pin control mode, the SPI pins SDIO, $\overline{CS}$ and SCLK are used as static control pins.

SPI control mode is enabled by forcing pin $\overline{CS}$ LOW. Once SPI control mode has been enabled, the device will remain in this mode. The transition from Pin control mode to SPI control mode is illustrated in Figure 7.

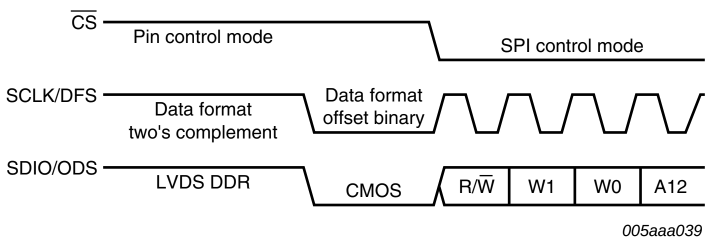



**Fig 7. Control mode selection**

When the device enters SPI control mode, the output data standard and data format are determined by the level on pin SDIO as soon as a transition is triggered by a falling edge on $\overline{CS}$.

### 11.1.2 Operating mode selection

The active ADC1610S operating mode (Power-up, Power-down or Sleep) can be selected via the SPI interface (see Table 20) or using in Pin control mode, as described in Table 10.

**Table 10. Operating mode selection pin PWD/OEB**

| Pin PWD/OEB | Power mode | Output high-z |
|---|---|---|
| 0 | Power-down | yes |
| 1/3 VCCA | Sleep | yes |
| 2/3 VCCA | Power-up | yes |
| VCCA | Power-up | no |

### 11.1.3 Selecting the output data standard

The output data standard (CMOS or LVDS DDR) can be selected via the SPI interface (see Table 23) or using pin ODS in Pin control mode. LVDS DDR is selected when ODS is HIGH, otherwise CMOS is selected.

### 11.1.4 Selecting the output data format

The output data format can be selected via the SPI interface (offset binary, two's complement or gray code; see Table 23) or using pin DFS in Pin control mode (offset binary or two's complement). Offset binary is selected when DFS is LOW. When DFS is HIGH, two's complement is selected.

## 11.2 Analog inputs

### 11.2.1 Input stage

The analog input of the ADC1610S supports differential or single-ended input drive. Optimal performance is achieved using differential inputs with the common-mode input voltage ($V_{I(cm)}$) on pins INP and INM set to $0.5V_{DDA}$.

The full-scale analog input voltage range is configurable between 1 V (p-p) and 2 V (p-p) via a programmable internal reference (see Section 11.3 and Table 22 further details).

The equivalent circuit of the sample and hold input stage, including Electrostatic Discharge (ESD) protection and circuit and package parasitics, is shown in Figure 8.

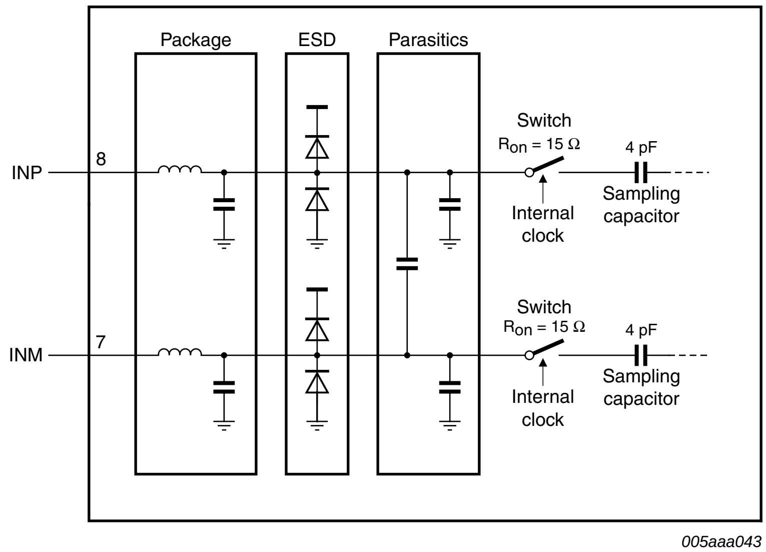



**Fig 8. Input sampling circuit**

The sample phase occurs when the internal clock (derived from the clock signal on pin CLKP/CLKM) is HIGH. The voltage is then held on the sampling capacitors. When the clock signal goes LOW, the stage enters the hold phase and the voltage information is transmitted to the ADC core.

### 11.2.2 Anti-kickback circuitry

Anti-kickback circuitry (R-C filter in Figure 9) is needed to counteract the effects of a charge injection generated by the sampling capacitance.

The RC filter is also used to filter noise from the signal before it reaches the sampling stage. The value of the capacitor should be chosen to maximize noise attenuation without degrading the settling time excessively.

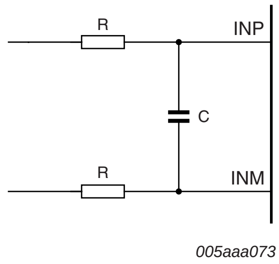



**Fig 9. Anti-kickback circuit**

The component values are determined by the input frequency and should be selected so as not to affect the input bandwidth.

**Table 11. RC coupling versus input frequency, typical values**

| Input frequency | Resistance | Capacitance |
|---|---|---|
| 3 MHz | 25 Ω | 12 pF |
| 70 MHz | 12 Ω | 8 pF |
| 170 MHz | 12 Ω | 8 pF |

### 11.2.3 Transformer

The configuration of the transformer circuit is determined by the input frequency. The configuration shown in Figure 10 would be suitable for a baseband application.

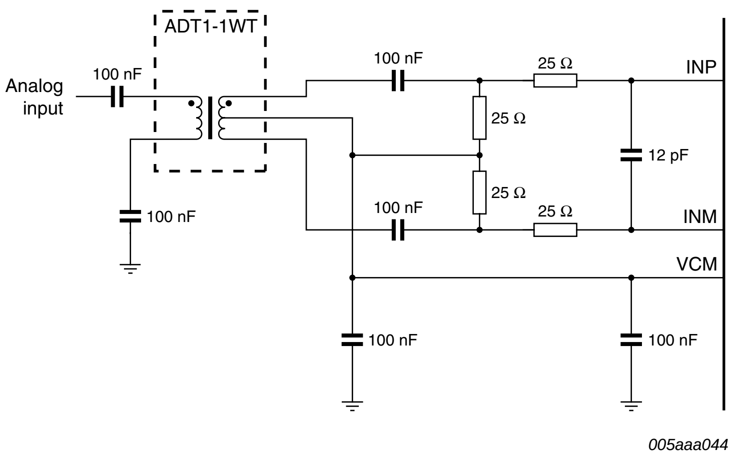



**Fig 10. Single transformer configuration suitable for baseband applications**

The configuration shown in Figure 11 is recommended for high frequency applications. In both cases, the choice of transformer will be a compromise between cost and performance.

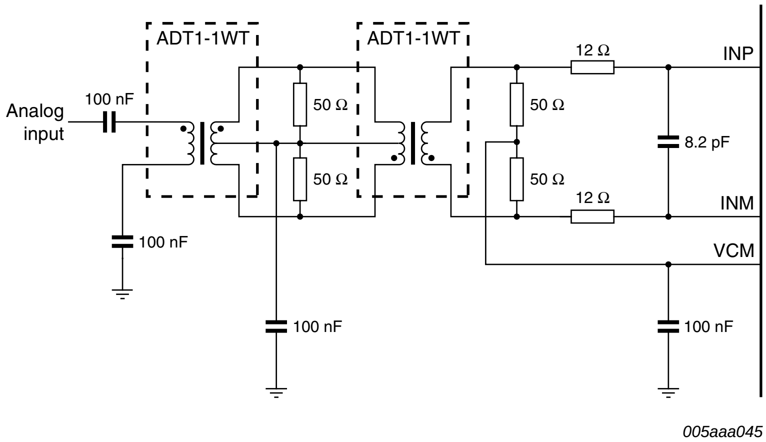



**Fig 11. Dual transformer configuration suitable for high intermediate frequency application**

## 11.3 System reference and power management

### 11.3.1 Internal/external references

The ADC1610S has a stable and accurate built-in internal reference voltage to adjust the ADC full-scale. This reference voltage can be set internally via SPI or with pins VREF and SENSE (programmable in 1 dB steps between 0 dB and –6 dB via control bits INTREF[2:0] when bit INTREF_EN = 1; see Table 22). See Figure 13, Figure 14, Figure 15, Figure 16. The equivalent reference circuit is shown in Figure 12. External reference is also possible by providing a voltage on pin VREF as described in Figure 15.

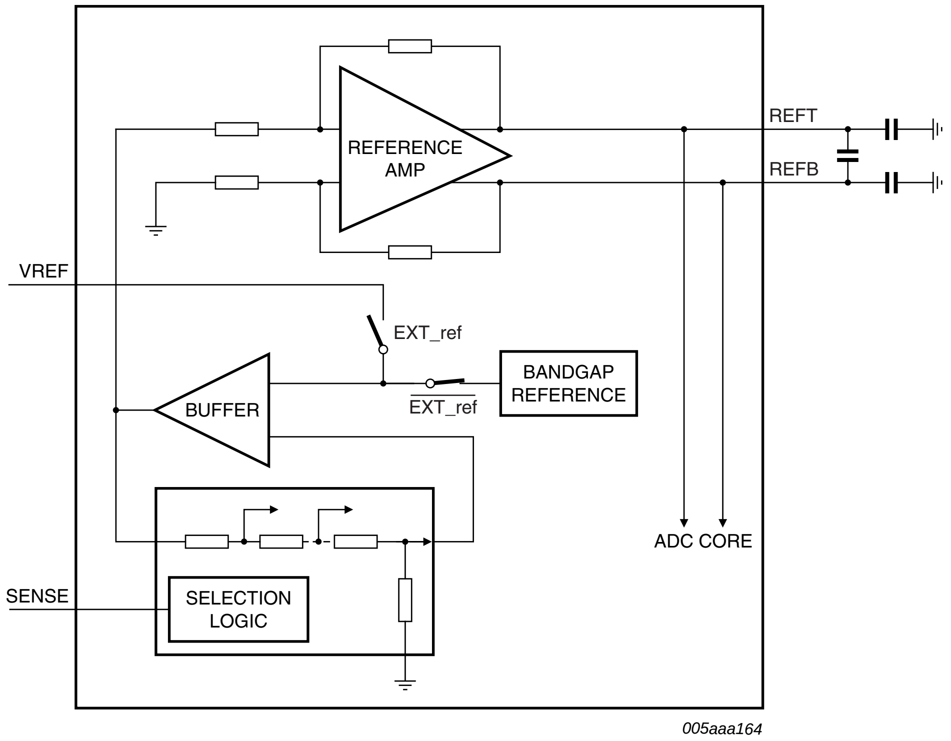



**Fig 12. Reference equivalent schematic**

If bit INTREF_EN is set to 0, the reference voltage will be determined either internally or externally as detailed in Table 12.

**Table 12. Reference selection**

| Selection | SPI bit INTREF_EN | SENSE pin | VREF pin | full-scale (p-p) |
|---|---|---|---|---|
| internal (Figure 13) | 0 | AGND | 330 pF capacitor to AGND | 2 V |
| internal (Figure 14) | 0 | pin VREF connected to pin SENSE and via a 330 pF capacitor to AGND | | 1 V |
| external (Figure 15) | 0 | $V_{DDA}$ | external voltage between 0.5 V and 1 V[1] | 1 V to 2 V |
| internal via SPI (Figure 16) | 1 | pin VREF connected to pin SENSE and via 330 pF capacitor to AGND | | 1 V to 2 V |

[1] The voltage on pin VREF is doubled internally to generate the internal reference voltage.

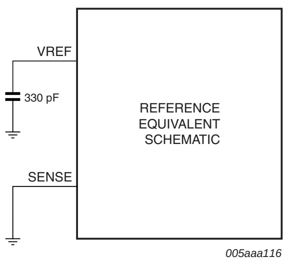



**Fig 13. Internal reference, 2 V (p-p) full scale**

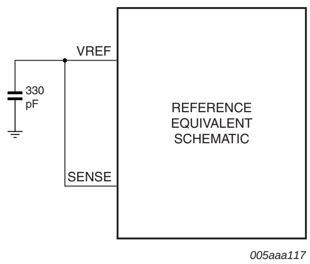



**Fig 14. Internal reference, 1 V (p-p) full scale**

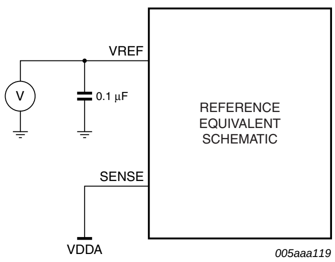



**Fig 15. External reference, 1 V (p-p) to 2 V (p-p) full-scale**

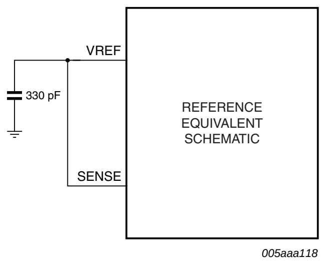



**Fig 16. Internal reference via SPI, 1 V (p-p) to 2 V (p-p) full-scale**

Figure 13 to Figure 16 illustrate how to connect the SENSE and VREF pins to select the required reference voltage source.

### 11.3.2 Reference gain control

The reference gain is programmable between 0 dB to –6 dB in 1 dB steps via the SPI (see Table 22). The corresponding full-scale input voltage range varies between 2 V (p-p) and 1 V (p-p), as shown in Table 13:

**Table 13. Reference SPI gain control**

| INTREF[2:0] | Gain (dB) | Full-scale (V (p-p)) |
|---|---|---|
| 000 | 0 dB | 2 V |
| 001 | –1 dB | 1.78 V |
| 010 | –2 dB | 1.59 V |
| 011 | –3 dB | 1.42 V |
| 100 | –4 dB | 1.26 V |
| 101 | –5 dB | 1.12 V |
| 110 | –6 dB | 1 V |
| 111 | reserved | x |

### 11.3.3 Common-mode output voltage ($V_{O(cm)}$)

A 0.1 μF filter capacitor should be connected between pin VCM and ground to ensure a low-noise common-mode output voltage. When AC-coupled, pin VCM can be used to set the common-mode reference for the analog inputs, for instance via a transformer middle point.

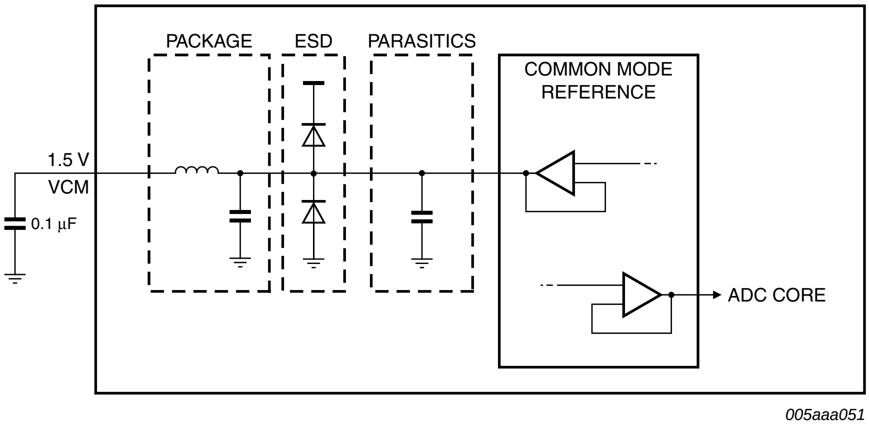



**Fig 17. Equivalent schematic of the common-mode reference circuit**

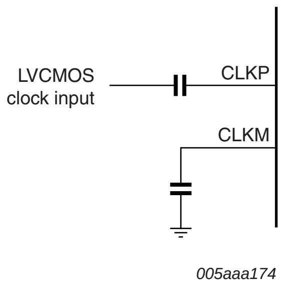
### 11.3.4 Biasing

The common-mode input voltage ($V_{I(cm)}$) on pins INP and INM should be set externally to $0.5V_{DDA}$ for optimal performance and should always be between 0.9 V and 2 V.

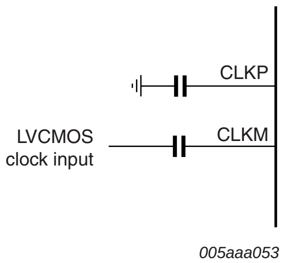
## 11.4 Clock input

### 11.4.1 Drive modes

The ADC1610S can be driven differentially (SINE, LVPECL or LVDS) with little or no degradation on dynamic performances. It can also be driven by a single-ended LVCMOS signal connected to pin CLKP (CLKM should be connected to ground via a capacitor) or CLKM (CLKP should be connected to ground via a capacitor).

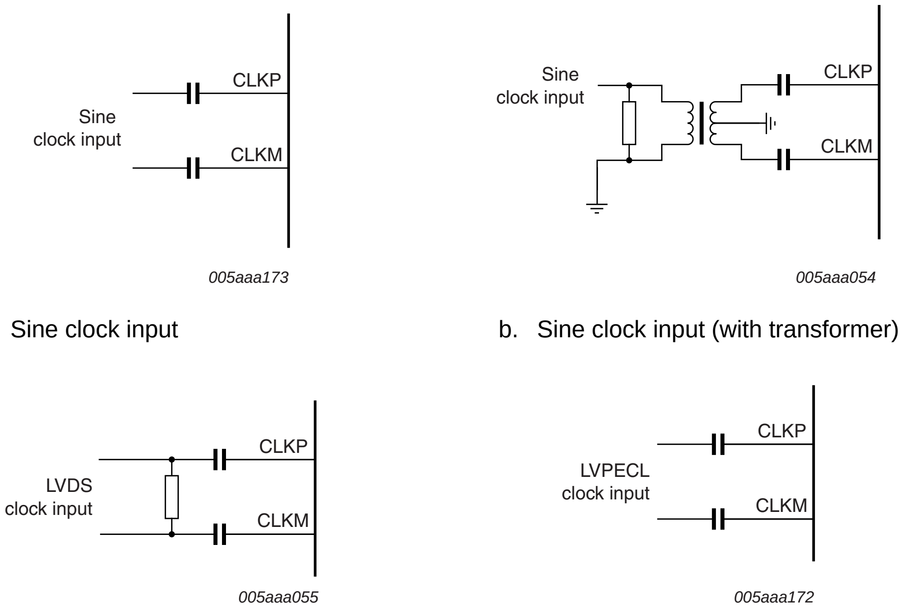



a. Rising edge LVCMOS




b. Falling edge LVCMOS

**Fig 18. LVCMOS single-ended clock input**




a. Sine clock input    b. Sine clock input (with transformer)

c. LVDS clock input    d. LVPECL clock input

**Fig 19. Differential clock input**

### 11.4.2 Equivalent input circuit

The equivalent circuit of the input clock buffer is shown in Figure 21. The common-mode voltage of the differential input stage is set via internal 5 kΩ resistors.

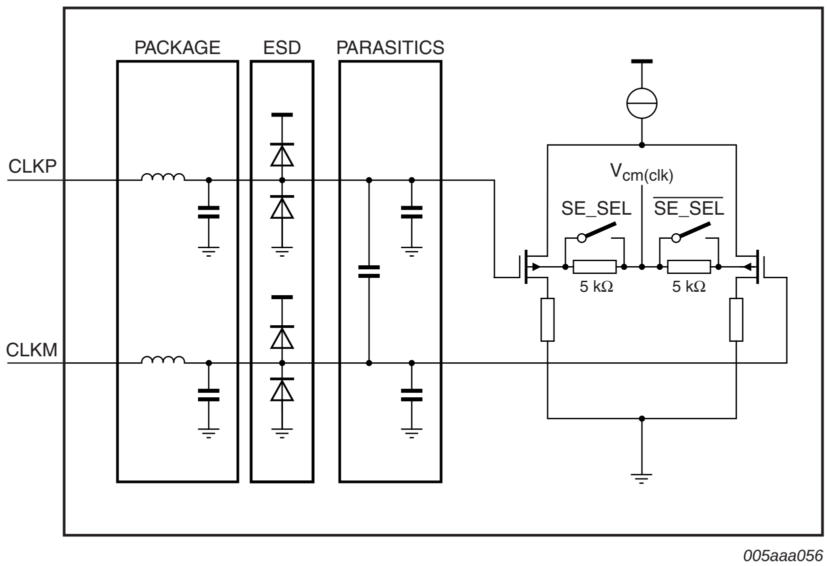



**Fig 20. Equivalent input circuit**

Single-ended or differential clock inputs can be selected via the SPI interface (see Table 21). If single-ended is enabled, the input pin (CLKM or CLKP) is selected via control bit SE_SEL.

If single-ended is implemented without setting SE_SEL to the appropriate value, the unused pin should be connected to ground via a capacitor.

### 11.4.3 Duty cycle stabilizer

The duty cycle stabilizer can improve the overall performances of the ADC by compensating the duty cycle of the input clock signal. When the duty cycle stabilizer is active (bit DCS_EN = 1; see Table 21), the circuit can handle signals with duty cycles of between 30 % and 70 % (typical). When the duty cycle stabilizer is disabled (DCS_EN = 0), the input clock signal should have a duty cycle of between 45 % and 55 %.

### 11.4.4 Clock input divider

The ADC1610S contains an input clock divider that divides the incoming clock by a factor of 2 (when bit CLKDIV = 1; see Table 21). This feature allows the user to deliver a higher clock frequency with better jitter performance, leading to a better SNR result once acquisition has been performed.

## 11.5 Digital outputs

### 11.5.1 Digital output buffers: CMOS mode

The digital output buffers can be configured as CMOS by setting bit LVDS/CMOS to 0 (see Table 23).

Each digital output has a dedicated output buffer. The equivalent circuit of the CMOS digital output buffer is shown in Figure 22. The buffer is powered by a separate power supply, pins OGND and $V_{DDO}$, to ensure 1.8 V to 3.3 V compatibility and is isolated from the ADC core. Each buffer can be loaded by a maximum of 10 pF.

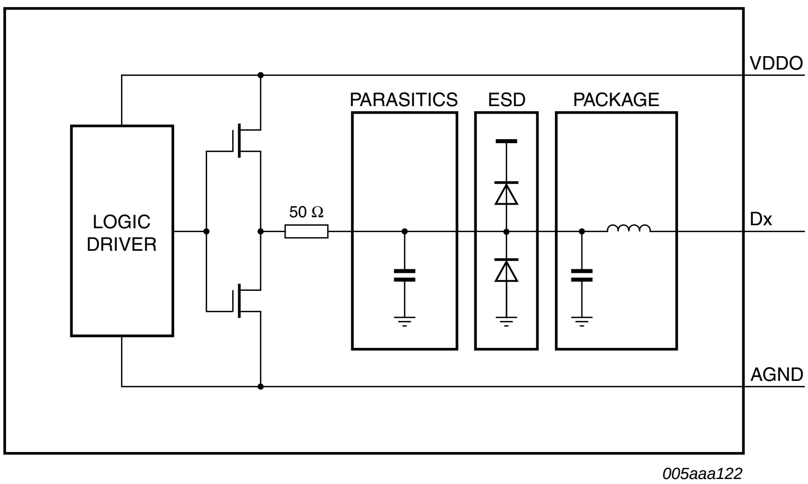



**Fig 21. CMOS digital output buffer**

The output resistance is 50 Ω and is the combination of the an internal resistor and the equivalent output resistance of the buffer. There is no need for an external damping resistor. The drive strength of both data and DAV buffers can be programmed via the SPI in order to adjust the rise and fall times of the output digital signals (see Table 30):

### 11.5.2 Digital output buffers: LVDS DDR mode

The digital output buffers can be configured as LVDS DDR by setting bit LVDS/CMOS to 1 (see Table 23).

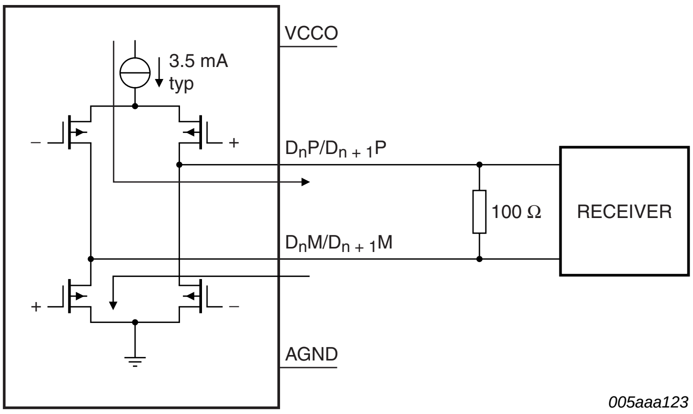



**Fig 22. LVDS DDR digital output buffer - externally terminated**

Each output should be terminated externally with a 100 Ω resistor (typical) at the receiver side (Figure 23) or internally via SPI control bits LVDS_INT_TER[2:0] (see Figure 24 and Table 32).

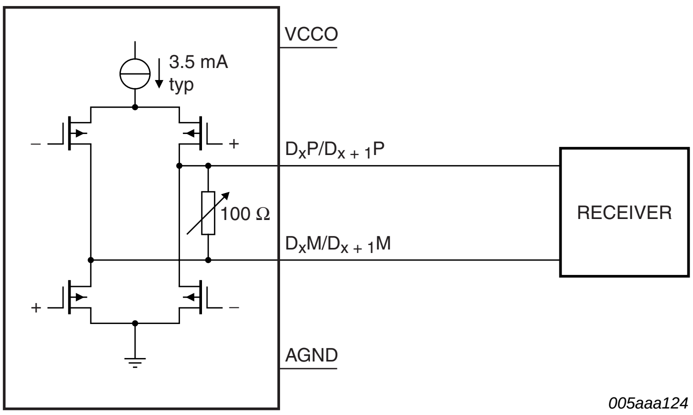



**Fig 23. LVDS DDR digital output buffer - internally terminated**

The default LVDS DDR output buffer current is set to 3.5 mA. It can be programmed via the SPI (bits DAVI[1:0] and DATAI[1:0]; see Table 31) in order to adjust the output logic voltage levels.

Table 14. LVDS DDR output register 2

| LVDS_INT_TER[1:0] | Resistor value (Ω) |
|---|---|
| 000 | no internal termination |
| 001 | 300 |
| 010 | 180 |
| 011 | 110 |
| 100 | 150 |
| 101 | 100 |
| 110 | 81 |
| 111 | 60 |

### 11.5.3 Data valid (DAV) output clock

A data valid output clock signal (DAV) can be used to capture the data delivered by the ADC1610S. Detailed timing diagrams for CMOS and LVDS DDR modes are shown in Figure 4 and Figure 5 respectively.

### 11.5.4 Out-of-Range (OTR)

An out-of-range signal is provided on pin OTR. The latency of OTR is fourteen clock cycles. The OTR response can be speeded up by enabling Fast OTR (bit FASTOTR = 1; see Table 29). In this mode, the latency of OTR is reduced to only four clock cycles. The Fast OTR detection threshold (below full-scale) can be programmed via bits FASTOTR_DET[2:0].

Table 15. Fast OTR register

| FASTOTR_DET[2:0] | Detection level (dB) |
|---|---|
| 000 | −20.56 |
| 001 | −16.12 |
| 010 | −11.02 |
| 011 | −7.82 |
| 100 | −5.49 |
| 101 | −3.66 |
| 110 | −2.14 |
| 111 | −0.86 |

### 11.5.5 Digital offset

By default, the ADC1610S delivers output code that corresponds to the analog input. However it is possible to add a digital offset to the output code via the SPI (bits DIG_OFFSET[5:0]; see Table 25).

### 11.5.6 Test patterns

For test purposes, the ADC1610S can be configured to transmit one of a number of predefined test patterns (via bits TESTPAT_SEL[2:0]; see Table 26). A custom test pattern can be defined by the user (TESTPAT_USER; see Table 27 and Table 28) and is selected when TESTPAT_SEL[2:0] = 101. The selected test pattern will be transmitted regardless of the analog input.

### 11.5.7 Output codes versus input voltage

Table 16. Output codes

| $V_{INP} - V_{INM}$ | Offset binary | Two's complement | OTR pin |
|---|---|---|---|
| < −1 | 0000 0000 0000 0000 | 1000 0000 0000 0000 | 1 |
| −1 | 0000 0000 0000 0000 | 1000 0000 0000 0000 | 0 |
| −0.99996948 | 0000 0000 0000 0001 | 1000 0000 0000 0001 | 0 |
| −0.99993896 | 0000 0000 0000 0010 | 1000 0000 0000 0010 | 0 |
| −0.99990845 | 0000 0000 0000 0011 | 1000 0000 0000 0011 | 0 |
| −0.99987793 | 0000 0000 0000 0100 | 1000 0000 0000 0100 | 0 |
| .... | .... | .... | 0 |
| −0.00006104 | 0111 1111 1111 1110 | 1111 1111 1111 1110 | 0 |
| −0.00003052 | 0111 1111 1111 1111 | 1111 1111 1111 1111 | 0 |
| 0 | **1000 0000 0000 0000** | **0000 0000 0000 0000** | 0 |
| +0.00003052 | 1000 0000 0000 0001 | 0000 0000 0000 0001 | 0 |
| +0.00006104 | 1000 0000 0000 0010 | 0000 0000 0000 0010 | 0 |
| .... | .... | .... | 0 |
| +0.99987793 | 1111 1111 1111 1011 | 0111 1111 1111 1011 | 0 |
| +0.99990845 | 1111 1111 1111 1100 | 0111 1111 1111 1100 | 0 |
| +0.99993896 | 1111 1111 1111 1101 | 0111 1111 1111 1101 | 0 |
| +0.99996948 | 1111 1111 1111 1110 | 0111 1111 1111 1110 | 0 |
| +1 | 1111 1111 1111 1111 | 0111 1111 1111 1111 | 0 |
| > +1 | 1111 1111 1111 1111 | 0111 1111 1111 1111 | 1 |

## 11.6 Serial peripheral interface

### 11.6.1 Register description

The ADC1610S serial interface is a synchronous serial communications port that allows for easy interfacing with many commonly-used microprocessors. It provides access to the registers that control the operation of the chip.

This interface is configured as a 3-wire type (SDIO as bidirectional pin)

Pin SCLK is the serial clock input and $\overline{CS}$ is the chip select pin.

Each read/write operation is initiated by a LOW level on $\overline{CS}$. A minimum of three bytes will be transmitted (two instruction bytes and at least one data byte). The number of data bytes is determined by the value of bits W1 and W2 (see Table 18).

Table 17. Instruction bytes for the SPI

| | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Description | R/$\overline{W}$[1] | W1[2] | W0[2] | A12 | A11 | A10 | A9 | A8 |
| | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

[1] Bit R/$\overline{W}$ indicates whether it is a read (1) or a write (0) operation.

[2] Bits W1 and W0 indicate the number of bytes to be transferred after the instruction byte (see Table 18).

**Table 18. Number of data bytes to be transferred after the instruction bytes**

| W1 | W0 | Number of bytes transmitted |
|---|---|---|
| 0 | 0 | 1 byte |
| 0 | 1 | 2 bytes |
| 1 | 0 | 3 bytes |
| 1 | 1 | 4 bytes or more |

Bits A12 to A0 indicate the address of the register being accessed. In the case of a multiple byte transfer, this address is the first register to be accessed. An address counter is increased to access subsequent addresses.

The steps involved in a data transfer are as follows:

1. A falling edge on $\overline{CS}$ in combination with a rising edge on SCLK determine the start of communications.
2. The first phase is the transfer of the 2-byte instruction.
3. The second phase is the transfer of the data which can vary in length but will always be a multiple of 8 bits. The MSB is always sent first (for instruction and data bytes).
4. A rising edge on $\overline{CS}$ indicates the end on data transmission.

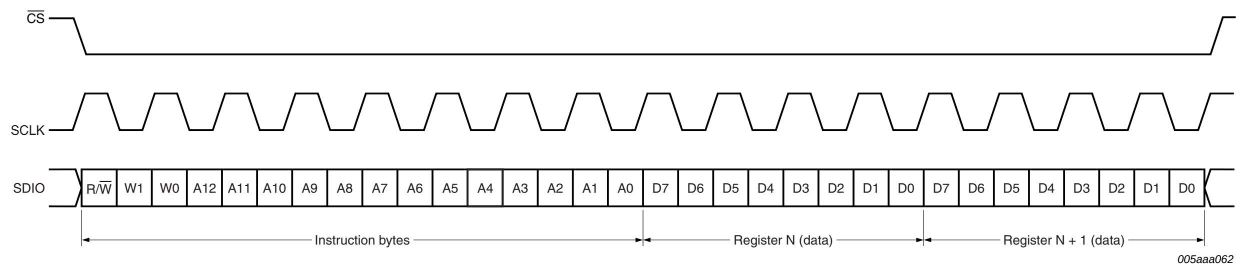



**Fig 24. SPI mode timing**

## 11.6.2 Default modes at start-up

During circuit initialization, it does not matter which output data standard has been selected. At power-up, the device enters Pin control mode.

A falling edge on $\overline{CS}$ will trigger a transition to SPI control mode. When the ADC1610S enters SPI control mode, the output data standard (CMOS/LVDS DDR) is determined by the level on pin SDIO (see Figure 25). Once in SPI control mode, the output data standard can be changed via bit LVDS/CMOS in Table 23.

When the ADC1610S enters SPI control mode, the output data format (two's complement or offset binary) is determined by the level on pin SCLK (gray code can only be selected via the SPI). Once in SPI control mode, the output data format can be changed via bit DATA_FORMAT[1:0] in Table 23.

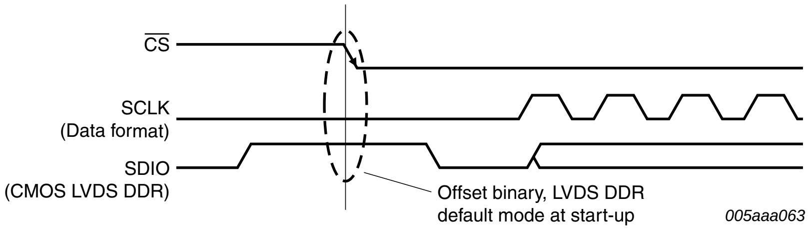



**Fig 25. Default mode at start-up: SCLK LOW = offset binary; SDIO HIGH = LVDS DDR**

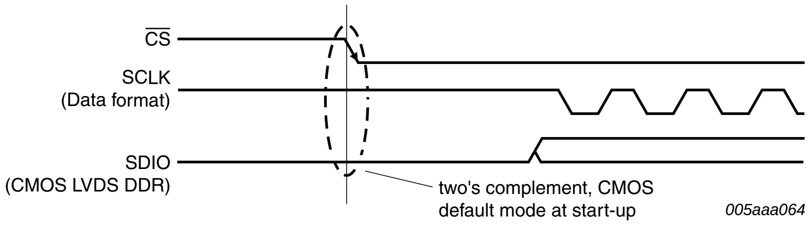



**Fig 26. Default mode at start-up: SCLK HIGH = two's complement; SDIO LOW = CMOS**

### 11.6.3 Register allocation map

**Table 19. Register allocation map**

| AddrHex | Register name | R/W | Bit definition | | | | | | | | Default |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Bin |
| 0005 | Reset and operating mode | R/W | SW_RST | RESERVED[2:0] | | | - | - | OP_MODE[1:0] | | 0000 0000 |
| 0006 | Clock | R/W | - | - | - | SE_SEL | DIFF_SE | - | CLKDIV | DCS_EN | 0000 0001 |
| 0008 | Internal reference | R/W | - | - | - | - | INTREF_EN | INTREF[2:0] | | | 0000 0000 |
| 0011 | Output data standard | R/W | - | - | - | LVDS_CMOS | OUTBUF | OUTBUS_SWAP | DATA_FORMAT[1:0] | | 0000 0000 |
| 0012 | Output clock | R/W | - | - | - | - | DAVINV | DAVPHASE[2:0] | | | 0000 1110 |
| 0013 | Offset | R/W | - | - | DIG_OFFSET[5:0] | | | | | | 0000 0000 |
| 0014 | Test pattern 1 | R/W | - | - | - | - | - | TESTPAT_SEL[2:0] | | | 0000 0000 |
| 0015 | Test pattern 2 | R/W | TESTPAT_USER[15:8] | | | | | | | | 0000 0000 |
| 0016 | Test pattern 3 | R/W | TESTPAT_USER[7:0] | | | | | | | | 0000 0000 |
| 0017 | Fast OTR | R/W | - | - | - | - | FASTOTR | FASTOTR_DET[2:0] | | | 0000 0000 |
| 0020 | CMOS output | R/W | - | - | - | - | DAV_DRV[1:0] | | DATA_DRV[1:0] | | 0000 1110 |
| 0021 | LVDS DDR O/P 1 | R/W | - | - | DAVI_x2_EN | DAVI[1:0] | | DATAI_x2_EN | DATAI[1:0] | | 0000 0000 |
| 0022 | LVDS DDR O/P 2 | R/W | - | - | - | - | BIT_BYTE_WISE | LVDS_INT_TER[2:0] | | | 0000 0000 |

**Table 20. Reset and operating mode control register (address 0005h) bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 | SW_RST | R/W | | reset digital section |
| | | | **0** | no reset |
| | | | 1 | performs a reset on SPI registers |
| 6 to 4 | RESERVED[2:0] | | 000 | reserved |
| 3 to 2 | - | | 00 | not used |
| 1 to 0 | OP_MODE[1:0] | R/W | | operating mode |
| | | | **00** | normal (power-up) |
| | | | 01 | power-down |
| | | | 10 | sleep |
| | | | 11 | normal (power-up) |

**Table 21. Clock control register (address 0006h) bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 to 5 | - | | 000 | not used |
| 4 | SE_SEL | R/W | | single-ended clock input pin select |
| | | | **0** | CLKM |
| | | | 1 | CLKP |
| 3 | DIF_SE | R/W | | differential/single ended clock input select |
| | | | **0** | fully differential |
| | | | 1 | single-ended |
| 2 | - | | 0 | not used |
| 1 | CLKDIV | R/W | | clock input divide by 2 |
| | | | **0** | disabled |
| | | | 1 | enabled |
| 0 | DCS_EN | R/W | | duty cycle stabilizer |
| | | | 0 | disabled |
| | | | **1** | enabled |

**Table 22. Internal reference control register (address 0008h) bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 to 4 | - | | 0 | not used |
| 3 | INTREF_EN | R/W | | programmable internal reference enable |
| | | | **0** | disable |
| | | | 1 | active |
| 2 to 0 | INTREF[2:0] | R/W | | programmable internal reference |
| | | | **000** | 0 dB (FS = 2 V) |
| | | | 001 | −1 dB (FS = 1.78 V) |
| | | | 010 | −2 dB (FS = 1.59 V) |
| | | | 011 | −3 dB (FS = 1.42 V) |
| | | | 100 | −4 dB (FS = 1.26 V) |
| | | | 101 | −5 dB (FS = 1.12 V) |
| | | | 110 | −6 dB (FS = 1 V) |
| | | | 111 | reserved |

**Table 23. Output data standard control register (address 0011h) bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 to 5 | - | | 000 | not used |
| 4 | LVDS_CMOS | R/W | | output data standard: LVDS DDR or CMOS |
| | | | **0** | CMOS |
| | | | 1 | LVDS DDR |
| 3 | OUTBUF | R/W | | output buffers enable |
| | | | **0** | output enabled |
| | | | 1 | output disabled (high Z) |
| 2 | OUTBUS_SWAP | | 0 | outbus swapping |
| | | | **0** | no swapping |
| | | | 1 | output bus is swapping (MSB becomes LSB and vice versa) |
| 1 to 0 | DATA_FORMAT[1:0] | R/W | | output data format |
| | | | **00** | offset binary |
| | | | 01 | two's complement |
| | | | 10 | gray code |
| | | | 11 | offset binary |

**Table 24. Output clock register (address 0012h) bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 to 4 | - | | 0000 | not used |
| 3 | DAVINV | R/W | | output clock data valid (DAV) polarity |
| | | | 0 | normal |
| | | | **1** | inverted |
| 2 to 0 | DAVPHASE[2:0] | R/W | | DAV phase select |
| | | | 000 | output clock shifted (ahead) by 3 ns |
| | | | 001 | output clock shifted (ahead) by 2.5 ns |
| | | | 010 | output clock shifted (ahead) by 2 ns |
| | | | 011 | output clock shifted (ahead) by 1.5 ns |
| | | | 100 | output clock shifted (ahead) by 1 ns |
| | | | 101 | output clock shifted (ahead) by 0.5 ns |
| | | | **110** | default value as defined in timing section |
| | | | 111 | output clock shifted (delayed) by 0.5 ns |

**Table 25. Offset register (address 0013h) bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 to 6 | - | | 00 | not used |
| 5 to 0 | DIG_OFFSET[5:0] | R/W | | digital offset adjustment |
| | | | 011111 | +31 LSB |
| | | | ... | ... |
| | | | **000000** | 0 |
| | | | ... | ... |
| | | | 100000 | −32 LSB |

**Table 26. Test pattern register 1 (address 0014h) bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 to 3 | - | | 00000 | not used |
| 2 to 0 | TESTPAT_SEL[2:0] | R/W | | digital test pattern select |
| | | | **000** | off |
| | | | 001 | mid scale |
| | | | 010 | −FS |
| | | | 011 | +FS |
| | | | 100 | toggle ‘1111..1111’/’0000..0000’ |
| | | | 101 | custom test pattern |
| | | | 110 | ‘1010..1010.’ |
| | | | 111 | ‘010..1010’ |

**Table 27. Test pattern register 2 (address 0015h) bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 to 0 | TESTPAT_USER[15:8] | R/W | **00000000** | custom digital test pattern (bits 13 to 6) |

**Table 28. Test pattern register 3 (address 0016h) bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 to 0 | TESTPAT_USER[7:0] | R/W | **00000000** | custom digital test pattern (bits 7 to 0) |

**Table 29. Fast OTR register (address 0017h) bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 to 4 | - | | 0000 | not used |
| 3 | FASTOTR | R/W | | fast Out-of-Range (OTR) detection |
| | | | **0** | disabled |
| | | | 1 | enabled |
| 2 to 0 | FASTOTR_DET[2:0] | R/W | | set fast OTR detect level |
| | | | **000** | −20.56 dB |
| | | | 001 | −16.12 dB |
| | | | 010 | −11.02 dB |
| | | | 011 | −7.82 dB |
| | | | 100 | −5.49 dB |
| | | | 101 | −3.66 dB |
| | | | 110 | −2.14 dB |
| | | | 111 | −0.86 dB |

**Table 30. CMOS output register (address 0020h) bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 to 4 | - | | 0000 | not used |
| 3 to 2 | DAV_DRV[1:0] | R/W | | drive strength for DAV CMOS output buffer |
| | | | 00 | low |
| | | | 01 | medium |
| | | | 10 | high |
| | | | **11** | very high |
| 1 to 0 | DATA_DRV[1:0] | R/W | | drive strength for DATA CMOS output buffer |
| | | | 00 | low |
| | | | 01 | medium |
| | | | **10** | high |
| | | | 11 | very high |

**Table 31. LVDS DDR output register 1 (address 0021h) bit description**

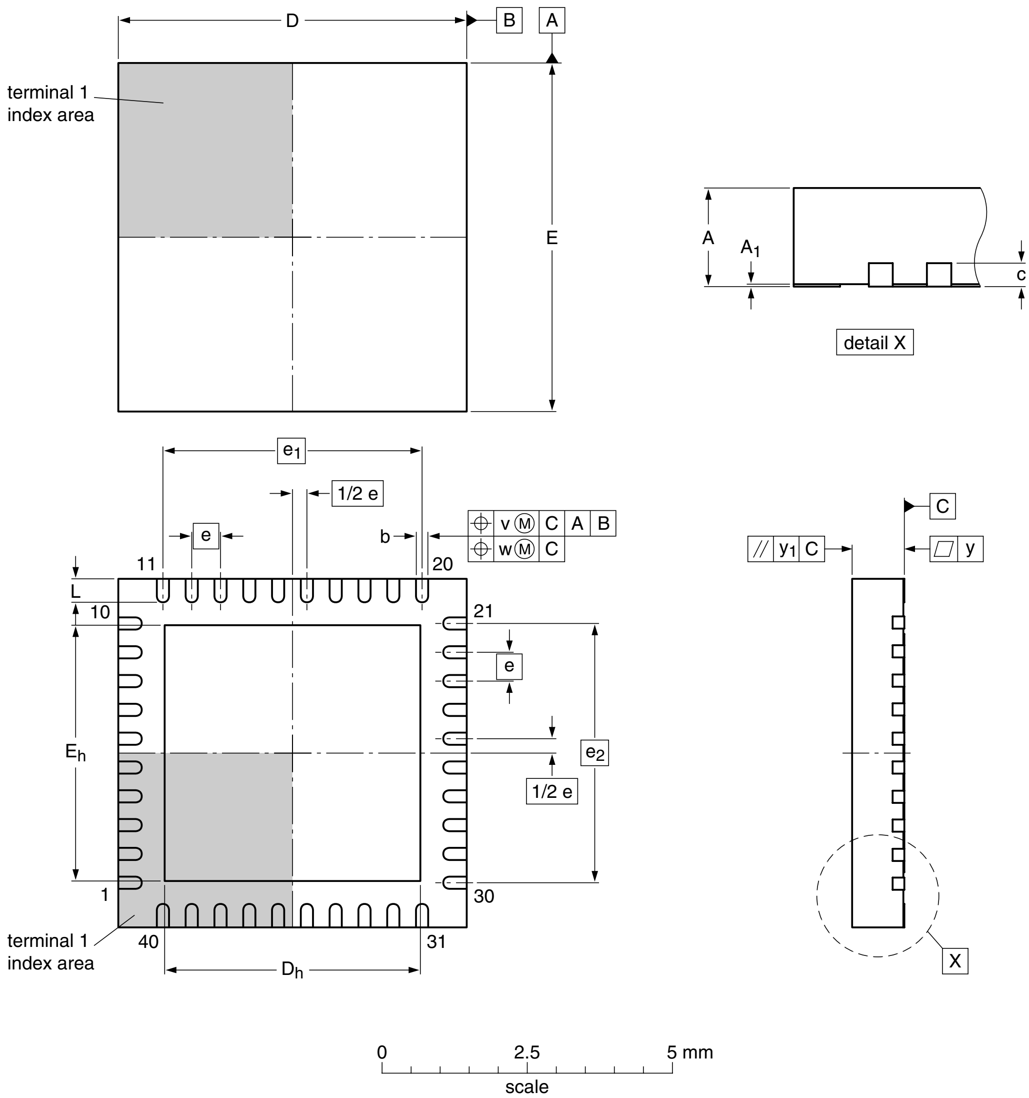
| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 to 6 | - | | 00 | not used |
| 5 | DAVI_x2_EN | R/W | | double LVDS current for DAV LVDS buffer |
| | | | **0** | disabled |
| | | | 1 | enabled |
| 4 to 3 | DAVI[1:0] | R/W | | LVDS current for DAV LVDS buffer |
| | | | **00** | 3.5 mA |
| | | | 01 | 4.5 mA |
| | | | 10 | 1.25 mA |
| | | | 11 | 2.5 mA |
| 2 | DATAI_x2_EN | R/W | | double LVDS current for DATA LVDS buffer |
| | | | **0** | disabled |
| | | | 1 | enabled |
| 1 to 0 | DATAI[1:0] | R/W | | LVDS current for DATA LVDS buffer |
| | | | **00** | 3.5 mA |
| | | | 01 | 4.5 mA |
| | | | 10 | 1.25 mA |
| | | | 11 | 2.5 mA |

**Table 32. LVDS DDR output register 2 (address 0022h) bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 to 4 | - | | 0000 | not used |
| 3 | BIT_BYTE_WISE | R/W | | DDR mode for LVDS output |
| | | | **0** | bit wise (even data bits output on DAV rising edge/odd data bits output on DAV falling edge) |
| | | | 1 | byte wise (MSB data bits output on DAV rising edge/LSB data bits output on DAV falling edge) |
| 2 to 0 | LVDS_INT_TER[2:0] | R/W | | internal termination for LVDS buffer (DAV and DATA) |
| | | | **000** | no internal termination |
| | | | 001 | 300 Ω |
| | | | 010 | 180 Ω |
| | | | 011 | 110 Ω |
| | | | 100 | 150 Ω |
| | | | 101 | 100 Ω |
| | | | 110 | 81 Ω |
| | | | 111 | 60 Ω |

## 12. Package outline

**HVQFN40: plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 x 6 x 0.85 mm** **SOT618-6**




Dimensions

| Unit | | $A^{(1)}$ | $A_1$ | b | c | $D^{(1)}$ | $D_h$ | $E^{(1)}$ | $E_h$ | e | $e_1$ | $e_2$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | max | 1.00 | 0.05 | 0.30 | | 6.1 | 4.55 | 6.1 | 4.55 | | | | 0.5 | | | | |
| mm | nom | 0.85 | 0.02 | 0.21 | 0.2 | 6.0 | 4.40 | 6.0 | 4.40 | 0.5 | 4.5 | 4.5 | 0.4 | 0.1 | 0.05 | 0.05 | 0.1 |
| | min | 0.80 | 0.00 | 0.18 | | 5.9 | 4.25 | 5.9 | 4.25 | | | | 0.3 | | | | |

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

*sot618-6_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT618-6 | | MO-220 | - - - | | | ~~09-02-23~~ 09-03-04 |

**Fig 27. Package outline SOT618-6 (HVQFN40)**

## 13. Revision history

**Table 33. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| ADC1610S_SER_2 | 20100412 | Objective data sheet | - | ADC1610S125_1 |
| Modifications: | • Figure 12 "Reference equivalent schematic" has been updated | | | |
| ADC1610S125_1 | 20090528 | Objective data sheet | - | - |

# 14. Legal information

## 14.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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## 16. Contents





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**Document identifier: ADC1610S_SER_2**