PROCESS

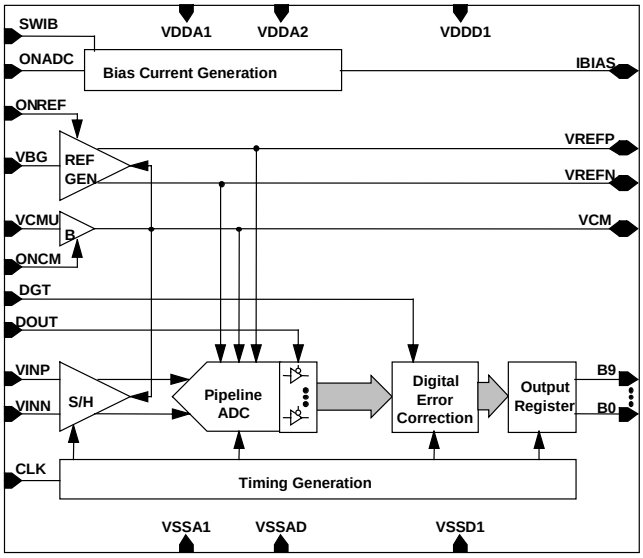
C35B3 (0.35um)

DESCRIPTION

The AD1020 is a high-speed pipeline ADC core cell achieving sampling rates up to 20 MS/s. A S/H circuit is built-in to provide low jitter noise and an optional single-ended to fully differential conversion. The reference voltages are internally generated from a bandgap reference that must be supplied to the cell or must be supplied externally to the cell. A power down capability is included for very low power dissipation in stand-by mode.

FEATURES

- Small Area: 1.57mm^2
- Size x= 2189.7µm y= 717.4µm
- Supply Voltage 2.7-3.6 V
- Junction Temp. Range –40 to +85°C
- Resolution 10-Bit
- Maximum Sampling Rate 20 MS/s
- Sample and Hold Input Stage
- 2 Vpp or 4 Vpp Input Signal Range
- Single Ended or Fully Differential Input
- Power Consumption of 200 mW
- Power Down Mode



TECHNICAL DATA

(Tjunction=-40 to 85° C, VDDA=VDD=+2.7V to +3.6V, fclk=20MHz, VREFP and VREFN as specified, unless otherwise specified)

DC ACCURACY

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Resolution (No missing Code)		10	10	10	Bit
DNL	Differential Linearity Error		-0.9	±0.4	+1	LSB
INL	Integral Linearity Error		-1	±0.6	+1	LSB
OFF	Offset Error		-10	0	10	LSB
GAINERR	Gain Error for Internal Ref. [1]	Op. Mode 1	-5	0	+5	LSB
GAINERR	Gain Error for External Ref. [2]	Op. Mode 3,6	+23	+28	+33	LSB

REFERENCE CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VBG	ext. Bandgap Reference Voltage			1.25	2.5 [3]	V
VCMU	Unbuffered C. Mode Voltage		1.35	VDDA/2	1.8	V
VCM	Buffered C. Mode Voltage			VCMU		V
VREFP	Pos. Reference Voltage			VCM+0.4VBG		V
VREFN	Neg. Reference Voltage			VCM-0.4VBG		V
VREF	Difference between VREFP and VREFN		1	1	2 [3]	V
R_{bg}	ext. Bandgap Ref. Impedance			10		kΩ
I_{bg}	ext. Bandgap Ref. Input Current			5.6 [4] | 103 [5]		µA
C_{cmu}	Unbuff. Comm. Mode Imped.			2.2		pF
C_{cm}	Comm. Mode Impedance (Op. Modes 2, 3, 5 and 6)			22.5		pF
R_{refp}	Pos. Reference Impedance			18		kΩ
C_{refp}	(Op. Modes 3 and 6)			7.1		pF
R_{refn}	Neg. Reference Impedance			18		kΩ
C_{refn}	(Op. Modes 3 and 6)			7.1		pF

ANALOG INPUT

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Vind	Diff. Input Voltage Range, related to VCMU		-VREF		VREF	V
R_{in}	Input Impedance		100			MΩ
C_{in}				1		pF
F_{inmax}	Max. Input Signal Frequency				10	MHz

[1] Offset and Gain Error correspond to measured reference voltages. This measured reference voltage VREF has a value of 960mV instead of 1000mV and 1950mV instead of 2000mV for VREF=1V and VREF=2V, respectively. This is because of an additional trop of the bandgap voltage caused by it's pad-resistor.

[2] Offset and Gain Error correspond to measured reference voltages outside the chip. The real voltage reference VREF at the macro cell has the value 972mV instead of 1000mV and 1945mV instead of 2000mV for VREF=1V and VREF=2V, respectively. This is because of the voltage trop caused by the pad-resistors.

[3] Only for fully differential mode.

[4] For VBG=1.25V and VDDA=3.3V

[5] For VBG=2.5V and VDDA=3.3V

AC ACCURACY (VREF=1V)

Symbol	Parameter	Conditions	Min	Typ		Max	Units
THD	Total Harmonic Distortion	f_{in}=180kHz		-69 [1]	-68 [2]		dB
THD	Total Harmonic Distortion	f_{in}=4.5MHz		-69 [1]	-61 [2]		dB
THD	Total Harmonic Distortion	f_{in}=10MHz		-66 [1]	-58 [2]		dB
SFDR	Spurious Free Dynamic Range	f_{in}=180kHz		70 [1]	69 [2]		dB
SFDR	Spurious Free Dynamic Range	f_{in}=4.5MHz		70 [1]	59 [2]		dB
SFDR	Spurious Free Dynamic Range	f_{in}=10MHz		68 [1]	59 [2]		dB
SNR	Signal to Noise Ratio	f_{in}=180kHz		57 [1]	57 [2]		dB
SNR	Signal to Noise Ratio	f_{in}=4.5MHz		57 [1]	57 [2]		dB
SNR	Signal to Noise Ratio	f_{in}=10MHz		56 [1]	56 [2]		dB
SINAD	Signal to (Noise+Dist.) Ratio	f_{in}=180kHz		57 [1]	57 [2]		dB
SINAD	Signal to (Noise+Dist.) Ratio	f_{in}=4.5MHz		57 [1]	56 [2]		dB
SINAD	Signal to (Noise+Dist.) Ratio	f_{in}=10MHz		56 [1]	54 [2]		dB
ENOB	Effective Number of Bits	f_{in}=180kHz		9.2 [1]	9.2 [2]		Bit
ENOB	Effective Number of Bits	f_{in}=4.5MHz		9.2 [1]	9.0 [2]		Bit
ENOB	Effective Number of Bits	f_{in}=10MHz		9.0 [1]	8.7 [2]		Bit
TT-IMD	Two-Tone third order Intermodulation Distortion	f_{in1}=4MHz [3] f_{in2}=4.5MHz		74 [1]	-		dBc
TT-SFDR	Two-Tone Spurious Free Dynamic Range	f_{in1}=4MHz [3] f_{in2}=4.5MHz		70 [1]	-		dBc
FPBW	Full Power Bandwidth			50			MHz

AC ACCURACY (VREF=2V)

Symbol	Parameter	Conditions	Min	Typ		Max	Units
THD	Total Harmonic Distortion	f_{in}=180kHz		-68 [1]	-		dB
THD	Total Harmonic Distortion	f_{in}=4.5MHz		-68 [1]	-		dB
THD	Total Harmonic Distortion	f_{in}=10MHz		-63 [1]	-		dB
SFDR	Spurious Free Dynamic Range	f_{in}=180kHz		68 [1]	-		dB
SFDR	Spurious Free Dynamic Range	f_{in}=4.5MHz		68 [1]	-		dB
SFDR	Spurious Free Dynamic Range	f_{in}=10MHz		64 [1]	-		dB
SNR	Signal to Noise Ratio	f_{in}=180kHz		59 [1]	-		dB
SNR	Signal to Noise Ratio	f_{in}=4.5MHz		59 [1]	-		dB
SNR	Signal to Noise Ratio	f_{in}=10MHz		58 [1]	-		dB
SINAD	Signal to (Noise+Dist.) Ratio	f_{in}=180kHz		58 [1]	-		dB
SINAD	Signal to (Noise+Dist.) Ratio	f_{in}=4.5MHz		58 [1]	-		dB
SINAD	Signal to (Noise+Dist.) Ratio	f_{in}=10MHz		56 [1]	-		dB
ENOB	Effective Number of Bits	f_{in}=180kHz		9.4 [1]	-		Bit
ENOB	Effective Number of Bits	f_{in}=4.5MHz		9.4 [1]	-		Bit
ENOB	Effective Number of Bits	f_{in}=10MHz		9.1 [1]	-		Bit
TT-IMD	Two-Tone third order Intermodulation Distortion	f_{in1}=4MHz [3] f_{in2}=4.5MHz		70 [1]	-		dBc
TT-SFDR	Two-Tone Spurious Free Dynamic Range	f_{in1}=4MHz [3] f_{in2}=4.5MHz		65 [1]	-		dBc
FPBW	Full Power Bandwidth			50			MHz

[1] Measurements in Fully Differential Mode

[2] Measurements in Single Ended Mode

[3] Both signals, f_{in1} and f_{in2}, have an amplitude of -7dB full scale.

DIGITAL INPUTS AND OUTPUTS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VDD	Pos. digital Supply Voltage	VDD=VDDA	2.7	3.3	3.6	V
VSS	Neg. digital Supply Voltage	GND=GNDA	0	0	0	V
VIL	Digital Input Level		GND		0.3VDD	V
VIH			0.7VDD		VDD	V
VOL	Digital Output Level			GND		V
VOH				VDD		V
B[9:0]	Output Code	Vind=-VREF		000		HEX
		Vind=VREF		3FF		HEX

POWER REQUIREMENTS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VDDA	Pos. analog Supply Voltage	VDD=VDDA	2.7	3.3	3.6	V
VSSA	Neg. analog Supply Voltage	GND=GNDA	0	0	0	V
IDD [1)]	Supply Current Digital	Op. Mode 1		1.5	3	mA
IDDA [1)]	Supply Current Analog	Op. Mode 1		59	108	mA
Psup [1)]	Supply Power Consumption	Op. Mode 1		200	400	mW
Pdiss_tot [1)]	Total Power Dissipation Powerup Mode	Op. Mode 1		200	400	mW
IDD [2)]	Supply Current Digital	Op. Mode 6		1.5	3	mA
IDDA [2)]	Supply Current Analog	Op. Mode 6		38	69	mA
Psup [2)]	Supply Power Consumption	Op. Mode 6		130	260	mW
IREF [2)]	Reference Current	Op. Mode 6		170	340	µA
Pdiss_tot [2)]	Total Power Dissipation Powerup Mode	Op. Mode 6		131	261	mW
Pdiss_pd [3)]	Power Consumption Power Down Mode	Op. Mode 0		100	200	µW

TIMING CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
fclk	CLK Frequency		1		20	MHz
1/Ts	Sampling Rate			fclk		MS/sec
Jclk	CLOCK Jitter				$\frac{16*10^{-5}}{fin}$	psec
Tsd	Clock falling edge to sampling instant delay			1.1		nsec
Tod	Clock falling edge to data out delay			5		nsec
	Clock duty cycle		45	50	55	%
	Data Latency		5	5	5	CLK cycle
	Power Up Delay [4)]			20		CLK cycle

[1)] In Op. Mode 1 (internal references) with VREF=1V at 20MHz clock frequency.

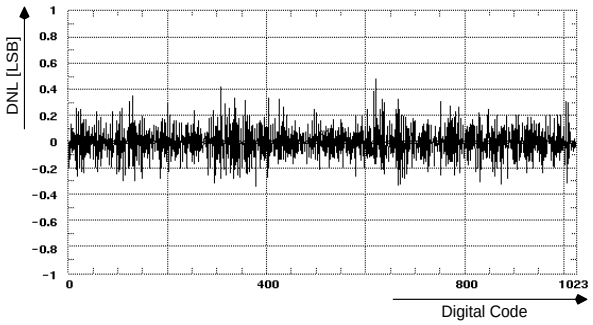
[2)] In Op. Mode 6 (external references) with VREF=1V at 20MHz clock frequency.

[3)] After 10us power down.

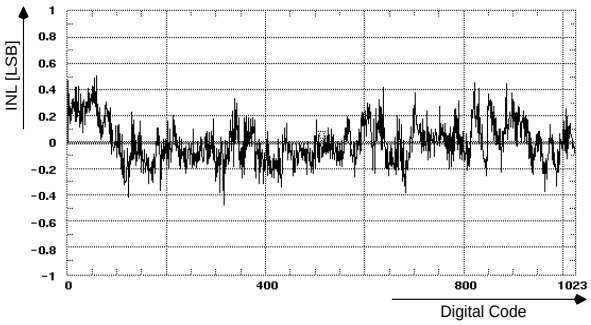
[4)] The digital output codes of the ADC are not valid during the first few clock cycles after a power up.

TYPICAL PERFORMANCE CHARACTERISTICS

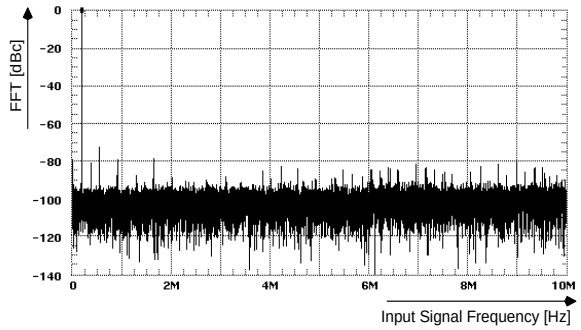
(T=25deg, VDDA=VDD=+3.3V, fclk=20MHz, VREFP=2V, VREFN=1V, Op. Mode 1 and Fully Differential Mode, unless otherwise specified)



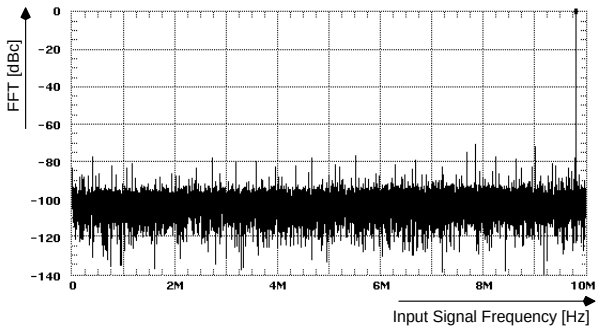
DNL @180kHz



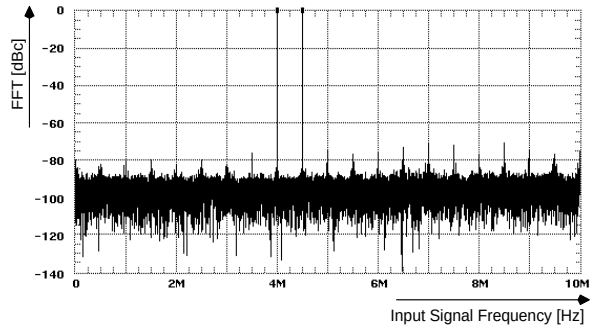
INL @180kHz



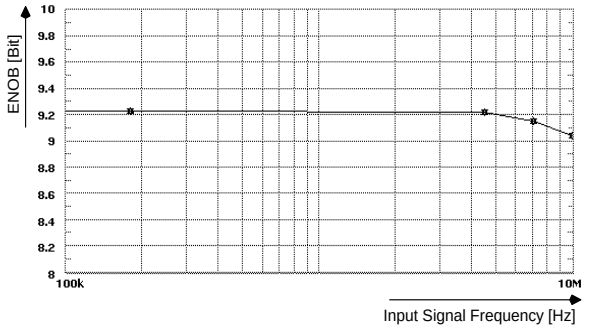
Spectrum @180kHz [1)]



Spectrum @9.8MHz [1)]



Two-Tone IMD @4.0MHz and 4.5MHz [2)]

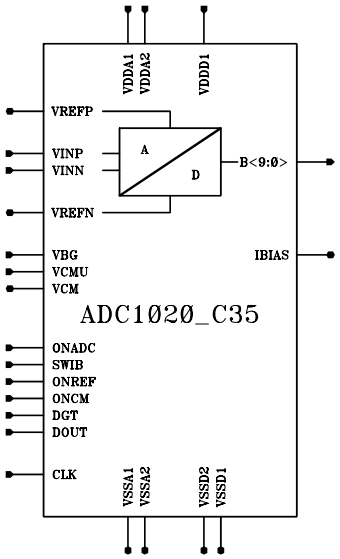


ENOB vs Input Signal Frequency [2)]

[1)] The spectrum consists of 16384 pins.

[2)] Measured with a 12MHz low pass filter for all frequencies.

SYMBOL



PINLIST

Pin	Description	I/O	Type
VINP	Pos. Input Voltage	I	Analog
VINN	Neg. Input Voltage	I	Analog
VBG	Input for Bandgap Reference Voltage	I	Analog
VREFP	Output or bypass of Internal Pos. Reference Voltage	I/O	Analog
VREFN	Output or bypass of Internal Neg. Reference Voltage	I/O	Analog
VCMU	Input for Unbuffered Common Mode Voltage for Analog Signals	I	Analog
VCM	Output or bypass of internally buffered VCM	I/O	Analog
CLK	Clock Input	I	Digital
B[9:0]	Digital Output Bits (B9 = MSB, B0 = LSB)	O	Digital
ONADC	Power Down Input for ADC (ONADC = 1 ⇔ normal operation)	I	Digital
ONREF	Power Down Input for Reference Generator (ONREF=1⇔ normal operation)	I	Digital
ONCM	Power Down Input for VCM buffer (ONCM=1⇔ normal operation)	I	Digital
DGT	Input for digital test mode; must be tied to VSSD1	I	Digital
DOUT	Input for ADC flash output data test mode; must be tied to VDDD1	I	Digital
SWIB	Bias current control pin; if High, the ADC uses internal bias current; otherwise it enables the external current input.	I	Digital
IBIAS	Output for monitoring internal bias current generation when SWIB="1" or input for injection of external bias current (10µA) when SWIB="0"	I/O	Analog
VDDA1	Top Analog Power Supply	I	Supply
VDDA2	Top Analog Power Supply	I	Supply
VDDD1	Top Digital Power Supply	I	Supply
VSSA1	Bottom Analog Power Supply	I	Supply
VSSA2	Biasing voltage for an N-Well shielding a bus from the substrate	I	Supply
VSSD1	Bottom Digital Power Supply	I	Supply
VSSD2	Bottom Digital Power Supply for Shielding	I	Supply

THEORY OF OPERATION

The AD1020 is a 10-bit ADC capable of sampling at 20 MS/s. It uses a fully differential pipelined architecture with 1.5-bit per stage and digital error correction to achieve improved linearity performance. A dedicated wide-band input sample-and-hold amplifier (S/H) is built-in to provide low-jitter, sub-sampling capability with inherent frequency down-conversion and, optionally, single-ended to fully differential signal conversion. The raw digital words are synchronized by a chain of delay stages and overlapped and processed by the digital error correction logic to produce the 10-bit digital output code.

OPERATING MODES

The modes of operation are summarized in the table bellow, and described in detail as follows.

Mode	Description	ONADC	ONREF	ONCM	SWIB
0	Complete Power Down	0	X	X	X
1	Normal conversion with internally buffered VCM, VREF and Ibias generation	1	1	1	1
2	Normal conversion with internal VREF and Ibias generation, externally buffered VCM	1	1	0	1
3	Normal conversion with internal Ibias generation, external VCM and VREF	1	0	0	1
4	Normal conversion with internally buffered VCM, VREF and external Ibias	1	1	1	0
5	Normal conversion with internal VREF generation, external VCM and Ibias	1	1	0	0
6	Normal conversion with external VCM, VREF and Ibias	1	0	0	0

Mode 0 - Power Down

In this mode all the circuitry is in power-down. The power dissipation is reduced to a minimum value.

Mode 1 - Normal Conversion

This is the normal conversion mode of the converter. The bias current is internally generated and the reference and the common mode voltages are internally buffered. The external bandgap reference voltage VBG determines the values of the reference voltages.

Mode 2 through Mode 6 - Conversion Mode with different Bypassing options

These conversion modes allow different bypassing options for the bias current generator, the reference generation and the buffer of the common mode voltages.

POWER SUPPLIES

The converter requires a single +3.3V power supply. The supplies for analog and digital are separated and may be connected together. However, for maximum noise immunity it is recommended to wire them on chip to separated pins, especially when the block is embedded in a large digital circuit. The supplies may then be connected together on PC-board level.
The proper use of blocking capacitors in the application is important!

REFERENCE VOLTAGES

If ONREF is set to high the converter needs a external bandgap reference VBG which defines the dynamic range of the input signal as described in the technical data section. If ONREF is set to low the external voltage references VREFP and VREFN define the dynamic range of the input signal.
A additional series resistor in the pad cell of VBG causes a wrong reference voltage generation in all modes with internal reference generation – see footnotes in the technical data section.
For external reference generation an additional resistor in the pad cells of VREFP and VREFN causes a voltage drop. This results in a smaller reference difference VREF.
The proper use of blocking capacitors in the application is important!

SYSTEM REQUIREMENTS

The ADC is sensitive to ground noise. So all parts of the whole system except the ADC should be quiet during the conversions. To minimize ground noise coming from digital output pads the connection of a series resistor should be used to limit the switching current. In the test circuit a series resistor of 1kΩ is used for the digital output bus.

CONVERSION MODES

The converter operates with fully-differential or single-ended inputs. The best performance of this ADC is reached for fully-differential inputs.

Single Ended Mode

To use the ADC1020 as a Single Ended Converter the input VINN must be connected to VCM. In this case the ADC performs a single-ended to fully-differential conversion. The second input VINP should be balanced around VCM.

Fully Differential Mode

To use the ADC1020 as a Fully Differential Converter both inputs VINP and VINN should be balanced around VCM.

CODE TABLES

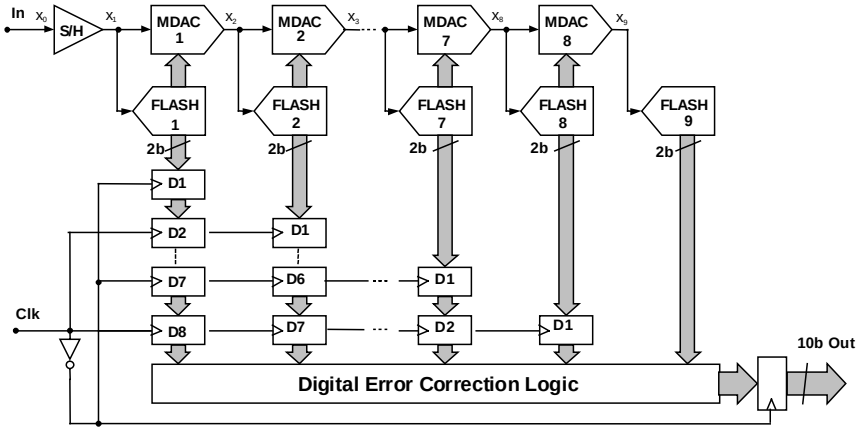
The digital representation of the data bus in both conversion modes is described in the following table.

$$VREF = VREFP - VREFN, \qquad 1LSB = \frac{VREFP - VREFN}{512}$$

Offset Binary

Output Code	Input Voltage: VIN-VINB
11 1111 1111	511LSB ... VREF
11 1111 1110	510LSB ... 511LSB
...	...
10 0000 0001	1LSB ... 2LSB
10 0000 0000	0 ... 1LSB
01 1111 1111	-1LSB ... 0
01 1111 1110	-2LSB ... -1LSB
...	...
00 0000 0001	-511LSB ... -510LSB
00 0000 0000	-VREF ... -511LSB

FUNCTIONAL BLOCK DIAGRAM



TIMING DIAGRAM

The sampling rate of the AD1020 is defined by the frequency of the CLK signal. The input signal voltage of the ADC is sampled in the falling edge of CLK. As the conversion stages operate in a staggered fashion in alternate phases of CLK, the duty-cycle of this signal must be 50%. The results are latched in the output register on the falling edge of CLK, with a latency of 5 CLK periods. The conversion timing is shown in Diagram 1.

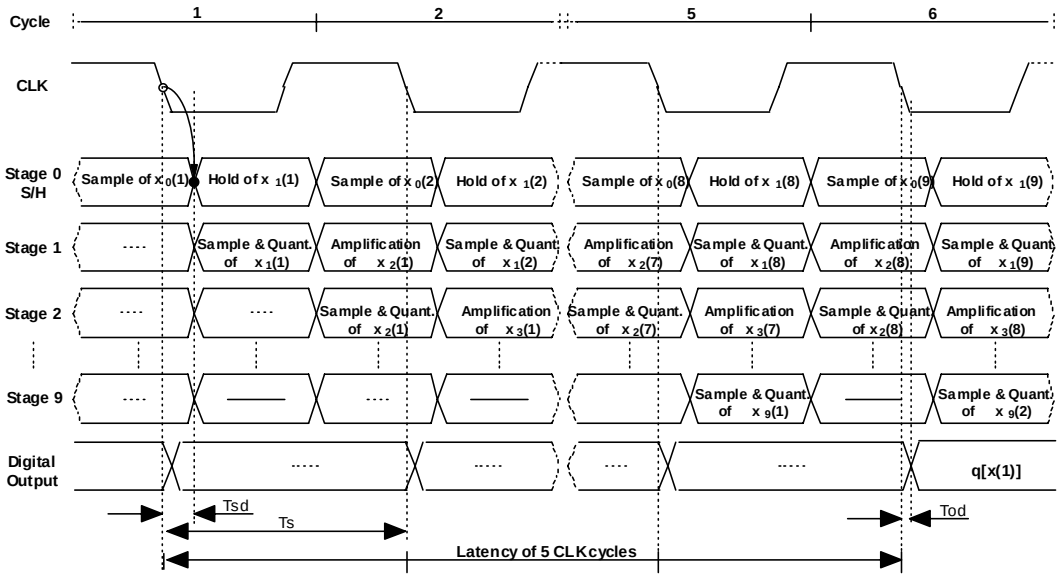


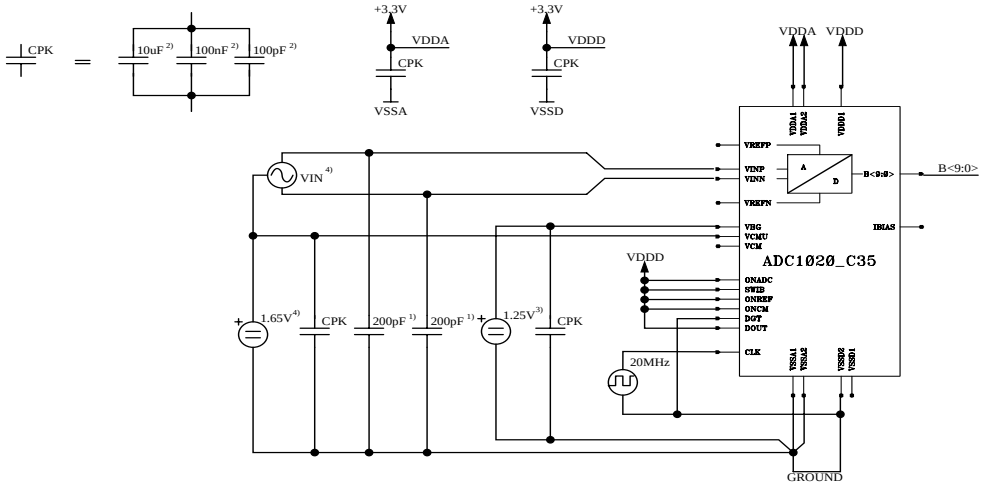
Diagram 1: Timing of the pipelining operation

TYPICAL APPLICATION

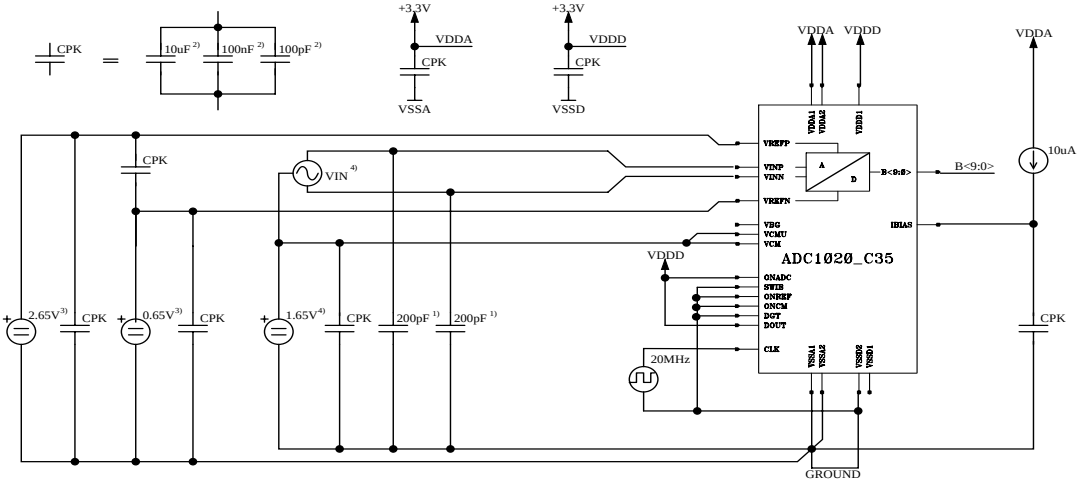
The ADC1020 is targeted for general purpose sampling ADC functions where high-speed conversion rates and medium precision are of critical importance.

APPLICATION

- Video
- Imaging
- Data acquisition systems
- High-speed data transmission
- Communications



Configuration: Op. Mode 1 at 20MS/sec, fully differential with VREF=1V



Configuration: Op. Mode 6 at 20MS/sec, fully differential with VREF=2V

---

1) The value of the capacitor depends on the input frequency.
For SMD capacitors use the type NPO and for normal capacitors use the type MKT for best performance.

2) For SMD capacitors use the type NPO and for normal capacitors use the type MKT for best performance.

3) The accuracy of both reference voltages must be higher than the resolution of the ADC. In typical applications both voltages are filtered by a second order low pass filter (f_c=5Hz) and buffered with an AD711.

4) The accuracy of both input voltages must be higher than the resolution of the ADC. In typical applications both voltages are filtered by a third order low pass filter (f_c=12MHz) and buffered with a THS3001.

Contact

austriamicrosystems AG
A 8141 Schloss Premstätten, Austria
T. +43 (0) 3136 500 5333
F. +43 (0) 3136 500 5755
support@austriamicrosystems.com

Copyright