ADC10DV200 Dual 10-bit, 200 MSPS Low-Power A/D Converter with Parallel LVDS/CMOS Outputs

National Semiconductor

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ADC10DV200

Dual 10-bit, 200 MSPS Low-Power A/D Converter with Parallel LVDS/CMOS Outputs

General Description

The ADC10DV200 is a monolithic analog-to-digital converter capable of converting two analog input signals into 10-bit digital words at rates up to 200 Mega Samples Per Second (MSPS). The digital output mode is selectable and can be either differential LVDS or CMOS signals. This converter uses a differential, pipelined architecture with digital error correction and an on-chip sample-and-hold circuit to minimize die size and power consumption while providing excellent dynamic performance. A unique sample-and-hold stage yields a full-power bandwidth of 900MHz. Fabricated in core CMOS process, the ADC10DV200 may be operated from a single 1.8V power supply. The ADC10DV200 achieves approximately 9.6 effective bits at Nyquist and consumes just 280mW at 170MSPS in CMOS mode and 450mW at 200MSPS in LVDS mode. The power consumption can be scaled down further by reducing sampling rates.

Applications

- Communications
- Medical Imaging
- Portable Instrumentation
- Digital Video

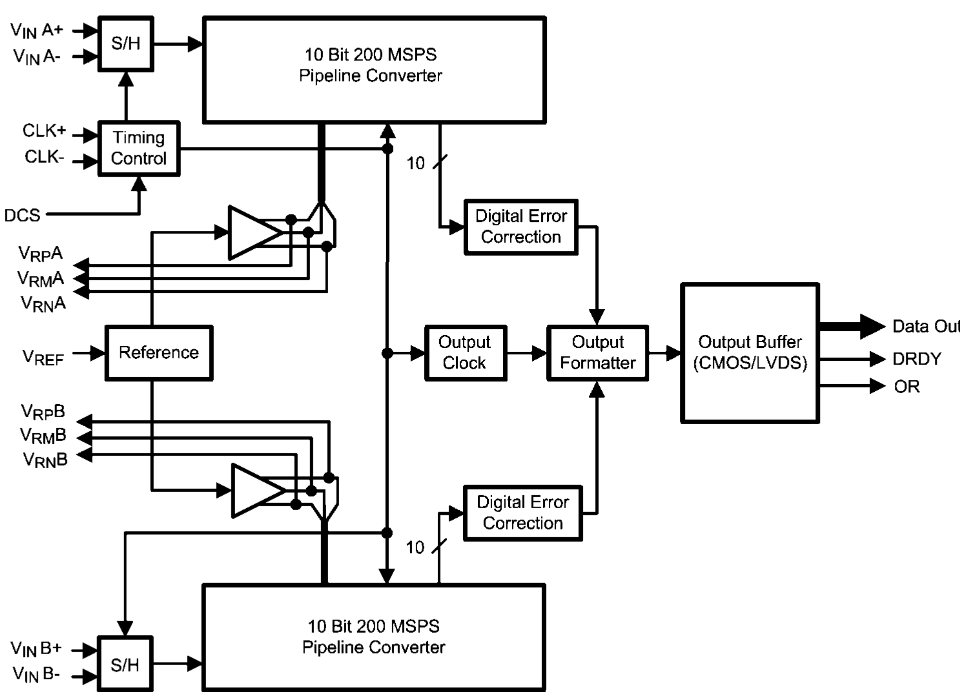
Features

- Single 1.8V power supply operation.
- Power scaling with clock frequency.
- Internal sample-and-hold.
- Internal or external reference.
- Power down mode.
- Offset binary or 2's complement output data format.
- LVDS or CMOS output signals.
- 60-pin LLP package, (9x9x0.8mm, 0.5mm pin-pitch)
- Clock Duty Cycle Stabilizer.
- IF Sampling Bandwidth > 900MHz.

Key Specifications

- Resolution 10 Bits
- Conversion Rate 200 MSPS
- ENOB 9.6 bits (typ) @Fin=70MHz
- SNR 59.9 dBFS (typ) @Fin=70MHz
- SINAD 59.9 dBFS (typ) @Fin=70MHz
- SFDR 82 dBFS (typ) @Fin=70MHz
- LVDS Power 450mW (typ) @Fs=200MSPS
- CMOS Power 280mW (typ) @Fs=170MSPS
- Operating Temp. Range −40°C to +85°C.

Block Diagram



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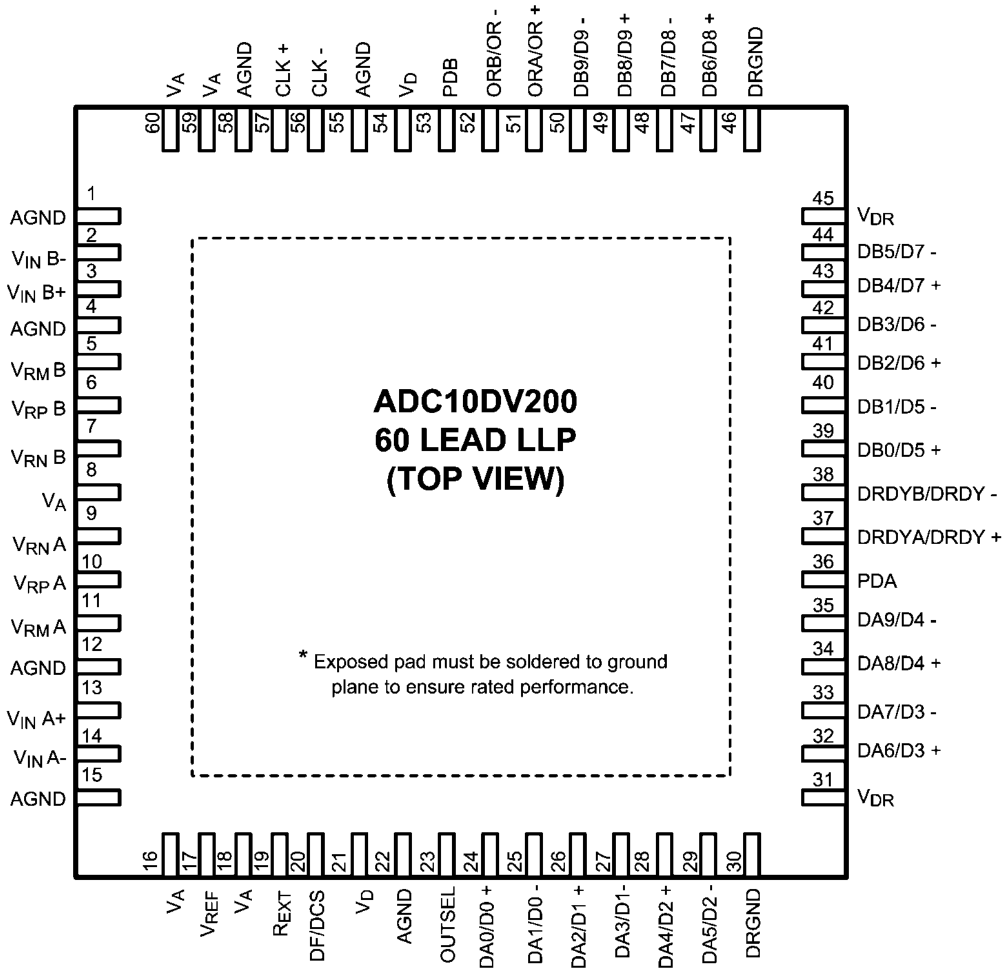
Connection Diagram



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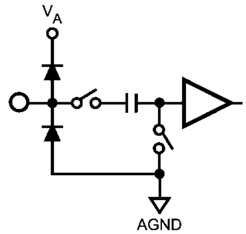
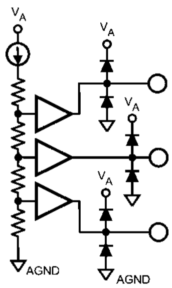
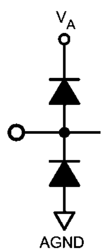
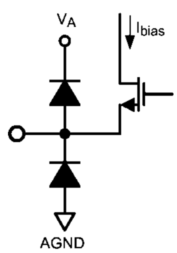
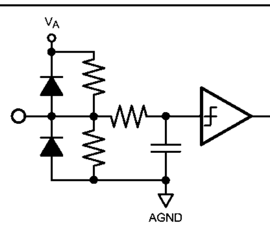
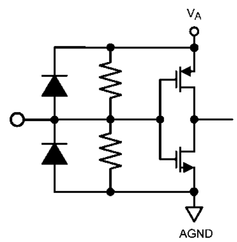
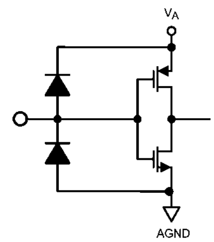
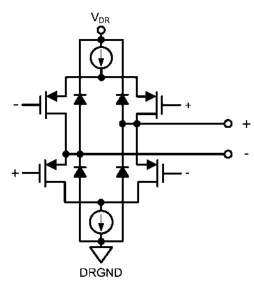
Ordering Information

Industrial (–40°C ≤ T_A ≤ +85°C)	Package
ADC10DV200CISQ	60 Pin LLP
ADC10DV200CISQE	60 Pin LLP, 250 pc. Tape and Reel
ADC10DV200EB	Evaluation Board

Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
ANALOG I/O			
13 3	$V_{IN}A+$ $V_{IN}B+$		Differential analog input pins. The differential full-scale input signal level is $1.5V_{P-P}$ with each input pin signal centered on a common mode voltage, V_{CM}.
14 2	$V_{IN}A-$ $V_{IN}B-$		
10 6	$V_{RP}A$ $V_{RP}B$		These pins should each be bypassed to AGND with a low ESL (equivalent series inductance) 0.1 µF capacitor placed very close to the pin to minimize stray inductance. An 0201 size 0.1 µF capacitor should be placed between V_{RP} and V_{RN} as close to the pins as possible. V_{RP} and V_{RN} should not be loaded. V_{RM} may be loaded to 1mA for use as a temperature stable 0.9V reference. It is recommended to use V_{RM} to provide the common mode voltage, V_{CM} for the differential analog inputs.
11 5	$V_{RM}A$ $V_{RM}B$		
9 7	$V_{RN}A$ $V_{RN}B$		
17	V_{REF}		Reference Voltage select pin and external reference input. The relationship between the voltage on the pin and the reference voltage is as follows: $1.4V \leq V_{REF} \leq VA$ — The internal 0.75V reference is used. $0.2V \leq V_{REF} \leq 1.4V$ — The external reference voltage is used. Note: When using an external reference, be sure to bypass with a 0.1µF capacitor to AGND as close to the pin as possible. $AGND \leq V_{REF} \leq 0.2V$ — The internal 0.5V reference is used.
19	R_{EXT}		Programming resistor for analog bias current. Nominally a 3.3kΩ to AGND for 200MSPS, or tie to V_A to use the internal frequency scaling current.
20	DF/DCS		Data Format/Duty Cycle Correction selection pin. (see *Table 1*)

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Equivalent Circuit</th><th>Description</th></tr>
<tr><td colspan="4">DIGITAL I/O</td></tr>
<tr><td>57
56</td><td>CLK +
CLK -</td><td>
</td><td>Clock input pins signal. The analog inputs are sampled on the rising edge of this signal. The clock can be configured for single-ended mode by shorting the CLK- pin to AGND. When in differential mode, the common mode voltage for the clock is internally set to 1.2V.</td></tr>
<tr><td>36
53</td><td>PD_A
PD_B</td><td rowspan="2">
</td><td>Two-state input controlling Power Down.
PD = V_A, Power Down is enabled and power dissipation is reduced.
PD = AGND, Normal operation.</td></tr>
<tr><td>23</td><td>OUTSEL</td><td>Two-state input controlling Output Mode.
OUTSEL = V_D, LVDS Output Mode.
OUTSEL = AGND, CMOS Output Mode.</td></tr>
<tr><td colspan="4">LVDS Output Mode</td></tr>
<tr><td>24, 25
26, 27
28, 29
32, 33
34, 35
39, 40
41, 42
43, 44
47, 48
49, 50</td><td>D0+,D0-
D1+, D1-
D2+, D2-
D3+, D3-
D4+, D4-
D5+, D5-
D6+, D6-
D7+, D7-
D8+, D8-
D9+, D9-</td><td rowspan="3">
</td><td>LVDS Output pairs for bits 0 through 9. A-channel and B-channel digital LVDS outputs are interleaved. A channel is ready at rising edge of DRDY and B channel is ready at the falling edge of DRDY.</td></tr>
<tr><td>37
38</td><td>DRDY+
DRDY-</td><td>Data Ready Strobe. This signal is a LVDS DDR clock used to capture the output data. A-channel data is valid on the rising edge of this signal and B-channel data is valid on the falling edge.</td></tr>
<tr><td>51
52</td><td>OR+
OR-</td><td>ADC over-range Signal. This signals timing is formatted similarly to the data output signals. A channel is valid on DRDY rising and B channel is valid on DRDY falling. This signal will go high when the respective channel exceeds the allowable range of the ADC. Nominally this signal will be low.</td></tr>
</table>

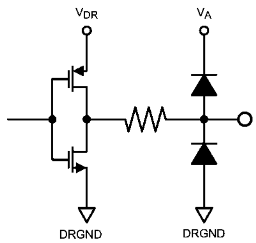
Pin No.	Symbol	Equivalent Circuit	Description
CMOS Output Mode			
24-29, 32-35	DA0-DA9		Digital data output pins that make up the 10-bit conversion result for Channel A. DA0 (pin 24) is the LSB, while DA9 (pin 35) is the MSB of the output word. Output levels are CMOS compatible.
39-44, 47-50	DB0-DB9		Digital data output pins that make up the 10-bit conversion result for Channel B. DB0 (pin 39) is the LSB, while DB9 (pin 50) is the MSB of the output word. Output levels are CMOS compatible.
37	DRDYA		Data Ready Strobe for channel A. This signal is used to clock the A-Channel output data. DRDYA is a SDR clock with same frequency as CLK rate and data is valid on the rising edges.
38	DRDYB		Data Ready Strobe for channel B. This signal is used to clock the B-Channel output data. DRDYB is a SDR clock with same frequency as CLK rate and data is valid on the rising edges.
51	ORA		Overrange indicator for channel A. A high on this pin indicates that the input exceeded the allowable range for the converter.
52	ORB		Overrange indicator for channel B. A high on this pin indicates that the input exceeded the allowable range for the converter.
ANALOG POWER			
8, 16, 18, 59, 60	V_A		Positive analog supply pins. These pins should be connected to a quiet source and be bypassed to AGND with 0.1 µF capacitors located close to the power pins.
1, 4, 12, 15, 22, 55, 58, EP	AGND		The ground return for the analog supply. Exposed pad must be soldered to AGND to ensure rated performance.
DIGITAL POWER			
21, 54	V_D		Positive digital supply pins. These pins should be connected to a quiet source and be bypassed to AGND with 0.1 µF capacitors located close to the power pins.
31, 45	V_{DR}		Positive driver supply pin for the output drivers. This pin should be connected to a quiet voltage source and be bypassed to DRGND with a 0.1 µF capacitor located close to the power pin.
30, 46	DRGND		The ground return for the digital output driver supply. This pin should be connected to the system digital ground.

TABLE 1. Voltage on DF/DCS Pin and Corresponding Chip Response

Voltage on DF/DCS				Results	Suggestions
Min	**Max**	**DF**	**DCS**		
0 mV	200mV	1	1	2's complement data, duty cycle correction on	Tie to AGND
250 mV	600 mV	0	0	Offset binary data, duty cycle correction off	Leave floating
750 mV	1250 mV	1	0	2's complement data, duty cycle correction off	
1400mV	V_A	0	1	Offset binary data, duty cycle correction on	Tie to VA

Absolute Maximum Ratings (Notes 3, 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_A, V_D V_{DR})	−0.3V to 2.2V
Voltage on Any Pin (Not to exceed 2.2V)	−0.3V to (V_A +0.3V)
Input Current at Any Pin other than Supply Pins (Note 4)	±25 mA
Package Input Current (Note 4)	±50 mA
Max Junction Temp (T_J)	+150°C
Thermal Resistance (θ_{JA})	30°C/W
ESD Rating (Note 6)	
Human Body Model	2500V
Machine Model	250V
Human Body Model	750V
Storage Temperature	−65°C to +150°C

Soldering process must comply with National Semiconductor's Reflow Temperature Profile specifications. Refer to www.national.com/packaging. (Note 7)

Operating Ratings (Notes 1, 3)

Operating Temperature	$-40°C \leq T_A \leq +85°C$
Supply Voltage (V_A, V_D, V_{DR})	+1.7V to +1.9V
Clock Duty Cycle	
(DCS Enabled)	30/70 %
(DCS disabled)	48/52 %
V_{CM}	0.8V to 1.0V

Converter Electrical Characteristics

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, $V_A = V_D = V_{DR} = +1.8V$, f_{CLK} = 200 MHz, CLK duty cycle = 50%, DCS = ON, Internal 0.75V Reference, LVDS Output. Typical values are for T_A = 25°C. **Boldface limits apply for $T_{MIN} \leq T_A \leq T_{MAX}$.** All other limits apply for T_A = +25°C (Notes 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits	Units (Limits)
STATIC CONVERTER CHARACTERISTICS					
	Resolution with No Missing Codes			**10**	Bits (min)
INL	Integral Non Linearity		±300	**±920**	mLSB (max)
DNL	Differential Non Linearity		±170	**±430**	mLSB (max)
PGE	Positive Gain Error		0.57	**3.11**	%FS (max)
NGE	Negative Gain Error		0.60	**2.72**	%FS (max)
TC PGE	Positive Gain Error Tempco	$-40°C \leq T_A \leq +85°C$	13		ppm/°C
TC NGE	Negative Gain Error Tempco	$-40°C \leq T_A \leq +85°C$	15		ppm/°C
V_{OFF}	Offset Error		0.1	**+0.75** **-0.75**	%FS (max)
TC V_{OFF}	Offset Error Tempco	$-40°C \leq T_A \leq +85°C$	4		ppm/°C
	Under Range Output Code		0	**0**	
	Over Range Output Code		1023	**1023**	
REFERENCE AND ANALOG INPUT CHARACTERISTICS					
V_{RM}	Common Mode Output Voltage		0.9	**1** **0.85**	V (min) V (max)
V_{CM}	Analog Input Common Mode Voltage		0.9		V
C_{IN}	V_{IN} Input Capacitance (each pin to AGND) (Note 11)	V_{IN} = 0.75 Vdc ± 0.5 V (CLK LOW)	1		pF
		V_{IN} = 0.75 Vdc ± 0.5 V (CLK HIGH)	2.5		pF
V_{RP}	Internal Reference Top		1.33		V
V_{RN}	Internal Reference Bottom		0.55		V
	Internal Reference Accuracy	(V_{RP}-V_{RN})	0.78		V
EXT V_{REF}	External Reference Voltage			0.5 1.0	V (Min) V (max)

Dynamic Converter Electrical Characteristics

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, $V_A = V_D = V_{DR}$ = +1.8V, f_{CLK} = 200 MHz, CLK duty cycle = 50%, DCS = ON, Internal 0.75V Reference, LVDS Output. Typical values are for T_A = 25°C. **Boldface limits apply for $T_{MIN} \leq T_A \leq T_{MAX}$.** All other limits apply for T_A = +25°C (Notes 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits	Units (Limits) (Note 2)
DYNAMIC CONVERTER CHARACTERISTICS, A_{IN} = -1dBFS					
FPBW	Full Power Bandwidth (Note 16)	-1 dBFS Input, –3 dB Corner	900		MHz
SNR	Signal-to-Noise Ratio (Note 13)	f_{IN} = 10 MHz	59.9		dBFS
		f_{IN} = 70 MHz	59.9	**59**	dBFS (min)
SFDR	Spurious Free Dynamic Range (Note 14)	f_{IN} = 10 MHz	82		dBFS
		f_{IN} = 70 MHz	82	**70**	dBFS (min)
ENOB	Effective Number of Bits	f_{IN} = 10 MHz	9.65		Bits
		f_{IN} = 70 MHz	9.65	**9.48**	Bits (min)
H2	Second Harmonic Distortion	f_{IN} = 10 MHz	-94		dBFS
		f_{IN} = 70 MHz	-94	**-70**	dBFS (min)
H3	Third Harmonic Distortion	f_{IN} = 10 MHz	-85		dBFS
		f_{IN} = 70 MHz	-84	**-70**	dBFS (min)
SINAD	Signal-to-Noise and Distortion Ratio (Note 15)	f_{IN} = 10 MHz	59.8		dBFS
		f_{IN} = 70 MHz	59.8	**58.9**	dBFS (min)
IMD	Intermodulation Distortion (Note 16)	$f_{IN}1$ = 69 MHz $A_{IN}1$ = -7 dBFS $f_{IN}2$ = 70 MHz $A_{IN}2$ = -7 dBFS	93		dBFS
	Cross Talk (Note 16)	$f_{IN}1$ = 69 MHz $A_{IN}1$ = -1 dBFS $f_{IN}2$ = 70MHz $A_{IN}2$ = -1 dBFS	97		dBFS

Power Supply Electrical Characteristics

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, $V_A = V_D = V_{DR}$ = +1.8V, f_{CLK} = 200 MHz, CLK duty cycle = 50%, DCS = ON, Internal 0.75V Reference, LVDS Output. Typical values are for T_A = 25°C. **Boldface limits apply for $T_{MIN} \leq T_A \leq T_{MAX}$.** All other limits apply for T_A = 25°C (Notes 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits	Units (Limits)
LVDS OUTPUT MODE					
I_A	Analog Supply Current	Full Operation, Internal Bias	160		mA
		Full Operation, External 3.3kΩ Bias	148	**184**	mA (max)
I_D	Digital Supply Current	Full Operation	36	**43**	mA (max)
I_{DR}	Output Driver Supply Current		64	**80**	mA (max)
	Power Consumption	Internal Bias	473		mW
		External 3.3kΩ Bias	450	**524**	mW (max)
	Power Down Power Consumption	PDA=PDB=V_A	57		mW
CMOS OUTPUT MODE (Note 12)					
I_A	Analog Supply Current	Full Operation, Internal Bias	138		mA
		Full Operation, External 3.3kΩ Bias	124		
I_D	Digital Supply Current	Full Operation	31		mA
	Power Consumption	Internal Bias	310		mW
		External 3.3kΩ Bias	280		
	Power Down Power Consumption	PDA=PDB=V_A	60		mW

Input/Output Logic Electrical Characteristics

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, $V_A = V_D = V_{DR}$ = +1.8V, f_{CLK} = 200 MHz, CLK duty cycle = 50%, DCS = ON, Internal 0.75V Reference. Typical values are for T_A = 25°C. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for T_A = 25°C (Notes 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits	Units (Limits)
DIGITAL INPUT CHARACTERISTICS (PD_A,PD_B,OUTSEL)					
$V_{IN(1)}$	Logical “1” Input Voltage (Note 16)	V_A = 1.9V		0.89	V (min)
$V_{IN(0)}$	Logical “0” Input Voltage (Note 16)	V_A = 1.7V		0.67	V (max)
$I_{IN(1)}$	Logical “1” Input Current	V_{IN} = 1.8V	10.6		µA
$I_{IN(0)}$	Logical “0” Input Current	V_{IN} = 0V	-7.6		µA
C_{IN}	Digital Input Capacitance		2		pF
LVDS OUTPUT CHARACTERISTICS (D0-D9,DRDY,OR)					
V_{OD}	LVDS differential output voltage	(Note 16)	330		mV_{P-P}
$\pm V_{OD}$	Output Differential Voltage Unbalance		0	50	mV
V_{OS}	LVDS common-mode output voltage	(Note 16)	1.25		V
$\pm V_{OS}$	Offset Voltage Unbalance			50	mV
R_L	Intended Load Resistance		100		Ω
CMOS OUTPUT CHARACTERISTICS (DA0-DA9,DB0-DB9,DRDY,OR) (Note 12)					
V_{OH}	Logical "1" Output Voltage	V_{DR} = 1.8V (Unloaded)	1.8		V
V_{OL}	Logical "0" Output Voltage	V_{DR} = 1.8V (Unloaded)	0		V
$+I_{OSC}$	Output Short Circuit Source Current	V_{OUT} = 0V	-20		mA
$-I_{OSC}$	Output Short Circuit Sink Current	$V_{OUT} = V_{DR}$	20		mA
C_{OUT}	Digital Output Capacitance		2		pF

Timing and AC Characteristics

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, $V_A = V_D = V_{DR}$ = +1.8V, f_{CLK} = 200 MHz, CLK duty cycle = 50%, DCS = ON, Internal 0.75V Reference. Typical values are for T_A = 25°C. Timing measurements are taken at 50% of the signal amplitude. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for T_A = 25°C (Notes 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits	Units (Limits)
LVDS OUTPUT MODE					
	Maximum Clock Frequency			**200**	MHz (max)
	Minimum Clock Frequency	DCS On DCS Off		65 45	MHz (min)
t_{CH}	Clock High Time	DCS On DCS Off		1.5 2.4	ns (min)
t_{CL}	Clock Low Time	DCS On DCS Off		1.5 2.4	ns (min)
t_{CONV}	Conversion Latency			**5/5.5 (A/B)**	Clock Cycles
t_{ODA}	Output Delay of CLK to A-Channel Data	Relative to rising edge of CLK	2.7	**1.46**	ns (min)
t_{ODB}	Output Delay of CLK to B-Channel Data	Relative to falling edge of CLK	2.7	**1.46**	ns (min)
t_{SU}	Data Output Setup Time	Relative to DRDY	1.2	**0.7**	ns (min)
t_H	Data Output Hold Time	Relative to DRDY	1.2	**0.7**	ns (min)
t_{AD}	Aperture Delay		0.7		ns
t_{AJ}	Aperture Jitter		0.3		ps rms
t_{SKEW}	Data-Data Skew		20	**470**	ps

Symbol	Parameter	Conditions	Typical (Note 10)	Limits	Units (Limits)
CMOS OUTPUT MODE (Notes 12, 16)					
	Maximum Clock Frequency			170	MHz
	Minimum Clock Frequency	DCS On DCS Off		65 25	MHz
t_{CH}	Clock High Time	DCS On DCS Off		1.76 2.82	ns
t_{CL}		DCS On DCS Off		1.76 2.82	ns
t_{CONV}	Conversion Latency			5.5	Clock Cycles
t_{OD}	Output Delay of CLK to DATA	Relative to falling edge of CLK	4.5	3.15 5.81	ns (min) ns (max)
t_{SU}	Data Output Setup Time(Note 16)	Relative to DRDY	2.5	1.79	ns (min)
t_H	Data Output Hold Time(Note 16)	Relative to DRDY	3.4	2.69	ns (min)
t_{AD}	Aperture Delay		0.7		ns
t_{AJ}	Aperture Jitter		0.3		ps rms

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is guaranteed to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the maximum Operating Ratings is not recommended.

Note 2: Units of dBFS indicates the value that would be attained with a full-scale input signal.

Note 3: All voltages are measured with respect to GND = AGND = DRGND = 0V, unless otherwise specified.

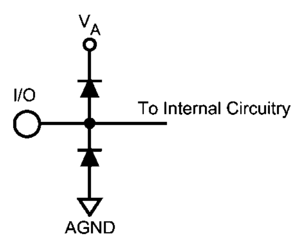
Note 4: When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < AGND, or $V_{IN} > V_A$), the current at that pin should be limited to ±5 mA. The ±50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of ±5 mA to 10.

Note 5: The maximum allowable power dissipation is dictated by $T_{J,max}$, the junction-to-ambient thermal resistance, (θ_{JA}), and the ambient temperature, (T_A), and can be calculated using the formula $P_{D,max} = (T_{J,max} - T_A)/\theta_{JA}$. The values for maximum power dissipation listed above will be reached only when the device is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Such conditions should always be avoided.

Note 6: Human Body Model is 100 pF discharged through a 1.5 kΩ resistor. Machine Model is 220 pF discharged through 0Ω resistor. Charged device model simulates a pin slowly acquiring charge (such as from a device sliding down the feeder in an automated assembler) then rapidly being discharged.

Note 7: Reflow temperature profiles are different for lead-free and non-lead-free packages.

Note 8: The inputs are protected as shown below. Input voltage magnitudes above V_A or below GND will not damage this device, provided current is limited per (Note 4). However, errors in the A/D conversion can occur if the input goes above V_A or below AGND.



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Note 9: With a full scale differential input of $1.5V_{P-P}$, the 10-bit LSB is 1.465mV.

Note 10: Typical figures are at T_A = 25°C and represent most likely parametric norms at the time of product characterization. The typical specifications are not guaranteed.

Note 11: The input capacitance is the sum of the package/pin capacitance and the sample and hold circuit capacitance.

Note 12: CMOS Specifications are for F_{CLK} = 170 MHz.

Note 13: SNR minimum and typical values are for LVDS mode. Typical values for CMOS mode are typically 0.2dBFS lower.

Note 14: SFDR minimum and typical values are for LVDS mode. Typical values for CMOS mode are typically 2dBFS lower.

Note 15: SINAD minimum and typical values are for LVDS mode. Typical values for CMOS mode are typically 0.1dBFS lower.

Note 16: This parameter is guaranteed by design and/or characterization and is not tested in production.

Specification Definitions

APERTURE DELAY is the time after the falling edge of the clock to when the input signal is acquired or held for conversion.

APERTURE JITTER (APERTURE UNCERTAINTY) is the variation in aperture delay from sample to sample. Aperture jitter manifests itself as noise in the output. The amount of SNR reduction can be calculated as

$$\text{SNR Reduction} = 20 \times \log_{10}[½ \times \pi \times f_A \times t_j]$$

CLOCK DUTY CYCLE is the ratio of the time during one cycle that a repetitive digital waveform is high to the total time of one period. The specification here refers to the ADC clock input signal.

COMMON MODE VOLTAGE (V_{CM}) is the common DC voltage applied to both input terminals of the ADC.

CONVERSION LATENCY is the number of clock cycles between initiation of conversion and when that data is presented to the output driver stage. Data for any given sample is available at the output pins the Pipeline Delay plus the Output Delay after the sample is taken. New data is available at every clock cycle, but the data lags the conversion by the pipeline delay.

CROSSTALK is coupling of energy from one channel into the other channel.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion Ratio or SINAD. ENOB is defined as (SINAD - 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated as:

Gain Error = Positive Full Scale Error – Negative Full Scale Error

It can also be expressed as Positive Gain Error and Negative Gain Error, which are calculated as:

PGE = Positive Full Scale Error - Offset Error
NGE = Offset Error - Negative Full Scale Error

INTEGRAL NON LINEARITY (INL) is a measure of the deviation of each individual code from a best fit straight line. The deviation of any given code from this straight line is measured from the center of that code value.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the intermodulation products to the total power in the original frequencies. IMD is usually expressed in dBFS.

LSB (LEAST SIGNIFICANT BIT) is the bit that has the smallest value or weight of all bits. This value is $V_{FS}/2^n$, where "V_{FS}" is the full scale input voltage and "n" is the ADC resolution in bits.

MISSING CODES are those output codes that will never appear at the ADC outputs. The ADC is guaranteed not to have any missing codes.

MSB (MOST SIGNIFICANT BIT) is the bit that has the largest value or weight. Its value is one half of full scale.

NEGATIVE FULL SCALE ERROR is the difference between the actual first code transition and its ideal value of ½ LSB above negative full scale.

OFFSET ERROR is the difference between the two input voltages [(V_{IN}+) – (V_{IN}-)] required to cause a transition from code 511 to 512.

OUTPUT DELAY is the time delay after the falling edge of the clock before the data update is presented at the output pins.

PIPELINE DELAY (LATENCY) See CONVERSION LATENCY.

POSITIVE FULL SCALE ERROR is the difference between the actual last code transition and its ideal value of 1½ LSB below positive full scale.

POWER SUPPLY REJECTION RATIO (PSRR) is a measure of how well the ADC rejects a change in the power supply voltage. PSRR is the ratio of the Full-Scale output of the ADC with the supply at the minimum DC supply limit to the Full-Scale output of the ADC with the supply at the maximum DC supply limit, expressed in dB.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or DC.

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dB, of the rms total of the first six harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

$$\text{THD} = 20 \times \log \sqrt{\frac{f_2^2 + \ldots + f_7^2}{f_1^2}}$$

where f_1 is the RMS power of the fundamental (output) frequency and f_2 through f_7 are the RMS power of the first six harmonic frequencies in the output spectrum.

SECOND HARMONIC DISTORTION (2ND HARM) is the difference expressed in dB, between the RMS power in the input frequency at the output and the power in its 2nd harmonic level at the output.

THIRD HARMONIC DISTORTION (3RD HARM) is the difference, expressed in dB, between the RMS power in the input frequency at the output and the power in its 3rd harmonic level at the output.

Timing Diagrams

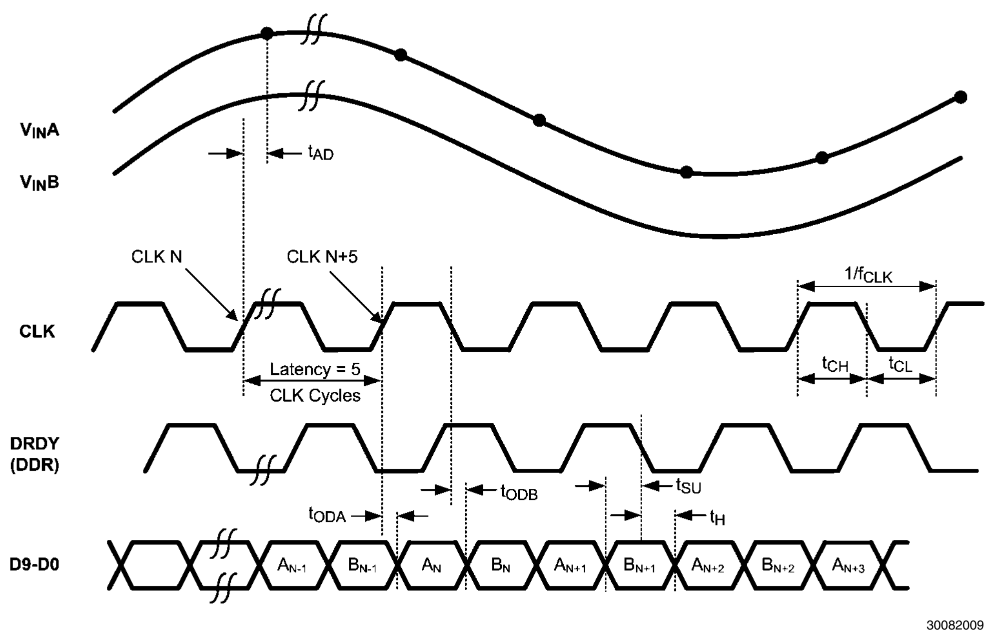


FIGURE 1. LVDS Output Timing

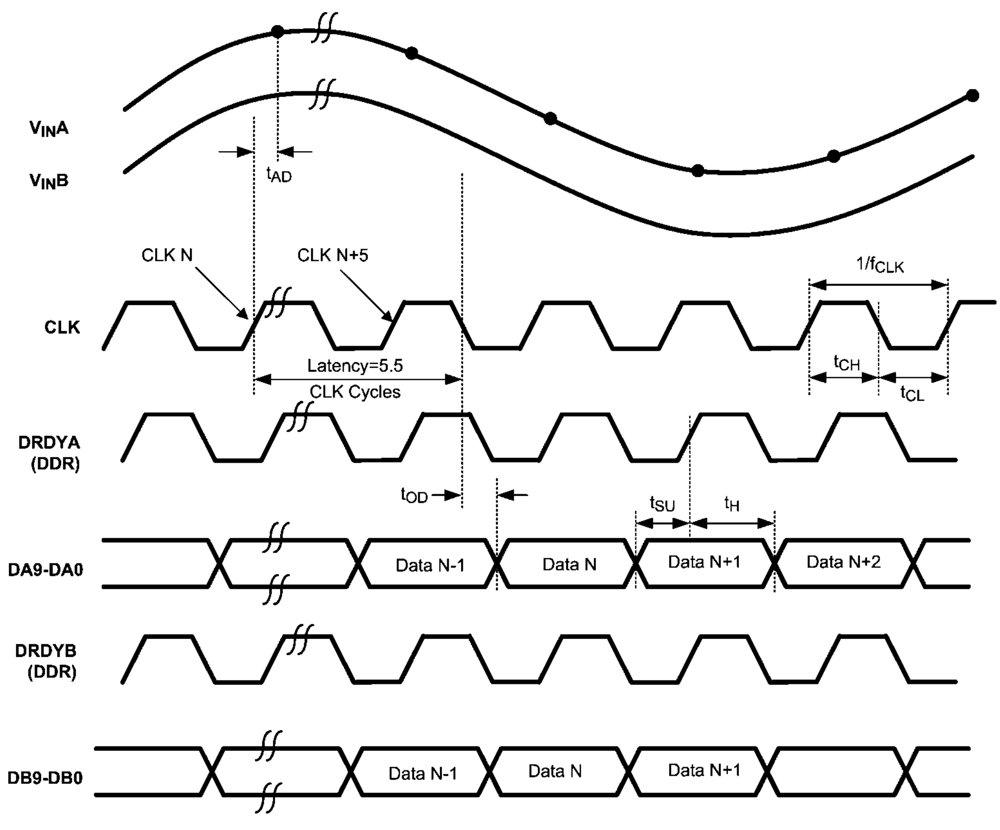


FIGURE 2. CMOS Output Timing

Transfer Characteristic

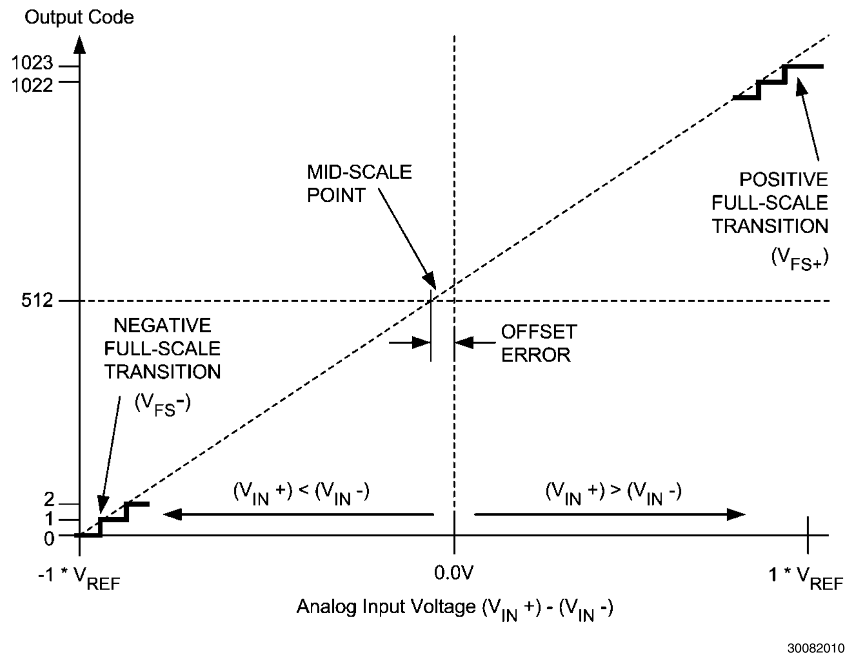
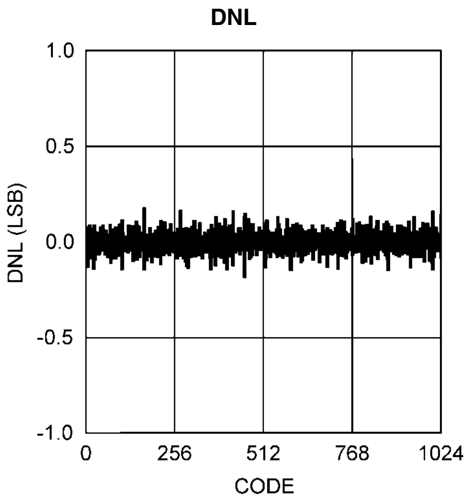


FIGURE 3. Transfer Characteristic

Typical Performance Characteristics DNL, INL

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, $V_A = V_D = V_{DR}$ = +1.8V, f_{CLK} = 200 MHz, 50% Duty Cycle, DCS Enabled, LVDS Output, $V_{CM} = V_{RM}$, T_A = 25°C.



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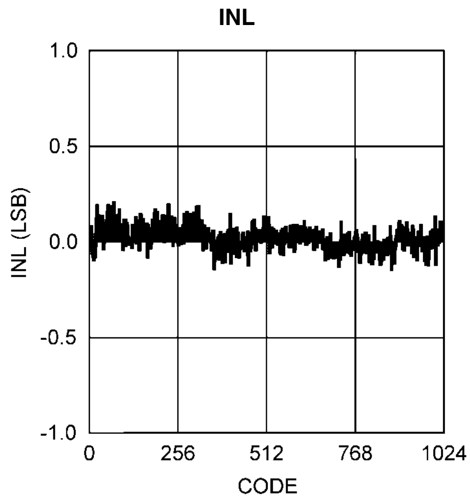

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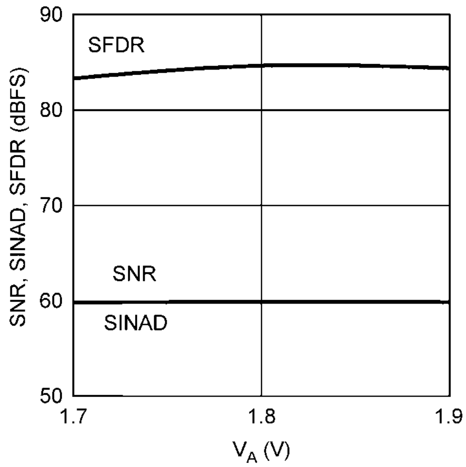
Typical Performance Characteristics

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, $V_A = V_D = V_{DR}$ = +1.8V, f_{CLK} = 200 MHz, 50% Duty Cycle, DCS disabled, LVDS Output, $V_{CM} = V_{RM}$, f_{IN} = 70 MHz, T_A = 25°C.

SNR, SINAD, SFDR vs. V_A



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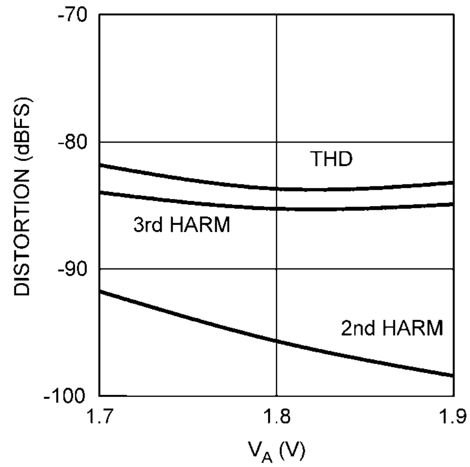
Distortion vs. V_A



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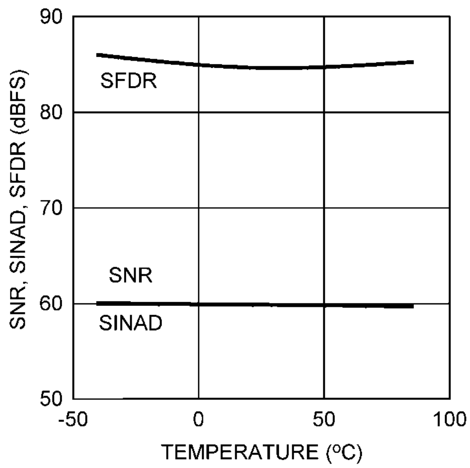
SNR, SINAD, SFDR vs. Temperature



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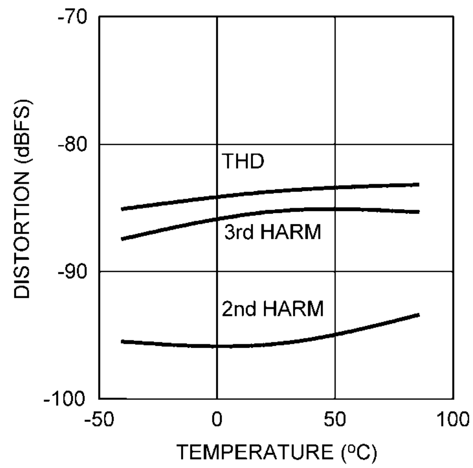
Distortion vs. Temperature



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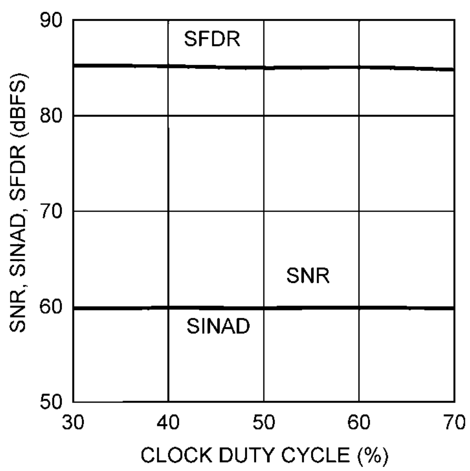
SNR, SINAD, SFDR vs. Clock Duty Cycle, f_{IN} = 10MHz



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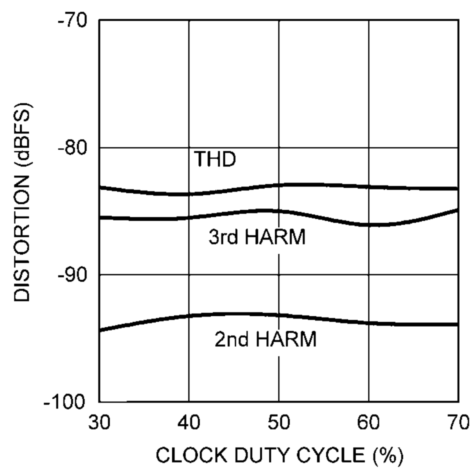
Distortion vs. Clock Duty Cycle, f_{IN} = 10MHz



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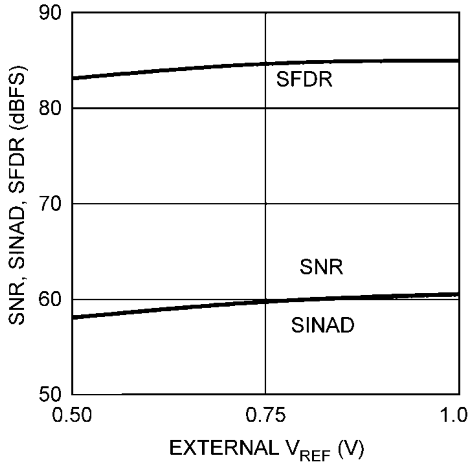
SNR, SINAD, SFDR vs. Ext. Reference Voltage



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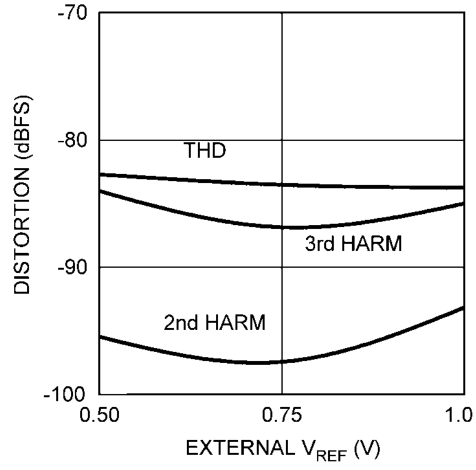
Distortion vs. Ext. Reference Voltage



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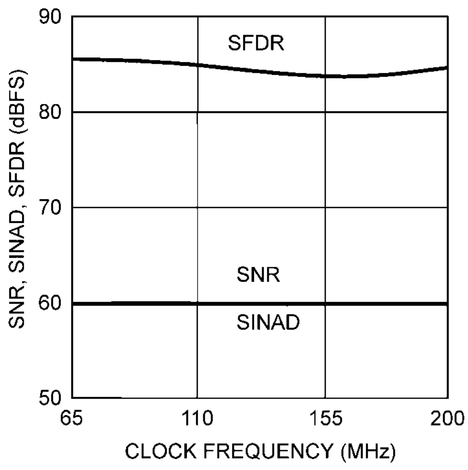
SNR, SINAD, SFDR vs. Clock Frequency



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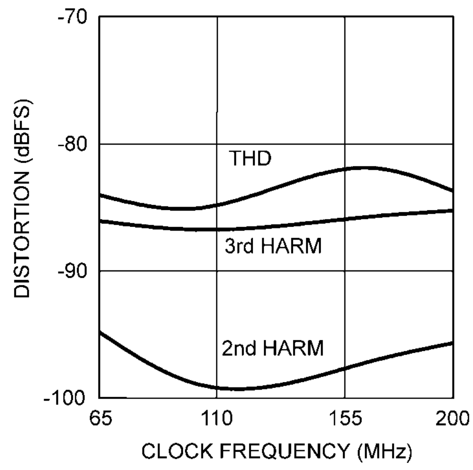
Distortion vs. Clock Frequency



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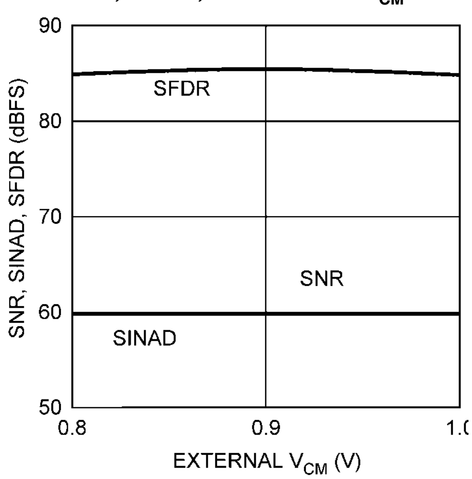
SNR, SINAD, SFDR vs. Ext. V_{CM}



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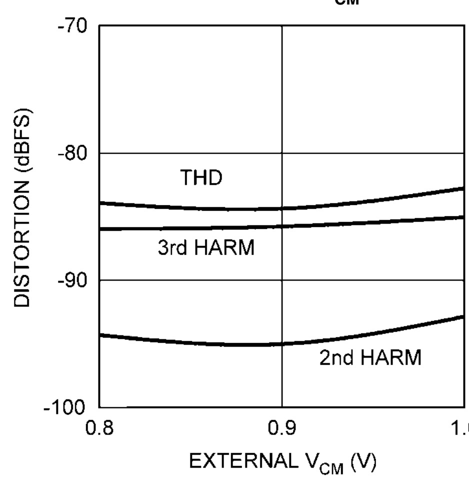
Distortion vs. Ext. V_{CM}



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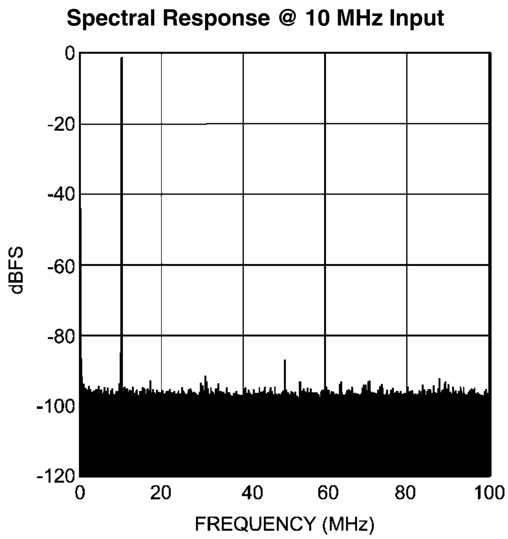

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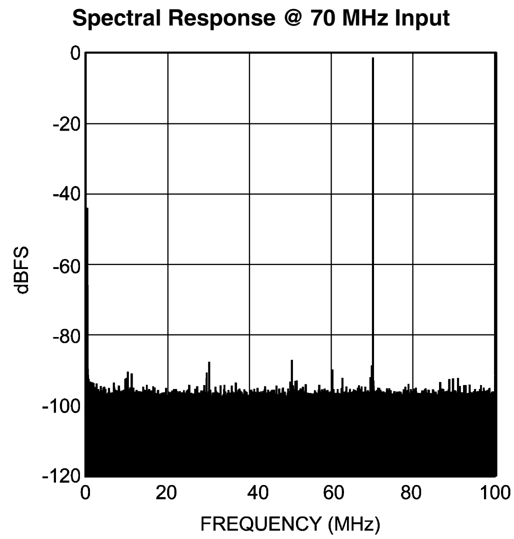

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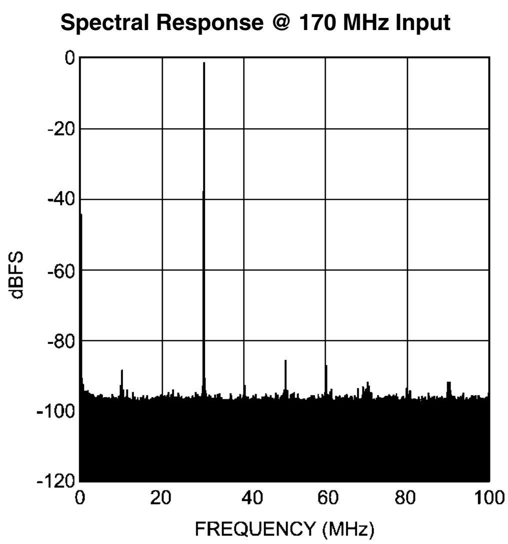

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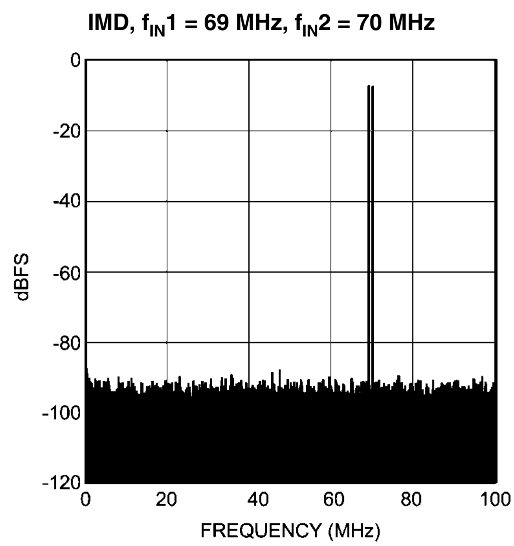

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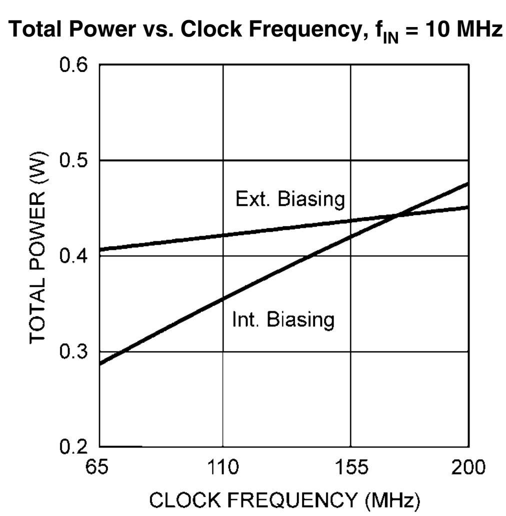

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Functional Description

Operating on a single +1.8V supply, the ADC10DV200 digitizes two differential analog input signals to 10 bits, using a differential pipelined architecture with error correction circuitry and an on-chip sample-and-hold circuit to ensure maximum performance. The user has the choice of using an internal 0.75V stable reference, or using an external 0.75V reference. Any external reference is buffered on-chip to ease the task of driving that pin. Duty cycle stabilization and output data format are selectable using the quad state function DF/DCS pin (pin 20). The output data can be set for offset binary or two's complement.

Applications Information

1.0 OPERATING CONDITIONS

We recommend that the following conditions be observed for operation of the ADC10DV200:

$1.7V \le V_A \le 1.9V$

$1.7V \le V_{DR} \le V_A$

45 MHz $\le f_{CLK} \le$ 200 MHz, with DCS off

65 MHz $\le f_{CLK} \le$ 200 MHz, with DCS on

0.75V internal reference

V_{REF} = 0.75V (for an external reference)

V_{CM} = 0.9V (from V_{RM})

2.0 ANALOG INPUTS

2.1 Signal Inputs

2.1.1 Differential Analog Input Pins

The ADC10DV200 has a pair of analog signal input pins for each of two channels. $V_{IN}+$ and $V_{IN}-$ form a differential input pair. The input signal, V_{IN}, is defined as

$$V_{IN} = (V_{IN}+) - (V_{IN}-)$$

*Figure 4*shows the expected input signal range. Note that the common mode input voltage, V_{CM}, should be 0.9V. Using V_{RM} (pins 5,11) for V_{CM} will ensure the proper input common mode level for the analog input signal. The positive peaks of the individual input signals should each never exceed 2.2V. Each analog input pin of the differential pair should have a maximum peak-to-peak voltage of 1.5V, be 180° out of phase with each other and be centered around V_{CM}.The peak-to-peak voltage swing at each analog input pin should not exceed the 1V or the output data will be clipped.

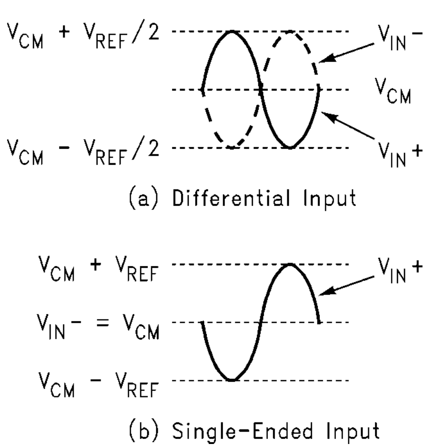

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FIGURE 4. Expected Input Signal Range

For single frequency sine waves the full scale error in LSB can be described as approximately

$$E_{FS} = 1024 \, (1 - \sin (90° + dev))$$

Where dev is the angular difference in degrees between the two signals having a 180° relative phase relationship to each other (see *Figure 5*). For single frequency inputs, angular errors result in a reduction of the effective full scale input. For complex waveforms, however, angular errors will result in distortion.

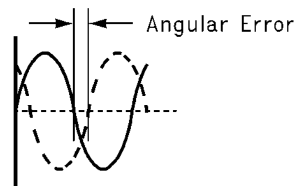

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FIGURE 5. Angular Errors Between the Two Input Signals Will Reduce the Output Level or Cause Distortion

It is recommended to drive the analog inputs with a source impedance less than 100Ω. Matching the source impedance for the differential inputs will improve even ordered harmonic performance (particularly second harmonic).

Table 2 indicates the input to output relationship of the ADC10DV200.

TABLE 2. Input to Output Relationship

V_{IN+}	V_{IN-}	Binary Output	2's Complement Output	
$V_{CM} - V_{REF}/2$	$V_{CM} + V_{REF}/2$	00 0000 0000	10 0000 0000	Negative Full-Scale
$V_{CM} - V_{REF}/4$	$V_{CM} + V_{REF}/4$	01 0000 0000	11 0000 0000	
V_{CM}	V_{CM}	10 0000 0000	00 0000 0000	Mid-Scale
$V_{CM} + V_{REF}/4$	$V_{CM} - V_{REF}/4$	11 0000 0000	01 0000 0000	
$V_{CM} + V_{REF}/2$	$V_{CM} - V_{REF}/2$	11 1111 1111	01 1111 1111	Positive Full-Scale

2.1.2 Driving the Analog Inputs

The V_{IN}+ and the V_{IN}− inputs of the ADC10DV200 have an internal sample-and-hold circuit which consists of an analog switch followed by a switched-capacitor amplifier.

Figure 6 and *Figure 7* show examples of single-ended to differential conversion circuits. The circuit in *Figure 6* works well for input frequencies up to approximately 70MHz, while the circuit in *Figure 7* works well above 70MHz.

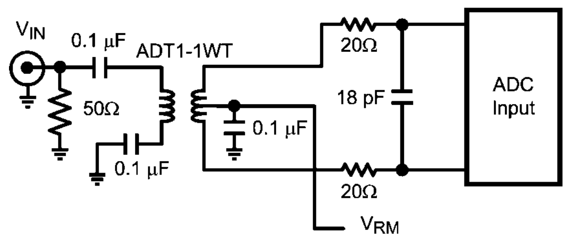


FIGURE 6. Low Input Frequency Transformer Drive Circuit

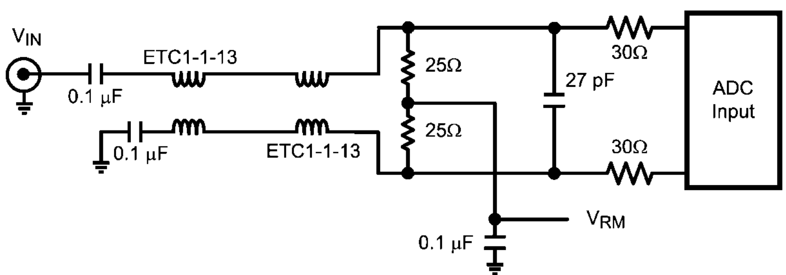


FIGURE 7. High Input Frequency Transformer Drive Circuit

One short-coming of using a transformer to achieve the single-ended to differential conversion is that most RF transformers have poor low frequency performance. A differential amplifier can be used to drive the analog inputs for low frequency applications. The amplifier must be fast enough to settle from the charging glitches on the analog input resulting from the sample-and-hold operation before the clock goes high and the sample is passed to the ADC core.

2.1.3 Input Common Mode Voltage

The input common mode voltage, V_{CM}, should be in the range of 0.8V to 1.0V and be a value such that the peak excursions of the analog signal do not go more negative than ground or more positive than the VA supply. It is recommended to use V_{RM} (pins 5,11) as the input common mode voltage.

If the ADC10DV200 is operated with V_A=1.8V, a resistor of approximately 1KΩ should be used from the V_{RM} pin to AGND. This will help maintain stability over the entire temperature range when using a high supply voltage.

2.2 Reference Pins

The ADC10DV200 is designed to operate with an internal or external voltage reference. The voltage on the V_{REF} pin selects the source and level of the reference voltage. An internal 0.75 Volt reference is used when a voltage between 1.4 V to VA is applied to the V_{REF} pin. An internal 0.5 Volt reference is used when a voltage between 0.2V and AGND is applied to the V_{REF} pin. If a voltage between 0.2V and 1.4V is applied to the V_{REF} pin, then that voltage is used for the reference. SNR will improve without a significant degradation in SFDR for V_{REF}=1.0V. SNR will decrease if V_{REF}=0.5V, yet linearity will be maintained. If using an external reference the V_{REF} pin should be bypassed to ground with a 0.1 µF capacitor close to the reference input pin.

It is important that all grounds associated with the reference voltage and the analog input signal make connection to the ground plane at a single, quiet point to minimize the effects of noise currents in the ground path.

The Reference Bypass Pins (V_{RP}, V_{RM}, and V_{RN}) for channels A and B are made available for bypass purposes. These pins should each be bypassed to AGND with a low ESL (equivalent series inductance) 0.1 µF capacitor placed very close to the pin to minimize stray inductance. A 0.1 µF capacitor should be placed between V_{RP} and V_{RN} as close to the pins as possible. This configuration is shown in *Figure 8*. It is necessary to avoid reference oscillation, which could result in reduced SFDR and/or SNR. V_{RM} may be loaded to 1mA for use as a temperature stable 0.9V reference. The remaining pins should not be loaded.

Smaller capacitor values than those specified will allow faster recovery from the power down mode, but may result in degraded noise performance. Loading any of these pins, other than V_{RM} may result in performance degradation.

The nominal voltages for the reference bypass pins are as follows:

V_{RM} = 0.9 V
V_{RP} = 1.33 V
V_{RN} = 0.55 V

2.3 DF/DCS Pin

Duty cycle stabilization and output data format are selectable using this quad state function pin. When enabled, duty cycle stabilization can compensate for clock inputs with duty cycles ranging from 30% to 70% and generate a stable internal clock, improving the performance of the part. See *Table 1* for DF/DCS voltage vs output format description. DCS mode of operation is limited to 65 MHz ≤ f_{CLK} ≤ 200 MHz.

3.0 DIGITAL INPUTS

Digital CMOS compatible inputs consist of CLK, PD_A, PD_B, and OUTSEL.

3.1 Clock Input

The CLK controls the timing of the sampling process. To achieve the optimum noise performance, the clock input should be driven with a stable, low jitter clock signal in the range indicated in the Electrical Table. The clock input signal should also have a short transition region. This can be achieved by passing a low-jitter sinusoidal clock source through a high speed buffer gate. The trace carrying the clock signal should be as short as possible and should not cross any other signal line, analog or digital, not even at 90°.

If the clock is interrupted, or its frequency is too low, the charge on the internal capacitors can dissipate to the point where the accuracy of the output data will degrade. This is what limits the minimum sample rate.

The clock line should be terminated at its source in the characteristic impedance of that line. Take care to maintain a constant clock line impedance throughout the length of the line. Refer to Application Note AN-905 for information on setting characteristic impedance. It is highly desirable that the the source driving the ADC clock pins only drive that pin.

The duty cycle of the clock signal can affect the performance of the A/D Converter. Because achieving a precise duty cycle is difficult, the ADC10DV200 has a Duty Cycle Stabilizer.

4.0 DIGITAL OUTPUTS

Digital outputs consist of the LVDS signals D0-D9, OR, and DRDY.

The ADC10DV200 has 12 LVDS compatible data output pins: 10 data output pins corresponding to the converted input value, a data ready (DRDY) signal that should be used to capture the output data and an over-range indicator (OR) which is set high when the sample amplitude exceeds the 10-Bit conversion range. Valid data is present at these outputs while the PD pin is low. A-Channel data should be captured and latched with the rising edge of the DRDY signal and B-Channel data should be captured and latched with the falling edge of DRDY.

To minimize noise due to output switching, the load currents at the digital outputs should be minimized. This can be achieved by keeping the PCB traces less than 2 inches long; longer traces are more susceptible to noise. The characteristic impedance of the LVDS traces should be 100Ω, and the effective capacitance < 10pF. Try to place the 100Ω termination resistor as close to the receiving circuit as possible. (See *Figure 8*)

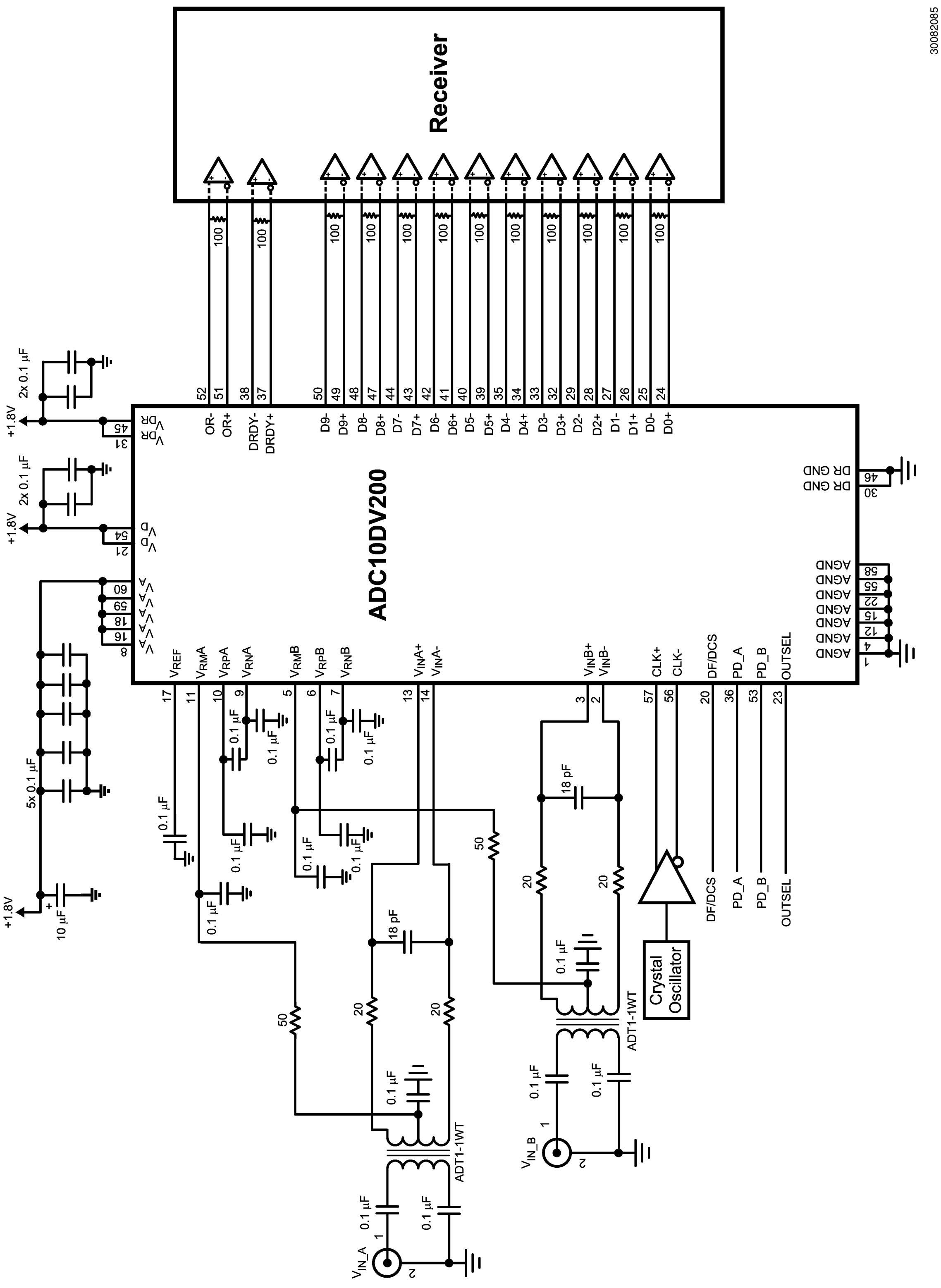


FIGURE 8. Application Circuit

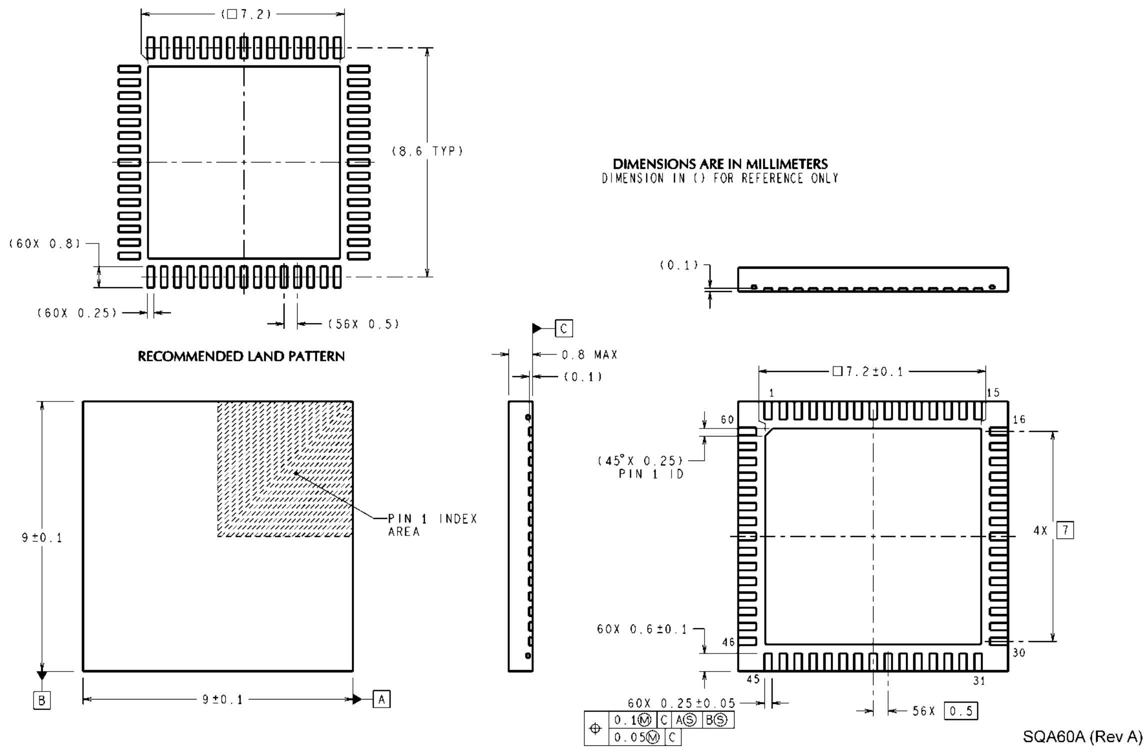
5.0 POWER SUPPLY CONSIDERATIONS

The power supply pins should be bypassed with a 0.1 µF capacitor and with a 100 pF ceramic chip capacitor close to each power pin. Leadless chip capacitors are preferred because they have low series inductance.

As is the case with all high-speed converters, the ADC10DV200 is sensitive to power supply noise. Accordingly, the noise on the analog supply pin should be kept below 100 mV_{P-P}.

No pin should ever have a voltage on it that is in excess of the supply voltages, not even on a transient basis. Be especially careful of this during power turn on and turn off.

Physical Dimensions inches (millimeters) unless otherwise noted



TOP View..............................SIDE View.............................BOTTOM View
60-Lead LLP Package
Ordering Numbers:
ADC10DV200CISQ
NS Package Number SQA60A

Notes

Notes

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Data Converters	www.national.com/adc	Samples	www.national.com/samples
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LVDS	www.national.com/lvds	Packaging	www.national.com/packaging
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage Reference	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Solutions	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
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