PROCESS

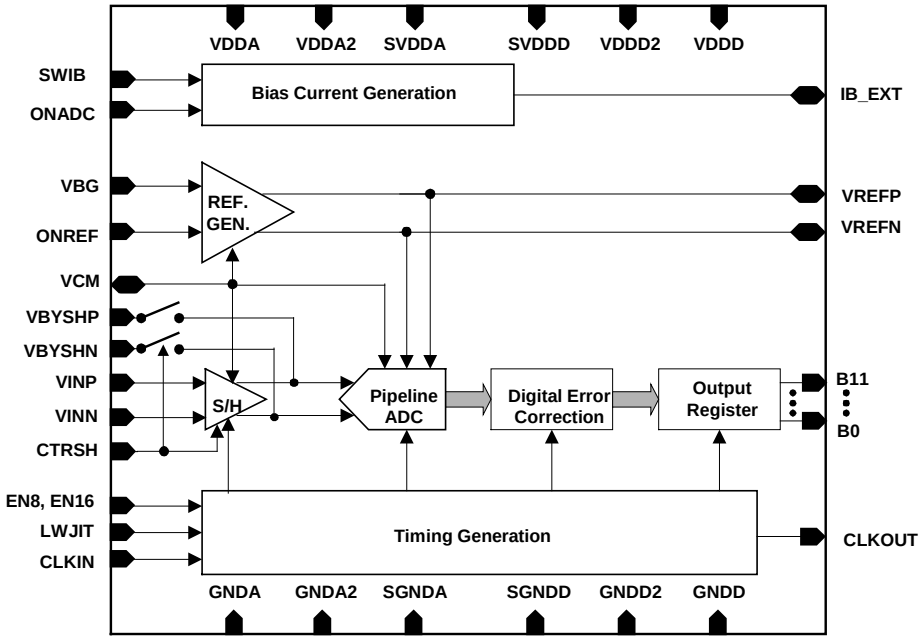
C35B3 (0.35um)

DESCRIPTION

The ADC1220 is a high-speed pipeline ADC core cell achieving sampling rates up to 20 MS/s. A S/H circuit is built-in to provide low jitter noise and a fully differential input. The reference voltages are internally generated from a bandgap reference that must be supplied to the cell or must be supplied externally to the cell. A power down capability is included for very low power dissipation in stand-by mode.

FEATURES

- Small Area: 3.87 mm^2
- Size x = 2261.5 µm y = 1711.55 µm
- Supply Voltage 3.0 - 3.6 V
- Junction Temp. Range: –40 to +125 °C
- Resolution 12-Bit
- Maximum Sampling Rate 20 MS/s
- Sample and Hold Input Stage
- 2 Vpp or 3 Vpp Input Signal Range
- Fully Differential Input
- Power Dissipation 380 mW
- Power Down Mode



TECHNICAL DATA

(Tjunction = –40 to 125 °C, VDDA = VDD = +3.0 V to +3.6 V, fclk = 20 MHz, VCM = VDDA/2, VREFP and VREFN or VBG as specified, unless otherwise specified)

DC ACCURACY

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Resolution (No missing Code)		12	12	12	Bit
DNL	Differential Linearity Error		–0.9	±0.5	+1	LSB
INL	Integral Linearity Error		–2.0	±0.5	+2.0	LSB
OFF	Offset Error		–10	0	10	LSB
GAINERR	Gain Error		+15	18	+50	LSB

REFERENCE CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VBG	ext. Bandgap Reference Voltage	Op.Mode 1		1.25 [1]	1.875 [2]	V
VCM	Common Mode Voltage		1.5	VDDA/2	1.8	V
VREFP	Pos. Reference Voltage	Op.Mode 4		VCM+0.4VBG		V
VREFN	Neg. Reference Voltage			VCM-0.4VBG		V
VREF	Difference between VREFP and VREFN		1	1 [1]	1.5 [2]	V
R_{bg}	ext. Bandgap Ref. Impedance	Op.Mode 1		10		kΩ
I_{bg}	ext. Bandgap Ref. Input Current	Op.Mode 1		48.0 [3] / 239.0 [4]		µA
C_{cm}	Comm. Mode Impedance			100		pF
R_{refp}	Pos. Reference Impedance	Op.Mode 4		4.3		kΩ
C_{refp}	(For external VREF generation)			30		pF
R_{refn}	Neg. Reference Impedance	Op.Mode 4		4.3		kΩ
C_{refn}	(For external VREF generation)			30		pF

ANALOG INPUT

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Vind	Diff. Input Voltage Range, related to VCM		–VREF [5]		VREF [5]	V
R_{in}	Input Impedance		100			MΩ
C_{in}				4.5		pF
F_{inmax}	Max. Input Signal Frequency				10	MHz

[1] For 2 Vpp input signal range.

[2] For 3 Vpp input signal range.

[3] VBG = 1.25 V and VDDA = 3.3 V

[4] VBG = 1.875 V and VDDA = 3.3 V

[5] It is strongly recommended not to overdrive the inputs of the ADC1220.

AC ACCURACY (2 Vpp input signal range)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
THD	Total Harmonic Distortion	f_{in} = 180 kHz		–83.00		dB
THD	Total Harmonic Distortion	f_{in} = 4.5 MHz		–83.00		dB
THD	Total Harmonic Distortion	f_{in} = 9.5 MHz		–81.50		dB
SFDR	Spurious Free Dynamic Range	f_{in} = 180 kHz		80.50		dB
SFDR	Spurious Free Dynamic Range	f_{in} = 4.5 MHz		80.00		dB
SFDR	Spurious Free Dynamic Range	f_{in} = 9.5 MHz		76.00		dB
SNR	Signal to Noise Ratio	f_{in} = 180 kHz		68.80		dB
SNR	Signal to Noise Ratio	f_{in} = 4.5 MHz		67.50		dB
SNR	Signal to Noise Ratio	f_{in} = 9.5 MHz		66.00		dB
SINAD	Signal to (Noise+Dist.) Ratio	f_{in} = 180 kHz		68.70		dB
SINAD	Signal to (Noise+Dist.) Ratio	f_{in} = 4.5 MHz		67.40		dB
SINAD	Signal to (Noise+Dist.) Ratio	f_{in} = 9.5 MHz		65.85		dB
ENOB	Effective Number of Bits	f_{in} = 180 kHz		11.10		Bit
ENOB	Effective Number of Bits	f_{in} = 4.5 MHz		10.90		Bit
ENOB	Effective Number of Bits	f_{in} = 9.5 MHz		10.65		Bit
TT-IMD	Two-Tone third order Intermodulation Distortion	f_{in1} = 4 MHz [1)] f_{in2} = 4.5 MHz		–80.00		dBc
TT-SFDR	Two-Tone Spurious Free Dynamic Range	f_{in1} = 4 MHz [1)] f_{in2} = 4.5 MHz		77.80		dBc
FPBW	Full Power Bandwidth			50		MHz

AC ACCURACY (3 Vpp input signal range)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
THD	Total Harmonic Distortion	f_{in} = 180 kHz		–82.60		dB
THD	Total Harmonic Distortion	f_{in} = 4.5 MHz		–78.90		dB
THD	Total Harmonic Distortion	f_{in} = 9.5 MHz		–76.40		dB
SFDR	Spurious Free Dynamic Range	f_{in} = 180 kHz		82.40		dB
SFDR	Spurious Free Dynamic Range	f_{in} = 4.5 MHz		80.30		dB
SFDR	Spurious Free Dynamic Range	f_{in} = 9.5 MHz		76.60		dB
SNR	Signal to Noise Ratio	f_{in} = 180 kHz		70.40		dB
SNR	Signal to Noise Ratio	f_{in} = 4.5 MHz		68.50		dB
SNR	Signal to Noise Ratio	f_{in} = 9.5 MHz		66.50		dB
SINAD	Signal to (Noise+Dist.) Ratio	f_{in} = 180 kHz		70.10		dB
SINAD	Signal to (Noise+Dist.) Ratio	f_{in} = 4.5 MHz		68.10		dB
SINAD	Signal to (Noise+Dist.) Ratio	f_{in} = 9.5 MHz		66.00		dB
ENOB	Effective Number of Bits	f_{in} = 180 kHz		11.35		Bit
ENOB	Effective Number of Bits	f_{in} = 4.5 MHz		11.00		Bit
ENOB	Effective Number of Bits	f_{in} = 9.5 MHz		10.67		Bit
TT-IMD	Two-Tone third order Intermodulation Distortion	f_{in1} = 4 MHz [1)] f_{in2} =4.5 MHz		–75.50		dBc
TT-SFDR	Two-Tone Spurious Free Dynamic Range	f_{in1} = 4 MHz [1)] f_{in2} = 4.5 MHz		75.50		dBc
FPBW	Full Power Bandwidth			50		MHz

[1)] Both signals, f_{in1} and f_{in2}, have an amplitude of –7 dBc full scale

DIGITAL INPUTS AND OUTPUTS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VDD	Pos. digital Supply Voltage	VDD = VDDA	3.0	3.3	3.6	V
VSS	Neg. digital Supply Voltage	GND = GNDA	0	0	0	V
VIL	Digital Input Level		GND		0.3 VDD	V
VIH			0.7 VDD		VDD	V
VOL	Digital Output Level			GND		V
VOH				VDD		V
B[11:0]	Output Code	Vind = –VREF		000		HEX
		Vind = VREF		FFF		HEX

POWER REQUIREMENTS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VDDA	Pos. analog Supply Voltage	VDD = VDDA	3.0	3.3	3.6	V
VSSA	Neg. analog Supply Voltage	GND = GNDA	0	0	0	V
IDDD [1)]	Supply Current Digital	Op. Mode 1		3.4	6.8	mA
IDDA [1)]	Supply Current Analog	Op. Mode 1		111.7	223.4	mA
Psup [1)]	Supply Power Consumption	Op. Mode 1		380	760	mW
Pdiss_tot [1)]	Total Power Dissipation Powerup Mode	Op. Mode 1		380	760	mW
IDDD [2)]	Supply Current Digital	Op. Mode 4		3.4	6.8	mA
IDDA [2)]	Supply Current Analog	Op. Mode 4		92	184	mA
Psup [2)]	Supply Power Consumption	Op. Mode 4		315	630	mW
IREF [2)]	Reference Current	Op. Mode 4		1	2	mA
Pdiss_tot [2)]	Total Power Dissipation Powerup Mode	Op. Mode 4		318	636	mW
Pdiss_pd [3)]	Power Consumption Power Down Mode	Op. Mode 0		180	360	µW

TIMING CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
fclk	CLK Frequency		1		20	MHz
1/Ts	Sampling Rate			fclk		MS/sec
Jclk	Clock Jitter				$\frac{4 \cdot 10^{-5}}{f_{in}}$	psec
Tsd	Clock falling edge to sampling instant delay			1.6		nsec
Tod	Clock falling edge to data out delay			10.5		nsec
Tclkd	Input Clock falling edge to output Clock delay			9.5		nsec
	Clock duty cycle		47.5	50	52.5	%
	Data Latency			5		CLK cycle
	Power Up Delay [4)]			40		CLK cycle

1) In Op. Mode 1 (internal references) with VREF = 1 V at 20 MHz clock frequency.

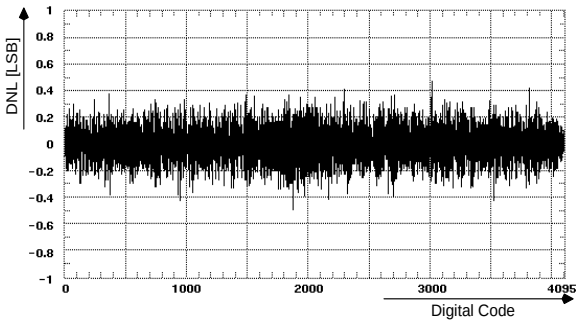
2) In Op. Mode 4 (external references) with VREF = 1 V at 20 MHz clock frequency.

3) After 10 µs power down.

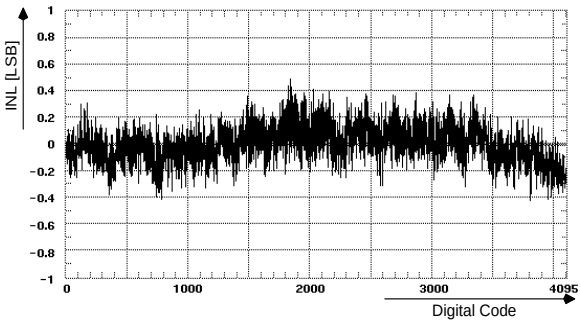
4) The digital output codes of the ADC are not valid during the first few clock cycles after a power up.

TYPICAL PERFORMANCE CHARACTERISTICS

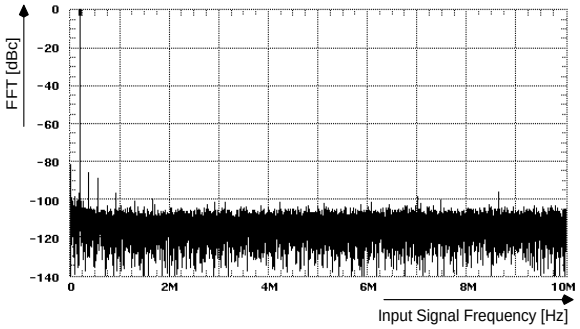
(T = 25 °C, VDDA = VDD = +3.3 V, fclk = 20 MHz, VBG = 1.25 V, VCM = VDDA/2, Op. Mode 1, unless otherwise specified)



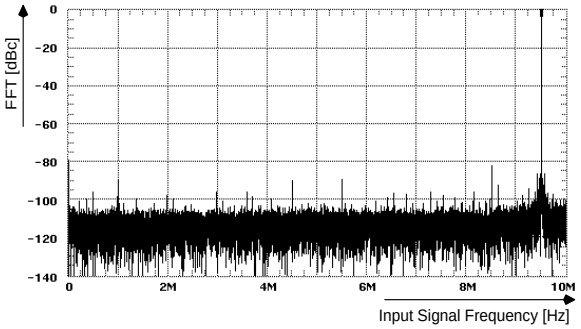
DNL @ 180 kHz



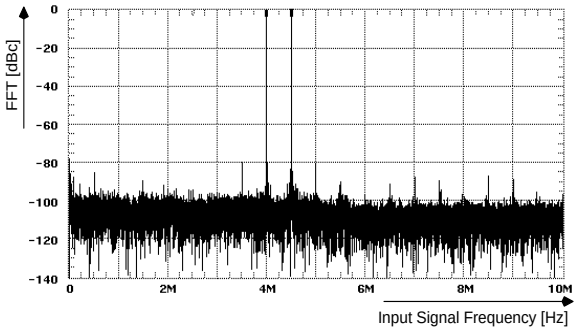
INL @ 180 kHz



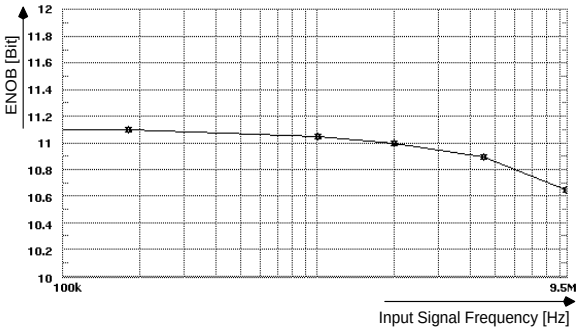
Spectrum @ 180 kHz [1)]



Spectrum @ 9.5 MHz [1) 2)]



Two-Tone IMD @ 4.0 MHz and 4.5 MHz [1) 3)]



ENOB vs. Input Signal Frequency

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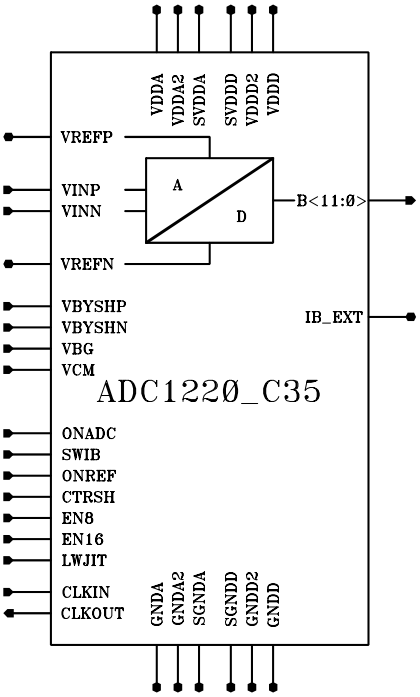
1) The spectrum consists of 16384 pins.

2) Measured with a 9.5 MHz band-pass filter

3) Measured with a 4.5 MHz low-pass filter.

SYMBOL



THEORY OF OPERATION

The ADC1220 is a low-power 12-bit ADC capable of sampling at 20 MS/s. It uses a fully differential pipelined architecture with a first 3.5-bit stage, followed by seven 1.5-bit per stage and digital error correction to achieve improved linearity performance. A dedicated wide-band input sample-and-hold amplifier (S/H) is built-in to provide low-jitter, sub-sampling capability with inherent frequency down-conversion and a fully differential input. The raw digital words are synchronized by a chain of delay stages and overlapped and processed by the digital error correction logic to produce the 12-bit digital output code.

PINLIST

Pin	Function	I/O	Type
VINP	Pos. Input Voltage	I	Analog
VINN	Neg. Input Voltage	I	Analog
VBYSHP	S&H Bypass Pos. Input Voltage	I	Analog
VBYSHN	S&H Bypass Neg. Input Voltage	I	Analog
VCM	Input for Common Mode Voltage	I	Analog
VREFP	Output or bypass of Internal Pos. Reference Voltage	I/O	Analog
VREFN	Output or bypass of Internal Neg. Reference Voltage	I/O	Analog
VBG	Input for Bandgap Reference Voltage	I	Analog
IB_EXT	Output for monitoring internal bias current generation when SWIB = "1" or input for injection of external bias current (10µA) when SWIB = "0"	I/O	Analog
CLKIN	Clock Input	I	Digital
CLKOUT	Clock Output	O	Digital
B11 to B0	Digital Output Bits (B11 = MSB, B0 = LSB)	O	Digital
ONADC	Power Down Input for ADC (ONADC = 1 ⇔ normal operation)	I	Digital
ONREF	Power Down Input for Reference Generator (ONREF = 1 ⇔ normal operation)	I	Digital
CTRSH	S&H Power Down and Bypass (CTRSH = 0 ⇔ normal operation)	I	Digital
SWIB	Bias current control pin; if High, the ADC uses internal bias current; otherwise it enables the external current input.	I	Digital
LWJIT	Jitter Reduction (LWJIT = 0 ⇔ normal operation)	I	Digital
EN8	Enables Decimation factor of 8 (EN8 = 0 ⇔ normal operation)	I	Digital
EN16	Enables Decimation factor of 16 (EN16 = 0 ⇔ normal operation)	I	Digital
VDDA	Analog pos. Power Supply	I	Supply
GNDA	Analog neg. Power Supply	I	Supply
VDDA2	Secondary pos. Analog Power Supply	I	Supply
VGNDA2	Secondary neg. Analog Power Supply	I	Supply
SVDDA	Substrate pos. Analog Power Supply	I	Supply
SGNDA	Substrate neg. Analog Power Supply	I	Supply
VDDD	Digital pos. Power Supply	I	Supply
GNDD	Digital neg. Power Supply	I	Supply
VDDD2	Secondary Digital pos. Power Supply	I	Supply
GNDD2	Secondary Digital neg. Power Supply	I	Supply
SVDDD	Substrate Digital pos. Power Supply	I	Supply
SGNDD	Substrate Digital neg. Power Supply	I	Supply

OPERATING MODES

The modes of operation are summarized in the table bellow, and described in detail as follows.

		Configuration						
Mode	**Objective**	**ONADC**	**SWIB**	**ONREF**	**CTRSH**	**EN8**	**EN16**	**LWJIT**
0	Complete Power Down	0	X	X	X	X	X	X
1	Normal conversion	1	1	1	0	0	0	0
2	Normal conversion with external VREF	1	1	0	0	0	0	0
3	Normal conversion with external Ibias	1	0	1	0	0	0	0
4	Normal conversion with external VREF and Ibias	1	0	0	0	0	0	0
5	Modes 1 to 4 with S&H bypass	1	X	X	1	0	0	0
6	Modes 1 to 5 with decimation by a factor of 8	1	X	X	X	1	0	0
7	Modes 1 to 5 with decimation by a factor of 16	1	X	X	X	0	1	0
8	Modes 1 to 7 with clock jitter reduction	1	X	X	X	X	X	1

Mode 0 - Power Down

In this mode all the circuitry is in power-down. The power dissipation is reduced to a minimum value.

Mode 1 - Normal Conversion

This is the normal conversion mode of the converter. The external bandgap reference voltage VBG determines the values of the reference voltages VREFP and VREFN. The bias current is internally generated and the reference voltages are internally buffered. The common mode voltage VCM must be supplied externally.

Mode 2 through Mode 5 - Conversion Mode with different Bypassing options

These conversion modes allow different bypassing options for the bias current generator, for the buffer of the reference voltage and the S&H. In case of S&H bypass the input signal must be fully differential because of the pipeline fully differential architecture.

Modes 6 and 7 - Conversion Mode with different Decimation factors

These conversion modes allow output data decimation factors of 8 and 16 with any of the previous modes, in order to reduce the digital Output Pads switching noise.

Mode 8 - Conversion Mode with Clock jitter reduction

This conversion mode allows the test of an internal clock with reduced jitter with any of the previous modes.

POWER SUPPLIES

The converter requires a single +3.3 V power supply. The supplies for analog and digital are separated. For maximum noise immunity it is recommended to wire them on chip to separated pins, especially when the block is embedded in a large digital circuit. The supplies may then be connected together on PC-board level.
The proper use of blocking capacitors in the application is important!

REFERENCE VOLTAGES

If ONREF is set to high the converter needs an external bandgap reference VBG that defines the dynamic range of the input signal as described in the technical data section. If ONREF is set to low the external voltage references VREFP and VREFN define the dynamic range of the input signal. The proper use of blocking capacitors in the application is important!

SYSTEM REQUIREMENTS

The ADC is sensitive to ground noise. So all parts of the whole system except the ADC should be quiet during the conversions. To minimize ground noise coming from digital output pads the connection of a series resistor should be used to limit the switching current. In the test circuit a series resistor of 1 kΩ is used for the digital output bus.

CONVERSION MODE

Fully Differential Mode

It is recommended to use the ADC1220 as a Fully Differential Converter. Both inputs VINP and VINN should be balanced around VCM.

CODE TABLES

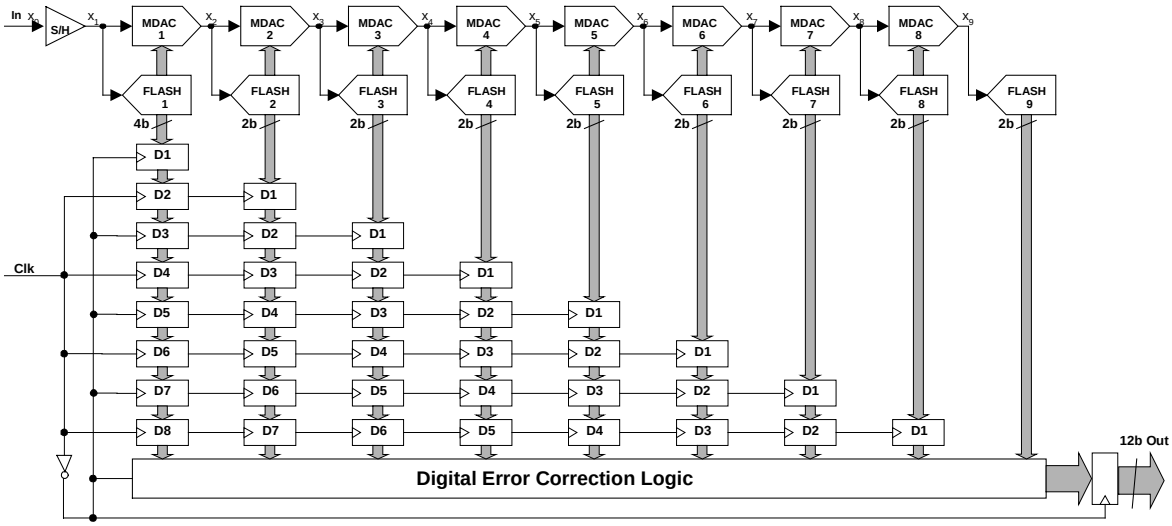
The digital representation of the data bus in both conversion modes is described in the following table.

$$VREF = VREFP - VREFN, \qquad 1LSB = \frac{VREFP - VREFN}{4096}$$

Offset Binary

Output Code	Input Voltage: VIN-VINB
1111 1111 1111	2047 LSB ... VREF
1111 1111 1110	2046 LSB ... 2047 LSB
...	...
1000 0000 0001	1 LSB ... 2 LSB
1000 0000 0000	0 ... 1 LSB
0111 1111 1111	–1 LSB ... 0
0111 1111 1110	–2 LSB ... –1 LSB
...	...
0000 0000 0001	–2047 LSB ... –2046 LSB
0000 0000 0000	–VREF ... –2047 LSB

FUNCTIONAL BLOCK DIAGRAM



TIMING DIAGRAM OF ADC1220

The sampling rate of the ADC1220 is defined by the frequency of the CLK signal. The input signal voltage of the ADC is sampled in the falling edge of CLK. As the conversion stages operate in a staggered fashion in alternate phases of CLK, the duty-cycle of this signal must be 50%. The results are latched in the output register on the falling edge of CLK, with a latency of 5 CLK periods. The conversion timing is shown in Diagram 1.

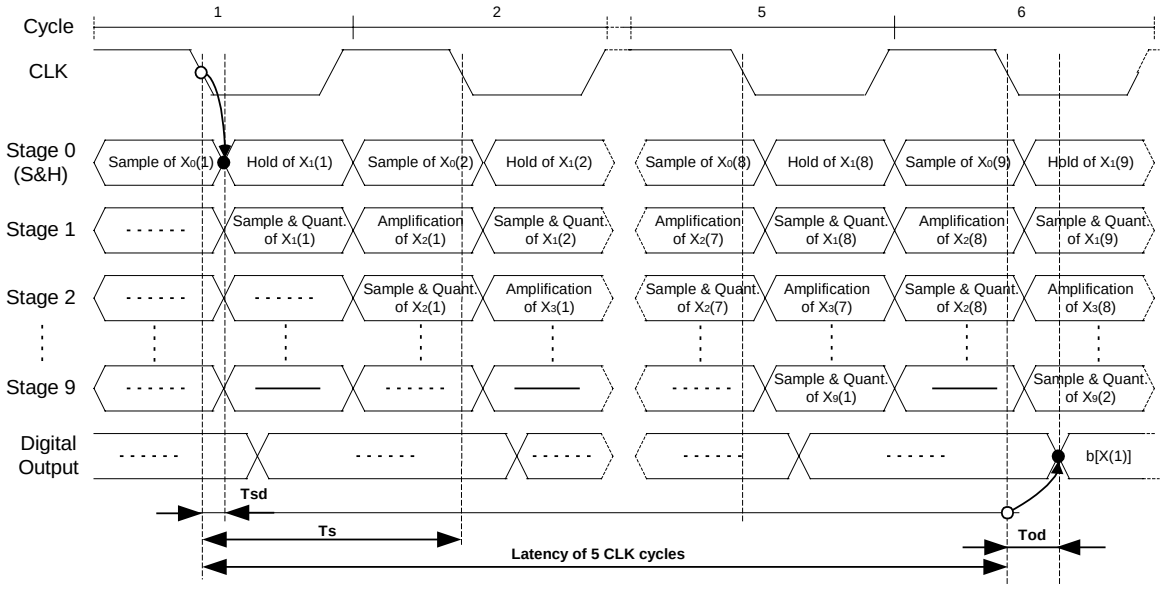
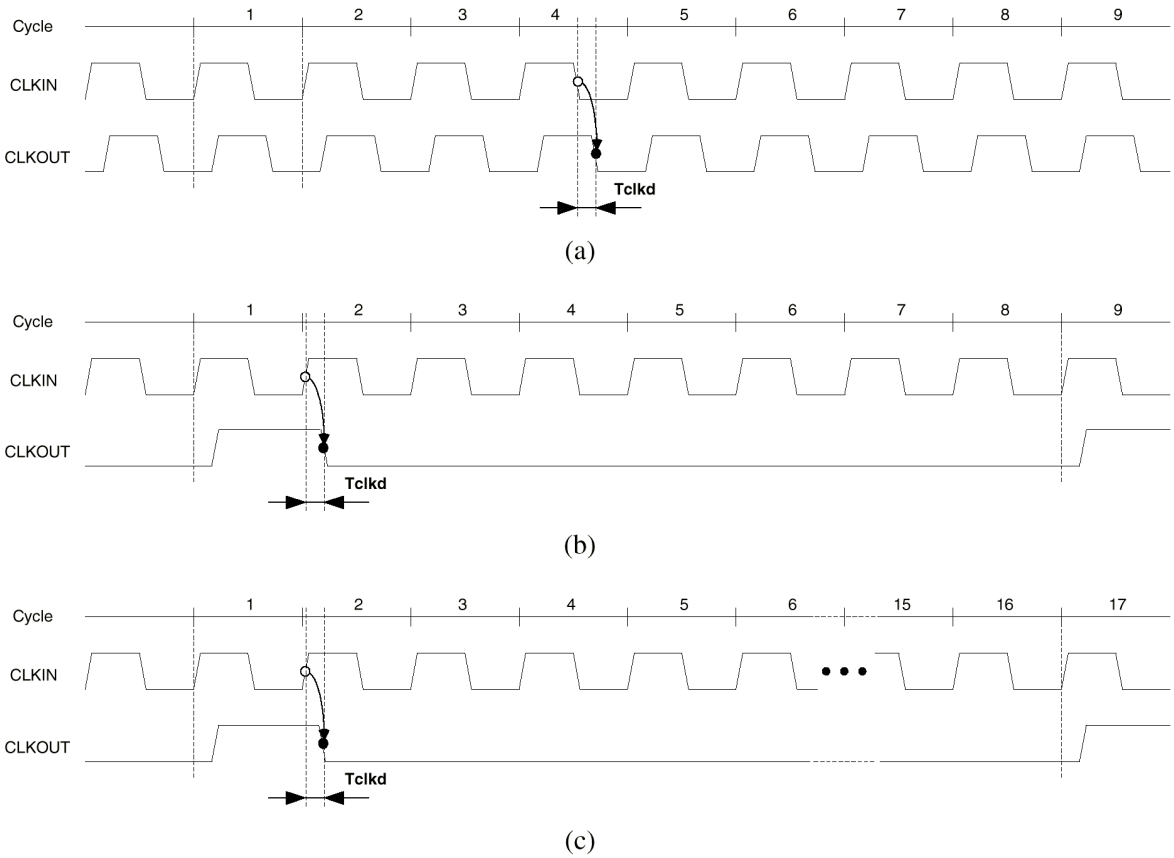


Diagram 1: Timing of the pipelining operation

The Diagram 2 presents the timing of the CLKOUT signal in normal operation (mode 0) and with decimation factors of 8 (mode 5) and 16 (mode 6). In all test modes that do not have a decimation factor specified, the CLKOUT signal is identical to that in normal operation mode.



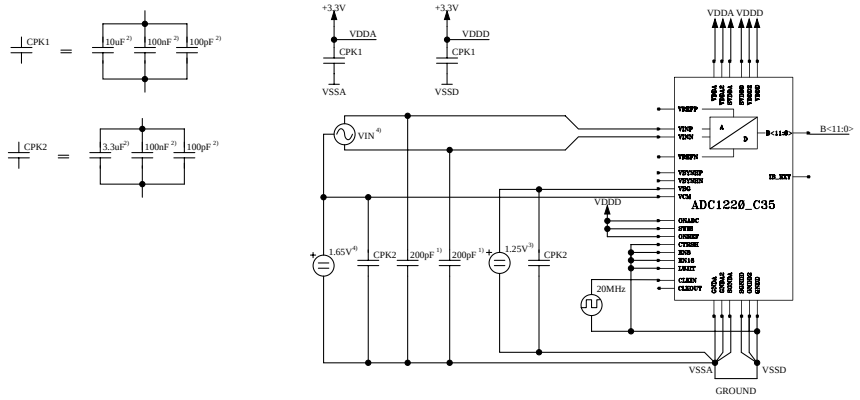
Timing Diagram 2: Timing of the CLKOUT signal operation in normal operation (a) and with decimation factor of 8 (b) and of 16 (c)

TYPICAL APPLICATION

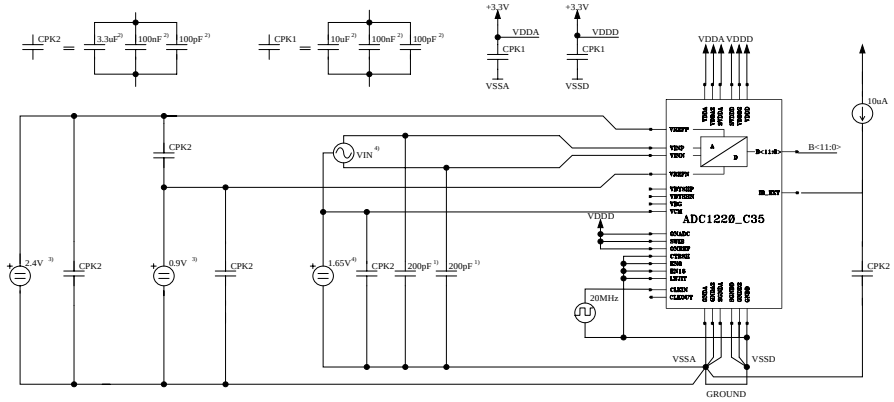
The ADC1220 is targeted for general purpose sampling ADC functions where high-speed conversion rates and medium precision are of critical importance.

APPLICATION

- Video
- Imaging
- Data acquisition systems
- High-speed data transmission
- Communications



Configuration: Op. Mode 1 at 20 MS/sec, 2 Vpp input signal range



Configuration: Op. Mode 4 at 20 MS/sec, 3 Vpp input signal range

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1) The value of the capacitor depends on the input frequency.
For SMD capacitors use the type NPO and for normal capacitors use the type MKT for best performance.

2) For SMD capacitors use the type NPO and for normal capacitors use the type MKT for best performance.

3) The accuracy of both reference voltages must be higher than the retion of the ADC. In typical applications both voltages are filtered by a second order low pass filter (f_c = 5 Hz) and buffered with an AD711.

4) The accuracy of both input voltages must be higher than the resolution of the ADC. In typical applications both voltages are filtered. For low inncies the input voltages are buffered with a AD8138 and for high frequencies a transformer is used.

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