National Semiconductor

ADVANCE INFORMATION
September 2007

ADC12DS080/ADC12DS105
Dual 12-Bit, 80/105 MSPS A/D Converter with Serial LVDS Outputs

General Description

NOTE: This is Advance Information for products currently in development. ALL specifications are design targets and are subject to change.

The ADC12DS080 and ADC12DS105 are high-performance CMOS analog-to-digital converters capable of converting two analog input signals into 12-bit digital words at rates up to 80/105 Mega Samples Per Second (MSPS) respectively. The digital outputs are serialized and provided on differential LVDS signal pairs. These converters use a differential, pipelined architecture with digital error correction and an on-chip sample-and-hold circuit to minimize power consumption and the external component count, while providing excellent dynamic performance. A unique sample-and-hold stage yields a full-power bandwidth of 1 GHz. The ADC12DS080/105 may be operated from a single +3.0 or 3.3V power supply and consumes low power. A power-down feature reduces the power consumption to very low levels while still allowing fast wake-up time to full operation. The differential inputs accept a 2V full scale differential input swing. A stable 1.2V internal voltage reference is provided, or the ADC12DS080/105 can be operated with an external 1.2V reference. Output data format (offset binary versus 2's complement) and duty cycle stabilizer are pin-selectable. The duty cycle stabilizer maintains performance over a wide range of clock duty cycles.

The ADC12DS080/105 is available in a 60-lead LLP package and operates over the industrial temperature range of –40°C to +85°C.

Features

- 1 GHz Full Power Bandwidth
- Clock Duty Cycle Stabilizer
- Single +3.0 or 3.3V supply operation
- Serial LVDS Outputs
- Serial Control Interface
- Overrange outputs
- 60-pin LLP package, (9x9x0.8mm, 0.5mm pin-pitch)

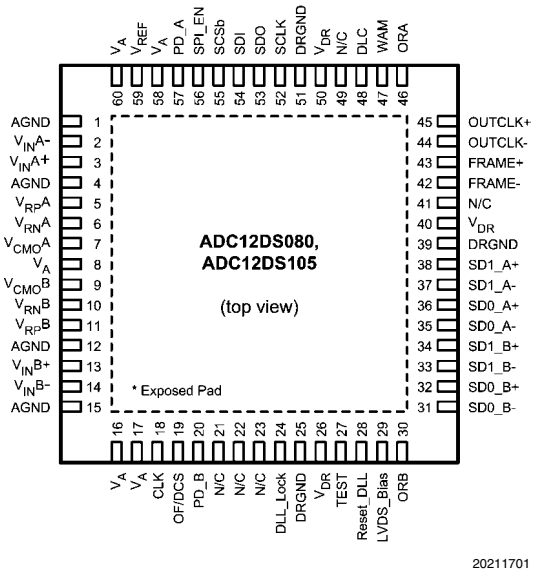
Key Specifications

- **For ADC12DS105**
- Resolution — 12 Bits
- Conversion Rate — 105 MSPS
- SNR (f_{IN} = 240 MHz) — 67 dBFS (typ)
- SFDR (f_{IN} = 240 MHz) — 83 dBFS (typ)
- Full Power Bandwidth — 1 GHz (typ)
- Power Consumption — 1 W (typ)

Applications

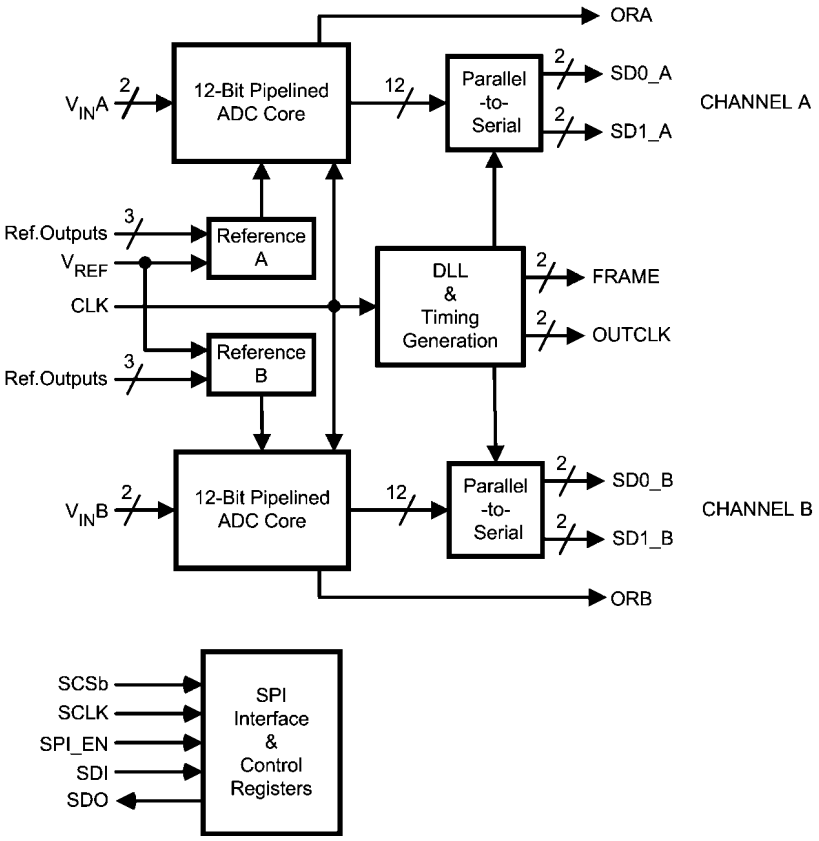
- High IF Sampling Receivers
- Wireless Base Station Receivers
- Test and Measurement Equipment
- Communications Instrumentation
- Portable Instrumentation

Connection Diagram



20211701

Block Diagram

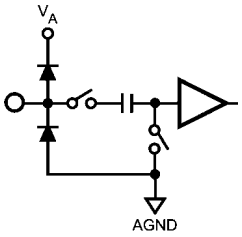
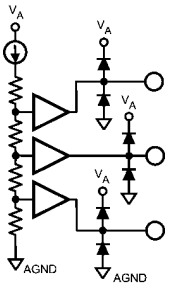
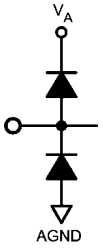
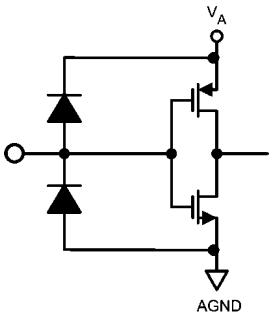
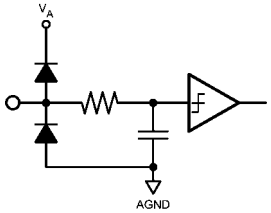


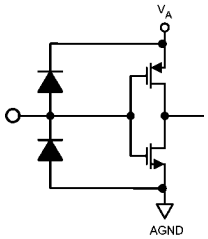
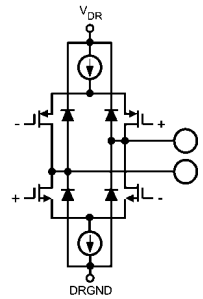
20211702

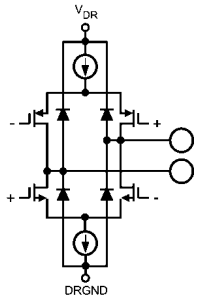
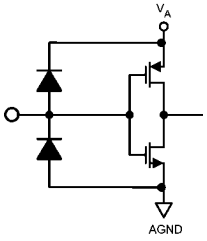
Ordering Information

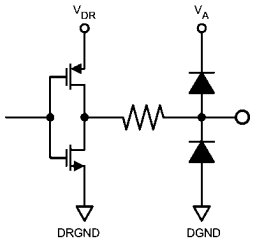
Industrial ($-40°C \leq T_A \leq +85°C$)	Package
ADC12DS080CISQ	60 Pin LLP
ADC12DS105CISQ	60 Pin LLP

Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
ANALOG I/O			
3 13	$V_{IN}A+$ $V_{IN}B+$		Differential analog input pins. The differential full-scale input signal level is $2V_{P-P}$ with each input pin signal centered on a common mode voltage, V_{CM}.
2 14	$V_{IN}A-$ $V_{IN}B-$		
5 11	$V_{RP}A$ $V_{RP}B$		These pins should each be bypassed to AGND with a low ESL (equivalent series inductance) 0.1 µF capacitor placed very close to the pin to minimize stray inductance. An 0201 size 0.1 µF capacitor should be placed between V_{RP} and V_{RN} as close to the pins as possible, and a 1 µF capacitor should be placed in parallel. V_{RP} and V_{RN} should not be loaded. V_{CMO} may be loaded to 1mA for use as a temperature stable 1.5V reference. It is recommended to use V_{CMO} to provide the common mode voltage, V_{CM}, for the differential analog inputs.
7 9	$V_{CMO}A$ $V_{CMO}B$		
6 10	$V_{RN}A$ $V_{RN}B$		
59	V_{REF}		Reference Voltage. This device provides an internally developed 1.2V reference. When using the internal reference, V_{REF} should be decoupled to AGND with a 0.1 µF and a 1µF, low equivalent series inductance (ESL) capacitor. This pin may be driven with an external 1.2V reference voltage. This pin should not be used to source or sink current.
29	LVDS_Bias		LVDS Driver Bias Resistor is applied from this pin to Analog Ground. The nominal value is 3.6KΩ
DIGITAL I/O			
18	CLK		The clock input pin. The analog inputs are sampled on the rising edge of the clock input.
28	Reset_DLL		Reset_DLL input. This pin is normally low. If the input clock frequency is changed abruptly, the internal timing circuits may become unlocked. Cycle this pin high for 1 microsecond to re-lock the DLL. The DLL will lock in several microseconds after Reset_DLL is asserted.
19	OF/DCS		This is a four-state pin controlling the input clock mode and output data format. OF/DCS = V_A, output data format is 2's complement without duty cycle stabilization applied to the input clock OF/DCS = AGND, output data format is offset binary, without duty cycle stabilization applied to the input clock. OF/DCS = (2/3)*V_A, output data is 2's complement with duty cycle stabilization applied to the input clock OF/DCS = (1/3)*V_A, output data is offset binary with duty cycle stabilization applied to the input clock. Note: This signal has no effect when SPI_EN is high and the SPI interface is enabled.

Pin No.	Symbol	Equivalent Circuit	Description
57 20	PD_A PD_B		This is a two-state input controlling Power Down. PD = V_A, Power Down is enabled and power dissipation is reduced. PD = AGND, Normal operation. Note: This signal has no effect when SPI_EN is high and the SPI interface is enabled.
27	TEST		Test Mode. When this signal is asserted high, a fixed test pattern (101001100011 msb->lsb) is sourced at the data outputs. With this signal deasserted low, the device is in normal operation mode. Note: This signal has no effect when SPI_EN is high and the SPI interface is enabled.
47	WAM		Word Alignment Mode. In single-lane mode this pin must be set to logic-0. In dual-lane mode only, when this signal is at logic-0 the serial data words are offset by half-word. With this signal at logic-1 the serial data words are aligned with each other. Note: This signal has no effect when SPI_EN is high and the SPI interface is enabled.
48	DLC		Dual-Lane Configuration. The dual-lane mode is selected when this signal is at logic-0. With this signal at logic-1, all data is sourced on a single lane (SD1_x) for each channel. Note: This signal has no effect when SPI_EN is high and the SPI interface is enabled.
45 44	OUTCLK+ OUTCLK-		Serial Clock. This pair of differential LVDS signals provides the serial clock that is synchronous with the Serial Data outputs. A bit of serial data is provided on each of the active serial data outputs with each falling and rising edge of this clock. The user has the ability to set the position of the clock edges at either the data-bit-cell boundries (0-degree phase) or at the center of the data-bit-cell boundries (180-degree phase). This differential output is always enabled while the device is powered up. In power-down mode this output is held in logic-low state. A 100-ohm termination resistor must always be used between this pair of signals at the far end of the transmission line.
43 42	FRAME+ FRAME-		Serial Data Frame. This pair of differential LVDS signals transitions at the serial data word boundries. The SD1_A+/- and SD1_B+/- output words always begin with the rising edge of the Frame signal. The falling edge of the Frame signal defines the start of the serial data word presented on the SD0_A+/- and SD0_B+/- signal pairs in the Dual-Lane mode. This differential output is always enabled while the device is powered up. In power-down mode this output is held in logic-low state. A 100-ohm termination resistor must always be used between this pair of signals at the far end of the transmission line.

Pin No.	Symbol	Equivalent Circuit	Description
38 37	SD1_A+ SD1_A-		Serial Data Output 1 for Channel A. This is a differential LVDS pair of signals that carries channel A ADC's output in serialized form. The serial data is provided synchronous with the OUTCLK output. In Single-Lane mode each sample's output is provided in succession. In Dual-Lane mode every other sample output is provided on this output. This differential output is always enabled while the device is powered up. In power-down mode this output holds the last logic state. A 100-ohm termination resistor must always be used between this pair of signals at the far end of the transmission line.
34 33	SD1_B+ SD1_B-		Serial Data Output 1 for Channel B. This is a differential LVDS pair of signals that carries channel B ADC's output in serialized form. The serial data is provided synchronous with the OUTCLK output. In Single-Lane mode each sample's output is provided in succession. In Dual-Lane mode every other sample output is provided on this output. This differential output is always enabled while the device is powered up. In power-down mode this output holds the last logic state. A 100-ohm termination resistor must always be used between this pair of signals at the far end of the transmission line.
36 35	SD0_A+ SD0_A-		Serial Data Output 0 for Channel A. This is a differential LVDS pair of signals that carries channel A ADC's alternating samples' output in serialized form in Dual-Lane mode. The serial data is provided synchronous with the OUTCLK output. In Single-Lane mode this differential output is held in high impedance state. This differential output is always enabled while the device is powered up. In power-down mode this output holds the last logic state. A 100-ohm termination resistor must always be used between this pair of signals at the far end of the transmission line.
32 31	SD0_B+ SD0_B-		Serial Data Output 0 for Channel B. This is a differential LVDS pair of signals that carries channel B ADC's alternating samples' output in serialized form in Dual-Lane mode. The serial data is provided synchronous with the OUTCLK output. In Single-Lane mode this differential output is held in high impedance state. This differential output is always enabled while the device is powered up. In power-down mode this output holds the last logic state. A 100-ohm termination resistor must always be used between this pair of signals at the far end of the transmission line.
56	SPI_EN		SPI Enable: The SPI interface is enabled when this signal is asserted high. In this case the direct control pins have no effect. When this signal is deasserted, the SPI interface is disabled and the direct control pins are enabled.
55	SCSb		Serial Chip Select: While this signal is asserted SCLK is used to accept serial data present on the SDI input and to source serial data on the SDO output. When this signal is deasserted, the SDI input is ignored and the SDO output is in tri-state mode.
52	SCLK		Serial Clock: Serial data are shifted into and out of the device synchronous with this clock signal.
54	SDI		Serial Data-In: Serial data are shifted into the device on this pin while SCSb signal is asserted.

Pin No.	Symbol	Equivalent Circuit	Description
53	SDO		Serial Data-Out: Serial data are shifted out of the device on this pin while SCSb signal is asserted. This output is in tri-state mode when SCSb is deasserted.
46 30	ORA ORB		Overrange. These CMOS outputs are asserted logic-high when their respective channel's data output is out-of-range in either high or low direction.
24	DLL_Lock		DLL_Lock Output. When the internal DLL is locked to the input CLK, this pin outputs a logic high. If the input CLK is changed abruptly, the internal DLL may become unlocked and this pin will output a logic low. Cycle Reset_DLL (pin 28) to re-lock the DLL to the input CLK.
ANALOG POWER			
8, 16, 17, 58, 60	V_A		Positive analog supply pins. These pins should be connected to a quiet source and be bypassed to AGND with 0.1 µF capacitors located close to the power pins.
1, 4, 12, 15, Exposed Pad	AGND		The ground return for the analog supply.
DIGITAL POWER			
26, 40, 49, 50	V_{DR}		Positive driver supply pin for the output drivers. This pin should be connected to a quiet voltage source and be bypassed to DRGND with a 0.1 µF capacitor located close to the power pin.
25, 39, 51	DRGND		The ground return for the digital output driver supply. This pins should be connected to the system digital ground, but not be connected in close proximity to the ADC's AGND pins.

Absolute Maximum Ratings (Notes 1, 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_A, V_{DR})	−0.3V to 4.2V
Voltage on Any Pin (Not to exceed 4.2V)	−0.3V to (V_A +0.3V)
Input Current at Any Pin other than Supply Pins (Note 4)	±5 mA
Package Input Current (Note 4)	±50 mA
Max Junction Temp (T_J)	+150°C
Thermal Resistance (θ_{JA})	30°C/W
ESD Rating	
Human Body Model (Note 6)	2500V
Machine Model (Note 6)	250V
Storage Temperature	−65°C to +150°C
Soldering process must comply with National Semiconductor's Reflow Temperature Profile specifications. Refer to www.national.com/packaging. (Note 7)	

Operating Ratings (Notes 1, 3)

Operating Temperature	−40°C ≤ T_A ≤ +85°C
Supply Voltage (V_A=V_{DR})	+2.7V to +3.6V
Clock Duty Cycle	
(DCS Enabled)	30/70 %
(DCS disabled)	45/55 %
V_{CM}	1.4V to 1.6V
|AGND-DRGND|	≤100mV

ADC12DS080 Converter Electrical Characteristics

This product is currently under development. As such, the parameters specified are DESIGN TARGETS. The specifications cannot be guaranteed until device characterization has taken place.

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, V_A = V_{DR} = +3.0V, Internal V_{REF} = +1.2V, f_{CLK} = 80 MHz, V_{CM} = V_{CMO}, C_L = 5 pF/pin. Typical values are for T_A = 25°C. **Boldface limits apply for T_{MIN} ≤ T_A ≤ T_{MAX}.** All other limits apply for T_A = 25°C (Notes 8, 9)

Symbol	Parameter	Conditions		Typical (Note 10)	Limits	Units (Limits)
STATIC CONVERTER CHARACTERISTICS						
	Resolution with No Missing Codes				**12**	Bits (min)
INL	Integral Non Linearity (Note 11)			±0.5		LSB (max) LSB (min)
DNL	Differential Non Linearity			±0.25		LSB (max) LSB (min)
	Under Range Output Code			0	**0**	
	Over Range Output Code			4095	**4095**	
REFERENCE AND ANALOG INPUT CHARACTERISTICS						
V_{CMO}	Common Mode Output Voltage			1.5	1.45 1.55	V (min) V (max)
V_{CM}	Analog Input Common Mode Voltage			1.5	1.4 1.6	V (min) V (max)
C_{IN}	V_{IN} Input Capacitance (each pin to GND) (Note 12)	V_{IN} = 1.5 Vdc ± 0.5 V	(CLK LOW)	8.5		pF
			(CLK HIGH)	3.5		pF
V_{REF}	External Reference Voltage			1.20	1.176 1.224	V (min) V (max)

ADC12DS080 Dynamic Converter Electrical Characteristics

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, $V_A = V_{DR}$ = +3.0V, Internal V_{REF} = +1.2V, f_{CLK} = 80 MHz, $V_{CM} = V_{CMO}$, C_L = 5 pF/pin, . Typical values are for T_A = 25°C. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for T_A = 25°C (Notes 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits	Units (Limits) (Note 2)
DYNAMIC CONVERTER CHARACTERISTICS, A_{IN} = -1dBFS					
FPBW	Full Power Bandwidth	-1 dBFS Input, –3 dB Corner	1.0		GHz
SNR	Signal-to-Noise Ratio	f_{IN} = 10 MHz	71.2		dBFS
		f_{IN} = 70 MHz	70		dBFS
		f_{IN} = 170 MHz	68		dBFS
SFDR	Spurious Free Dynamic Range	f_{IN} = 10 MHz	90		dBFS
		f_{IN} = 70 MHz	88		dBFS
		f_{IN} = 170 MHz	83		dBFS
ENOB	Effective Number of Bits	f_{IN} = 10 MHz	11.5		Bits
		f_{IN} = 70 MHz	11.3		Bits
		f_{IN} = 170 MHz	11		Bits
THD	Total Harmonic Disortion	f_{IN} = 10 MHz	–88		dBFS
		f_{IN} = 70 MHz	–85		dBFS
		f_{IN} = 170 MHz	–80		dBFS
H2	Second Harmonic Distortion	f_{IN} = 10 MHz	–100		dBFS
		f_{IN} = 70 MHz	–95		dBFS
		f_{IN} = 170 MHz	–85		dBFS
H3	Third Harmonic Distortion	f_{IN} = 10 MHz	–90		dBFS
		f_{IN} = 70 MHz	–88		dBFS
		f_{IN} = 170 MHz	–83		dBFS
SINAD	Signal-to-Noise and Distortion Ratio	f_{IN} = 10 MHz	71.1		dBFS
		f_{IN} = 70 MHz	69.8		dBFS
		f_{IN} = 170 MHz	67.7		dBFS

ADC12DS080 Logic and Power Supply Electrical Characteristics

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, $V_A = V_{DR}$ = +3.0V, Internal V_{REF} = +1.2V, f_{CLK} = 80 MHz, $V_{CM} = V_{CMO}$, C_L = 5 pF/pin. Typical values are for T_A = 25°C. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for T_A = 25°C (Notes 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits	Units (Limits)
DIGITAL INPUT CHARACTERISTICS (CLK, PD_A,PD_B,SCSb,SPI_EN,SCLK,SDI,TEST,WAM,DLC)					
$V_{IN(1)}$	Logical “1” Input Voltage	V_D = 3.6V		**2.0**	V (min)
$V_{IN(0)}$	Logical “0” Input Voltage	V_D = 3.0V		**0.8**	V (max)
$I_{IN(1)}$	Logical “1” Input Current	V_{IN} = 3.3V	10		µA
$I_{IN(0)}$	Logical “0” Input Current	V_{IN} = 0V	–10		µA
C_{IN}	Digital Input Capacitance		5		pF
DIGITAL OUTPUT CHARACTERISTICS (ORA,ORB,SDO)					
$V_{OUT(1)}$	Logical “1” Output Voltage	I_{OUT} = –0.5 mA , V_{DR} = 1.8V		**1.2**	V (min)
$V_{OUT(0)}$	Logical “0” Output Voltage	I_{OUT} = 1.6 mA, V_{DR} = 1.8V		**0.4**	V (max)
$+I_{SC}$	Output Short Circuit Source Current	V_{OUT} = 0V	–10		mA
$-I_{SC}$	Output Short Circuit Sink Current	$V_{OUT} = V_{DR}$	10		mA
C_{OUT}	Digital Output Capacitance		5		pF
POWER SUPPLY CHARACTERISTICS					

Symbol	Parameter	Conditions	Typical (Note 10)	Limits	Units (Limits)
I_A	Analog Supply Current	Full Operation	200		mA (max)
I_{DR}	Digital Output Supply Current	Full Operation	56		mA
	Power Consumption		845		mW (max)
	Power Down Power Consumption		30		mW

ADC12DS080 Timing and AC Characteristics

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, $V_A = V_{DR}$ = +3.0V, Internal V_{REF} = +1.2V, f_{CLK} = 80 MHz, $V_{CM} = V_{CMO}$, C_L = 5 pF/pin. Typical values are for T_A = 25°C. Timing measurements are taken at 50% of the signal amplitude. **Boldface limits apply for $T_{MIN} \leq T_A \leq T_{MAX}$.** All other limits apply for T_A = 25°C (Notes 8, 9)

Symb	Parameter	Conditions	Typical (Note 10)	Limits	Units (Limits)
	Maximum Clock Frequency	In Single-Lane Mode In Dual-Lane Mode		**65** **80**	MHz (max)
	Minimum Clock Frequency	In Single-Lane Mode In Dual-Lane Mode		**25** **52.5**	MHz (min)
t_{CONV}	Conversion Latency	Single-Lane Mode Dual-Lane, Offset Mode Dual-Lane, Word Aligned Mode		**7.5** **8** **9**	Clock Cycles
t_{AD}	Aperture Delay		0.6		ns
t_{AJ}	Aperture Jitter		0.1		ps rms

ADC12DS080 LVDS Electrical Characteristics

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, $V_A = V_{DR}$ = +3.0V, Internal V_{REF} = +1.2V, f_{CLK} = 80 MHz, $V_{CM} = V_{CMO}$, C_L = 5 pF/pin. Typical values are for T_A = 25°C. Timing measurements are taken at 50% of the signal amplitude. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for T_A = 25°C (Notes 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits	Units (Limits)
LVDS DC CHARACTERISTICS					
V_{OD}	Output Differential Voltage (SDO+) - (SDO-)	R_L = 100Ω	350	250 450	mV (min) mV (max)
delta V_{OD}	Output Differential Voltage Unbalance	R_L = 100Ω		±25	mV (max)
V_{OS}	Offset Voltage	R_L = 100Ω	1.25	1.125 1.375	V (min) V (max)
delta V_{OS}	Offset Voltage Unbalance	R_L = 100Ω		±25	mV (max)
IOS	Output Short Circuit Current	DO = 0V, V_{IN} = 1.1V,	-10		mA (max)
LVDS OUTPUT TIMING AND SWITCHING CHARACTERISTICS					
t_{DP}	Output Data Bit Period	Single-Lane Mode Dual-Lane Mode	1.04 2.08		ns
t_{HO}	Output Data Edge to Output Clock Edge Hold Time(Note 13)	Single-Lane Mode Dual-Lane Mode	320 840		ps
t_{SUO}	Output Data Edge to Output Clock Edge Set-Up Time(Note 13)	Single-Lane Mode Dual-Lane Mode	320 840		ps
t_{FP}	Frame Period	Single-Lane Mode Dual-Lane Mode	12.5 25		ns
t_{FDC}	Frame Clock Duty Cycle(Note 13)		50	45 55	% (min) % (max)
t_{DFS}	Data Edge to Frame Edge Skew	50% to 50%	TBD		ps (max)
t_R, t_F	LVDS Rise/Fall Time	C_L=5pF to GND, R_{OUT}=100Ω	TBD		ps (max)
t_{ODOR}	Output Delay of OR output	From rising edge of CLKL to ORA/ORB valid	4		ns
t_{DLD}	Serializer DLL Lock Time		TBD		µs
t_{SD}	Serializer Delay	R_L=100Ω	TBD		ns

ADC12DS105 Converter Electrical Characteristics

This product is currently under development. As such, the parameters specified are DESIGN TARGETS. The specifications cannot be guaranteed until device characterization has taken place.

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, $V_A = V_{DR}$ = +3.3V, Internal V_{REF} = +1.2V, f_{CLK} = 105 MHz, $V_{CM} = V_{CMO}$, C_L = 5 pF/pin. Typical values are for T_A = 25°C. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for T_A = 25°C (Notes 8, 9)

Symbol	Parameter	Conditions		Typical (Note 10)	Limits	Units (Limits)
STATIC CONVERTER CHARACTERISTICS						
	Resolution with No Missing Codes				**12**	Bits (min)
INL	Integral Non Linearity (Note 11)			±0.5		LSB (max) LSB (min)
DNL	Differential Non Linearity			±0.25		LSB (max) LSB (min)
	Under Range Output Code			0	**0**	
	Over Range Output Code			4095	**4095**	
REFERENCE AND ANALOG INPUT CHARACTERISTICS						
V_{CMO}	Common Mode Output Voltage			1.5	1.45 1.55	V (min) V (max)
V_{CM}	Analog Input Common Mode Voltage			1.5	1.4 1.6	V (min) V (max)
C_{IN}	V_{IN} Input Capacitance (each pin to GND) (Note 12)	V_{IN} = 1.5 Vdc ± 0.5 V	(CLK LOW)	8.5		pF
			(CLK HIGH)	3.5		pF
V_{REF}	External Reference Voltage			1.20	1.176 1.224	V (min) V (max)

ADC12DS105 Dynamic Converter Electrical Characteristics

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, $V_A = V_{DR}$ = +3.3V, Internal V_{REF} = +1.2V, f_{CLK} = 105 MHz, $V_{CM} = V_{CMO}$, C_L = 5 pF/pin, . Typical values are for T_A = 25°C. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for T_A = 25°C (Notes 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits	Units (Limits) (Note 2)
DYNAMIC CONVERTER CHARACTERISTICS, A_{IN} = -1dBFS					
FPBW	Full Power Bandwidth	-1 dBFS Input, –3 dB Corner	1.0		GHz
SNR	Signal-to-Noise Ratio	f_{IN} = 10 MHz	70.1		dBFS
		f_{IN} = 70 MHz	69.1		dBFS
		f_{IN} = 240 MHz	67		dBFS
SFDR	Spurious Free Dynamic Range	f_{IN} = 10 MHz	88		dBFS
		f_{IN} = 70 MHz	85		dBFS
		f_{IN} = 240 MHz	83		dBFS
ENOB	Effective Number of Bits	f_{IN} = 10 MHz	11.3		Bits
		f_{IN} = 70 MHz	11.2		Bits
		f_{IN} = 240 MHz	10.8		Bits
THD	Total Harmonic Disortion	f_{IN} = 10 MHz	–86		dBFS
		f_{IN} = 70 MHz	–85		dBFS
		f_{IN} = 240 MHz	–80		dBFS
H2	Second Harmonic Distortion	f_{IN} = 10 MHz	–95		dBFS
		f_{IN} = 70 MHz	–90		dBFS
		f_{IN} = 240 MHz	–85		dBFS

Symbol	Parameter	Conditions	Typical (Note 10)	Limits	Units (Limits) (Note 2)
H3	Third Harmonic Distortion	f_{IN} = 10 MHz	–88		dBFS
		f_{IN} = 70 MHz	–85		dBFS
		f_{IN} = 240 MHz	–83		dBFS
SINAD	Signal-to-Noise and Distortion Ratio	f_{IN} = 10 MHz	70		dBFS
		f_{IN} = 70 MHz	69		dBFS
		f_{IN} = 240 MHz	66.8		dBFS

ADC12DS105 Logic and Power Supply Electrical Characteristics

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, V_A = V_{DR} = +3.3V, Internal V_{REF} = +1.2V, f_{CLK} = 105 MHz, V_{CM} = V_{CMO}, C_L = 5 pF/pin. Typical values are for T_A = 25°C. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for T_A = 25°C (Notes 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits	Units (Limits)
DIGITAL INPUT CHARACTERISTICS (CLK, PD_A,PD_B,SCSb,SPI_EN,SCLK,SDI,TEST,WAM,DLC)					
$V_{IN(1)}$	Logical “1” Input Voltage	V_D = 3.6V		**2.0**	V (min)
$V_{IN(0)}$	Logical “0” Input Voltage	V_D = 3.0V		**0.8**	V (max)
$I_{IN(1)}$	Logical “1” Input Current	V_{IN} = 3.3V	10		µA
$I_{IN(0)}$	Logical “0” Input Current	V_{IN} = 0V	–10		µA
C_{IN}	Digital Input Capacitance		5		pF
DIGITAL OUTPUT CHARACTERISTICS (ORA,ORB,SDO)					
$V_{OUT(1)}$	Logical “1” Output Voltage	I_{OUT} = –0.5 mA , V_{DR} = 1.8V		**1.2**	V (min)
$V_{OUT(0)}$	Logical “0” Output Voltage	I_{OUT} = 1.6 mA, V_{DR} = 1.8V		**0.4**	V (max)
$+I_{SC}$	Output Short Circuit Source Current	V_{OUT} = 0V	–10		mA
$–I_{SC}$	Output Short Circuit Sink Current	V_{OUT} = V_{DR}	10		mA
C_{OUT}	Digital Output Capacitance		5		pF
POWER SUPPLY CHARACTERISTICS					
I_A	Analog Supply Current	Full Operation	250		mA (max)
I_{DR}	Digital Output Supply Current	Full Operation	71		mA
	Power Consumption		1060		mW (max)
	Power Down Power Consumption	Clock disabled	33		mW

ADC12DS105 Timing and AC Characteristics

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, V_A = V_{DR} = +3.3V, Internal V_{REF} = +1.2V, f_{CLK} = 105 MHz, V_{CM} = V_{CMO}, C_L = 5 pF/pin. Typical values are for T_A = 25°C. Timing measurements are taken at 50% of the signal amplitude. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for T_A = 25°C (Notes 8, 9)

Symb	Parameter	Conditions	Typical (Note 10)	Limits	Units (Limits)
	Maximum Clock Frequency	In Single-Lane Mode In Dual-Lane Mode		**65** **105**	MHz (max)
	Minimum Clock Frequency	In Single-Lane Mode In Dual-Lane Mode		**25** **52.5**	MHz (min)
t_{CONV}	Conversion Latency	Single-Lane Mode Dual-Lane, Offset Mode Dual-Lane, Word Aligned Mode		**7.5** **8** **9**	Clock Cycles
t_{AD}	Aperture Delay		0.6		ns
t_{AJ}	Aperture Jitter		0.1		ps rms

ADC12DS105 LVDS Electrical Characteristics

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, $V_A = V_{DR}$ = +3.3V, Internal V_{REF} = +1.2V, f_{CLK} = 105 MHz, $V_{CM} = V_{CMO}$, C_L = 5 pF/pin. Typical values are for T_A = 25°C. Timing measurements are taken at 50% of the signal amplitude. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for T_A = 25°C (Notes 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits	Units (Limits)
LVDS DC CHARACTERISTICS					
V_{OD}	Output Differential Voltage (SDO+) - (SDO-)	R_L = 100Ω	350	250 450	mV (min) mV (max)
delta V_{OD}	Output Differential Voltage Unbalance	R_L = 100Ω		±25	mV (max)
V_{OS}	Offset Voltage	R_L = 100Ω	1.25	1.125 1.375	V (min) V (max)
delta V_{OS}	Offset Voltage Unbalance	R_L = 100Ω		±25	mV (max)
IOS	Output Short Circuit Current	DO = 0V, V_{IN} = 1.1V,	-10		mA (max)
LVDS OUTPUT TIMING AND SWITCHING CHARACTERISTICS					
t_{DP}	Output Data Bit Period	Single-Lane Mode Dual-Lane Mode	0.79 1.59		ns
t_{HO}	Output Data Edge to Output Clock Edge Hold Time(Note 13)	Single-Lane Mode Dual-Lane Mode	195 595		ps
t_{SUO}	Output Data Edge to Output Clock Edge Set-Up Time(Note 13)	Single-Lane Mode Dual-Lane Mode	195 595		ps
t_{FP}	Frame Period	Single-Lane Mode Dual-Lane Mode	9.52 19.05		ns
t_{FDC}	Frame Clock Duty Cycle(Note 13)		50	45 55	% (min) % (max)
t_{DFS}	Data Edge to Frame Edge Skew	50% to 50%	TBD		ps (max)
t_R, t_F	LVDS Rise/Fall Time	C_L=5pF to GND, R_{OUT}=100Ω	TBD		ps (max)
t_{ODOR}	Output Delay of OR output	From rising edge of CLKL to ORA/ORB valid	4		ns
t_{DLD}	Serializer DLL Lock Time		TBD		µs
t_{SD}	Serializer Delay	R_L=100Ω	TBD		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is guaranteed to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the maximum Operating Ratings is not recommended.

Note 2: This parameter is specified in units of dBFS - indicating the value that would be attained with a full-scale input signal.

Note 3: All voltages are measured with respect to GND = AGND = DRGND = 0V, unless otherwise specified.

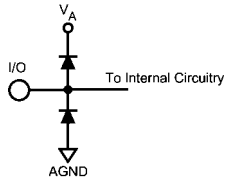
Note 4: When the input voltage at any pin exceeds the power supplies (that is, $V_{IN} < AGND$, or $V_{IN} > V_A$), the current at that pin should be limited to ±5 mA. The ±50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of ±5 mA to 10.

Note 5: The maximum allowable power dissipation is dictated by $T_{J,max}$, the junction-to-ambient thermal resistance, (θ_{JA}), and the ambient temperature, (T_A), and can be calculated using the formula $P_{D,max} = (T_{J,max} - T_A)/\theta_{JA}$. The values for maximum power dissipation listed above will be reached only when the device is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Such conditions should always be avoided.

Note 6: Human Body Model is 100 pF discharged through a 1.5 kΩ resistor. Machine Model is 220 pF discharged through 0 Ω

Note 7: Reflow temperature profiles are different for lead-free and non-lead-free packages.

Note 8: The inputs are protected as shown below. Input voltage magnitudes above V_A or below GND will not damage this device, provided current is limited per (Note 4). However, errors in the A/D conversion can occur if the input goes above 2.6V or below GND as described in the Operating Ratings section.



20211711

Note 9: With a full scale differential input of $2V_{P-P}$, the 12-bit LSB is 488 µV.

Note 10: Typical figures are at T_A = 25°C and represent most likely parametric norms at the time of product characterization. The typical specifications are not guaranteed.

Note 11: Integral Non Linearity is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive and negative full-scale.

Note 12: The input capacitance is the sum of the package/pin capacitance and the sample and hold circuit capacitance.

Note 13: This parameter is guaranteed by design and/or characterization and is not tested in production.

Specification Definitions

APERTURE DELAY is the time after the falling edge of the clock to when the input signal is acquired or held for conversion.

APERTURE JITTER (APERTURE UNCERTAINTY) is the variation in aperture delay from sample to sample. Aperture jitter manifests itself as noise in the output.

CLOCK DUTY CYCLE is the ratio of the time during one cycle that a repetitive digital waveform is high to the total time of one period. The specification here refers to the ADC clock input signal.

COMMON MODE VOLTAGE (V_{CM}) is the common DC voltage applied to both input terminals of the ADC.

CONVERSION LATENCY is the number of clock cycles between initiation of conversion and when that data is presented to the output driver stage. Data for any given sample is available at the output pins the Pipeline Delay plus the Output Delay after the sample is taken. New data is available at every clock cycle, but the data lags the conversion by the pipeline delay.

CROSSTALK is coupling of energy from one channel into the other channel.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion Ratio or SINAD. ENOB is defined as (SINAD - 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated as:

Gain Error = Positive Full Scale Error – Negative Full Scale Error

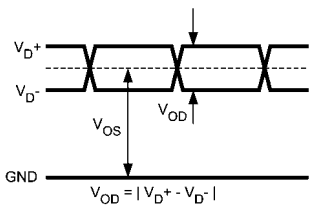
It can also be expressed as Positive Gain Error and Negative Gain Error, which are calculated as:

PGE = Positive Full Scale Error - Offset Error
NGE = Offset Error - Negative Full Scale Error

INTEGRAL NON LINEARITY (INL) is a measure of the deviation of each individual code from a best fit straight line. The deviation of any given code from this straight line is measured from the center of that code value.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the intermodulation products to the total power in the original frequencies. IMD is usually expressed in dBFS.

LSB (LEAST SIGNIFICANT BIT) is the bit that has the smallest value or weight of all bits. This value is $V_{FS}/2^n$, where "V_{FS}" is the full scale input voltage and "n" is the ADC resolution in bits.



LVDS Differential Output Voltage (V_{OD}) is the absolute value of the difference between the differential output pair voltages (V_D+ and V_D-), each measured with respect to ground.

MISSING CODES are those output codes that will never appear at the ADC outputs. The ADC is guaranteed not to have any missing codes.

MSB (MOST SIGNIFICANT BIT) is the bit that has the largest value or weight. Its value is one half of full scale.

NEGATIVE FULL SCALE ERROR is the difference between the actual first code transition and its ideal value of ½ LSB above negative full scale.

OFFSET ERROR is the difference between the two input voltages [(V_{IN}+) – (V_{IN}-)] required to cause a transition from code 2047 to 2048.

OUTPUT DELAY is the time delay after the falling edge of the clock before the data update is presented at the output pins.

PIPELINE DELAY (LATENCY) See CONVERSION LATENCY.

POSITIVE FULL SCALE ERROR is the difference between the actual last code transition and its ideal value of 1½ LSB below positive full scale.

POWER SUPPLY REJECTION RATIO (PSRR) is a measure of how well the ADC rejects a change in the power supply voltage. PSRR is the ratio of the Full-Scale output of the ADC with the supply at the minimum DC supply limit to the Full-Scale output of the ADC with the supply at the maximum DC supply limit, expressed in dB.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or DC.

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dB, of the rms total of the first six harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

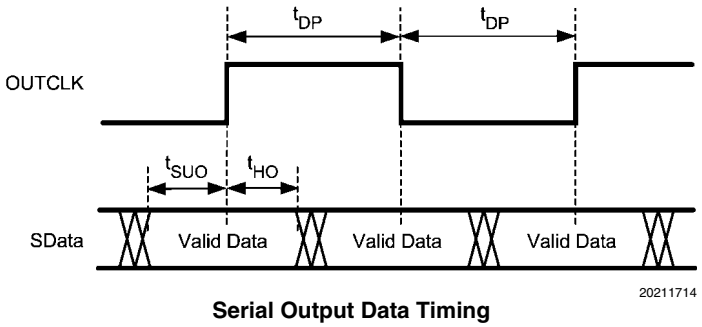
$$THD = 20 \times \log \sqrt{\frac{f_2^2 + \ldots + f_7^2}{f_1^2}}$$

where f_1 is the RMS power of the fundamental (output) frequency and f_2 through f_7 are the RMS power of the first six harmonic frequencies in the output spectrum.

SECOND HARMONIC DISTORTION (2ND HARM) is the difference expressed in dB, between the RMS power in the input frequency at the output and the power in its 2nd harmonic level at the output.

THIRD HARMONIC DISTORTION (3RD HARM) is the difference, expressed in dB, between the RMS power in the input frequency at the output and the power in its 3rd harmonic level at the output.

Timing Diagrams



Serial Output Data Timing

FIGURE 1.

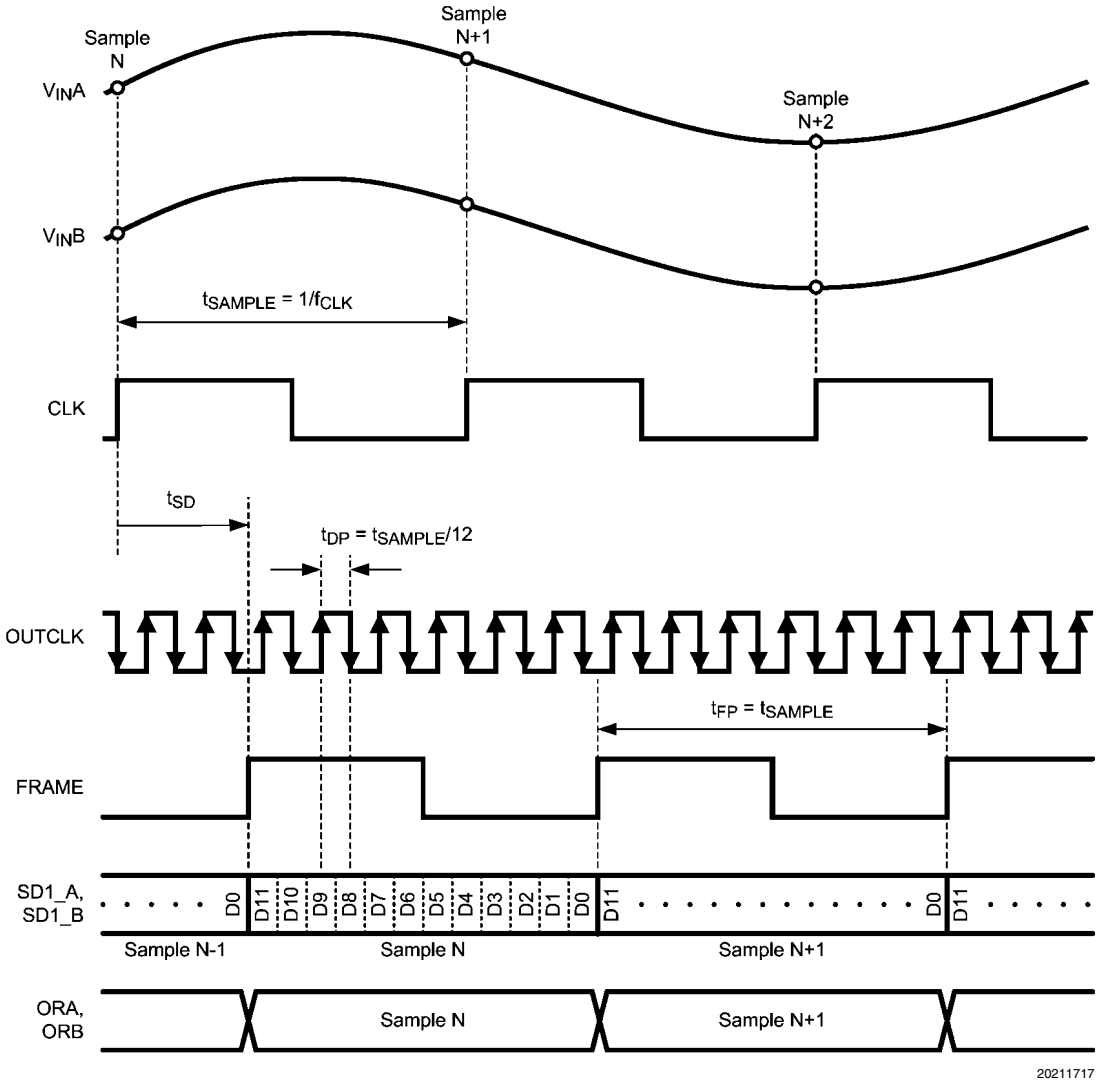


FIGURE 2. Serial Output Data Format in Single-Lane Mode

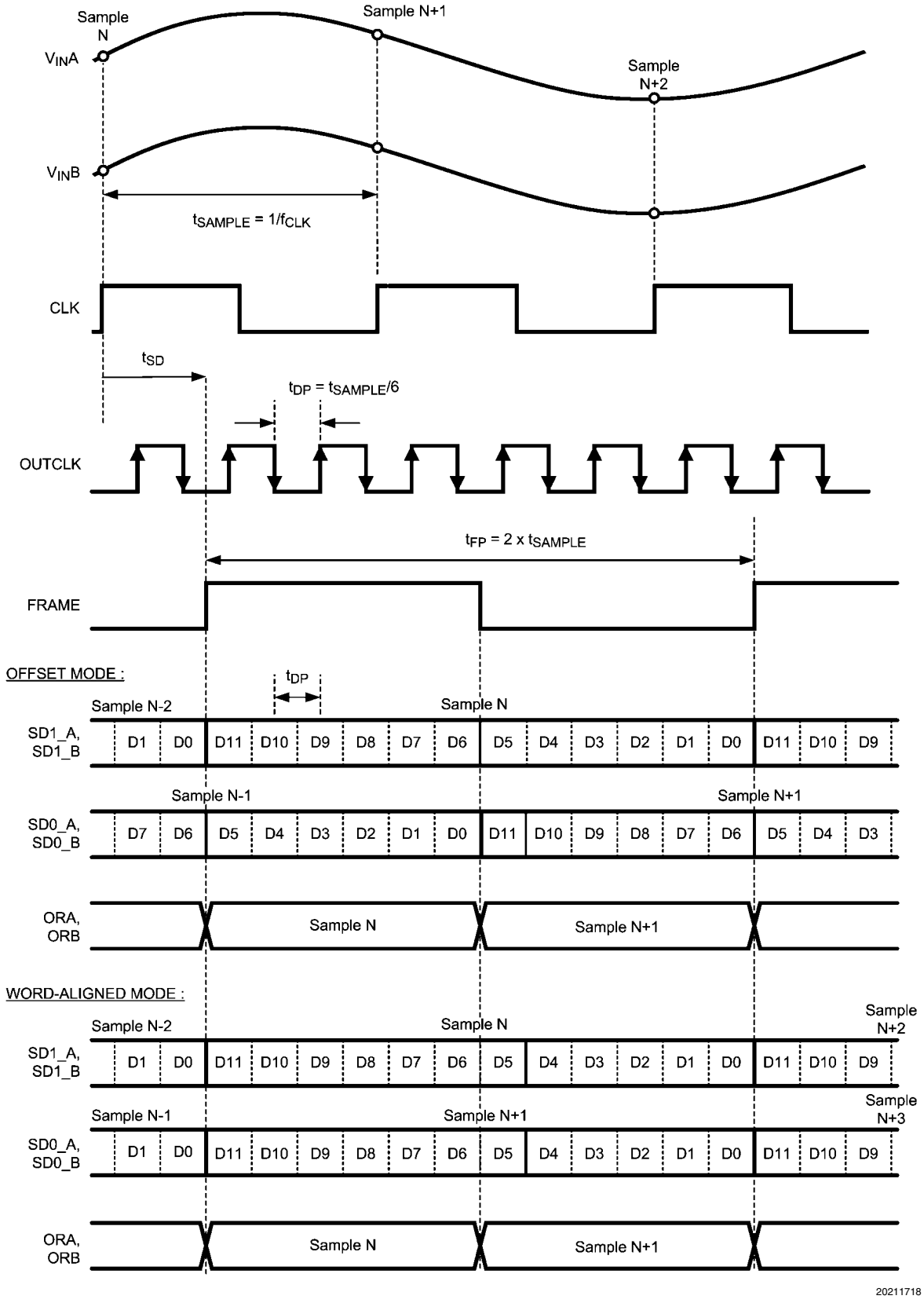


FIGURE 3. Serial Output Data Format in Dual-Lane Mode

Transfer Characteristic

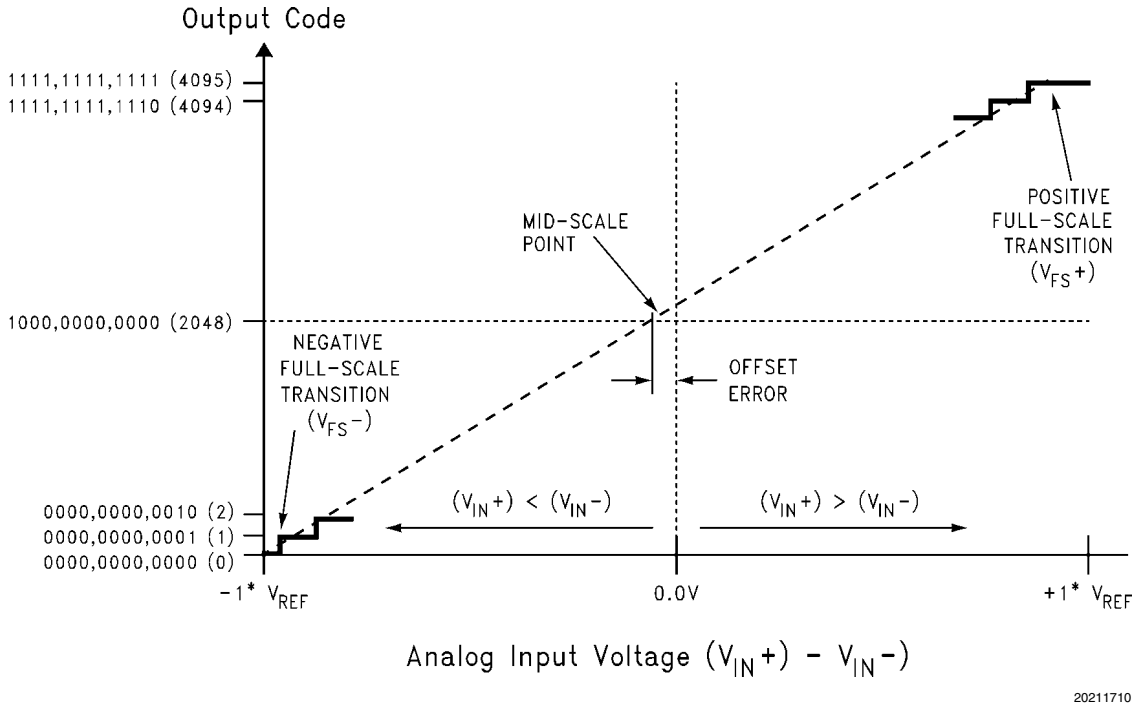


FIGURE 4. Transfer Characteristic

Functional Description

Operating on a single +3.0 or 3.3V supply, the ADC12DS080/105 digitizes two differential analog input signals to 12 bits, using a differential pipelined architecture with error correction circuitry and an on-chip sample-and-hold circuit to ensure maximum performance.

Serial Output Data Format : The digital data for each channel is provided in a serial format. Two modes of operation are available for the serial data format. Single-lane serial format (shown in *Figure 2*) uses one set of differential data signals per channel. Dual-lane serial format (shown in *Figure 3*) uses two sets of differential data signals per channel in order to slow down the data and clock frequency by a factor of 2. At slower rates of operation (typically below 65 Msps) the single-lane mode may the most efficient to use. At higher rates the user may want to employ the dual-lane scheme. In either case DDR-type clocking is used. For each data channel, an over-range indication is also provided. The OR signal is updated with each frame of data.

Serial Control Interface

The ADC12DS080/105 has a serial interface that allows access to the control registers. The serial interface is a generic 4-wire synchronous interface that is compatible with SPI type interfaces that are used on many microcontrollers and DSP controllers.

The ADC's input clock must be running for the Serial Control Interface to operate. The SPI interface is enabled when the SPI_EN (pin 56) signal is asserted high. In this case the direct control pins have no effect. When this signal is deasserted, the SPI interface is disabled and the direct control pins are enabled. Please note that the Power Down function is not available when the SPI is enabled.

Each serial interface access cycle is exactly 16 bits long. A register-write can be accomplished in one cycle - with the data field returning the contents of the register addressed in the command field of the same cycle. A random access register-read requires 2 cycles - one to load the address and the second to read the register addressed in the previous cycle. Register space supported by this interface is 16, although only a subset is implemented in this device. *Figure 5* shows the access protocol used by this interface. Each signal's function is described below. The Read Timing is shown in *Figure 6*, while the Write Timing is shown in *Figure 7*

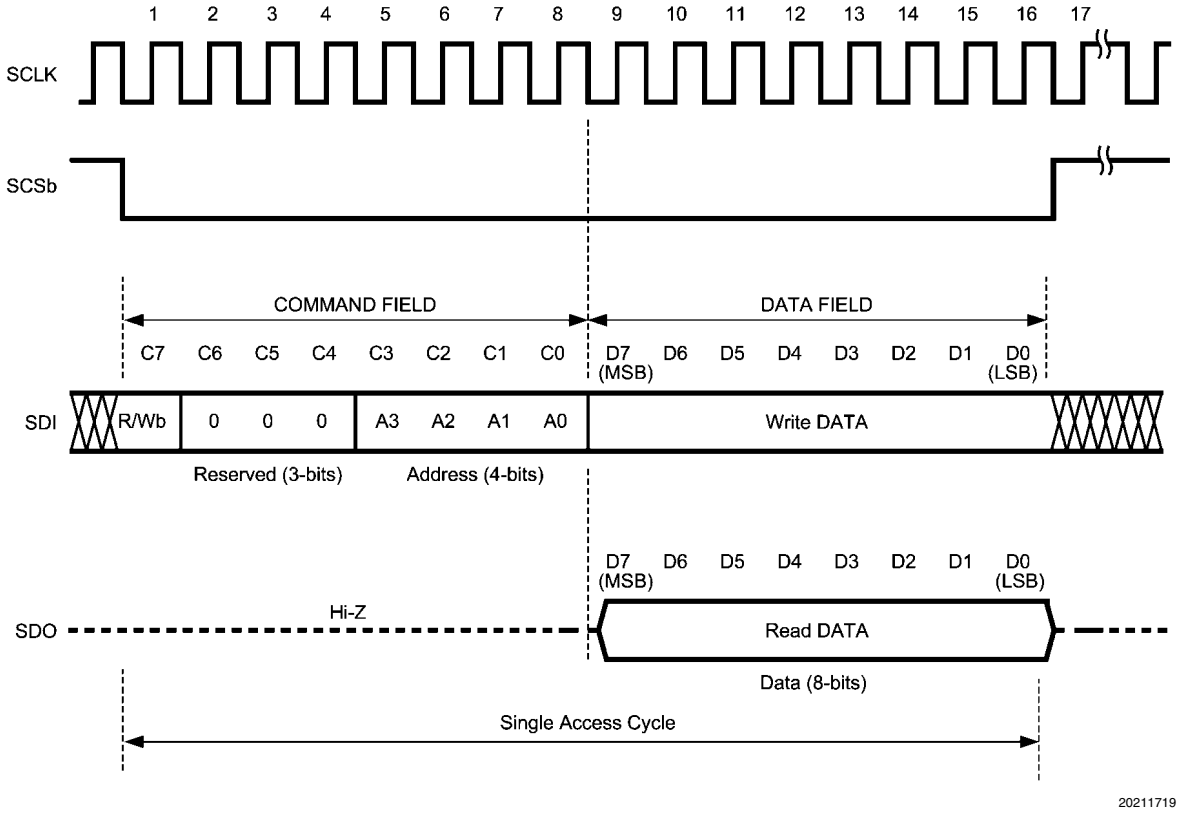


FIGURE 5. Serial Interface Protocol

SIGNAL DESCRIPTIONS

SCLK: Used to register the input data (SDI) on the rising edge; and to source the output data (SDO) on the falling edge. User may disable clock and hold it in the low-state, as long as clock pulse-width min spec is not violated when clock is enabled or disabled.

SCSb: Serial Interface Chip Select. Each assertion starts a new register access - i.e., the SDATA field protocol is required. The user is required to deassert this signal after the 16th clock. If the SCSb is deasserted before the 16th clock, no address or data write will occur. The rising edge captures the address just shifted-in and, in the case of a write operation, writes the addressed register. There is a minimum pulse-

width requirement for the deasserted pulse - which is specified in the Electrical Specifications section.

SDI: Serial Data. Must observe setup/hold requirements with respect to the SCLK. Each cycle is 16-bits long.

R/Wb:	A value of '1' indicates a read operation, while a value of '0' indicates a write operation.
Reserved:	Reserved for future use. Must be set to 0.
ADDR:	Up to 16 registers can be addressed.
DATA:	In a write operation the value in this field will be written to the register addressed in this cycle when SCSb is deasserted. In a read operation this field is ignored.

SDO: This output is normally tri-stated and is driven only when SCSb is asserted. Upon SCSb assertion, contents of the register addressed during the first byte are shifted out with the second 8 SCLK falling edges. Upon power-up, the default register address is 00h.

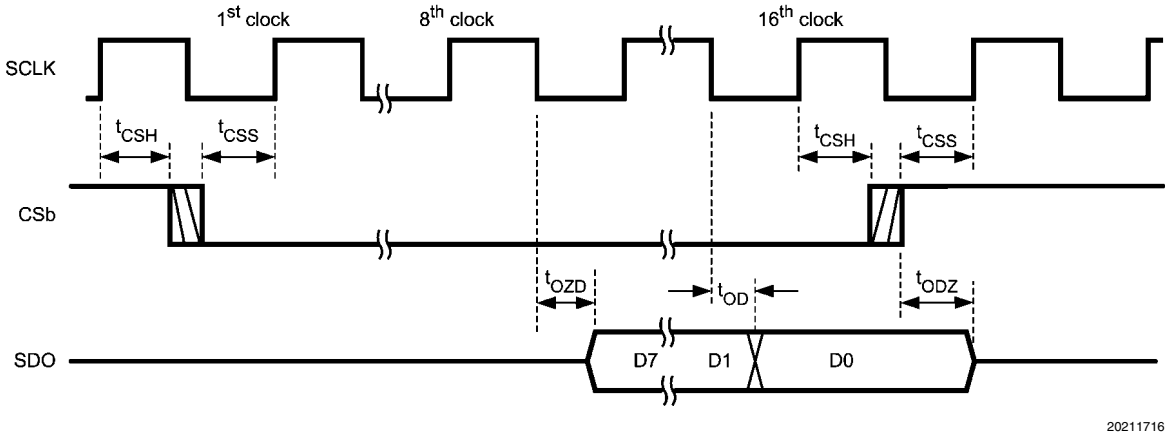


FIGURE 6. Read Timing

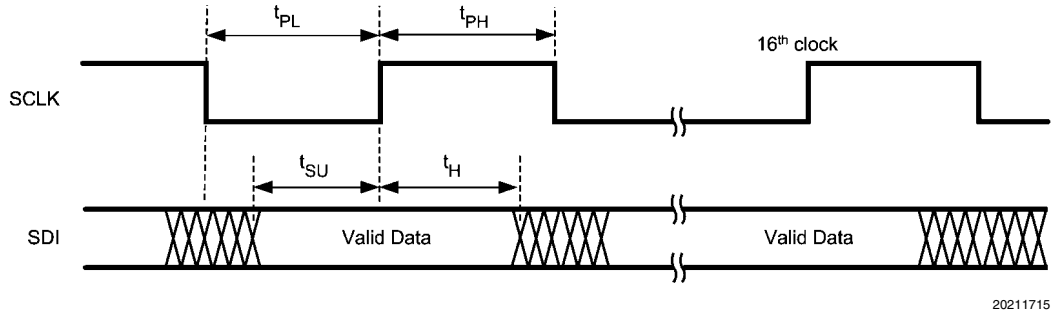


FIGURE 7. Write Timing

Device Control Register, Address 0h

7 6	5	4	3	2	1	0
OM	DLE	DCS	DF	WAM	Reserved	

Bits (7:6) Operational Mode

0 0 Normal Operation.

0 1 Test Output mode. A fixed test pattern (101001100011 msb->lsb) is sourced at the data outputs.

1 0 Test Output mode. Data pattern defined by user in registers 01h and 02h is sourced at data outputs.

1 1 Reserved.

Bit 5 Data Lane Configuration. When this bit is set to '0', the serial data interface is configured for dual-lane mode where the data words are output on two data outputs (SD1 and SD0) at half the rate of the single-lane interface. When this bit is set to '1', serial data is output on the SD1 output only and the SD0 outputs are held in a high-impedance state

Bit 4 Duty Cycle Stabilizer. When this bit is set to '0' the DCS is off. When this bit is set to '1', the DCS is on.

Bit 3 Data Format. When this bit is set to '1' the data output is in the "twos complement" form. When this bit is set to '0' the data output is in the "offset binary" form.

Bit 2 Word Alignment Mode.
This bit must be set to '0' in the single-lane mode of operation.
In dual-lane mode, when this bit is set to '0' the serial data words are offset by half-word. This gives the least latency through the device. When this bit is set to '1' the serial data words are in word-aligned mode. In this mode the serial data on the SD1 lane is additionally delayed by one CLK cycle. (Refer to).

Bit 1 Reserved. Must be set to '0'.

Bit 0 Reserved. Must be set to '0'.

Reset State : 08h

User Test Pattern Register 0, Address 1h

7	6	5	4	3	2	1	0
Reserved				User Test Pattern (11:8)			

Bits (7:6) Reserved. Must be set to '0'.

Bits (5:0) User Test Pattern. Most-significant 6 bits of the 12-bit pattern that will be sourced out of the data outputs in Test Output Mode.

Reset State : 00h

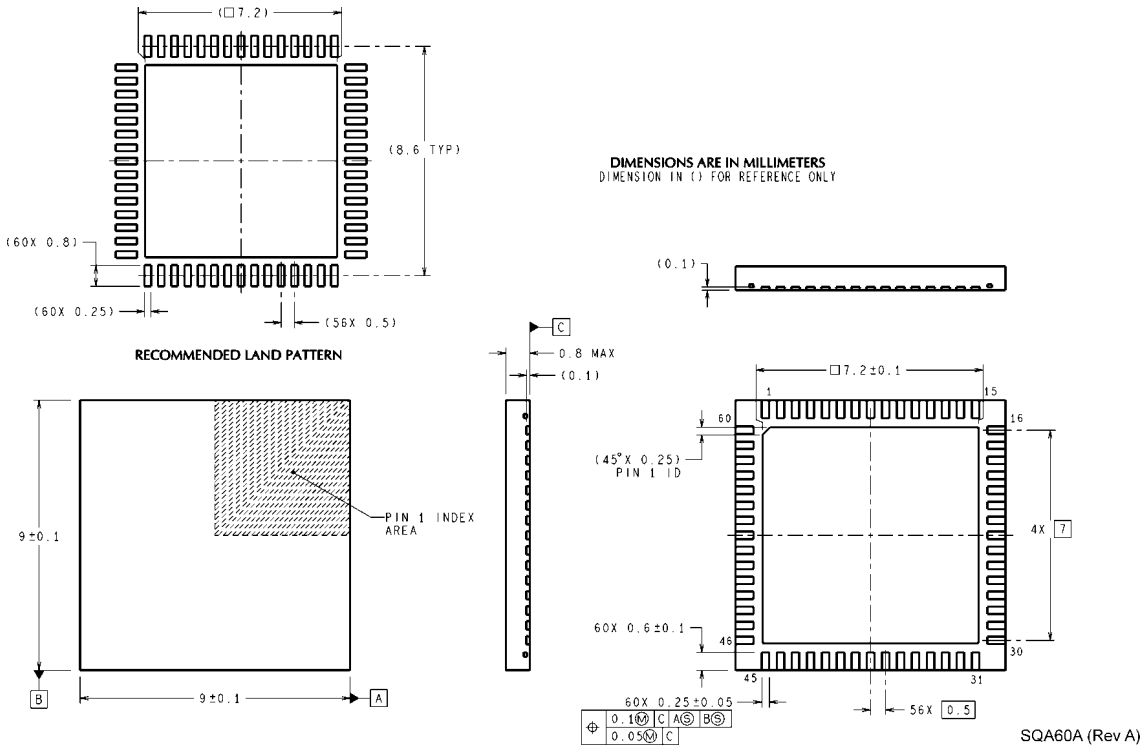
User Test Pattern Register 1, Address 2h

7	6	5	4	3	2	1	0
User Test Pattern (7:0)							

Bits (7:0) User Test Pattern. Least-significant 8 bits of the 12-bit pattern that will be sourced out of the data outputs in Test Output Mode.

Reset State : 00h

Physical Dimensions inches (millimeters) unless otherwise noted



TOP View.....SIDE View.....BOTTOM View
60-Lead LLP Package
Ordering Numbers:
ADC12DS080CISQ / ADC12DS105CISQ
NS Package Number SQA60A

Notes

Notes

National Semiconductor Americas Customer Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

National Semiconductor Europe Customer Support Center
Fax: +49 (0) 180-530-85-86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +49 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor Asia Pacific Customer Support Center
Email: ap.support@nsc.com

National Semiconductor Japan Customer Support Center
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560