National Semiconductor

ADC12D1800RF

ADVANCE INFORMATION
July 1, 2011

12-Bit, Single 3.6 GSPS Ultra High-Speed ADC

1.0 General Description

The 12-bit 1.8 GSPS ADC12D1800RF is an RF-sampling GSPS ADC that can directly sample input frequencies up to and above 2.7 GHz. The ADC12D1800RF augments the very large Nyquist zone of National's GSPS ADCs with excellent noise and linearity performance at RF frequencies, extending its usable range beyond the 3rd Nyquist zone.

The ADC12D1800RF provides a flexible LVDS interface which has multiple SPI programmable options to facilitate board design and FPGA/ASIC data capture. The LVDS outputs are compatible with IEEE 1596.3-1996 and supports programmable common mode voltage. The product is packaged in a lead-free 292-ball thermally enhanced BGA package over the rated industrial temperature range of -40°C to +85°C.

2.0 Features

- Excellent noise and linearity up to and above f_{IN} = 2.7 GHz
- Configurable to either 3.6 GSPS interleaved or 1800 MSPS dual ADC
- New DESCLKIQ Mode for high bandwidth, high sampling rate apps
- Pin-compatible with ADC1xD1x00, ADC12Dx00RF
- AutoSync feature for multi-chip synchronization
- Internally terminated, buffered, differential analog inputs
- Interleaved timing automatic and manual skew adjust
- Test patterns at output for system debug
- Time Stamp feature to capture external trigger
- Programmable gain, offset, and t_{AD} adjust feature
- 1:1 non-demuxed or 1:2 demuxed LVDS outputs

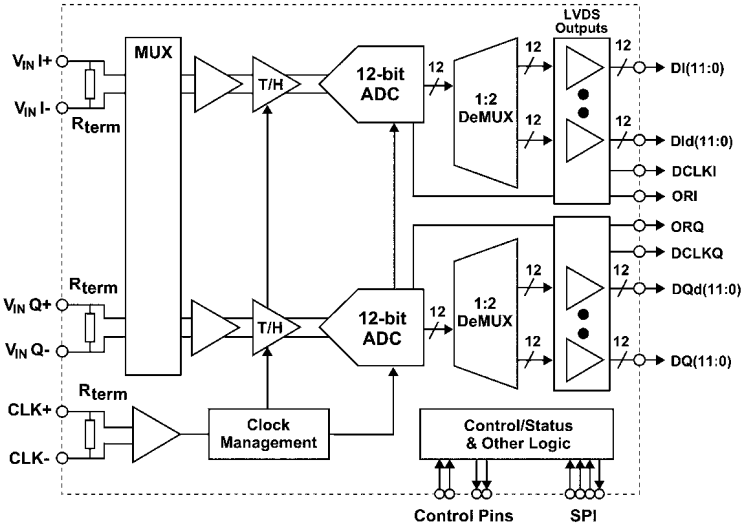
3.0 Applications

- 3G/4G Wireless Basestation
  - Receive Path
  - DPD Path
- Wideband Microwave Backhaul
- RF Sampling Software Defined Radio
- Military Communications
- SIGINT
- RADAR / LIDAR
- Wideband Communications
- Consumer RF
- Test and Measurement

4.0 Key Specifications

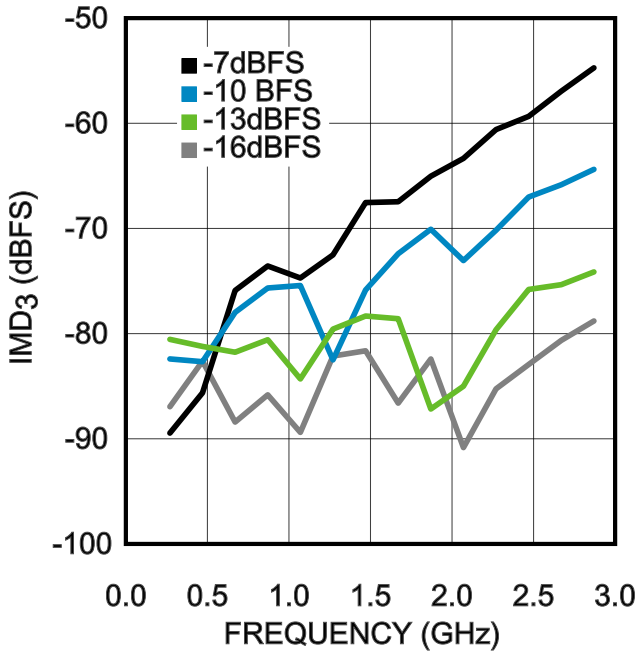
Resolution	12 Bits
Interleaved 3.6 GSPS ADC	
IMD_3 (Fin = 2.7GHz @ -13dBFS)	-62 dBc (typ)
IMD_3 (Fin = 2.7GHz @ -16dBFS)	-64 dBc (typ)
Noise Floor	-155.0 dBm/Hz (typ)
Noise Power Ratio	TBD dB (typ)
Power	4.4W (typ)
Dual 1800 MSPS ADC, Fin = 498 MHz	
ENOB	9.2 Bits (typ)
SNR	57.7 dB (typ)
SFDR	70 dBc (typ)
Power per Channel	2.2W (typ)

5.0 Block Diagram



Simplified Block Diagram

6.0 RF Performance



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ADC12D1800RF Non-DES Mode IMD_3

7.0 Connection Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	GND	V_A	SDO	TPM	NDM	V_A	GND	V_E	GND_E	DId0+	V_DR	DId3+	GND_DR	DId6+	V_DR	DId9+	GND_DR	DId11+	DId11-	GND_DR	A
B	Vbg	GND	ECEb	SDI	CalRun	V_A	GND	GND_E	V_E	DId0-	DId2+	DId3-	DId5+	DId6-	DId8+	DId9-	DId10+	DI0+	DI1+	DI1-	B
C	Rtrim+	Vcmo	Rext+	SCSb	SCLK	V_A	NC	V_E	GND_E	DId1+	DId2-	DId4+	DId5-	DId7+	DId8-	DId10-	DI0-	V_DR	DI2+	DI2-	C
D	DNC	Rtrim-	Rext-	GND	GND	CAL	DNC	V_A	V_A	DId1-	V_DR	DId4-	GND_DR	DId7-	V_DR	GND_DR	V_DR	DI3+	DI4+	DI4-	D
E	V_A	Tdiode+	DNC	GND													GND_DR	DI3-	DI5+	DI5-	E
F	V_A	GND_TC	Tdiode-	DNC													GND_DR	DI6+	DI6-	GND_DR	F
G	V_TC	GND_TC	V_TC	V_TC													DI7+	DI7-	DI8+	DI8-	G
H	VinI+	V_TC	GND_TC	V_A				GND	GND	GND	GND	GND	GND				DI9+	DI9-	DI10+	DI10-	H
J	VinI-	GND_TC	V_TC	VbiasI				GND	GND	GND	GND	GND	GND				V_DR	DI11+	DI11-	V_DR	J
K	GND	VbiasI	V_TC	GND_TC				GND	GND	GND	GND	GND	GND				ORI+	ORI-	DCLKI+	DCLKI-	K
L	GND	VbiasQ	V_TC	GND_TC				GND	GND	GND	GND	GND	GND				ORQ+	ORQ-	DCLKQ+	DCLKQ-	L
M	VinQ-	GND_TC	V_TC	VbiasQ				GND	GND	GND	GND	GND	GND				GND_DR	DQ11+	DQ11-	GND_DR	M
N	VinQ+	V_TC	GND_TC	V_A				GND	GND	GND	GND	GND	GND				DQ9+	DQ9-	DQ10+	DQ10-	N
P	V_TC	GND_TC	V_TC	V_TC													DQ7+	DQ7-	DQ8+	DQ8-	P
R	V_A	GND_TC	V_TC	V_TC													V_DR	DQ6+	DQ6-	V_DR	R
T	V_A	GND_TC	GND_TC	GND													V_DR	DQ3-	DQ5+	DQ5-	T
U	GND_TC	CLK+	PDI	GND	GND	RCOut1-	DNC	V_A	V_A	DQd1-	V_DR	DQd4-	GND_DR	DQd7-	V_DR	V_DR	GND_DR	DQ3+	DQ4+	DQ4-	U
V	CLK-	DCLK _RST+	PDQ	CalDly	DES	RCOut2+	RCOut2-	V_E	GND_E	DQd1+	DQd2-	DQd4+	DQd5-	DQd7+	DQd8-	DQd10-	DQ0-	GND_DR	DQ2+	DQ2-	V
W	DCLK _RST-	GND	DNC	DDRPh	RCLK-	V_A	GND	GND_E	V_E	DQd0-	DQd2+	DQd3-	DQd5+	DQd6-	DQd8+	DQd9-	DQd10+	DQ0+	DQ1+	DQ1-	W
Y	GND	V_A	FSR	RCLK+	RCOut1+	V_A	GND	V_E	GND_E	DQd0+	V_DR	DQd3+	GND_DR	DQd6+	V_DR	DQd9+	GND_DR	DQd11+	DQd11-	GND_DR	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

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FIGURE 1. ADC12D1800RF Connection Diagram

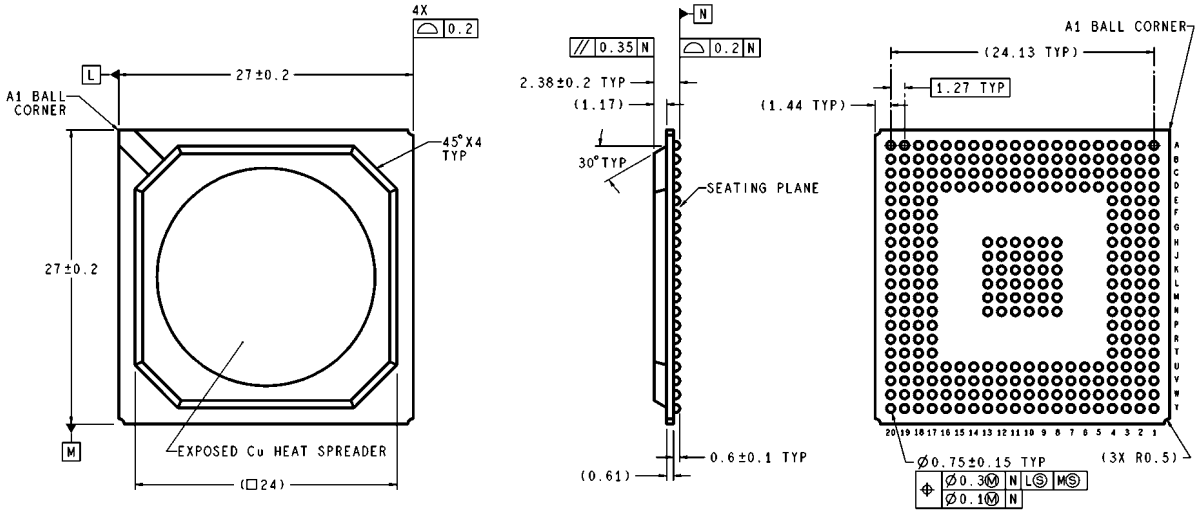
The center ground pins are for thermal dissipation and must be soldered to a ground plane to ensure rated performance.

8.0 Ordering Information

Industrial Temperature Range (-40°C < T_A < +85°C)	NS Package
ADC12D1800RFIUT/NOPB	Lead-free 292-Ball BGA Thermally Enhanced Package
ADC12D1800RFRB	Reference Board

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. IBIS models are available at: http://www.national.com/analog/adc/ibis_models.

8.0 Physical Dimensions inches (millimeters) unless otherwise noted



DIMENSIONS ARE IN MILLIMETERS

UFH292A (Rev A)

NOTES: UNLESS OTHERWISE SPECIFIED

REFERENCE JEDEC REGISTRATION MS-034, VARIATION BAL-2.

292-Ball BGA Thermally Enhanced Package
Order Number ADC12D1800RFUIT
NS Package Number UFH292A

Notes

Notes

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