National Semiconductor

ADC1210/ADC1211 12-Bit CMOS A/D Converters

General Description

The ADC1210, ADC1211 are low power, medium speed, 12-bit successive approximation, analog-to-digital converters. The devices are complete converters requiring only the application of a reference voltage and a clock for operation. Included within the device are the successive approximation logic, CMOS analog switches, precision laser trimmed thin film R-2R ladder network and FET input comparator.

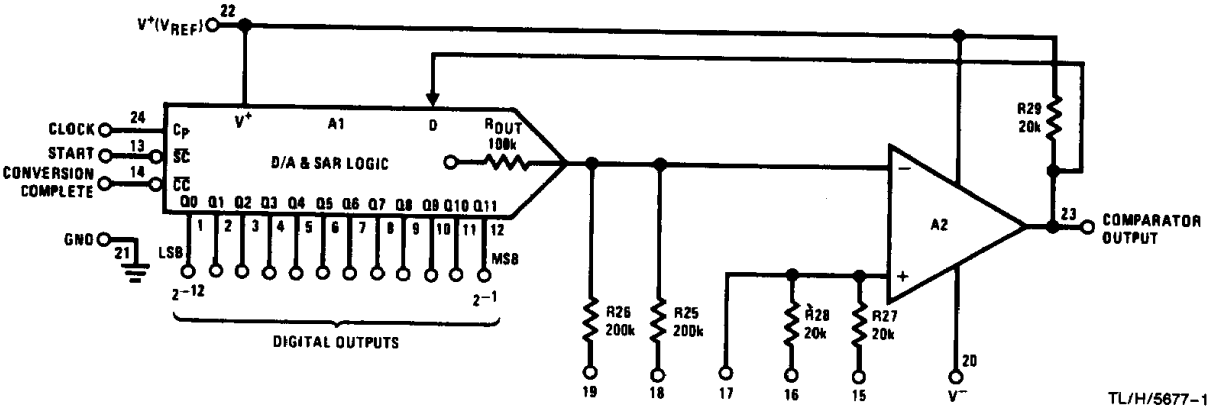
The ADC1210 offers 12-bit resolution and 12-bit accuracy, and the ADC1211 offers 12-bit resolution with 10-bit accuracy. The inverted binary outputs are directly compatible with CMOS logic. The ADC1210, ADC1211 will operate over a wide supply range, convert both bipolar and unipolar analog inputs, and operate in either a continuous conversion mode or logic-controlled START-STOP conversion mode. The devices are capable of making a 12-bit conversion in 100 μs typ, and can be connected to convert 10 bits in 30 μs.

Both devices are available in military and industrial temperature ranges.

Features

- 12-bit resolution
- ±¾ LSB or ±2 LSB nonlinearity
- Single +5V to ±15V supply range
- 100 μs 12-bit, 30 μs 10-bit conversion rate
- CMOS compatible outputs
- Bipolar or unipolar analog inputs
- 200 kΩ analog input impedance

Block Diagram



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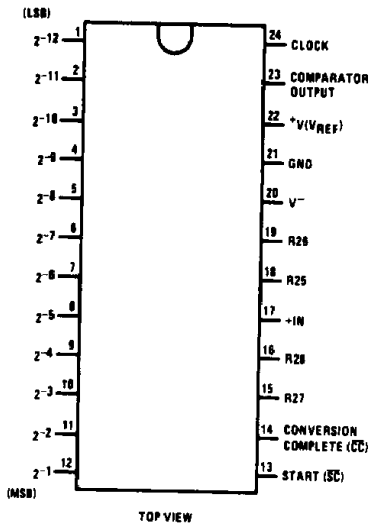
Connection Diagram

Dual-In-Line Package



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Order Number ADC1210HD, ADC1210HCD, ADC1211HD, ADC1211HCD
See NS Package D24D

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Maximum Reference Supply Voltage (V^+)	16V
Maximum Negative Supply Voltage (V^-)	−20V
Voltage At Any Logic Pin	$V^+ + 0.3V$
Analog Input Voltage	±15V
Maximum Digital Output Current	±10 mA
Maximum Comparator Output Current	50 mA
Comparator Output Short-Circuit Duration	5 Seconds
Power Dissipation	See Curves
Operating Temperature Range	
ADC1210HD, ADC1211HD	−55°C to +125°C
ADC1210HCD, ADC1211HCD	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
ESD Susceptibility (Note 4)	TBD V

DC Electrical Characteristics (Notes 1 and 2)

Parameter	Conditions	ADC1210			ADC1211			Units
		Min	Typ	Max	Min	Typ	Max	
Resolution		12			12			Bits
Linearity Error	(Note 3) f_{CLK} = 65 kHz, T_A = 25°C f_{CLK} = 65 kHz			 ±0.0183 ±0.0366			±0.0488	 % FS % FS
Full Scale Error	T_A = 25°C, Unadjusted			0.20			0.50	% FS
Zero Scale Error	T_A = 25°C, Unadjusted			0.20			0.50	% FS
Quantization Error				±1/2			±1/2	LSB
Input Resistor Values	R27, R28		20			20		kΩ
Input Resistor Values	R25, R26		200			200		kΩ
Input Resistor Ratios	R25/R26, R27/R28			0.8			0.8	%
Logic "1" Input Voltage		8			8			V
Logic "0" Input Voltage				2			2	V
Logic "1" Input Current	V_{IN} = 10.24V			1			1	μA
Logic "0" Input Current	V_{IN} = 0V			−1			−1	μA
Logic "1" Output Voltage	$I_{OUT} \leq -1$ μA	9.2			9.2			V
Logic "0" Output Voltage	$I_{OUT} \leq 1$ μA			0.5			0.5	V
Positive Supply Current	V^+ = 15V, f_{CLK} = 65 kHz, T_A = 25°C		5	8		5	8	mA
Negative Supply Current	V^- = −15V, T_A = 25°C		4	6		4	6	mA

AC Electrical Characteristics T_A = 25°C, (Notes 1 and 2)

Parameter	Conditions	Min	Typ	Max	Units
Conversion Time			100	200	μs
Maximum Clock Frequency			130	65	kHz
Clock Pulse Width		100	50		ns
Propagation Delay From Clock to Data Output	$t_r \leq t_f \leq 10$ ns		60	150	ns
(Q0 to Q11)					
Propagation Delay from Clock to Conversion	$t_r \leq t_f \leq 10$ ns		60	150	ns
Complete					
Clock Rise and Fall Time				5	μs
Input Capacitance			10		pF
Start Conversion Set-Up Time		30			ns

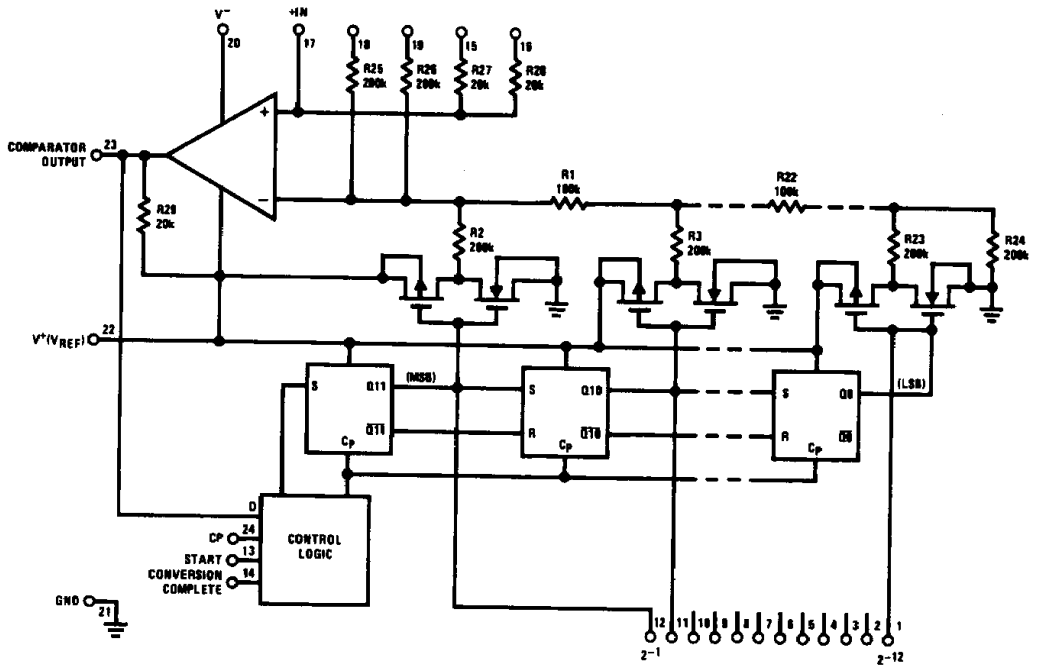
Note 1: Unless otherwise noted, these specifications apply for V^+ = 10.240V, V^- = −15V, over the temperature range −55°C to +125°C for the ADC1210HD, ADC1211HD, and −25°C to +85°C for the ADC1210HCD, ADC1211HCD.

Note 2: All typical values are for T_A = 25°C.

Note 3: Unless otherwise noted, this specification applies over the temperature range −25°C to +85°C. Provision is made to adjust zero scale error to 0V and full-scale to 10.2375V during testing. Standard linearity test circuit is shown in *Figure 5a*.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Schematic Diagram



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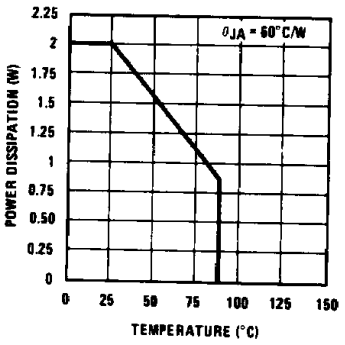
Note: 3 bits shown for clarity

Power Dissipation vs Temperature



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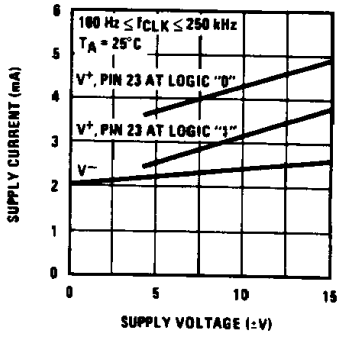
Supply Current vs Supply Voltage



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1.0 THEORY OF OPERATION

The ADC1210, ADC1211 are successive approximation analog-to-digital converters, i.e., the conversion takes place 1 bit at a time by comparing the output of the internal D/A to the (unknown) input voltage. The START input (pin 13), when taken low, causes the register to reset synchronously on the next CLOCK low-to-high transition. The MSB, Q11 is set to the low state, and the remaining bits, Q0 through Q10, will be set to the high state. The register will remain in this state until the $\overline{SC}$ input is taken high. When START goes high, the conversion will begin on the low-to-high transition of the CLOCK pulse. Q11 will then assume the state of pin 23. If pin 23 is high, Q11 will be high; if pin 23 is low, Q11 will remain low. At the same time, the next bit Q10 is set low. All remaining bits, Q0–Q9 will remain unchanged (high). This process will continue until the LSB (Q0) is found. When the conversion process is completed, it is indicated by CONVERSION COMPLETE ($\overline{CC}$) (pin 14) going low. The logic levels at the data output pins (pins 1–12) are the complemented-binary representation of the converted analog signal with Q11 being the MSB and Q0 being the LSB. The register will remain in the above state until the $\overline{SC}$ is again taken low.

An application example is shown in *Figure 1*. In this case, a 0 to −10.2375V input is being converted using the ADC1210 with V+ = 10.240V, V− = −15V. *Figure 1b* is the timing diagram for full scale input. *Figure 1c* is the timing diagram for zero scale input, *Figure 1d* is the timing diagram for −3.4125V input (010101010101 = output).

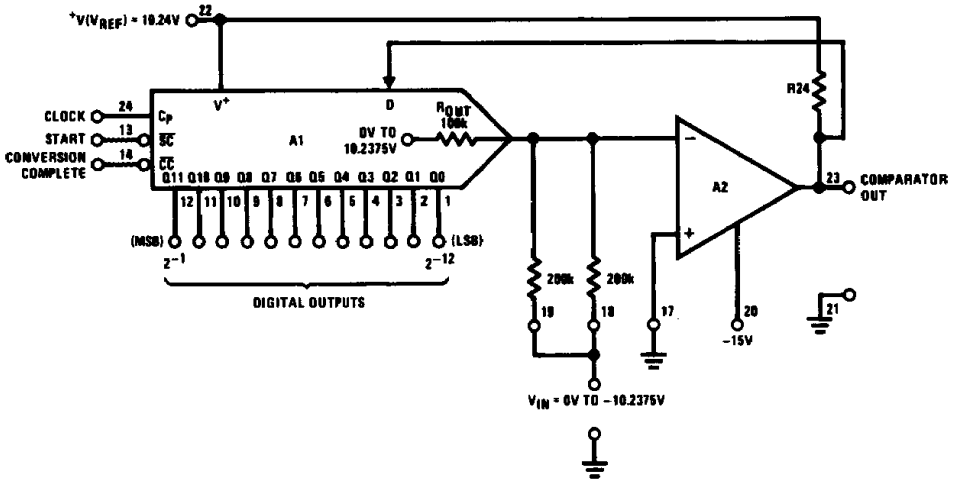

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FIGURE 1a. ADC1210 Connected for 0V to −10.2375V (Natural Binary Output)

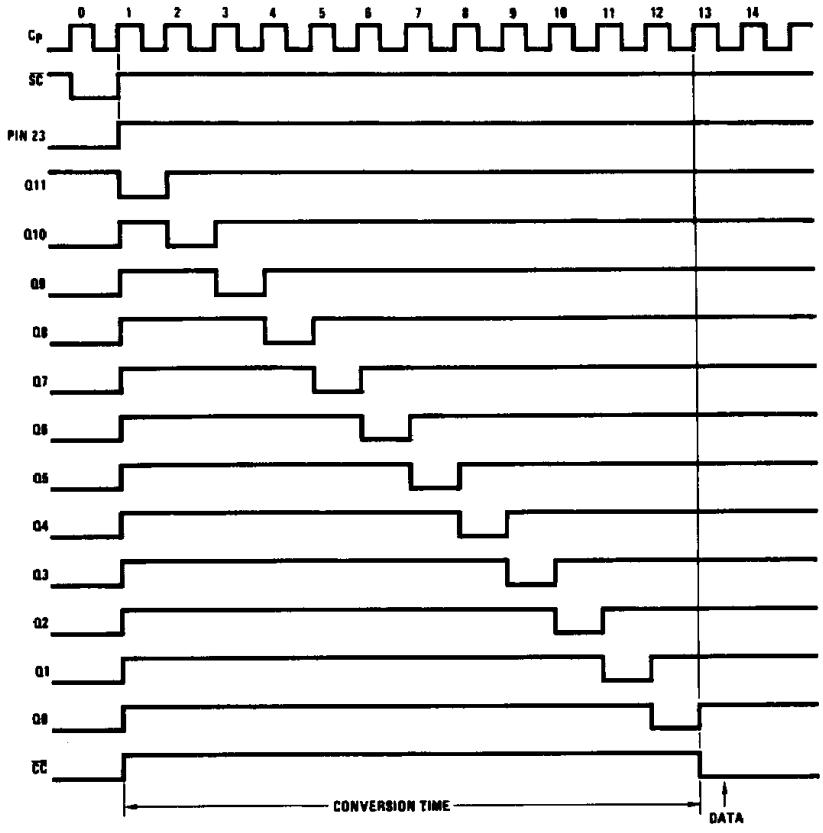

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FIGURE 1b. Timing Diagram for V_{IN} = Full Scale Input

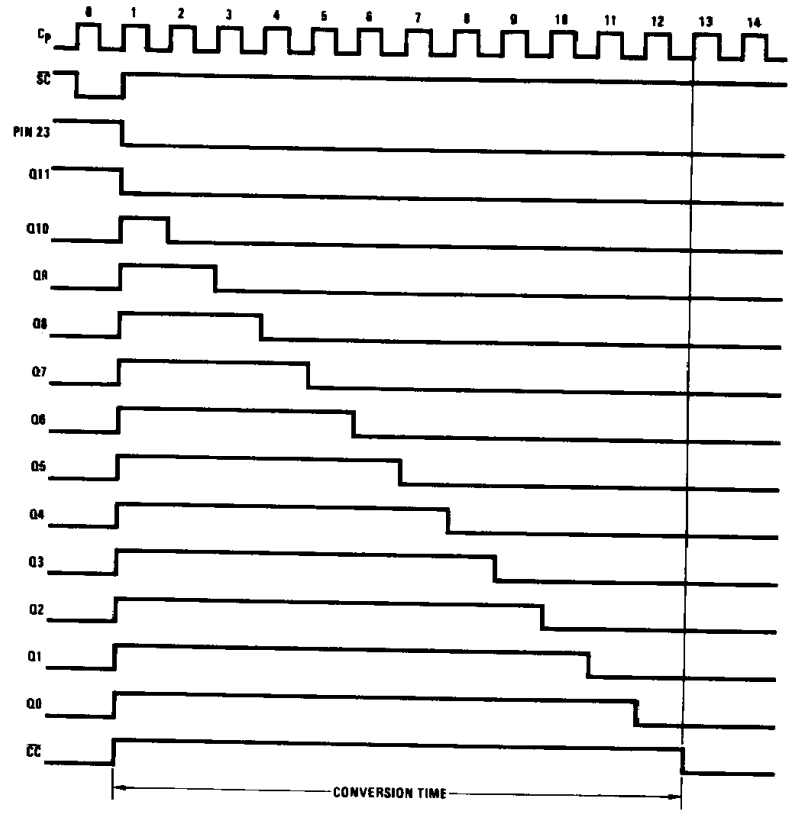

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FIGURE 1c. Timing Diagram for V_{IN} = Zero Scale

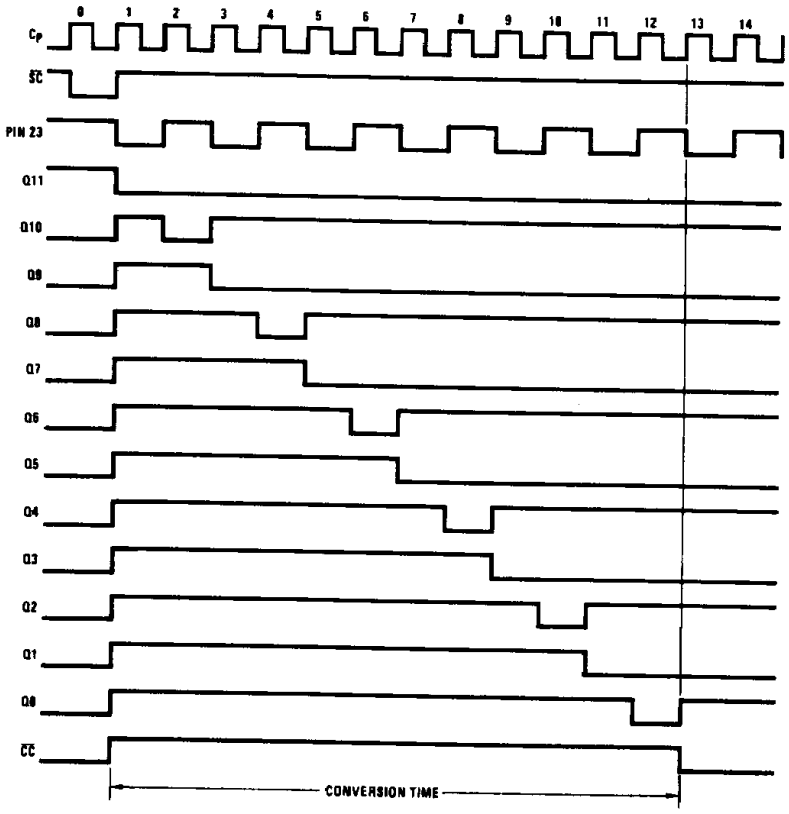

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FIGURE 1d. Timing Diagram for V_{IN} = −3.4125V (010101010101)

TABLE 1. Pin Assignments and Explanations

Pin Number	Mnemonic	Function
1–12	Q11–Q0	Digital (data) output pins. This information is a parallel 12-bit complemented binary representation of the converted analog signal. All data is valid when "Conversion Complete" goes low. Logic levels are ground and V^+.
13	$\overline{SC}$	Start Conversion is a logic input which causes synchronous reset of the successive approximation register and initiates conversion. Logic levels are ground and V^+.
14	$\overline{CC}$	"Conversion Complete" is a digital output signal which indicates the status of the converter. When $\overline{CC}$ is high, conversion is taking place, when low conversion is completed. Logic levels are ground and V^+.
15, 16	R27, R28	R27 and R28 are two application resistors connected to the comparator non-inverting input. The resistors may be used in various modes of operation. Their nominal values are 20 kΩ each. See Applications section.
17	+IN	Non-inverting input of the analog comparator. This node is used in various configurations and for compensation of the loop. See Applications section.
18, 19	R25, R26	R25 and R26 are two application resistors that are tied internally to the inverting input of the comparator. Their nominal values are 200 kΩ each. See Applications section. The R-2R ladder network will have the same temperature coefficient as these resistors.
20	V^-	Negative supply voltage for bias of the analog comparator. Optionally may be grounded or operated with voltages to −20V.
21	GND	Ground for both digital and analog signals.
22	V^+ (V_{REF})	V^+ sets both maximum full scale and input and output logic levels.
23	CO	Comparator output.
24	C_P	Clock is an input which causes the successive approximation (shift) register to advance through the conversion sequence. Logic levels are ground and V^+.

2.0 APPLICATIONS

2.1 Power Supply Considerations and Decoupling

Pin 22 is both the positive supply and voltage reference input to the ADC1210, ADC1211. The magnitude of V^+ determines the input logic "1" threshold and the output voltage from the CMOS SAR. The device will operate over a range of V^+ from 5V to 15V. However, in order to preserve 12-bit accuracy, V^+ should be well regulated (0.01%) and isolated from external switching transients. It is therefore recommended that pin 22 be decoupled with a 4.7 μF tantalum capacitor in parallel with a 0.1 μF ceramic disc capacitor.

The V^- supply (pin 20) provides negative bias for the FET comparator. Although pin 20 may be grounded in some applications, it must be at least 2V more negative than the most negative analog input signal. When a negative supply is used, pin 20 should also be bypassed with 4.7 μF in parallel with 0.1 μF.

Grounding and circuit layout are extremely important in preserving 12-bit accuracy. The user is advised to employ separate digital and analog returns, and to make these PC board traces as "heavy" as practical.

2.2 Short Cycle for Improved Conversion Time (Figure 2)

The ADC1210, ADC1211 counting sequence may be truncated to decrease conversion time. For example, when using the ADC1211, 2 clock intervals may be "saved" if 10-bit conversion accuracy is taking place. The Q2 output should be "OR'd" with CONVERSION COMPLETE ($\overline{CC}$) in order to ensure that the register does not lock-up upon power turn-on.

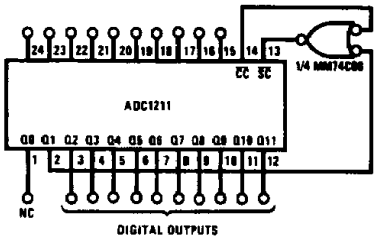

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FIGURE 2. Short Cycling the ADC1211 to Improve 10-Bit Conversion Time (Continuous Conversion)

2.3 Logic Compatibility

The ADC1210, ADC1211 is intended to interface with CMOS logic levels: i.e., the logic inputs and outputs are directly compatible with series 54C/74C and CD4000 family of logic components. The outputs of the ADC1210, ADC1211 will not drive LPTTL, TTL or PMOS logic directly without degrading accuracy. Various recommended interface techniques are shown in *Figures 3 and 4.*

2.4 Operating Configurations

Several recommended operating configurations are shown in *Figure 5.*

Applications Information (Continued)

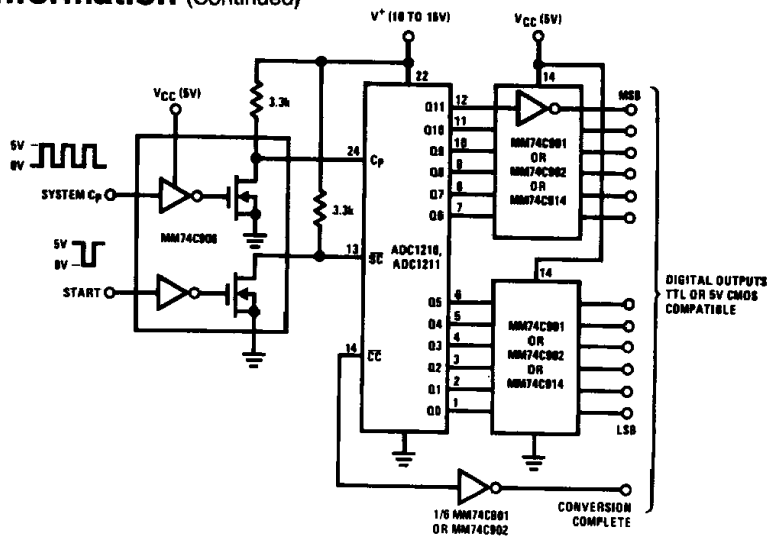

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FIGURE 3. Interfacing an ADC1210, ADC1211 Running on $V^+ > V_{CC}$. Example: $V^+ = 10.24V$, System $V_{CC} = 5V$

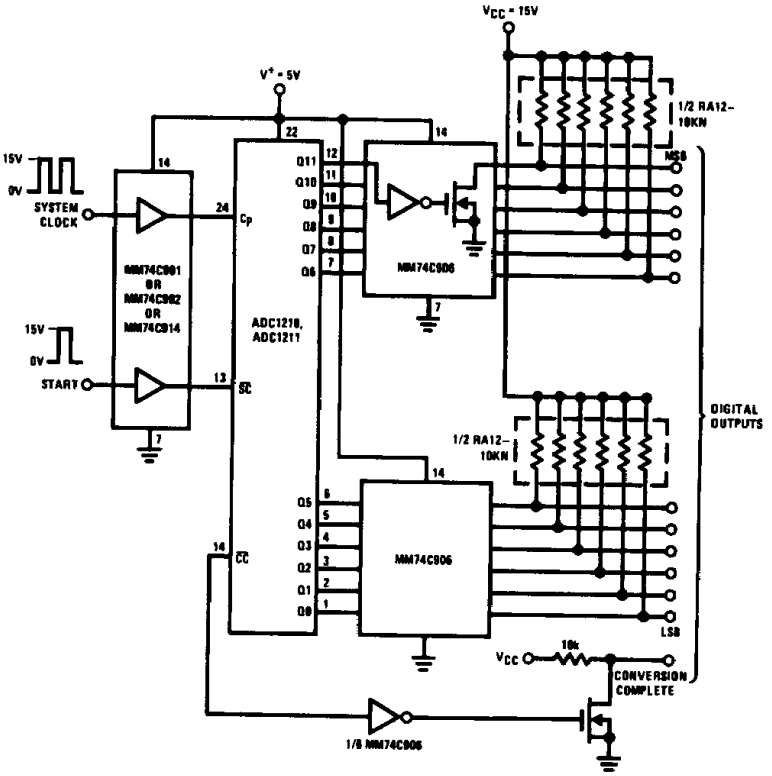

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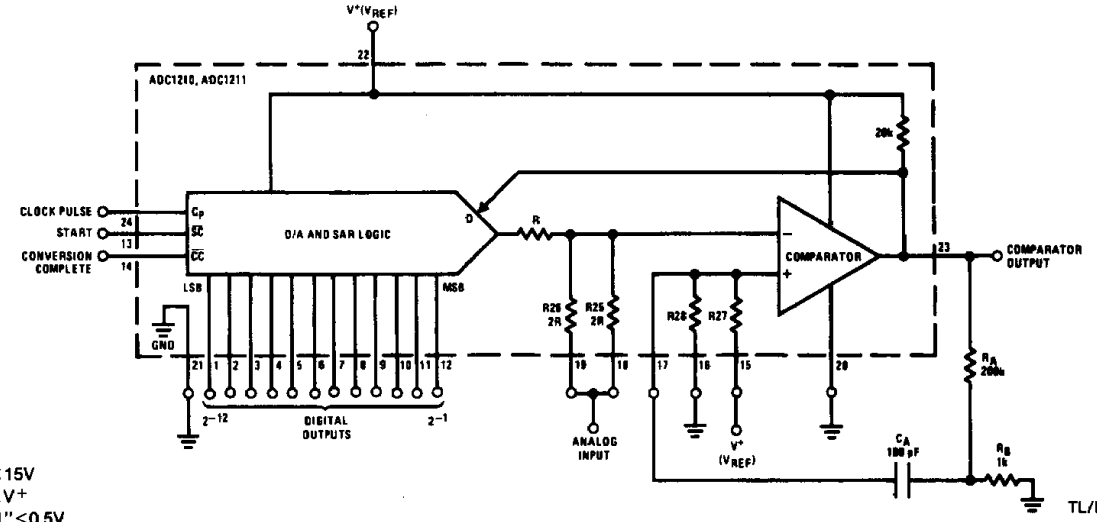
FIGURE 4. Interfacing an ADC1210, ADC1211 Running on $V^+ < V_{CC}$. Example: $V^+ = 5V$, $V_{CC} = 15V$

2.5 Offset and Full Scale Adjust

A variety of techniques may be employed to adjust Offset and Full Scale on the ADC1210, ADC1211. A straight-forward Full Scale Adjust is to incrementally vary V^+ (V_{REF}) to match the analog input voltage. A recommended technique is shown in *Figure 6*. An LM199 and low drift op amp(e.g., the LH0044) are used to provide the precision reference. The ADC1210, ADC1211 is put in the continuous convert mode by shorting pins 13 and 14. An analog voltage equal to V_{REF} minus 1½ LSB (10.23625V) is applied to pins 18 and 19, and R1 is adjusted until the LSB flickers equally between logic "1" and logic "0" (all other outputs must be stable logic "0"). Offset Null is accomplished by then applying an analog input voltage equal to ½ LSB at pins 18 and 19. R2 is adjusted until the LSB output flickers equally between logic "1" and logic "0" (all other bits are stable). In the circuit of *Figure 6*, the ADC1210, ADC1211 is configured for Complementary Binary logic and the values shown are for $V^+ = 10.240V$, $V_{FS} = 10.2375V$, LSB = 2.5 mV.

An alternate technique is shown in *Figure 7*. In this instance, an LH0071 is used to provide the reference voltage. An analog input voltage equal to V_{REF} minus 1½ LSB (10.23625V) is applied to pins 18 and 19.

Applications Information (Continued)



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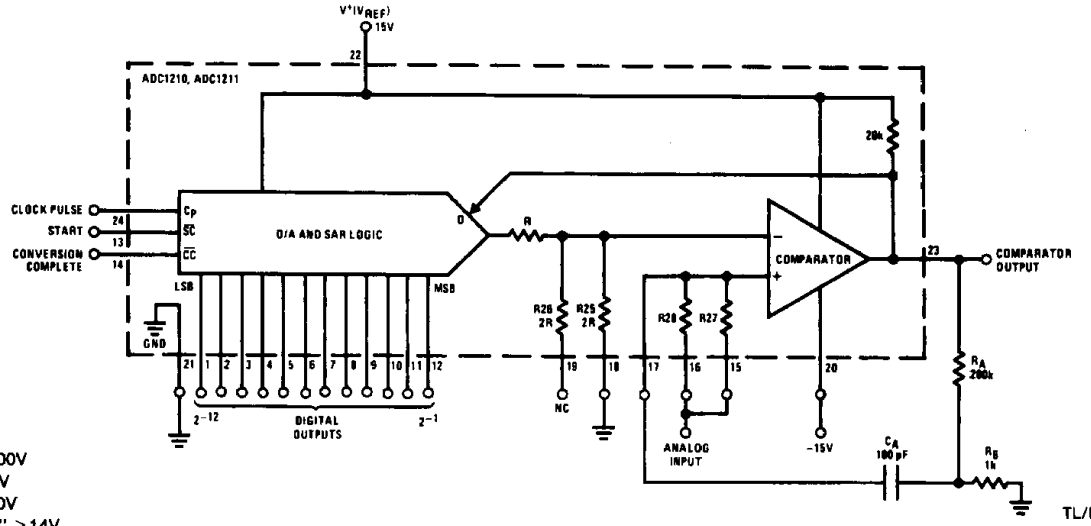
$5V \leq V^+ \leq 15V$
$0V \leq V_{IN} \leq V^+$
Logical "1" $\leq 0.5V$
Logical "0" $\cong V^+$

FIGURE 5a. Single Supply Configuration, Complementary Logic



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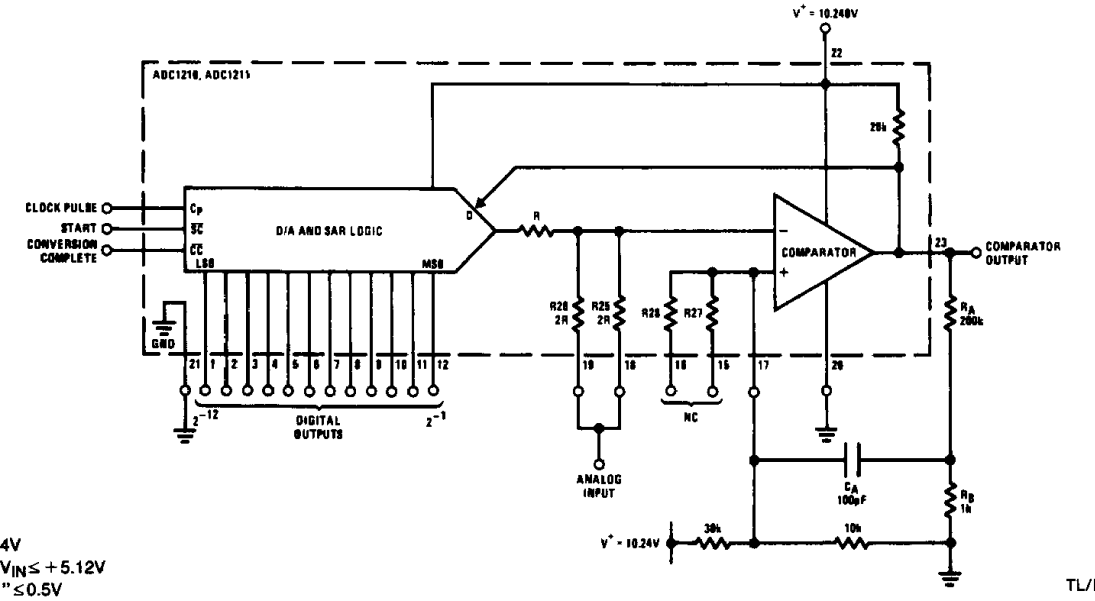
$V^+ = 15.000V$
$V^- = -15V$
$0 \leq V_{IN} \leq 10V$
Logical "1" $\geq 14V$
Logical "0" $\leq 0.5V$

FIGURE 5b. High Voltage CMOS Compatible, 0V to 10V Input



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$V^+ = 10.24V$
$-5.12V \leq V_{IN} \leq +5.12V$
Logical "1" $\leq 0.5V$
Logical "0" $\cong 10V$

FIGURE 5c. Bipolar Input, Complementary Logic

Applications Information (Continued)

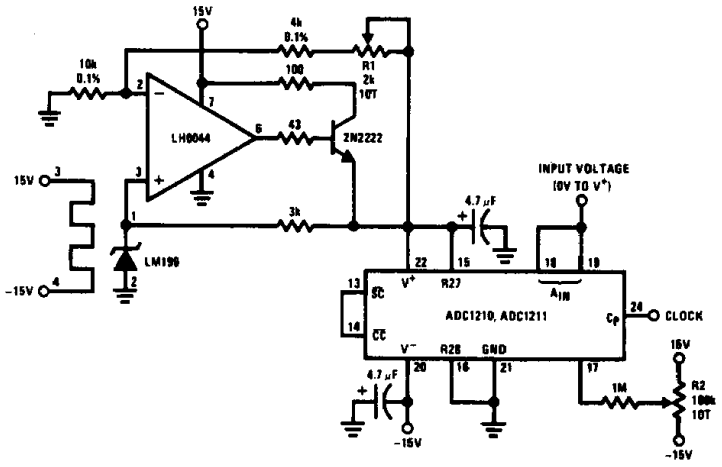

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FIGURE 6. Offset and Full Scale Adjustment for Complementary Binary

R1 is adjusted until the LSB output flickers equally between logic "1" and logic "0" (all other outputs must be a stable logic "0"). For Offset Null, an analog voltage equal to 1/2 LSB (1.25 mV) is then applied to pins 18 and 19, and R2, is adjusted until the LSB output flickers equally between logic "1" and "0".

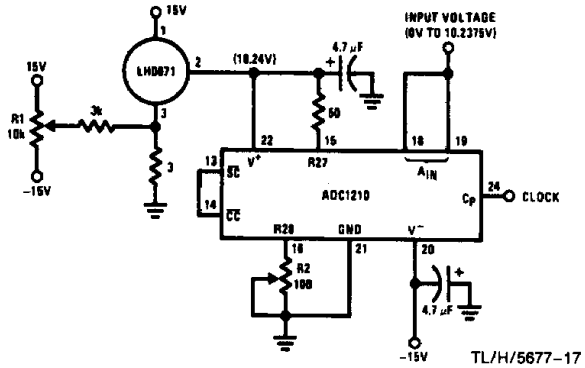

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FIGURE 7. Offset and Full-Scale Adjustment Technique Using LH0071

In both techniques shown, adjusting the Full-Scale first and then Offset minimizes adjustment interaction. At least one iteration is recommended as a self-check.

2.6 START PULSE CONSIDERATIONS

To assure reliable conversion accuracy, the $\overline{\text{START}}$ ($\overline{\text{SC}}$) pulse applied to pin 13 of the ADC1210 should be synchronized to the conversion clock. One simple way to do that is the circuit shown in *Figure 8*. Note that once a conversion cycle is initiated, the $\overline{\text{START}}$ signal cannot effect the conversion operation until it is completed.

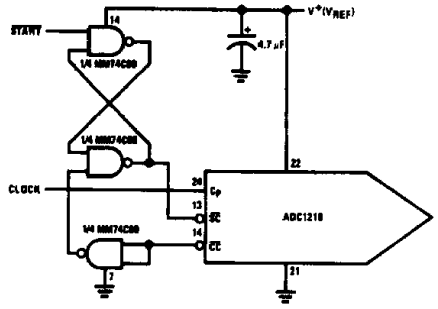

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FIGURE 8. Synchronizing the $\overline{\text{START}}$ Pulse

The circuit insures that in no case can the ADC1210 make an error in the Most Significant Bit (MSB) decision. Without the circuit, it is possible for energy from the trailing edge of an asynchronous $\overline{\text{START}}$ pulse to be coupled into the ADC1210's comparator. If the analog input is near half-scale, the charge injected can force an error in the MSB decision. The circuit allows one clock period for this energy to dissipate before the decision is recorded.

2.7 ADC1210 CONVERSION AT 26 μs

The ADC1210 can run at 500 kHz clock frequency, or 12-bit conversion time of 26 μs (*Figure 9*). The comparator output is clamped low until the successive approximation register (SAR) is ready to strobe in the data at the rising edge of the conversion clock. Comparator oscillation is suppressed and kept from influencing the conversion decisions, eliminating the need for the AC hysteresis circuit above clock frequency of 65 kHz that is recommended.

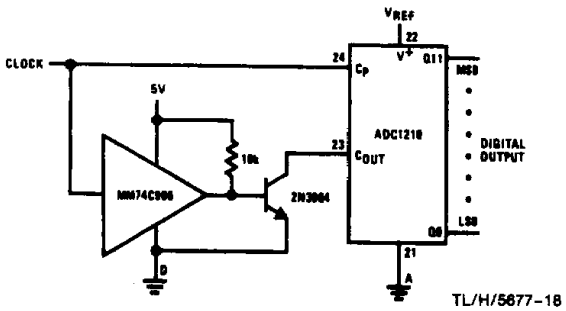

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FIGURE 9. Conversion at 26 μs

A complementary phased clock is required. The positive phase is used to clock the converter SAR as is normally the case. The same signal is buffered and inverted by the transistor. The open collector is wire-ORed to the output of the comparator. During the first half of the clock cycle (50% duty cycle), the comparator output is clamped and disabled, though its internal operation is still in normal working order. The last half cycle of the clock unclamps the comparator output. Thus, the output is permitted to slew to the final logic state just before the decision is logged into the SAR. The MM74C906 buffer (or with two inverting buffers) provides adequate propogation delay such that the comparator output data is held long enough to resolve any internal logic setup time requirements.

Applications Information (Continued)

The 500 kHz clock implies that the absolute minimum amount of time for the comparator output is *unclamped* is 1 μs. Therefore, if the clock is not 50% duty cycle, this 1 μs requirement must be observed.

3.0 DEFINITION OF TERMS

Resolution: The Resolution of an A/D is an expression of the smallest change in input which will increment (or decrement) the output from one code to the next adjacent code. It is defined in number of bits, or 1 part in 2^n. The ADC1210 and ADC1211 have a resolution of 12 bits or 1 part in 4,096 (0.0244%).

Quantization Uncertainty: Quantization Uncertainty is a direct consequence of the resolution of the converter. All analog voltages within a given range are represented by a single digital output code. There is, therefore, an inherent conversion error even for a perfect A/D. As an example, the transfer characteristic of a perfect 3-bit A/D is shown in *Figure 10*.

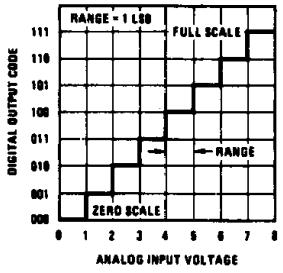

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FIGURE 10. Quantization Uncertainty of a Perfect 3-Bit A/D

As can be seen, all input voltages between 0V and 1V are represented by an output code of 000. All input voltages between 1V and 2V are represented by an output code of 001, etc. If the midpoint of the range is assumed to be the nominal value (e.g., 0.5V), there is an Uncertainty of ±1/2 LSB. It is common practice to offset the converter 1/2 LSB in order to reduce the Uncertainty to ±1/2 LSB is shown in *Figure 11*, rather than +1, −0 shown in *Figure 10*. Quantization Uncertainty can only be reduced by increasing Resolution. It is expressed as ±1/2 LSB or as an error percentage of full scale (±0.0122% FS for the ADC1210).

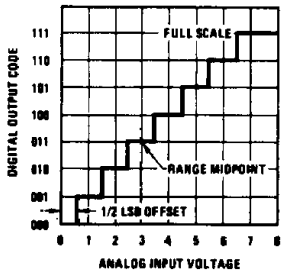

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FIGURE 11. Transfer Characteristic Offset 1/2 LSB to Minimize Quantizing Uncertainty

Linearity Error: Linearity Error is the maximum deviation from a straight line passing through the end points of the A/D transfer characteristic. It is measured after calibrating Zero and Full Scale Error. Linearity is a performance characteristic intrinsic to the device and cannot be externally adjusted.

Zero Scale Error (or Offset): Zero Scale Error is a measure of the difference between the output of an ideal and the actual A/D for zero input voltage. As shown in *Figure 12*, the effect of Zero Scale Error is to shift the transfer characteristic to the right or left along the abscissa. Any voltage more negative than the LSB transition gives an output code of 000. In practice, therefore, the voltage at which the 000 to 001 transition takes place is ascertained, this input voltage's departure from the ideal value is defined as the Zero Scale Error (Offset) and is expressed as a percentage of FS. In the example of *Figure 12*, the offset is 2 LSB's or 0.286% of FS.

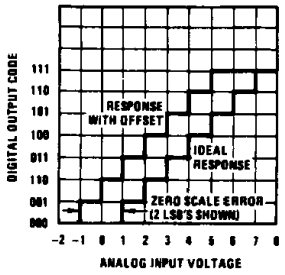

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FIGURE 12. A/D Transfer Characteristic with Offset

The Zero Scale Error of the ADC1210, ADC1211 is caused primarily by offset voltage in the comparator. Because it is common practice to offset the A/D 1/2 LSB to minimize Quantization Error, the offsetting techniques described in the Applications Section may be used to null Zero Scale Error and accomplish the 1/2 LSB offset at the same time.

Full Scale Error (or Gain Error): Full Scale Error is a measure of the difference between the output of an ideal A/D converter and the actual A/D for an input voltage equal to full scale. As shown in *Figure 13*, the Full Scale Error effect is to rotate the transfer characteristic angularly about the origin. Any voltage more positive than the Full Scale transition gives an output code of 111. In practice, therefore, the voltage at which the transition from 111 to 110 occurs is ascertained. The input voltage's departure from the ideal value is defined as Full Scale Error and is expressed as a percentage of FS. In the example of *Figure 13*, Full Scale Error is 1 1/2 LSB's or 0.214% of FS.

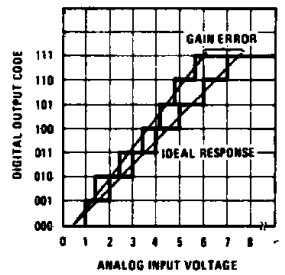

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FIGURE 13. Full Scale (Gain Error)

Full Scale Error of the ADC1210, ADC1211 is due primarily to mismatch in the R-2R ladder equivalent output impedance and input resistors R25, R26, R27, and R28. The gain error may be adjusted to zero as outlined in section 2.5.

Applications Information (Continued)

Monotonicity and Missing Codes: Monotonicity is a property of a D/A which requires an increasing or constant output voltage for an increasing digital input code. Monotonicity of a D/A converter does not, in itself, guarantee that an A/D built with that D/A will not have missing codes. However, the ADC1210 and ADC1211 are guaranteed to have no missing codes.

Conversion Time: The ADC1210, ADC1211 are successive approximation A/D converters requiring 13 clock intervals for a conversion to specified accuracy for the ADC1210 and 11 clocks for the ADC1211. There is a trade-off between accuracy and clock frequency due to settling time of the ladder and propagation delay through the comparator. By modifying the hysteresis network around the comparator, conversions with 10-bit accuracy can be made in 30 μs. Replace R_A, R_B and C_A in *Figure 5* with a 10 MΩ resistor between pin 23 (Comparator Output) and pin 17 (+ IN), and increase the clock rate to 366 kHz.

In order to prevent errors during conversion, the analog input voltage should not be allowed to change by more than $\pm 1/2$ LSB. This places a maximum slew rate of 12.5 $\mu V/\mu s$ on the analog input voltage. The usual solution to this restriction is to place a Sample and Hold in front of the A/D. For additional application information, refer to application note AN245.