STLC3075

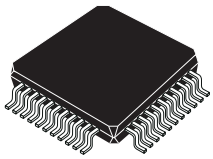
Integrated POTS interface for home access gateway and WLL

Features

- Monochip SLIC optimized for WLL & VoIP applications
- Implements all Borsht function key features
- Single supply (4.5V to 12V) for fly-back configuration
- Single supply (5.5V to 12V) for buck-boost configuration
- Built in DC/DC converter controller
- Soft battery reversal with programmable transition time
- On-hook transmission
- Programmable off-hook detector threshold
- Metering pulse generation and filter
- Integrated ringing
- Integrated ring trip
- Parallel control interface (3.3V logic level)
- Programmable constant current feed
- Surface mount package
- Integrated thermal protection
- Dual gain value option
- Automatic recognition flyback and buckboost configuration
- BCDIIIS 90V technology
- -40 °C to +85°C operating range

Description

The STLC3075 is a SLIC device specifically designed for WLL (Wireless Local Loop), and ISDN terminal adaptors and VoIP applications. One distinctive characteristic of this device is its ability to operate with a single supply voltage (from +4.5V to +12V) and to self generate the negative battery by means of an on-chip DC/DC converter controller that drives an external MOS switch.



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The battery level is properly adjusted depending on the operating mode. A useful characteristic for these applications is the integrated ringing generator.

The control interface is parallel with open drain output and 3.3V logic levels.

The metering pulses are generated on-chip starting from two logic signals (0, 3.3V): one signal defining the metering pulse frequency, the other signal defining the metering pulse duration. An on-chip circuit then provides the proper shaping and filtering. Metering pulse amplitude and shaping (rising and decay time) can be programmed by external components.

A dedicated cancellation circuit avoids possible CODEC input saturation due to metering pulse echo.

Constant current feed can be set from 20mA to 40mA. Off-hook detection threshold is programmable from 5mA to 9mA.

The device, which is developed in BCDIIIS technology (90V process), operates in the extended temperature range and integrates a thermal protection that sets the device in power down when T_j exceeds 140°C.

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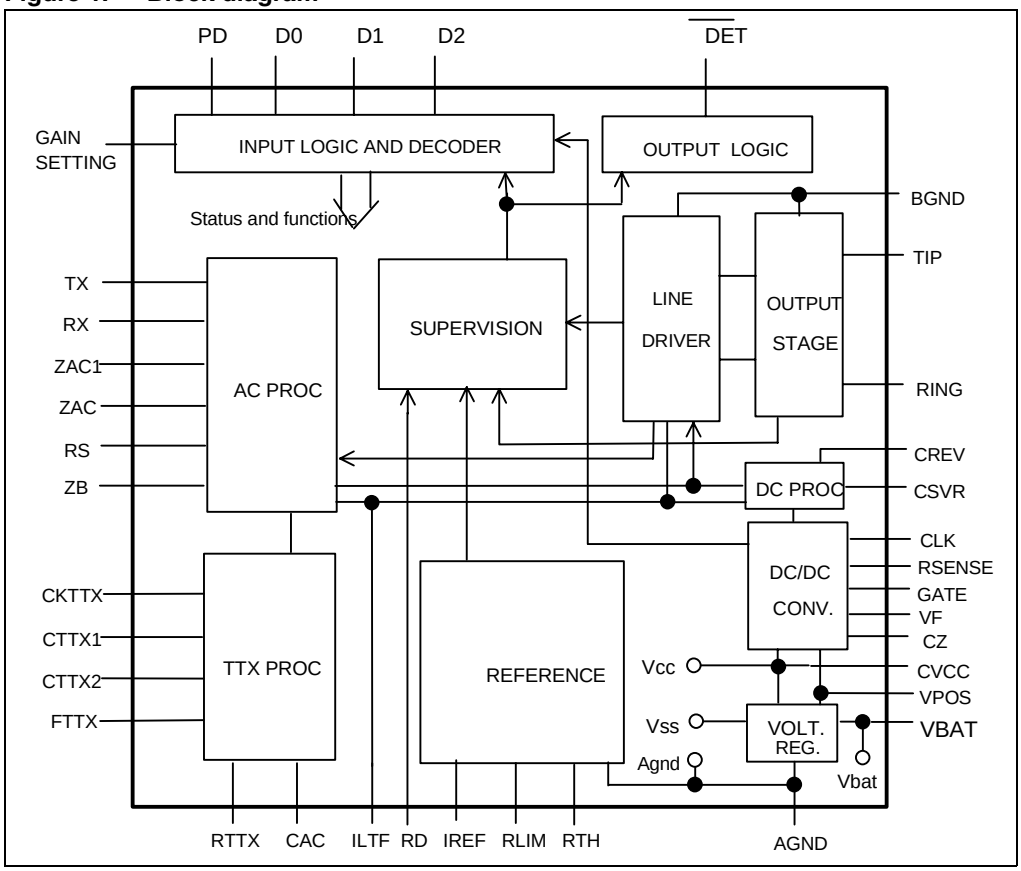
1 Block diagram

Figure 1. Block diagram



2 Pin description

Figure 2. Pin connection

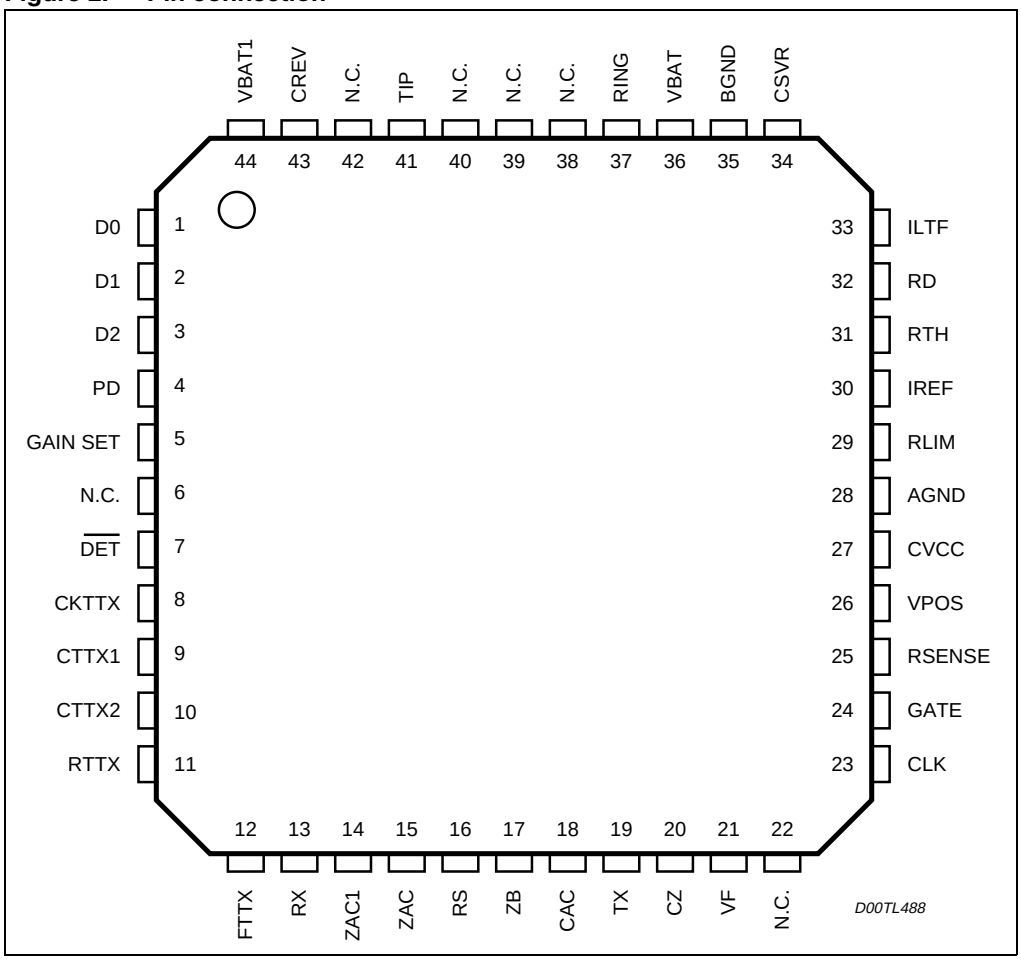


Table 1. Pin description

N°	Pin	Function
1	D0	Control interface: input bit 0
2	D1	Control interface: input bit 1
3	D2	Control interface: input bit 2
4	PD	Power down input. Normally connected to CVCC (or to logic level high)
5	Gain SET	Control gain interface: 0 Level R_{xgain} = 0dB T_{xgain} = -12dB 1 Level R_{xgain} = +6dB T_{xgain} = -12dB
6, 22, 38, 39, 40, 42	NC	Not connected
7	DET	Logic interface output of the supervision detector (active low)
8	CKTTX	Metering pulse clock input (12 kHz or 16kHz square wave)
9	CTTX1	Metering burst shaping external capacitor
10	CTTX2	Metering burst shaping external capacitor
11	RTTX	Metering pulse cancellation buffer output. TTX filter network should be connected to this point. If not used, should be left open.
12	FTTX	Metering pulse buffer input this signal is sent to the line and used to perform TTX filtering
13	RX	4 wires input port (RX input). A 100kΩ external resistor must be connected to AGND via the bias input stage. This signal refers to AGND. If connected to single supply CODEC output it must be DC decoupled with proper capacitor.
14	ZAC1	RX buffer output (the AC impedance is connected from this node to ZAC)
15	ZAC	AC impedance synthesis
16	RS	Protection resistors image (the image resistor is connected from this node to ZAC)
17	ZB	Balance network for 2 to 4 wire conversion (the balance impedance ZB is connected from this node to AGND. ZA impedance is connected from this node to ZAC1).
18	CAC	AC feedback input, AC/DC split capacitor (CAC)
19	TX	4 wire output port (TX output). The signal is referred to AGND. If connected to single supply CODEC input it must be DC decoupled with proper capacitor.
20	CZ	Flyback compensation
21	VF	Feedback input for DC/DC converter controller
23	CLK	Power switch controller clock (typ. 125KHz). This pin can also be connected to CVCC or AGND. When the CLK pin is connected to CVCC an internal auto-oscillation is internally generated and it is used instead of the external clock. When the CLK pin is connected to AGND, the GATE output is disabled.

Table 1. Pin description (continued)

N°	Pin	Function
24	GATE	Driver for external power MOS transistor (P-channel in buckboost configuration, N-channel in flyback configuration).
25	R_{SENSE}	Voltage input for current sensing. R_{SENSE} resistor should be connected close to this pin and V_{POS} pin (Buckboost) or GND (Flyback). The PCB layout should minimize the extra resistance introduced by the copper tracks.
26	V_{POS}	Positive supply input
27	CVCC	Internal positive voltage supply filter
28	AGND	Analog ground. Must be shorted with BGND.
29	RLIM	Constant current feed programming pin (via RLIM). RLIM should be connected close to this pin and AGND pin to avoid noise injection.
30	IREF	Internal bias current setting pin. RREF should be connected close to this pin and AGND pin to avoid noise injection.
31	RTH	Off-hook threshold programming pin (via RTH). RTH should be connected close to this pin and AGND pin to avoid noise injection.
32	RD	DC feedback and ring trip input. RD should be connected close to this pin and AGND pin to avoid noise injection.
33	ILTF	Transversal line current image output
34	CSVR	Battery supply filter capacitor
35	BGND	Battery ground, must be shorted with AGND
36	VBAT	Regulated battery voltage self generated by the device via DC/DC converter. Must be shorted to VBAT1.
37	RING	2 wire ports; RING wire (Ib is the current sunk into this pin)
41	TIP	2 wire ports; TIP wire (Ia is the current sourced from this pin)
43	CREV	Reverse polarity transition time control. A proper capacitor connected between this pin and AGND is setting the reverse polarity transition time. This is the same transition time used to shape the 'trapezoidal ringing' during ringing injection.
44	VBAT1	Frame connection. Must be shorted to VBAT

3 Functional description

The STLC3075 is a device specifically developed for WLL VoIP and ISDN-TA applications. It is based on a SLIC core, on purpose optimized for these applications, with the addition of a DC/DC converter controller to meet the WLL and ISDN-TA design requirements.

The SLIC performs the standard feeding, signalling and transmission functions.

STLC3075 can be set in three different operating modes via the D0, D1, D2 pins of the control logic interface (0 to 3.3V logic levels). The loop status is carried out on the $\overline{DET}$ pin (active low).

The $\overline{DET}$ pin is an open drain output to allow easy interfacing with both 3.3V and 5V logic levels.

The four possible SLIC's operating modes are:

- Power down
- High impedance feeding (HI-Z)
- Active
- Ringing

Table 2 shows how to set the different SLIC operating modes.

Table 2. SLIC operating modes

PD	D0	D1	D2	Operating mode
0	0	0	X	Power down
1	0	0	X	H.I. feeding (HI-Z)
1	0	1	0	Active normal polarity
1	0	1	1	Active reverse polarity
1	1	1	0	Active TTX injection (N.P.)
1	1	1	1	Active TTX injection (R.P.)
1	1	0	0/1	Ring (D2 bit toggles @ fring)

3.1 DC/DC converter

The DC/DC converter controller drives an external power MOS transistor N-Ch plus transformer (Flyback configuration) or P-Ch plus inductor (Buckboost configuration), in order to generate the negative battery voltage needed for the device operation.

The DC/DC converter controller is synchronized with an external CLK (125kHz typ.) or with an internal clock generated when the pin CLK is connected to CVCC. One R_{SENSE} in series to PGND supply (Flyback) or to V_{POS} supply (Buckboost) allows to fix the maximum allowed input peak current.

This feature is implemented in order to avoid overload on V_{POS} supply in case of line transient (ex. ring trip detection). The 110mΩ typical value guarantees an average current consumption from V_{POS} < 700mA for buckboost configuration. The 220mΩ typical value guarantees an average current consumption from V_{POS} < 800mA for flyback configuration.

The self generated battery voltage is set to a predefined value in on-hook state.

The typical value of -50V can be adjusted via one external resistor (RF1). When RING mode is selected this typical value is increased to -70V.

Once the line goes in off-hook condition, the DC/DC converter automatically adjusts the generated battery voltage in order to feed the line with a fixed DC current (programmable via RLIM) optimizing the power dissipation.

3.2 Operating modes

3.2.1 Power down

When this mode is selected the SLIC is switched off and the TIP and RING pins are in high impedance. The line detectors are also disabled therefore the off-hook condition cannot be detected.

The power down mode can be selected in emergency condition when it is necessary to cut any current delivered to the line.

The power down mode is also forced by STLC3075 in case of thermal overload (T_j > 140°C). In this case the device goes back to the previous status as soon as the junction temperature decrease under the hysteresis threshold.

No AC transmission is possible.

3.2.2 High impedance feeding (HI-Z)

This operating mode is normally selected when the telephone is in on-hook in order to monitor the line status keeping the power consumption at the minimum.

The output voltage in on-hook condition is equal to the self generated battery voltage (-50V typical).

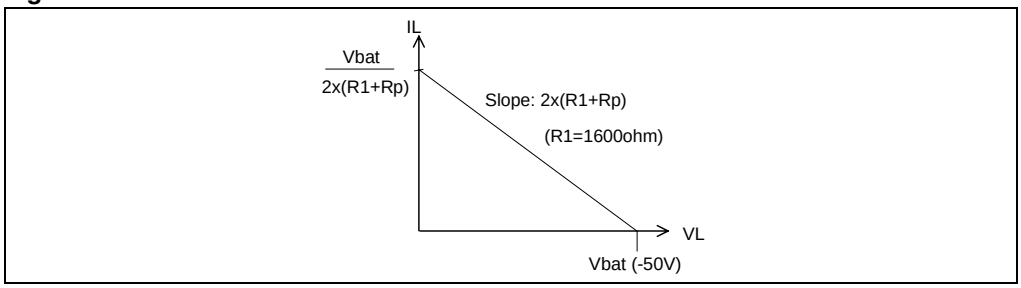
When off-hook occurs the $\overline{DET}$ becomes active (low logic level).

The off-hook threshold value in HI-Z mode is the same as the programmed value in ACTIVE mode.

The DC characteristics in HI-Z mode are equal to the self generated battery with 2x(1600Ω+Rp) in series (see *Figure 3*), where Rp is the external protection resistance.

No AC transmission is possible.

Figure 3. DC characteristics in HI-Z mode.



3.2.3 Active

DC characteristics & supervision

When this mode is selected the STLC3075 provides both DC feeding and AC transmission.

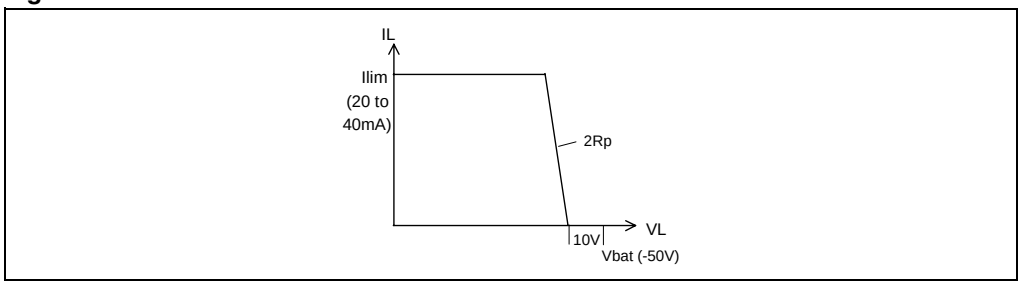
The STLC3075 feeds the line with a constant current fixed by RLIM (20mA to 40mA range). The on-hook voltage is typically 40V allowing on-hook transmission; the self generated Vbat is -50V typical.

If the loop resistance is very high and the line current cannot reach the programmed constant current feed value, the STLC3075 behaves like a 40V voltage source with a series impedance equal to the protection resistors 2xRp (typ. 2x50Ω). *Figure 4.* shows the typical DC characteristics in active mode.

The line status (on/off hook) is monitored by the SLIC'S supervision circuit. The off-hook threshold can be programmed via the external resistor RTH in the range from 5mA to 9mA.

Independently on the programmed constant current value, the TIP and RING buffers have a current source capability limited to 80mA typical.

Figure 4. DC characteristics in active mode



Moreover the power available at Vbat is controlled by the DC/DC converter that limits the peak current drawn from the V_{POS} supply. The maximum allowed current peak is set by R_{SENSE} resistor.

AC characteristics

The SLIC provides the standard SLIC transmission functions.

Once in active mode the SLIC can operate with two different Tx, Rx gains set by the gain set control bit (See *Table 3* below).

Table 3. Gain set in active mode

Gain set	4 to 2 wires gain	2 to 4 wires gain	Impedance synthesis scale factor
0	0dB	-6dB	x 50
1	+6dB	-12dB	x 25

- **Input impedance synthesis**: can be real or complex and is set by a scaled (x50 or x25) external ZAC impedance
- **Transmit and receive**: The AC signal present on the 2W port (TIP/RING) is transferred to the Tx output with a -6dB or -12dB gain and from the Rx input to the 2W port with a 0dB or +6dB gain
- **2 to 4 wires conversion**: The balance impedance can be real or complex, the proper cancellation is obtained by means of two external impedances ZA and ZB

Once in active mode (D1=1) the SLIC can operate in different states setting properly D0 and D2 control bits (see also *Table 4*).

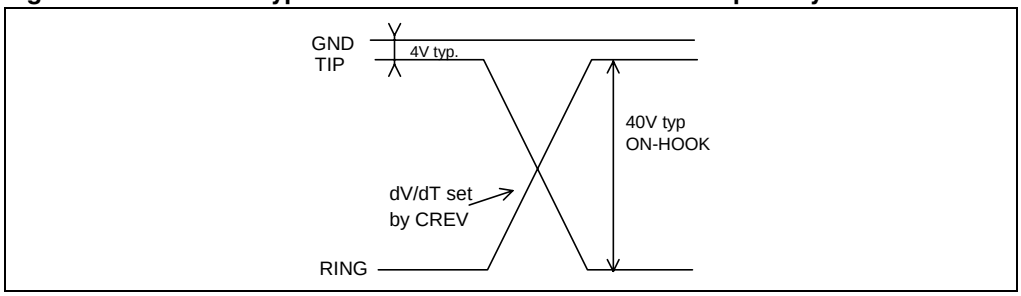
Table 4. SLIC states in active mode

D0	D1	D2	Operating mode
0	1	0	Active normal polarity
0	1	1	Active reverse polarity
1	1	0	Active TTX injection (N.P.)
1	1	1	Active TTX injection (R.P.)

Polarity reversal

The D2 bit controls the line polarity, the transition between the two polarities is performed in a 'soft' way. This means that the TIP and RING wires exchange their polarities following a ramp transition (see *Figure 5*). The transition time is controlled by an external capacitor CREV. This capacitor also sets the shape of the ringing trapezoidal waveform. When the control pins set the battery reversal, the line polarity is reversed with a proper transition time set via an external capacitor (CREV).

Figure 5. TIP/RING typical transition from direct to reverse polarity



Metering pulse injection (TTX)

The metering pulses circuit consists of a burst shaping generator that generates a square shaped wave and a low pass filter to reduce the harmonic distortion of the output signal.

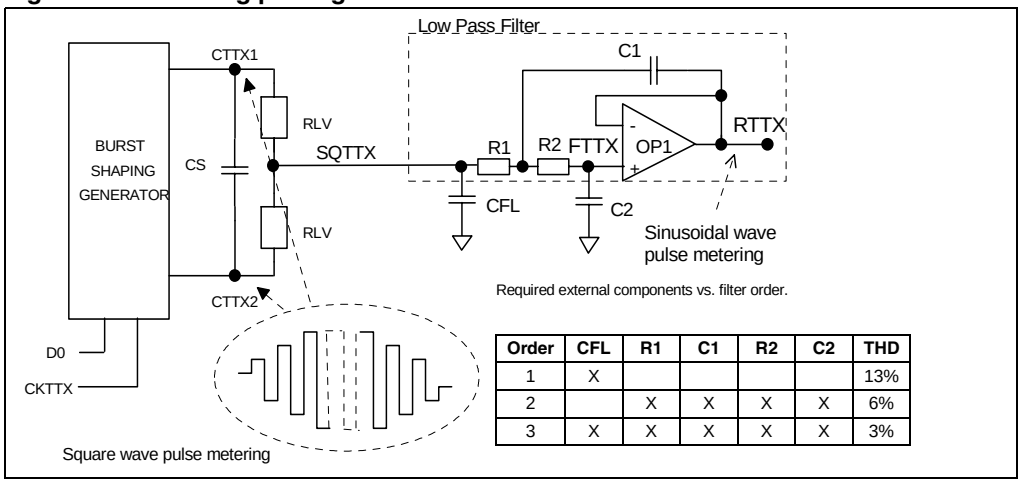
The metering pulse is obtained from two logic signals:

- **CKTTX**: is a square wave at the TTX frequency (12 or 16KHz) that must be permanently applied to the CKTTX pin or at least for all the duration of the TTX pulse (including rising and decay phases).
- **D0**: enables the TTX generation circuit and defines the TTX pulse duration.

These two signals are processed by a dedicated circuitry integrated on chip that generates the metering pulse as an amplitude modulated shaped square wave (SQTTX) (see *Figure 6*).

Both the amplitude and the envelope of the square wave (SQTTX) can be programmed by means of external components. In particular the amplitude is set by the two RLV resistors while the shaping is set by the CS capacitor.

Figure 6. Metering pulse generation circuit



Required external components vs. filter order.

Order	CFL	R1	C1	R2	C2	THD
1	X					13%
2		X	X	X	X	6%
3	X	X	X	X	X	3%

The waveform so generated is then filtered and injected on the line.

The low pass filter is obtained by using the integrated buffer OP1 connected between pin FTTX (OP1 non inverting input) and RTTX (OP1 output) (see *Figure 6*) and by implementing a “Sallen and Key” configuration. Depending on the external components count it is possible to build an optimized application depending on the distortion level required. In particular harmonic distortion levels equal to 13%, 6% and 3% can be obtained respectively with first, second and third order filters (see *Figure 6*).

The circuit showed in the “Application diagram” is related to the simple first order filter.

Once the shaped and filtered signal is obtained at RTTX buffer output it is injected on the TIP/RING pins with a +6dB gain or +12dB gain.

It should be noted that this is the nominal condition obtained in presence of ideal TTX echo cancellation (obtained via proper setting of RTTX and CTTX).

In addition the effective level obtained on the line will depend on the line impedance and the protection resistors value. In typical applications (TTX line impedance =200Ω, RP = 50Ω, and

ideal TTX echo cancellation), the metering pulse level on the line equals 1.33 or 2.66 times the level applied to the RTTX pin.

As already mentioned the metering pulse echo cancellation is obtained by means of two external components (RTTX and CTTX) that should match the line impedance at the TTX frequency. This simple network has a double effect:

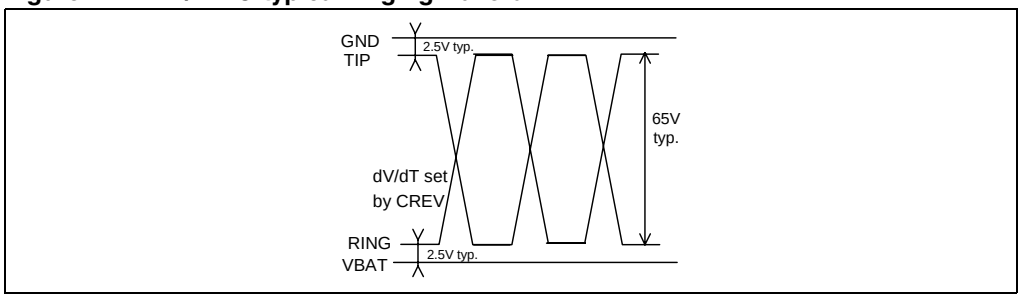
- it synthesizes a low output impedance at the TIP/RING pins at the TTX frequency
- it cuts the eventual TTX echo that would have been transferred from the line to the TX output

3.2.4 Ringing

When this mode is selected, the STLC3075 self generates a higher negative battery (-70V typ.) in order to allow a balanced ringing signal of typically 65V peak.

In this condition both the DC and AC feedback loops are disabled and the SLIC line drivers operate as voltage buffers. The ring waveform is obtained by toggling the D2 control bit at the desired ring frequency. This bit in fact controls the line polarity (0=direct; 1= reverse). As in the active mode the line voltage transition is performed with a ramp transition, obtaining in this way a trapezoidal balanced ring waveform (see *Figure 7*). The shaping is defined by the CREV external capacitor.

Figure 7. TIP/RING typical ringing waveform



Selecting the proper capacitor value it is possible to get different crest factor values.

The following table shows the crest factor values obtained with a 20Hz and 25Hz ring frequency and with 1REN. These value are valid either with European or USA specification:

Table 5. CREST factor values @ 20 and 25Hz

CREV	CREST factor @20Hz	CREST factor @25Hz
22nF	1.2	1.26
27nF	1.25	1.32
33nF	1.33	Not(1)

1. Distortion already less than 10%

The ring trip detection is performed by sensing the variation of the AC line impedance from on-hook (relatively high) to off-hook (low). This particular ring trip method allows to operate without DC offset superimposed on the ring signal and therefore obtaining the maximum possible ring level on the load starting from a given negative battery.

It should be noted that such a method is optimized for operation on short loop applications and may not operate properly in the case of long loop applications (> 500Ω).

Once the ring trip is detected, the $\overline{DET}$ output is activated (logic level low). At this point the card controller or a simple logic circuit stops the D2 toggling in order to effectively disconnect the ring signal and then set the STLC3075 in the proper operating mode (normally active).

Ring level in presence of more telephones in parallel

As already mentioned in the previous section, the maximum current that can be drawn from the V_{POS} supply is controlled and limited via the external R_{SENSE}. This also limits the power available at the self generated negative battery.

If for any reason the ringer load is too low, the self generated battery drops in order to keep the power consumption to the fixed limit and consequently the ring voltage level is also reduced.

In the typical buckboost configuration with R_{SENSE} = 110mΩ the peak current from V_{POS} is limited to around 900mApk, which correspond to an average current of 700mA max. In this condition the STLC3075 can drive up to 3REN with a ring frequency fr=25Hz (1REN = 1800Ω + 1.0µF, european standard).

In order to drive up to 5REN (1REN= 6930Ω + 8µF, US standard) it is necessary to modify the external components as follows:

CREV = 15nF; RD = 2.2KΩ; R_{SENSE} = 100mΩ

In flyback configuration the value of R_{SENSE} = 220mΩ guarantees to match both European and USA standard. In order to drive 5REN (US standard) it is necessary to modify the external component: R_D = 2K2.

3.2.5 Layout recommendation

A properly designed PCB layout is a basic issue to guarantee a correct behavior and good noise performance.

Particular care must be taken on the ground connection. Using the configurations shown on *Figure 10* and *Figure 11* permits to avoid possible problems.

The ground of the power supply (V_{POS}) has to be connected to the center of the star, named as SYSTEM-GND. This point should show a resistance as low as possible, that means it should be a ground plane.

In particular to avoid noise problems the layout should prevent any coupling between the DC/DC converter components and analog pins that are referred to AGND (ex: RD, IREF, RTH, RLIM, VF). As a first recommendation the components CV, L, T1, D1, CV_{POS}, R_{SENSE} should be kept as close as possible to each other and isolated from the other components.

Additional improvements can be obtained

- by decoupling the center of the star from the analog ground of STLC3075 using small chokes
- by adding a capacitor in the range of 100nF between V_{POS} and AGND in order to filter the switch frequency on V_{POS}

3.2.6 External components list

In order to properly define the external components value the following system parameters have to be defined:

- the AC input impedance shown by the SLIC at the line terminals Zs to which the return loss measurement is referred. It can be real (typ. 600Ω) or complex.
- the AC balance impedance, it is the equivalent impedance of the line 'Zl' used for evaluation of the trans-hybrid loss performances (2/4 wire conversion). It is usually a complex impedance.
- the value of the two protection resistors Rp in series with the line termination.
- the line impedance at the TTX frequency Zlttx
- the metering pulse level amplitude measured at line termination V_{LOTTX}. In case of low order filtering, V_{LOTTX} represents the amplitude (Vrms) of the fundamental frequency component (typ. 12 or 16kHz)
- the pulse metering envelope rise and decay time constant τ
- the slope of the ringing waveform $\Delta V_{TR}/\Delta_T$
- the value of the constant current limit current 'Ilim'
- the value of the off-hook current threshold I_{TH}
- the value of the ring trip rectified average threshold current I_{RTH}
- the value of the required self generated negative battery V_{BATR} in ring mode (max value is 70V). This value can be obtained from the desired ring peak level + 5V.
- the value of the maximum current peak drawn from V_{POS} 'IPK'.

Table 6. External components for buckboost configuration

Name	Function	Formula	Typ. value
RRX	Rx input bias resistor		100kΩ 5%
RREF	Bias setting current	RREF = 1.3/Ibias Ibias = 50µA	26kΩ 1%
CSVR	Negative battery filter	CSVR = 1/(2π · fp · 1.8MΩ) fp = 50Hz	1.5nF 10% 100V
RD	Ring trip threshold setting resistor	RD = 100/I_{RTH} 2KΩ < RD < 5KΩ	4.12kΩ 1%@ IRTH = 24mA
CAC	AC/DC split capacitance		22µF 20% 15V @ RD = 4.12kΩ
RP	Line protection resistor	Rp > 30Ω	50Ω 1%
RLIM	Current limiting programming	RLIM = 1300/Ilim 32.5kΩ < RLIM < 65kΩ	52.3kΩ 1% @ Ilim = 25mA
RTH	Off-hook threshold programming (Active mode)	RTH = 290/I_{TH} 27kΩ < RTH < 52kΩ	32.4kΩ 1% @ I_{TH} = 9mA
CREV	Reverse polarity transition time programming	CREV = ((1/3750) · $\Delta T/\Delta V_{TR}$)	22nF 10% 10V @ 12V/ms
RDD	Pull up resistors		100kΩ
CVCC	Internally supply filter capacitor		100nF 20% 10V

Table 6. External components for buckboost configuration (continued)

Name	Function	Formula	Typ. value
CV_{POS}	Positive supply filter capacitor with low impedance for switch mode power supply		100µF(1)
CV	Battery supply filter capacitor with low impedance for switch mode power supply		100µF 20% 100V(2)
CVB	High frequency noise filter		470nF 20% 100V
CRD(3)	High frequency noise filter		100nF 10% 15V
Q1	DC/DC converter switch P ch. MOS transistor	RDS(ON)≤1.2Ω, VDS = -100V Total gate charge= 20nC max. with VGS=4.5V and VDS=1V ID>500mA	Possible choices: IRF9510 or IRF9520 or IRF9120 or equivalent
D1	DC/DC converter series diode	V_r > 100V, t_{RR} ≤50ns	SMBYW01-200 or equivalent
R_{SENSE}	DC/DC converter peak current limiting	R_{SENSE} = 100mV/I_{PK}	110mΩ @ I_{PK} = 900mA
RF1	Negative battery programming level	250KΩ < RF1 < 300KΩ(4)	300kΩ 1% @ V_{BATR} = -70V
RF2	Negative battery programming level		9.1kΩ 1%
L	DC/DC converter inductor	DC resistance ≤0.1Ω(5)	L=100µH SUMIDA CDRH125 or equivalent

1. CV_{POS} should be defined depending on the power supply current capability and maximum allowable ripple
2. For low ripple application use 2x47m F in parallel.
3. Can be saved if proper PCB layout avoid noise coupling on RD pin (high impedance input).
4. RF1 sets the self generated battery voltage in RING and ACTIVE(II=0) mode as shown in *Table 7*. VBATR should be defined considering the ring peak level required (Vringpeak=VBATR-6V typ.). This relation is valid providing that the V_{POS} power supply current capability and the R_{SENSE} programming allow to source all the current requested by the particular ringer load configuration
5. For high efficiency in HI-Z mode coil resistance @125kHz must be < 3Ω

Table 7. VBAT values in RING and ACTIVE modes

	267kΩ	280kΩ	294kΩ	300kΩ
VBAT (ACTIVE)	-46V	-48V	-49V	-50V
VBATR (RING)	-62V	-65V	-68V	-70V

Table 8. External components for flyback configuration

Name	Function	Formula	Typ. value
RRX	Rx input bias resistor		100kΩ 5%
RREF	Bias setting current	RREF = 1.3/Ibias; Ibias = 50µA	26kΩ 1%
CSVR	Negative battery filter	CSVR = 1/(2π · fp · 1.8MΩ) fp = 50Hz	1.5nF 10% 100V
RD	Ring trip threshold setting resistor	RD = 100/I_{RTH} 2KΩ < RD < 5KΩ	4.12kΩ 1% @ IRTH = 24mA
CAC	AC/DC split capacitance		22µF 20% 15V @ RD = 4.12kΩ
RP	Line protection resistor	Rp > 30Ω	50Ω 1%
RLIM	Current limiting programming	RLIM = 1300/Ilim 32.5kΩ < RLIM < 65kΩ	52.3kΩ 1% @ Ilim = 25mA
RTH	Off-hook threshold programming (Active mode)	RTH = 290/I_{TH} 27kΩ < RTH < 52kΩ	32.4kΩ 1% @ I_{TH} = 9mA
CREV	Reverse polarity transition time programming	CREV = ((1/3750)· ΔT/ΔV_{TR})	22nF 10% 10V @ 12V/ms
RDD	Pull up resistors		100kΩ
CVCC	Internally supply filter capacitor		100nF 20% 10V
CV_{POS}	Positive supply filter capacitor with low impedance for switch mode power supply		100µF(1)
CV	Battery supply filter capacitor with low impedance for switch mode power supply		100µF 20% 100V(2)
CVB	High frequency noise filter		470nF 20% 100V
CRD(3)	High frequency noise filter		100nF 10% 15V
CZ	Flyback compensation capacitor		2.2nF, 20%
CSF	Sense filter capacitor		120pF, 20%
RSF	Sense filter resistor		1kΩ
R_{SENSE}	DC/DC converter peak current limiting	R_{SENSE} = 375mV/I_{PK}	220mΩ @ I_{PK} = 1.7A
Q1	DC/DC converter switch N channel MOS transistor	RDS(ON)≤0.05Ω, VDSS = 30V VDG=30V, ID = 6.5A Low threshold drive	STN4NF03L or equivalent
D1	DC/DC converter series diode	V_r > 350V, t_{RR} ≤80ns	SMBYTW01-400 or equivalent
T1	DC/DC converter transformer	Flyback transformer 4W, turns ratio 1:16 for V_{POS} range from 4.5V to 8.5V	Tyco COEV MAGNETICS MGPWG-00007 or Coilcraft FA2469-AL(4)

Table 8. External components for flyback configuration

Name	Function	Formula	Typ. value
T1	DC/DC converter transformer	Flyback transformer 4W, turns ratio 1:8 for V_{POS} range from 8.5V to 12V	Tyco COEV MAGNETICS MGPWG-00008 or Coilcraft FA2470-AL(5)
RF1	Negative battery programming level	250KΩ<RF1<300KΩ(6)	300kΩ 1% @ V_{BATR} = -70V
RF2	Negative battery programming level		9.1kΩ 1%

1. CV_{POS} should be defined depending on the power supply current capability and maximum allowable ripple.
2. For low ripple application use 2x47m F in parallel.
3. Can be saved if proper PCB layout avoid noise coupling on RD pin (high impedance input).
4. Coilcraft type FA2469-AL, Flyback transformer 4W, 1:16 with a V_{POS} range from 4.5V to 8.5V @ +20°C unless otherwise specified. Also check *Table 9* for further electrical specifications
5. Coilcraft type FA2470-AL, Flyback transformer 4W, 1:8 with a V_{POS} range from 8.5V to 12V @ +20°C unless otherwise specified. Also check *Table 10* for further electrical specifications
6. RF1 sets the self generated battery voltage in RING and ACTIVE(Il=0) mode as as shown in *Table 7*. V_{BATR} should be defined considering the ring peak level required (Vringpeak=V_{BATR}-6V typ.). This relation is valid providing that the V_{POS} power supply current capability and the R_{SENSE} programming allow to source all the current requested by the particular ringer load configuration.

Table 9. Coilcraft type FA2469-AL electrical specifications

Test description	Limit	Unit	Tol	Notes
Inductance	0.0205	mH	Max	1-3, 10KHz, 100mVmrs
Leakage inductance	0.414	uH	Max	1-3, 100KHz, 100mVmrs Short pins 4,6
DC resistance	0.036	ohm	Max	1-3
DC resistance	16.50	ohm	Max	4-6
Turns ratio	16:1	-	+/-4%	(4-6):(1-3), 10KHz, 100mVAC
HI POT	1.500	VAC		VDC to be applied for 1 second from pins 1,3 to pins 4,6. 500µA max leakage current

Table 10. Coilcraft type FA2470-AL electrical specifications

Test description	Limit	Unit	Tol	Notes
Inductance	0.0205	mH	Max	1-3, 10KHz, 100mVmrs
Leakage inductance	0.40	uH	Max	1-3, 100KHz, 100mVmrs Short pins 4,6
DC resistance	0.036	ohm	Max	1-3
DC resistance	7.92	ohm	Max	4-6
Turns ratio	8:1	-	+/-3.3%	(4-6):(1-3), 10KHz, 100mVAC
HI POT	1.500	VAC		VDC to be applied for 1 second from pins 1,3 to pins 4,6. 500µA max leakage current

Table 11. External components @gain set = 0

Name	Function	Formula	Typ. value
RS	Protection resistance image	RS = 50 · (2Rp)	5kΩ @ Rp = 50Ω
ZAC	Two wire AC impedance	ZAC = 50 · (Zs - 2Rp)	25kΩ 1% @ Zs = 600Ω
ZA(1)	SLIC impedance balancing network	ZA = 50 · Zs	30kΩ 1% @ Zs = 600Ω
ZB(1)	Line impedance balancing network	ZB = 50 · Zl	30kΩ 1% @ Zl = 600Ω
CCOMP	AC feedback loop compensation	fo = 250kHz CCOMP = 1/(2π· fo· 100· (RP))	120pF 10% 10V @ Rp = 50Ω
CH	Trans-hybrid Loss frequency compensation	CH = CCOMP	120pF 10% 10V
RTTX(2)	Pulse metering cancellation resistor	RTTX = 50Re (Zlttx+2Rp)	15kΩ @ Zlttx = 200Ω real
CTTX(2)	Pulse metering cancellation capacitor	CTTX = 1/{50 · 2π· fttx [-Im(Zlttx)]}	100nF 10% 10V(3) @ Zlttx = 200Ω real
RLV	Pulse metering level resistor	RLV = $63.3 \cdot 10^{3} \cdot \alpha \cdot V_{LOTTX}$ α = (|Zlttx + 2Rp|/|Zlttx|)	16.2kΩ @ V_{LOTTX} = 170mVrms
CS	Pulse metering shaping capacitor	CS = τ/(2· RLV)	100nF 10% 10V @ τ = 3.2ms, RLV = 16.2kΩ
CFL	Pulse metering filter capacitor	CFL = 2/(2π· fttx· RLV)	1.5nF 10% 10V @fttx = 12kHz RLV = 16.2kΩ

1. In case Zs=Zl, ZA and ZB can be replaced by two resistors of same value: RA=RB=|Zs|.
2. Defining ZTTX as the impedance of RTTX in series with CTTX, RTTX and CTTX can also be calculated from the following formula: ZTTX=50*(Zlttx+2Rp).
3. In this case CTTX is just operating as a DC decoupling capacitor (fp=100Hz).

Table 12. External components @gain set = 1

Name	Function	Formula	Typ. value
RS	Protection resistance image	RS = 50 · (2Rp)	5kΩ @ Rp = 50Ω
ZAC	Two wire AC impedance	ZAC = 50 · (Zs - 2Rp)	25kΩ 1% @ Zs = 600Ω
ZA(1)	SLIC impedance balancing network	ZA = 50 · Zs	30kΩ 1% @ Zs = 600Ω
ZB(1)	Line impedance balancing network	ZB = 50 · Zl	30kΩ 1% @ Zl = 600Ω
CCOMP	AC feedback loop compensation	fo = 250kHz CCOMP = 1/(2π· fo· 100· (RP))	120pF 10% 10V @ Rp = 50Ω
CH	Trans-hybrid Loss frequency compensation	CH = CCOMP	120pF 10% 10V
RTTX(2)	Pulse metering cancellation resistor	RTTX = 50Re (Zlttx+2Rp)	15kΩ @ Zlttx = 200Ω real
CTTX (2)	Pulse metering cancellation capacitor	CTTX = 1/{50 · 2π· fttx [-lm(Zlttx)]}	100nF 10% 10V (3) @ Zlttx = 200Ω real
RLV	Pulse metering level resistor	RLV = $63.3 \cdot 10^{3} \cdot \alpha \cdot V_{LOTTX}$ $\alpha = (\lvert Zlttx + 2Rp \rvert / \lvert Zlttx \rvert)$	16.2kΩ @ V_{LOTTX} = 170mVrms
CS	Pulse metering shaping capacitor	CS = τ/(2· RLV)	100nF 10% 10V @ τ = 3.2ms, RLV = 16.2kΩ
CFL	Pulse metering filter capacitor	CFL = 2/(2π· fttx· RLV)	1.5nF 10% 10V @fttx = 12kHz RLV = 16.2kΩ

1. In case Zs=Zl, ZA and ZB can be replaced by two resistors of same value: RA=RB=|Zs|.
2. Defining ZTTX as the impedance of RTTX in series with CTTX, RTTX and CTTX can also be calculated from the following formula: ZTTX=50*(Zlttx+2Rp).
3. In this case CTTX is just operating as a DC decoupling capacitor (fp=100Hz).

Figure 8. Application diagram with N-channel

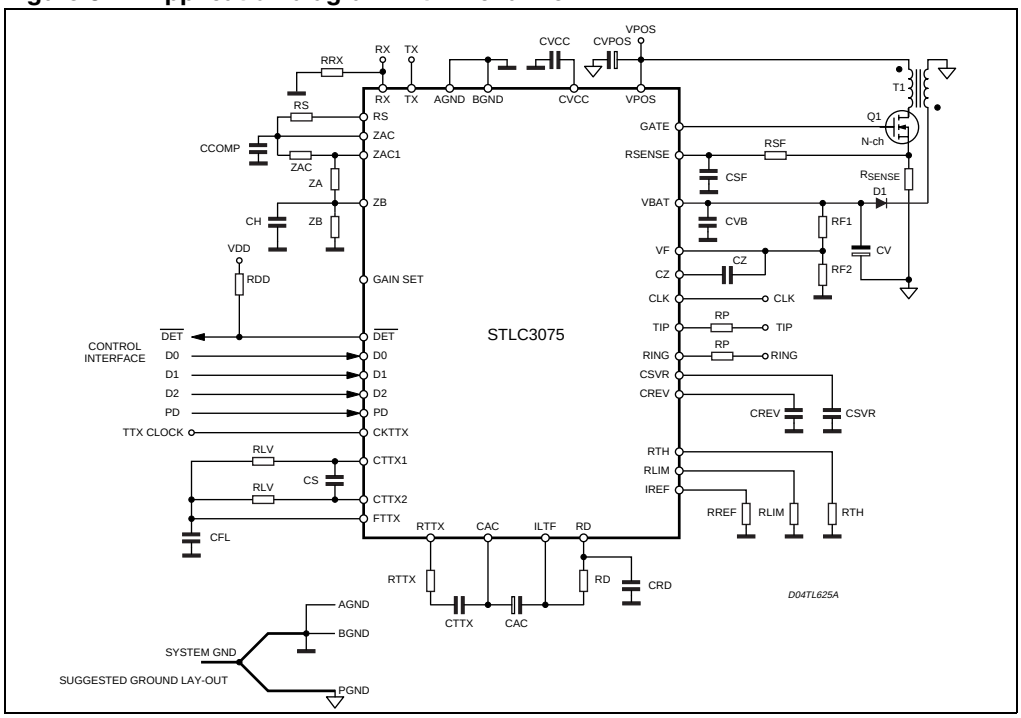


Figure 9. Application diagram without metering pulse generation with N-channel

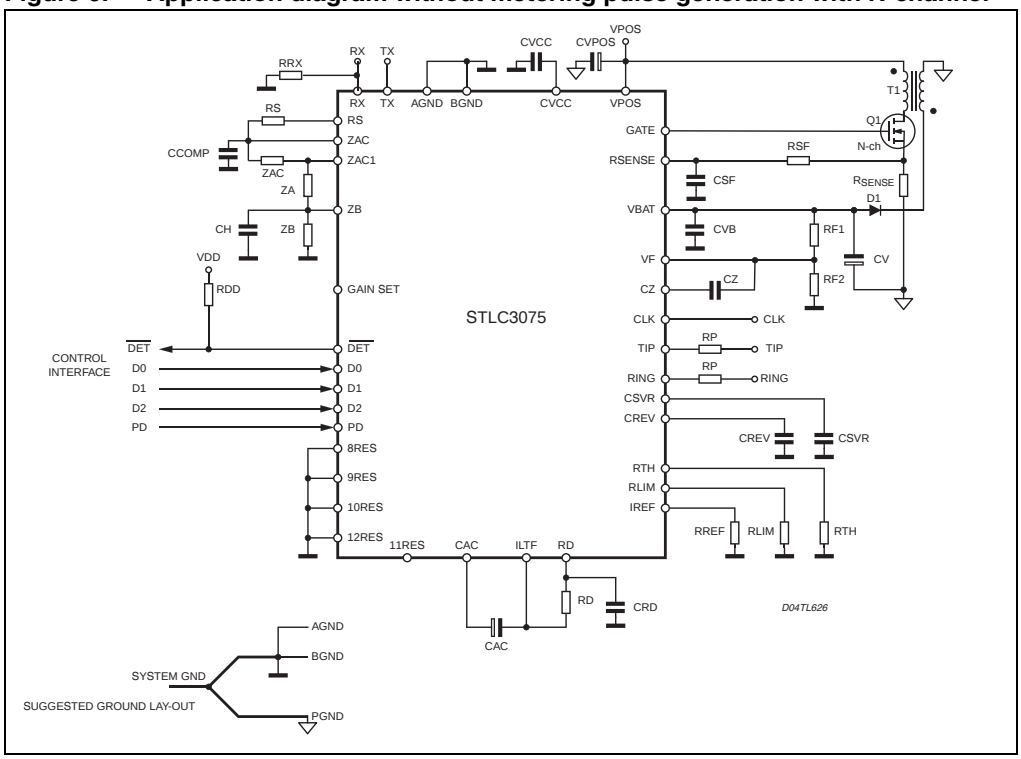


Figure 10. Application diagram with P-channel

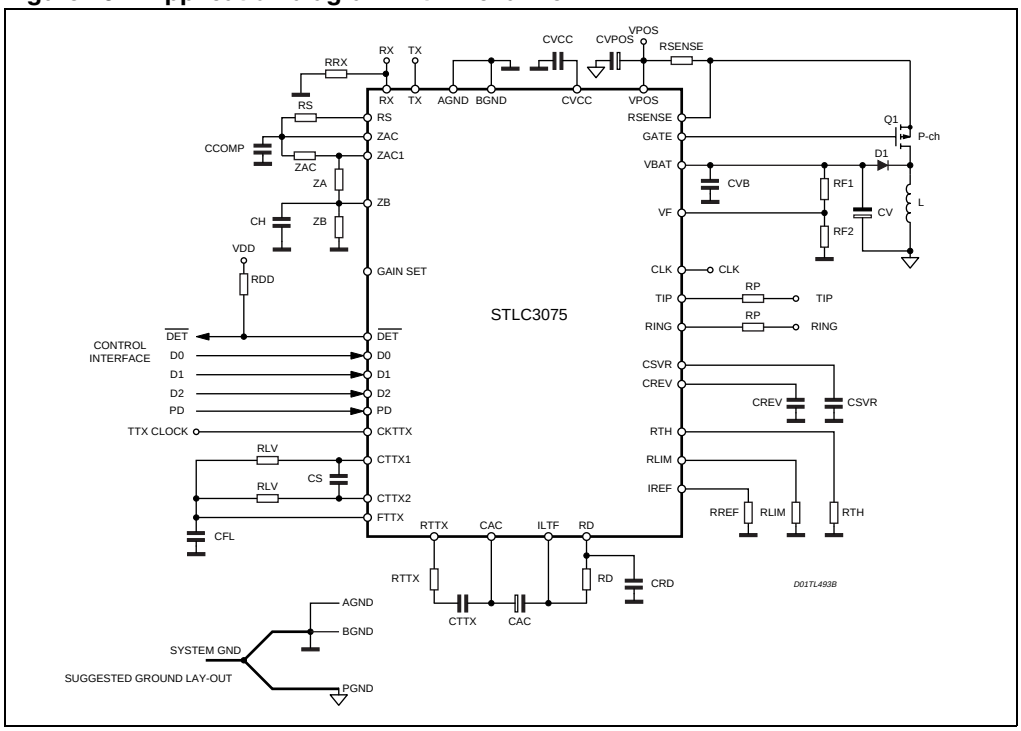
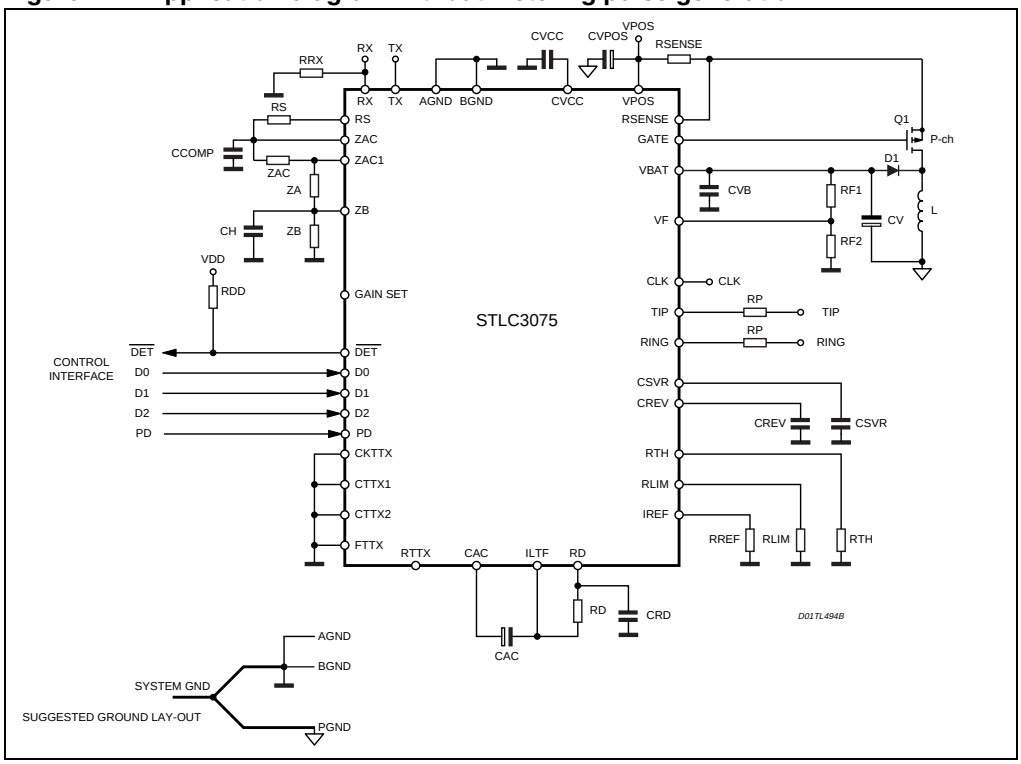


Figure 11. Application diagram without metering pulse generation



(*) Buckboost configuration.

4 Electrical characteristics

Test conditions: V_{POS} = 6.0V, AGND = BGND, normal polarity, T_{amb} = 25°C.
External components as listed in the 'Typical values' column of the above external components tables.

Note: Testing of all parameters is performed at 25°C. Characterization as well as design rules used allow correlation of tested performances at other temperatures. All parameters listed here are met in the operating range of: -40 to +85°C.

Table 13. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{POS}	Positive supply voltage	-0.4 to +13	V
A/BGND	AGND to BGND	-1 to +1	V
V_{dig}	Pin D0, D1, D2, $\overline{DET}$, CKTTX	-0.4 to 5.5	V
T_j	Max. junction temperature	150	°C
V_{btot} (1)	Vbtot=|V_{POS}|+|Vbat|. (Total voltage applied to the device supply pins).	90	V
ESD rating	Human body model	±1750	V
	Charged device model	±500	V

1. Vbat is self generated by the on-chip DC/DC converter and can be programmed via RF1 and RF2. RF1 and RF2 must be selected in order to fulfil the a.m. limits (see components tables).

Table 14. Operating range

Symbol	Parameter	Value	Unit
V_{POS}	Positive supply voltage	4.5 to +12	V
A/BGND	AGND to BGND	-100 to +100	mV
V_{dig}	Pin D0, D1, D2, $\overline{DET}$, CKTTX, PD	-0.25 to 5.25	V
T_{op}	Ambient operating temperature range	-40 to +85	°C
V_{bat}(1)	Self generated battery voltage	-74 max.	V

1. Vbat is self generated by the on-chip DC/DC converter and can be programmed via RF1 and RF2. RF1 and RF2 must be selected in order to fulfil the a.m. limits (see *Table 6: External components for buckboost configuration*)

Table 15. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal resistance junction to ambient typical.	60	°C/W

Table 16. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
DC characteristics						
V_{lohi}	Line voltage	Il = 0 HI-Z (High impedance feeding) T_{amb} = 0°C to 85°C	44	50		V
V_{lohi}	Line voltage	Il = 0 HI-Z (High impedance feeding) T_{amb} = -40°C to 85°C	42	48		V
V_{loa}	Line voltage	Il = 0, Active mode, T_{amb} = 0°C to 85°C	33	40		V
V_{loa}	Line voltage	Il = 0, active mode, T_{amb} = -40°C to 85°C	31	37		V
Ilim	Lim. current programming range	Active mode	20		40	mA
Ilima	Lim. current accuracy	Active mode Rel. to programmed value 20mA to 40mA	-10		10	%
Rfeed HI	Feeding resistance	HI-Z (High Impedance feeding)	2.4		3.6	kΩ
AC characteristics						
L/T	Long. to transv. (see appendix for test circuit)	Rp = 50Ω, 1% tolerance Active N. P., R_L = 600Ω (*) f = 300 to 3400Hz	50	58		dB
T/L	Transv. to long. (see appendix for test circuit)	Rp = 50Ω, 1% tolerance Active N. P., R_L = 600Ω (*) f = 300 to 3400Hz	40	45		dB
T/L	Transv. to long. (see appendix for test circuit)	Rp = 50Ω, 1% tolerance Active N. P., R_L = 600Ω (*) f = 1kHz	48	53		dB
2WRL	2W return loss	300 to 3400Hz Active N. P., R_L = 600Ω (*)	22	26		dB
THL	Trans-hybrid loss	300 to 3400Hz 20Log|VRX/VTX| Active N. P., R_L = 600Ω (*)	30			dB
Ovl	2W overload level	At line terminals on ref. imped. Active N. P., R_L = 600Ω (*)	3.2			dBm
TXoff	TX output offset	Active N. P., R_L = 600Ω (*)	-250		250	mV
G24	Transmit gain abs.	0dBm @ 1020Hz Active N. P., R_L = 600Ω (*)	-6.4		-5.6	dB
G42	Receive gain abs.	0dBm @ 1020Hz Active N. P., R_L = 600Ω (*)	-0.4		0.4	dB

Table 16. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
G24f	TX gain variation vs. frequency	Rel. 1020Hz; 0dBm 300 to 3400Hz Active N. P., R_L = 600Ω (*)	-0.12		0.12	dB
G24f	RX gain variation vs. freq.	Rel. 1020Hz; 0dBm 300 to 3400Hz Active N. P., R_L = 600Ω (*)	-0.12		0.12	dB
V2Wp	Idle channel noise at line 0dB gain set	Psophometric filtered Active N. P., R_L = 600Ω (*) T_{amb} = 0 to +85°C		-73	-68	dBmp
V2Wp	Idle channel noise at line 0dB gain set	Psophometric filtered Active N. P., R_L = 600Ω (*) T_{amb} = -40 to +85°C		-68		dBmp
V4Wp	Idle channel noise at line 0dB gain set	Psophometric filtered Active N. P., R_L = 600Ω (*) T_{amb} = 0 to +85°C		-75	-70	dBmp
V4Wp	Idle channel noise at line 0dB gain set	Psophometric filtered Active N. P., R_L = 600Ω (*) T_{amb} = -40 to +85°C		-75		dBmp
Thd	Total harmonic distortion	Active N. P., R_L = 600Ω (*)			-44	dB
VTTX	Metering pulse level on line	Active - TTX; Gain Set = 1 Zl = 200Ω fttx = 12kHz	260	340		mVrms
CLKfreq	CLK operating range		-10%	125	10%	kHz
(*) R_L: Line resistance						
Ring						
Vring	Line voltage	RING D2 toggling @ fr = 25Hz Load = 3REN Crest Factor = 1.25 1REN = 1800Ω + 1.0µF T_{amb} = 0 to +85°C	45	49		Vrms
Vring	Line voltage	RING D2 toggling @ fr = 25Hz Load = 3REN Crest Factor = 1.25 1REN = 1800Ω + 1.0µF T_{amb} = -40 to +85°C	44	48		Vrms

Table 16. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Detectors						
IOFFTHA	Off/hook current threshold	Active mode, RTH = 32.4kΩ 1% (Prog. ITH = 9mA)	10.5			mA
ROFTHA	Off/hook loop resistance threshold	Active mode, RTH = 32.4kΩ 1% (Prog. ITH = 9mA)			3.4	kΩ
IONTHA	On/hook current threshold	Active mode, RTH = 32.4kΩ 1% (Prog. ITH = 9mA)			6	mA
RONTHA	On/hook loop resistance threshold	Active mode, RTH = 32.4kΩ 1% (Prog. ITH = 9mA)	8			kΩ
IOFFTHI	Off/hook current threshold	Hi Z mode, RTH = 32.4kΩ 1% (Prog. ITH = 9mA)	10.5			mA
ROFFTHI	Off/hook loop resistance threshold	Hi Z mode, RTH = 32.4kΩ 1% (Prog. ITH = 9mA)			800	Ω
IONTHI	On/hook current threshold	Hi Z mode, RTH = 32.4kΩ 1% (Prog. ITH = 9mA)			6	mA
RONTHI	On/hook loop resistance threshold	Hi Z mode, RTH = 32.4kΩ 1% (Prog. ITH = 9mA)	8			kΩ
Irt	Ring trip detector threshold range	RING	20		50	mA
Irta	Ring trip detector threshold accuracy	RING	-15		15	%
Trtd	Ring trip detection time	RING		TBD		ms
Td	Dialling distortion	Active mode	-1		1	ms
Rlrt(1)	Loop resistance				500	Ω
ThAl	Tj for th. alarm activation			160		°C
(1) Rlrt = Maximum loop resistance (incl. telephone) for correct ring trip detection.						
Digital interface Inputs: D0, D1, D2, PD, CLK Outputs: $\overline{DET}$						
Vih	In put high voltage		2			V
Vil	Input low voltage				0.8	V
Iih	Input high current		-10		10	µA
Iil	Input low current		-10		10	µA
Vol	Output low voltage	Iol = 1mA			0.45	V

Table 16. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
PSRR and power consumption						
PSERRC	Power supply rejection V_{POS} to 2W port	Vripple = 100mVrms 50 to 4000Hz	26	36		dB
Ivpos	V_{POS} supply current @ II = 0	HI-Z on-hook Active on-hook RING (line open)		13 50 55	25 80 90	mA mA mA
Ipk(1)	Peak current limiting accuracy	RING off-hook R_{SENSE} = 110mΩ	-20%	900	+20%	mApk

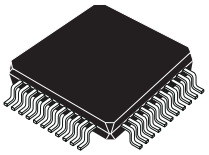
1. Buck-Boost configuration

5 Package mechanical data

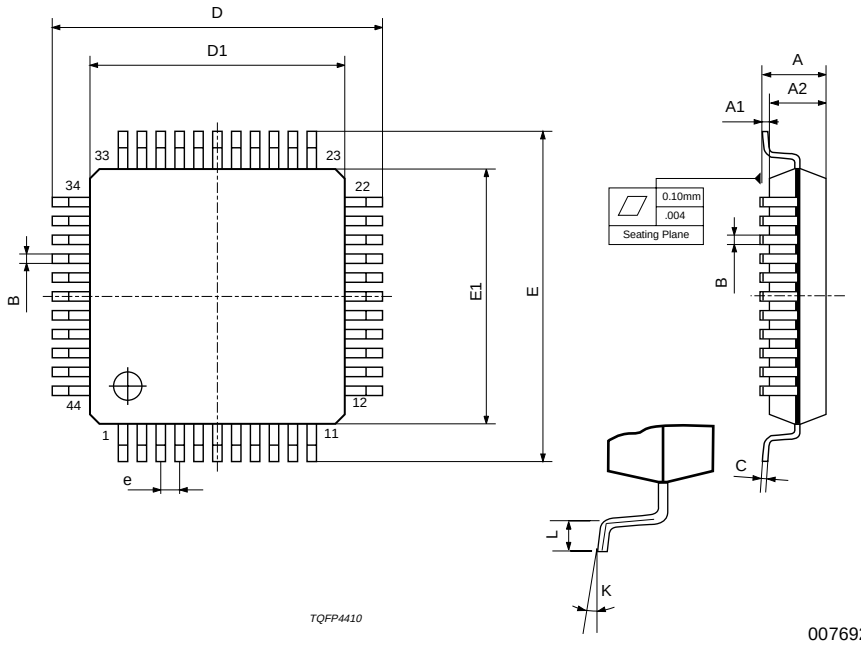
Figure 12. Mecanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.015	0.018
C	0.09		0.20	0.004		0.008
D	11.80	12.00	12.20	0.464	0.472	0.480
D1	9.80	10.00	10.20	0.386	0.394	0.401
D3		8.00			0.315	
E	11.80	12.00	12.20	0.464	0.472	0.480
E1	9.80	10.00	10.20	0.386	0.394	0.401
E3		8.00			0.315	
e		0.80			0.031	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	0°(min.), 3.5°(typ.), 7°(max.)					

OUTLINE AND MECHANICAL DATA



TQFP44 (10 x 10 x 1.4mm)



6 Ordering information

Table 17. Order codes

Part number	Package
E-STLC3075	TQFP44

7 Revision history

Table 18. Document revision history

Date	Revision	Changes
04-Oct-2004	1	Initial release
04-Nov-2004	2	Removed all max. values of the 'Line voltage' parameter on page 16/26. Changed the unit from mA to% of the 'Ilima' parameter on page 16/26.
09-Feb-2005	3	Added pin 4 PD in applications and block diagram. Added Table 2 'ESD rating'.
22-Apr-2005	4	Changed figures 9 and 10.
14-Jul-2005	5	Changed VTTX value.
07-Feb-2007	6	Added RRX resistance in the *Figure 9* and *Figure 10*. Updated *Section 3.1* and *Section 3.2.4*. Updated R_{SENSE} value and Ipk maximum value in *Table 11*. Updated *Figure 23*. Added Coilcraft references (FA2469-AL and FA2470-AL) to T1 parameter in *Table 8*. Moved *Table 13*, *Table 14* and *Table 15* to *Chapter 4: Electrical characteristics*.
09-Mar-2007	7	Added precision on single supply voltage range for fly-back and buck boost configurations on page 1.

Appendix A Measurement configurations

A.1 STLC3075 test circuits

Referring to the application diagram as shown on *Figure 10: Application diagram with P-channel* and using the typical values from *Table 6: External components for buckboost configuration* and *Table 11: External components @gain set = 0* find below the proper configuration for each measurement.

All measurements requiring DC current termination should be performed using 'Wandel & Glittering' DC Loop Holding Circuit GH-1' or equivalent.

Figure 13. 2W return loss 2WRL = 20Log(|Zref + Zs|/|Zref-Zs|) = 20Log(E/2Vs)

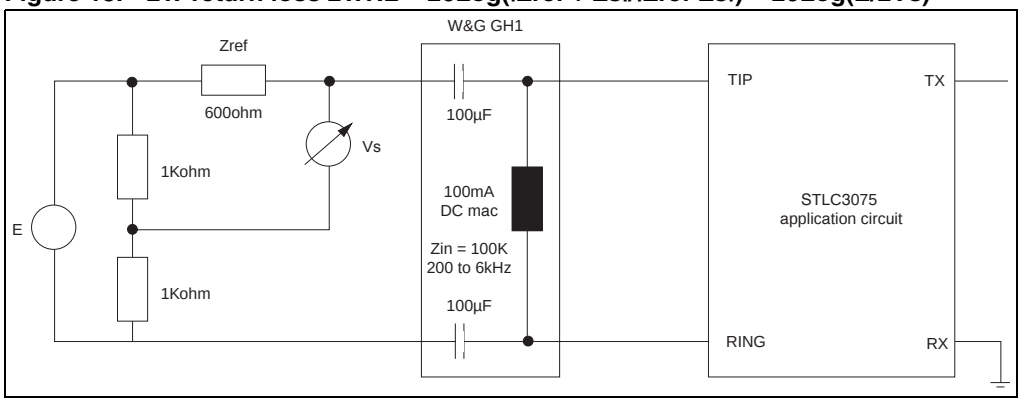


Figure 14. THL trans hybrid loss THL = 20Log|Vrx/Vtx/

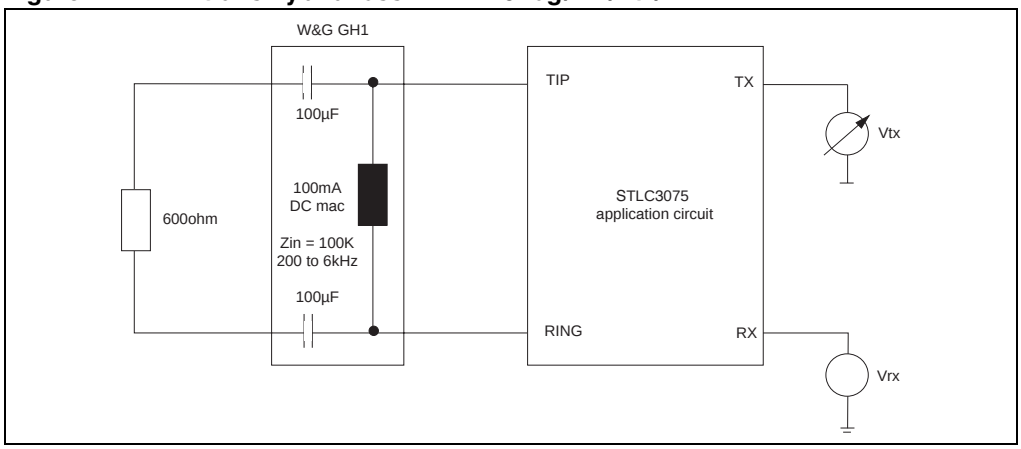


Figure 15. G24 transmit gain G24 = 20Log|2Vtx/E|

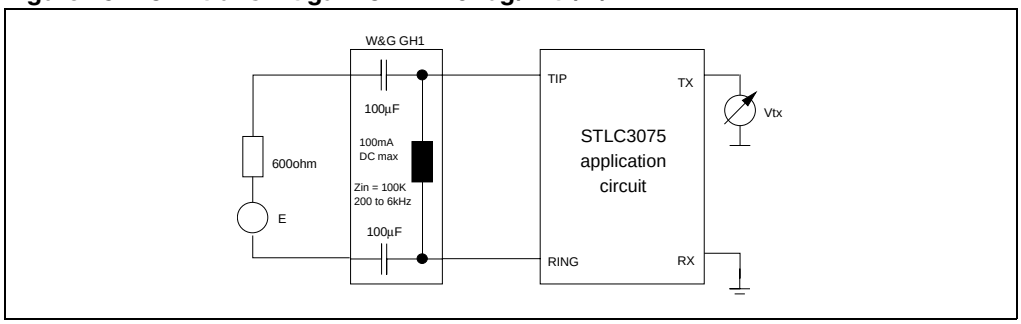


Figure 16. G42 receive gain G42 = 20Log|VI/Vrx|

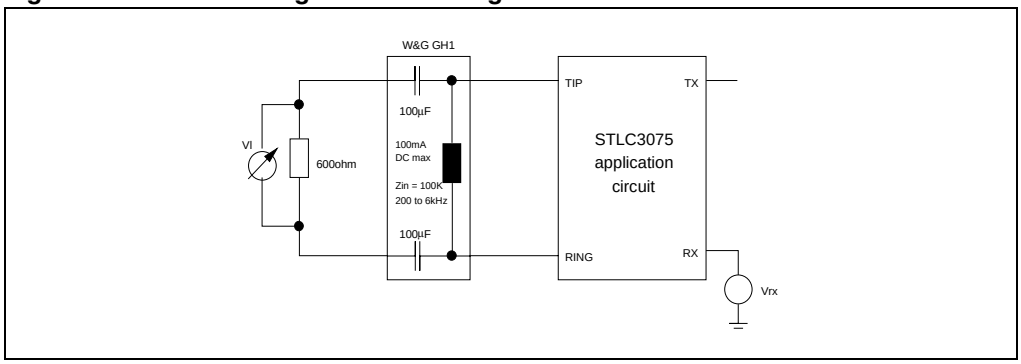


Figure 17. PSRRC power supply rejection V_{POS} to 2W port PSSRC = 20Log|Vn/VI|

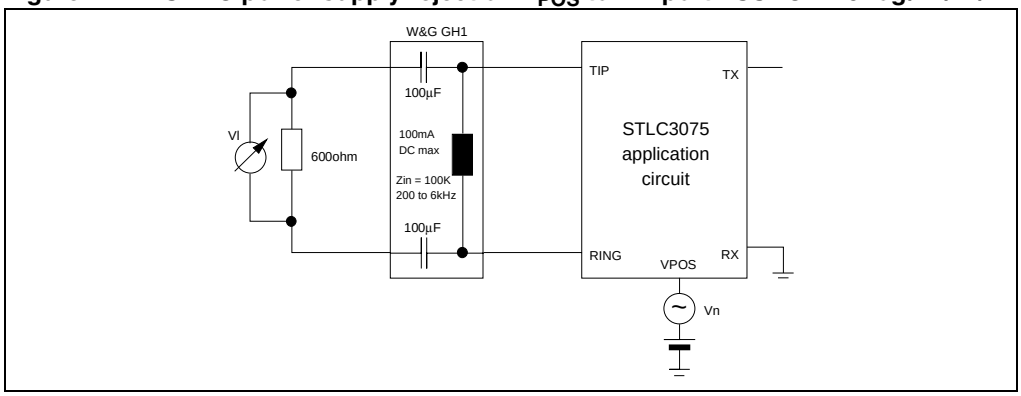


Figure 18. L/T longitudinal to transversal conversion L/T = 20Log|Vcm/VI|

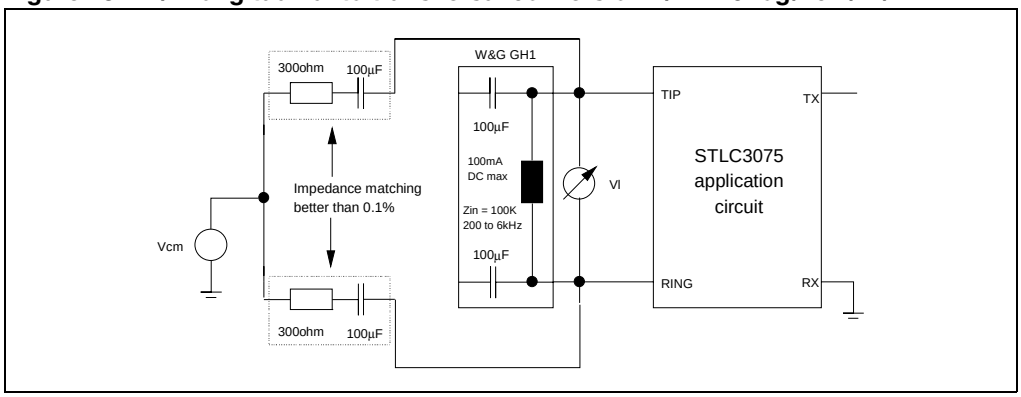


Figure 19. T/L transversal to longitudinal conversion T/L = 20Log|Vrx/Vcm/

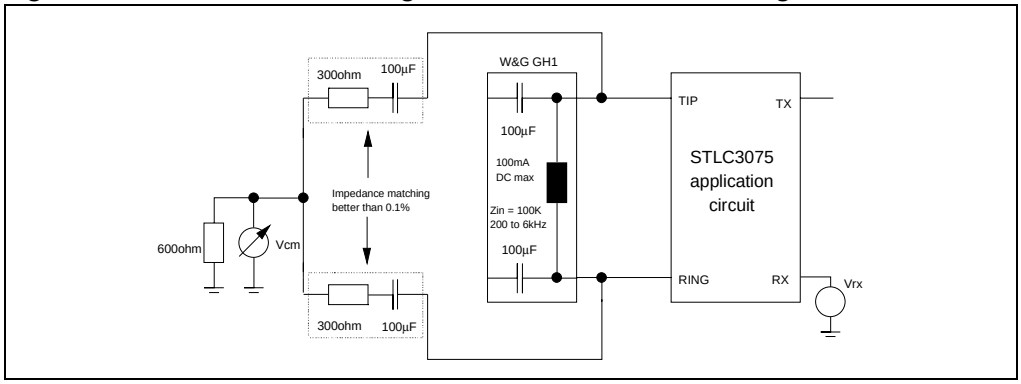


Figure 20. VTTX metering pulse level on line

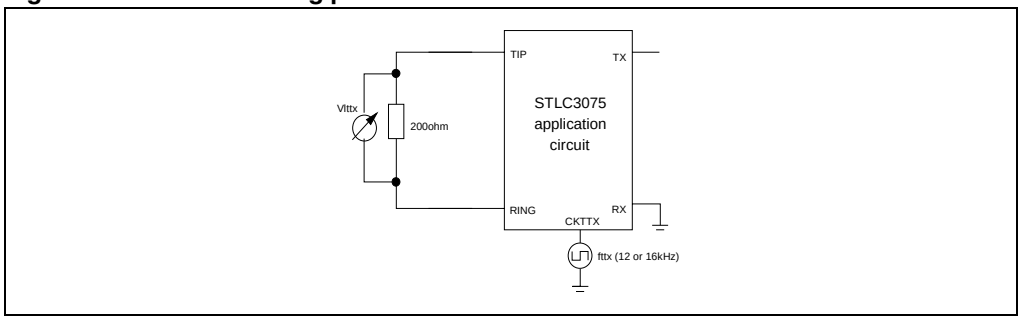
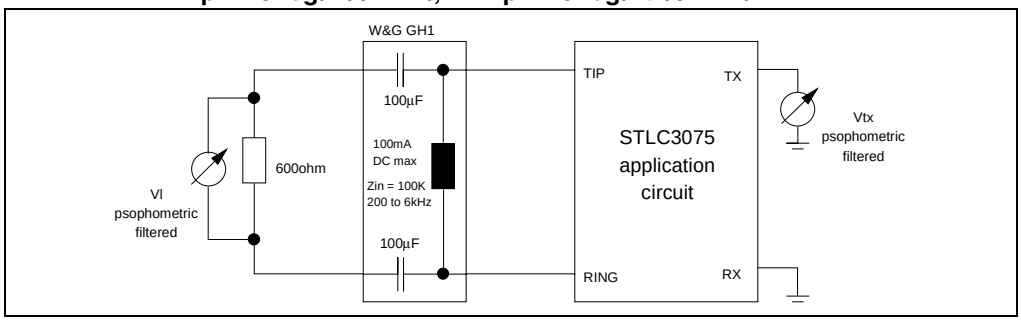


Figure 21. V2Wp and W4Wp: Idle channel sophometric noise at line and TX. V2Wp = 20Log|VI/0.774I; V4Wp = 20Log|Vtx/0.774I/



Appendix B Over voltage protection

Figure 22. Simplified configuration for indoor over voltage protection

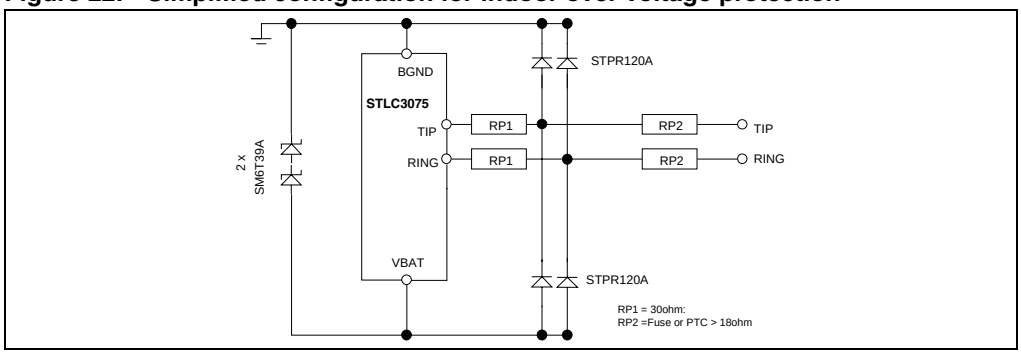
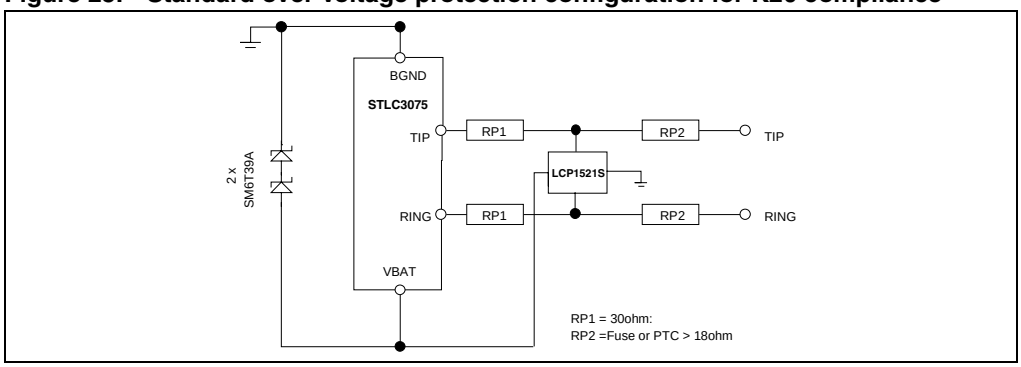
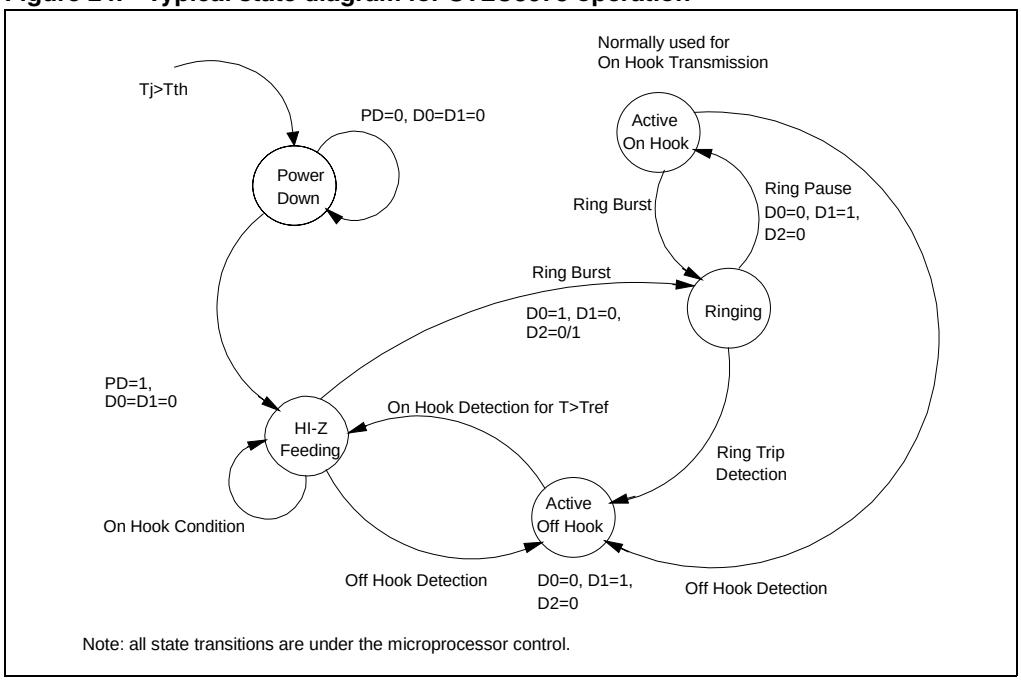


Figure 23. Standard over voltage protection configuration for K20 compliance



Appendix C Typical state diagram

Figure 24. Typical state diagram for STLC3075 operation



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