Rev 0; 2/08

MAXIM

Low-Power, Multifunction, Polyphase AFE

General Description

The MAXQ3180 is a dedicated electricity measurement front-end that collects and calculates polyphase voltage, current, power, energy, and many other metering and power-quality parameters of a polyphase load. The computed results can be retrieved by an external master through the on-chip serial peripheral interface (SPI™) bus. This bus is also used by the external master to configure the operation of the MAXQ3180 and monitor the status of operations.

The MAXQ3180 performs voltage and current measurements using an integrated ADC that can measure up to seven external differential signal pairs. An eighth differential signal pair is used to measure the die temperature. An internal amplifier automatically adjusts the current channel gain to compensate for low-current channel-signal levels.

Applications

3-Phase Multifunction Electricity Meters

Remote Terminal Unit (RTU) Applications for Electric Load Management

Features

- **Supports IEC 60687, IEC 61036, and IEC 61268 Standards**
- **Compatible with 3-Phase/3-Wire, 3-Phase/4-Wire, and Other 3-Phase Services**
- **Calculates Active/Reactive/Apparent Energy, RMS Voltage, RMS Current, Voltage Phasor Angle, and Line Frequency**
- **Less Than 0.1% Active Energy Error Over a Dynamic Range of 1000:1 at +25°C**
- **Less Than 0.2% Reactive Energy Error Over a Dynamic Range of 1000:1 at +25°C**
- **Better Than 0.5% Accuracy for RMS Voltage and RMS Current**
- **Two Pulse Outputs: One for Active Power and One Selectable Between Reactive and Apparent Power**
- **Programmable Pulse Width**
- **Programmable Startup Current Threshold**
- **Programmable Meter Constant**
- **Up to 21st Harmonic Measurement**
- **Neutral Line Current Measurement**
- **Calculates Amp-Hours in the Absence of Voltage Signals**
- **On-Chip User-Programmable Thresholds for Line Voltage Undervoltage and Overvoltage Detection**
- **On-Chip Digital Integrator Enables Direct Interface-to-Current Sensors with di/dt Output**
- **On-Chip Digital Temperature Sensor**
- **Precision Internal Voltage Reference 2.048V (30ppm/°C Typical); Also Supports an External Voltage Reference Input**
- **Active Energy of Each Phase and Combined 3-Phase (kWh), Positive and Negative**
- **Active Power of Each Phase and Combined 3-Phase (kW)**
- **Reactive Energy of Each Phase and Combined 3-Phase (kVarh), Quadrants 1 to 4**
- **Reactive Power of Each Phase and Combined 3-Phase (kVar)**
- **Apparent Energy of Each Phase and Combined 3-Phase (kVAh)**
- **Apparent Power of Each Phase and Combined 3-Phase (kVA)**
- **Line Frequency (Hz)**
- **Power Factor**
- **Overcurrent and Overvoltage Detection**
- **Voltage Sag Detection**
- **RMS Current and RMS Voltage**
- **Line-Cycle-Wise Instant Current, Voltage, and Power**
- **Phase Sequence Error Detection**
- **Phase Voltage Absence Detection**
- **Supports Software Meter Calibration**
- **Up to 3-Point Multipoint Calibration to Compensate for Transducer Nonlinearity**
- **Power-Fail Detection**
- **Bidirectional Reset Input/Output**
- **SPI-Compatible Serial Interface with Interrupt Request ($\overline{IRQ}$) Output**
- **Single 3.3V Supply, Low Power (10mW Typical)**
- **28-Pin TSSOP Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAXQ3180-RAN+	-40°C to +85°C	28 TSSOP

+Denotes a Pb-free/RoHS-compliant package.

Pin Configuration and Typical Application Circuit appear at end of data sheet.

MAXQ is a registered trademark of Maxim Integrated Products, Inc.
SPI is a trademark of Motorola, Inc.

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, go to:* ***www.maxim-ic.com/errata****.*

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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ABSOLUTE MAXIMUM RATINGS

Voltage Range on DVDD Relative to DGND .....-0.3V to +4.0V
Voltage Range on AVDD Relative to AGND.....-0.3V to +4.0V
Voltage Range on AGND Relative to DGND .....0.3V to +0.3V
Voltage Range on AVDD Relative to DVDD .....-0.3V to +0.3V
Voltage Range on Any Pin Relative to GND or AGND .....-0.3V to +4.0V

Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Soldering Temperature.....Refer to the IPC/JEDEC J-STD-020 Specification.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

METERING SPECIFICATIONS

(AV_{DD} = DV_{DD} = V_{RST} to 3.6V, Current Channel Dynamic Range 1000:1 at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Active Energy Error	DR 1000:1		0.1		%
Reactive Energy Error	DR 1000:1		0.2		%
Apparent Energy Error	DR 1000:1		0.5		%
RMS Voltage Error	DR 20:1		0.5		%
RMS Current Error	DR 500:1		0.5		%
Line Frequency Error			0.5		%
Power Factor Error			0.5		%
Active Energy Error with Harmonic Components	(Note 2)		0.1		%

ELECTRICAL CHARACTERISTICS

(AV_{DD} = DV_{DD} = V_{RST} to 3.6V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER-SUPPLY SPECIFICATIONS						
Digital Supply Voltage	DV_{DD}		V_{RST}		3.6	V
Power-Fail Interrupt Trip Point	V_{PFW}	Active mode, EPWRF = 1	2.84		3.13	V
Power-Fail Reset Trip Point	V_{RST}	Active mode	2.70		2.99	V
Analog Supply Voltage	AV_{DD}		V_{RST}		3.6	V
Analog Supply Current	I_{AVDD}	f_{CLK} = 8MHz		1.1	1.8	mA
Digital Supply Current	I_{DVDD}	f_{CLK} = 8MHz		9.0	14	mA
Low-Power Measurement Mode Current	I_{LPMM}	LOWPM = 1 (Note 1)		3		mA

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = V_{RST} to 3.6V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL I/O SPECIFICATIONS						
Input High Voltage	V_{IH}		0.7 x DV_{DD}			V
Input Low Voltage	V_{IL}				0.3 x DV_{DD}	V
Input Hysteresis	V_{IHYS}	DV_{DD} = 3.3V		550		mV
Input Leakage	I_L	V_{IN} = GND or DV_{DD}, pullup off		±0.01	±1	µA
Input Low Current	I_{IL}	V_{IN} = 0.4V, weak pullup on	-40			µA
$\overline{RESET}$ Pullup Resistance	R_{RESET}		27	32	36	kΩ
Output High Voltage (Except $\overline{RESET}$)	V_{OH}	I_{OH} = -4mA	DV_{DD} - 0.4			V
		I_{OH} = -6mA	DV_{DD} - 0.5			
Output Low Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
		I_{OL} = 6mA			0.5	
SYSTEM CLOCK SOURCES						
External Clock Input Frequency			0		8.12	MHz
External Clock Input Duty Cycle			45		55	%
External HF Crystal Frequency		Fundamental mode	1.00		8.12	MHz
XTAL1, XTAL2 Load Capacitance				30		pF
Internal RC Oscillator Frequency			7.4	8.0	8.6	MHz
Internal RC Oscillator Drift				250		ppm/°C
Internal RC Oscillator Current				50	120	µA
ANALOG-TO-DIGITAL CONVERTER						
Input Voltage Range			0		2	V
Offset Error				± 2		mV
Offset Error Drift				±8		µV/°C
Gain Error				0.025		%
Total Harmonic Distortion	THD	Input sine wave f = 1kHz		80		dB
Input Capacitance Differential		(Note 1)		32		pF
Input Bandwidth (-3dB)		(Note 1)		7		kHz
INTERNAL VOLTAGE REFERENCE						
Temperature Coefficient		(Note 1)		30		ppm/°C
Output Voltage				2.048		V
INTERNAL TEMPERATURE SENSOR						
Temperature Error		(Note 1)	-4		+4	°C

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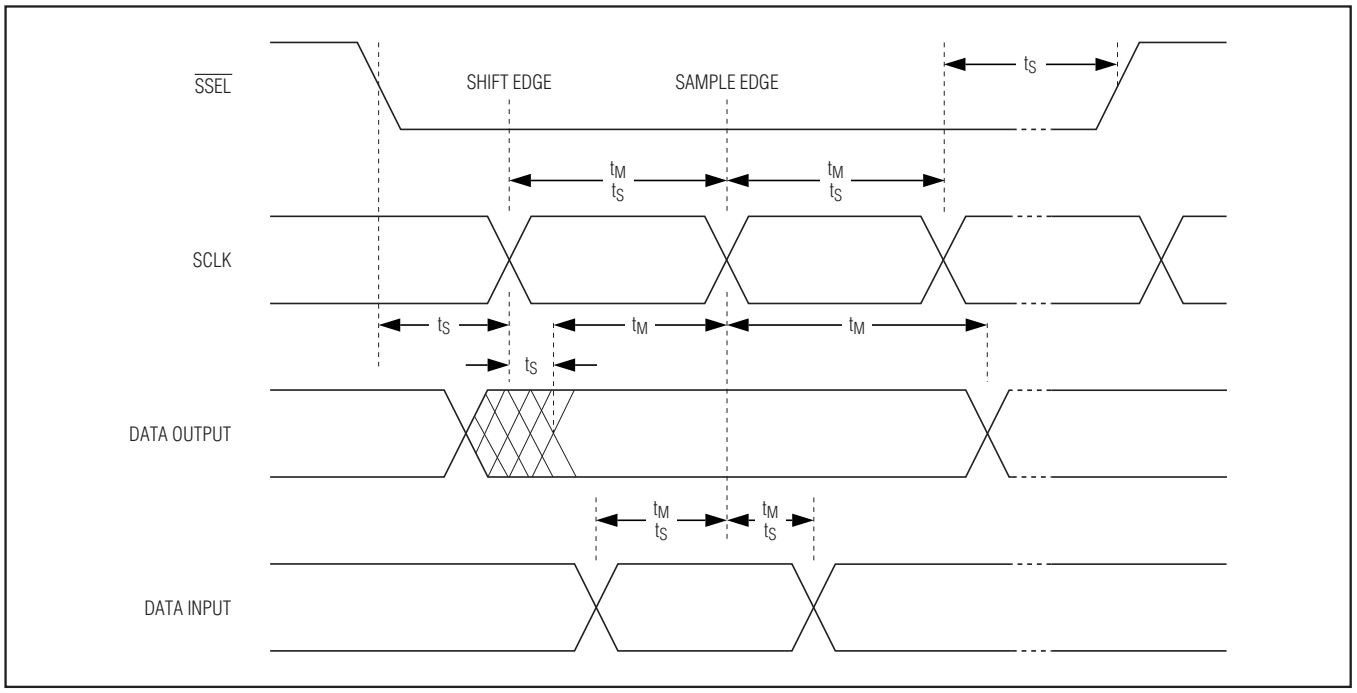
ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = V_{RST} to 3.6V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 3)

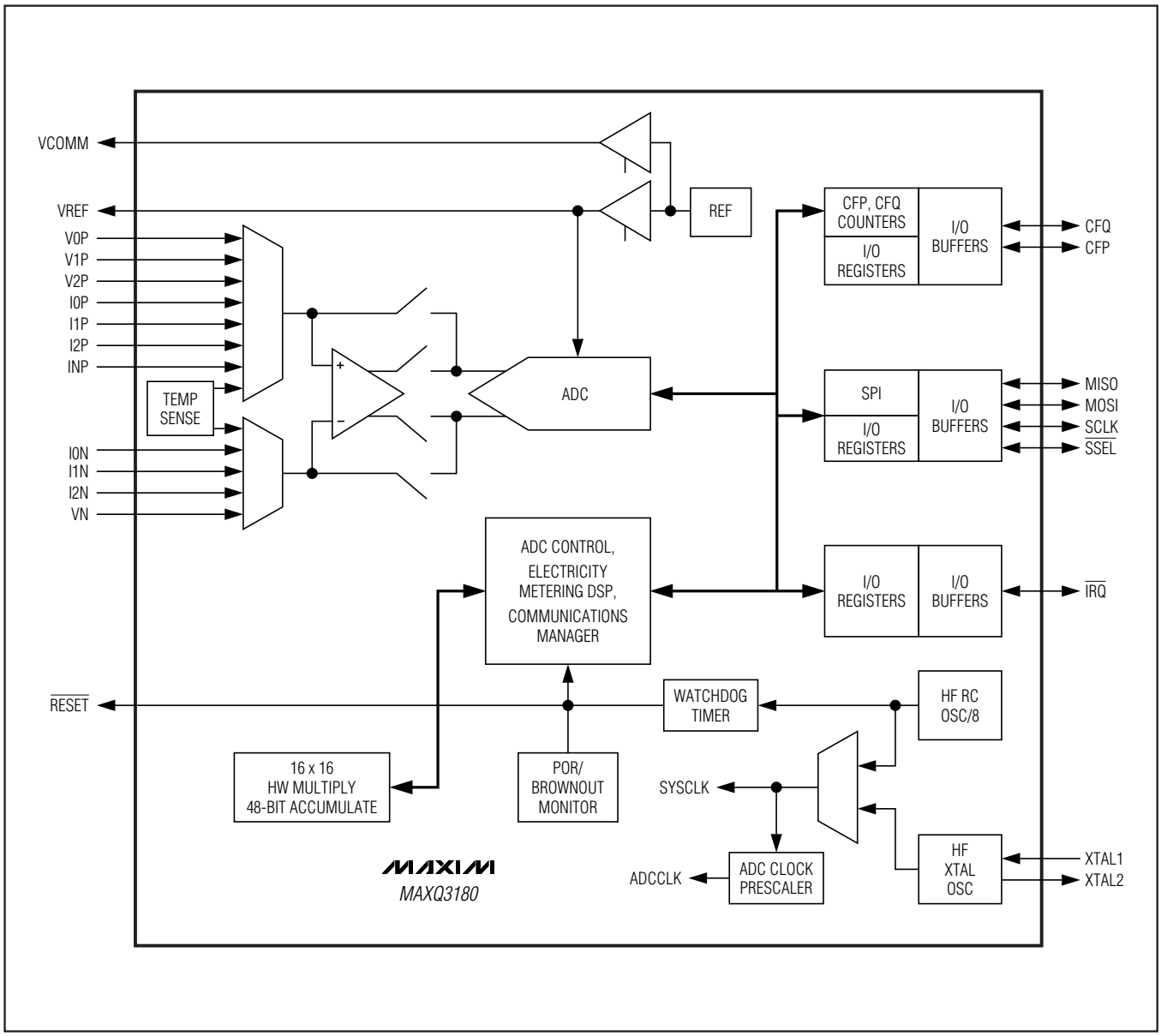
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPI SLAVE-MODE INTERFACE TIMING						
SCLK Input Pulse-Width High	t_{SCH}		4 x t_{CLCL}			ns
SCLK Input Pulse-Width Low	t_{SCL}		4 x t_{CLCL}			ns
$\overline{SSEL}$ Low to First SCLK Edge (Slave Enable)	t_{SE}		4 x t_{CLCL}			ns
Last SCLK Edge to $\overline{SSEL}$ High (Slave Disable)	t_{SD}		2 x t_{CLCL}			ns
MOSI Valid to SCLK Sample Edge (MOSI Setup)	t_{SIS}		3 x t_{CLCL}			ns
SCLK Sample Edge to MOSI Change (MOSI Hold)	t_{SIH}		t_{CLCL}			ns
SCLK Shift Edge to MISO Valid (MISO Hold)	t_{SOV}				3 x t_{CLCL}	ns

Note 1: Specifications guaranteed by design but not production tested.
Note 2: Conditions abide to Section 5.6.2.1 per IEC 61036.
Note 3: Specifications to -40°C are guaranteed by design and are not production tested.

SPI Slave Mode Timing



Block Diagram



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Pin Description

PIN	NAME	FUNCTION
1	VN	Analog Inputs for the Phase A, Phase B, Phase C, and Neutral Current Channels
2	INP	
3	I0P	
4	I0N	
5	I1P	
6	I1N	
7	I2P	
8	I2N	
9	AGND	Analog Ground
10	XTAL2	High-Frequency Crystal Input/Output. When using an external high-frequency crystal, the crystal oscillator circuit should be connected between XTAL1 and XTAL2. When using an externally driven clock (EXTCLK = 1), the clock should be input at XTAL1, with XTAL2 left unconnected.
11	XTAL1	
12	$\overline{IRQ}$	Interrupt Request Output. This line is driven low by the device to indicate to the master that an unmasked interrupt has occurred.
13	$\overline{SSEL}$	Slave Select Input. This line is the active-low slave select input for the SPI interface.
14	SCLK	Slave Clock Input. This line is the clock input for the SPI interface, which always operates in slave mode.
15	MOSI	Master Out-Slave In Input. This line is used by the master to transmit data to the slave (the MAXQ3180) over the SPI interface.
16	MISO	Master In-Slave Out Output. This line is used by the MAXQ3180 (the slave) to transmit data back to the master over the SPI interface.
17, 22	DVDD	Digital Supply Voltage
18	DGND	Digital Ground
19	CFP	Active Energy Pulse Output
20	CFQ	Reactive Energy Pulse Output
21	$\overline{RESET}$	Active-Low Reset Input/Output. An external master can reset the MAXQ3180 by driving this pin low. This pin includes a weak pullup resistor to allow for a combination of wired-OR external reset sources. An RC circuit is not required for power-up, as this function is provided internally. This pin also acts as a reset output when the source of the reset is internal to the device (power-fail, watchdog reset, etc.). In this case, the $\overline{RESET}$ pin is held low by the device until it exits the reset state, then the $\overline{RESET}$ pin is released.
23	VCOMM	Voltage Bias. This pin can be used to create an input common-mode DC offset for ADC channel conversions.
24	VREF	Voltage Reference. Reference voltage for the ADC. An external reference voltage can be connected to this pin when extremely high accuracy is required.
25	AVDD	Analog Supply Voltage
26	V0P	Analog Inputs for the Phase A, Phase B, and Phase C Voltage Channels
27	V1P	
28	V2P	

Detailed Description

Operating Modes

The MAXQ3180 has four basic modes of operation, each of which is described in the following sections. The Initialization Mode is the default mode upon power-up or following reset; entry to and exit from the other operating modes is only performed as a result of commands sent by the master.

Initialization Mode

This is the default operating mode for the MAXQ3180 following reset, power-up, or a switch into or out of Low-Power Measurement Mode (LPMM). In this mode, no power measurements are taken because the MAXQ3180 has not yet been configured. When entering this mode, the MAXQ3180 sets the status flag NOINIT to 1 and drives the $\overline{IRQ}$ pin low to indicate to the master that initialization is required. The master is responsible for performing the following series of operations:

- Interrogating the MAXQ3180 to determine that the NOINIT bit has been set.
- Loading all RAM configuration registers with appropriate values.
- Clearing the NOINIT bit to zero.

Once the NOINIT bit has been cleared to zero, the MAXQ3180 exits Initialization Mode and enters Run Mode (or LPMM mode if LOWPM = 1). It is the master's responsibility to ensure that all configuration registers have been set to their correct values before clearing the NOINIT bit.

Run Mode

This mode is the normal operating mode for the MAXQ3180. In this mode, the MAXQ3180 continuously executes the following operations:

- Scans analog front-end channels and collects raw voltage and current samples.
- Processes voltage and current samples through DSP filters as enabled and configured.
- Calculates power, energy, and other required quantities and stores these values in RAM registers.
- Responds to register write and read commands from the master.
- Outputs power pulses on CFP and CFQ as configured.
- Drives $\overline{IRQ}$ when an interrupt condition has been detected and the interrupt is not masked.

Low-Power Measurement Mode (LPMM)

This mode allows the MAXQ3180 to perform all normal electric-metering functions while operating at a reduced clock rate to conserve power. In this mode, the MAXQ3180 switches its system clock from the high-frequency external crystal (or external clock source) to its internal RC oscillator. The actual system clock frequency used is the RC oscillator output frequency divided by 8, which results in a system clock frequency of approximately 1MHz.

Entry to LPMM Mode only occurs at the request of the master. The master must set the LOWPM bit (STATUS.2) to 1 to place the MAXQ3180 into LPMM mode. Setting this bit automatically sets the NOINIT bit and returns the device to Initialization Mode. This is done because changing the clock frequency invalidates a number of configuration registers, which need to be reinitialized with new, updated values before metering-measurement operations can continue. Note that it is also possible to set LOWPM = 1 (and load configuration registers appropriately) immediately following reset, which causes the MAXQ3180 to transition directly from Initialization Mode to LPMM Mode once NOINIT has been cleared by the master.

The master can also instruct the MAXQ3180 to exit LPMM Mode by clearing the LOWPM bit. This causes NOINIT to be set as with LPMM entry, and the master must reset the appropriate configuration registers and clear NOINIT to allow measurement to continue.

Stop Mode

This mode places the MAXQ3180 into a power-saving state where it consumes the least possible amount of current. In Stop Mode, all functions are suspended, including the ADC and power and voltage measurement and processing. The MAXQ3180 does not respond to any commands from the master in this operating state.

Entry into Stop Mode only occurs at the request of the master. To place the MAXQ3180 into Stop Mode, the master must set the STOPM bit (STATUS.1) to 1. Once this bit has been written, the MAXQ3180 enters Stop Mode immediately following the end of the register write command (after the transmission of the final ACK byte by the MAXQ3180).

There are three possible ways to bring the MAXQ3180 back out of Stop Mode.

- **Power Cycle.** The MAXQ3180 automatically exits Stop Mode if a power-on reset occurs. Following exit from Stop Mode, all registers are cleared back to their default states, and the MAXQ3180 transitions to Initialization Mode.
- **External Reset.** The MAXQ3180 exits Stop Mode if an external reset is triggered by driving $\overline{RESET}$ low. Once the $\overline{RESET}$ pin is released and allowed to

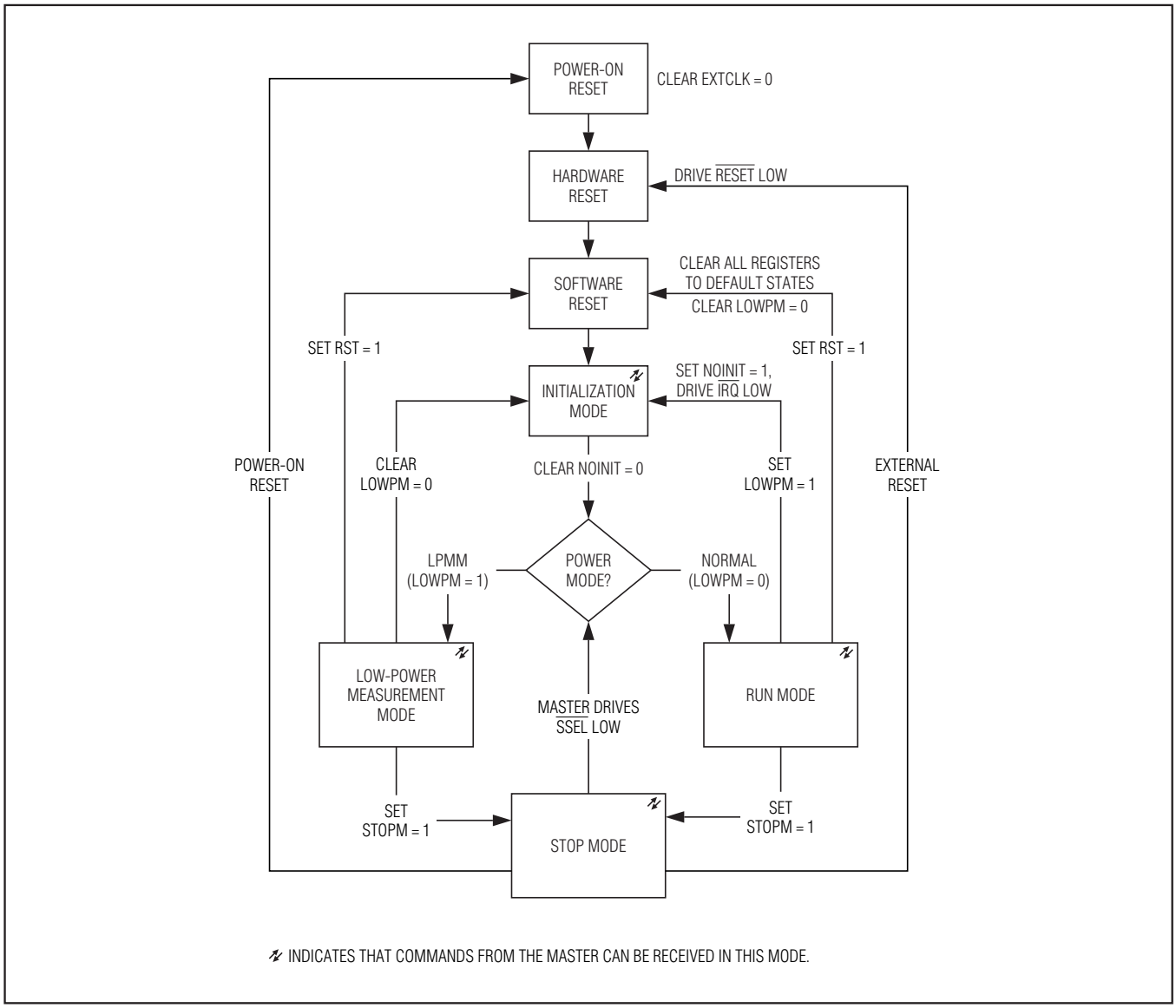

Figure 1. Operating Modes

return to a high state, the MAXQ3180 comes out of reset and goes into Initialization Mode. All registers are cleared to their default states when exiting Stop Mode in this manner.

- **External Interrupt.** Driving the $\overline{SSEL}$ pin low causes the MAXQ3180 to exit Stop Mode without undergoing a reset cycle. When exiting Stop Mode in this manner, all register and configuration settings are retained, and the MAXQ3180 automatically resumes electric-metering functions and sample processing.

Note that when the master is communicating with the MAXQ3180, the $\overline{SSEL}$ line is normally driven low at the beginning of each SPI command. This means that if the master sends an SPI command after the MAXQ3180 enters Stop Mode, the MAXQ3180 automatically exits Stop Mode and receives the command.

Reset Sources

There are several different sources that can cause the MAXQ3180 to undergo a reset cycle. For any type of hardware reset, the $\overline{\text{RESET}}$ pin is driven low when a reset occurs.

External Reset

This hardware reset is initiated by an external source (such as the master controller or a manual pushbutton press) driving the $\overline{\text{RESET}}$ pin on the MAXQ3180 low. The $\overline{\text{RESET}}$ line must be held low for at least four cycles of the currently selected clock for the external reset to take effect. Once the external reset takes effect, it remains in effect indefinitely as long as $\overline{\text{RESET}}$ is held low. Once the external reset has been released, the MAXQ3180 clears all registers to their default states and resumes execution in Initialization Mode.

When an external reset occurs outside of Stop Mode, execution (in Initialization Mode) resumes after four cycles of the currently selected clock (external high-frequency crystal for Run Mode, 1MHz internal RC oscillator for LPMM Mode). As the MAXQ3180 enters Initialization Mode, the LOWPM bit is always cleared to 0, meaning that the MAXQ3180 always switches to the high-frequency clock before it begins accepting commands in Initialization Mode.

When an external reset occurs from Stop Mode, execution (in Initialization Mode) resumes after 128 cycles of the internal RC oscillator (or approximately 128µs).

Power-On Reset

When the MAXQ3180 is first powered up, or when the power supply, DV_{DD}, drops below the V_{RST} power-fail trip point (outside of Stop Mode), the MAXQ3180 is held in power-on reset. Once the power supply rises above the V_{RST} level, the power-on reset state is released and all registers are reset to their defaults and execution resumes in Initialization Mode. The high-frequency external crystal (LOWPM = 0) is always selected as the clock source following any power-on or brownout reset.

In Stop Mode brownout detection is disabled, so a power-on reset does not occur until DV_{DD} drops to a lower level (V_{POR}). From the master's perspective, power-on resets and brownout resets both cause the MAXQ3180 to reset in the same way.

Watchdog Reset

The MAXQ3180 includes a hardware watchdog timer that is armed and periodically reset automatically during normal operation. Under normal circumstances, the MAXQ3180 always resets the watchdog timer often enough to prevent it from expiring. However, if an internal

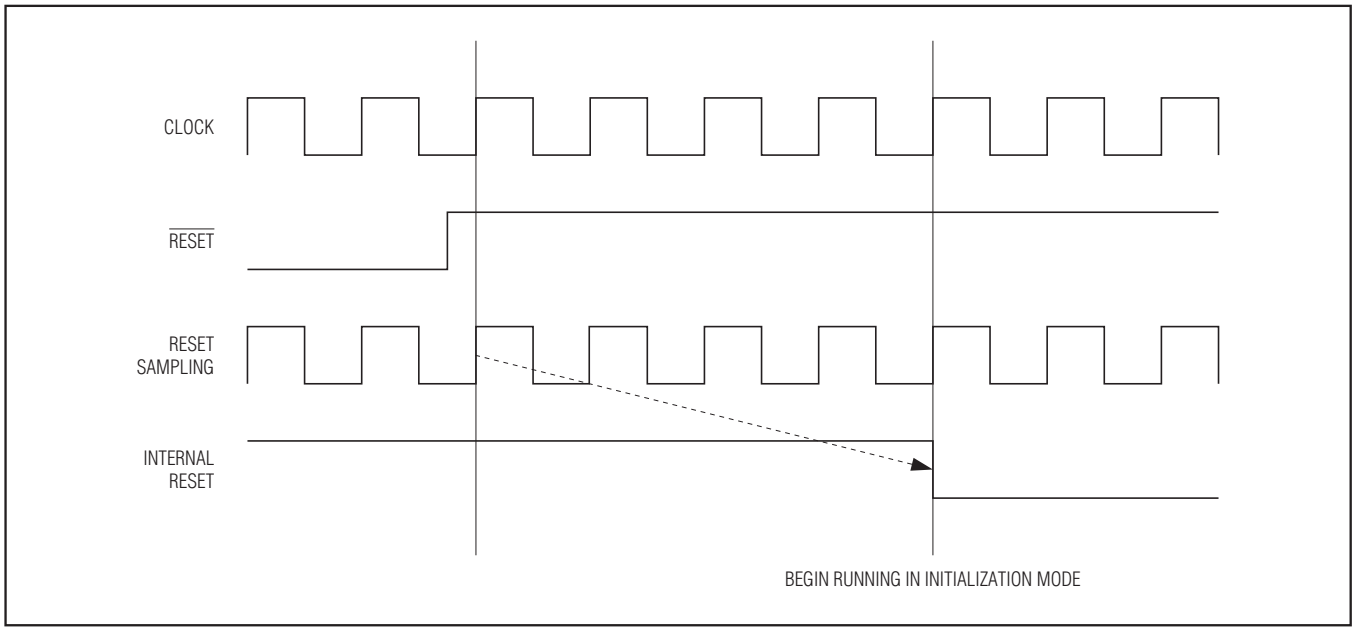

Figure 2. External Reset

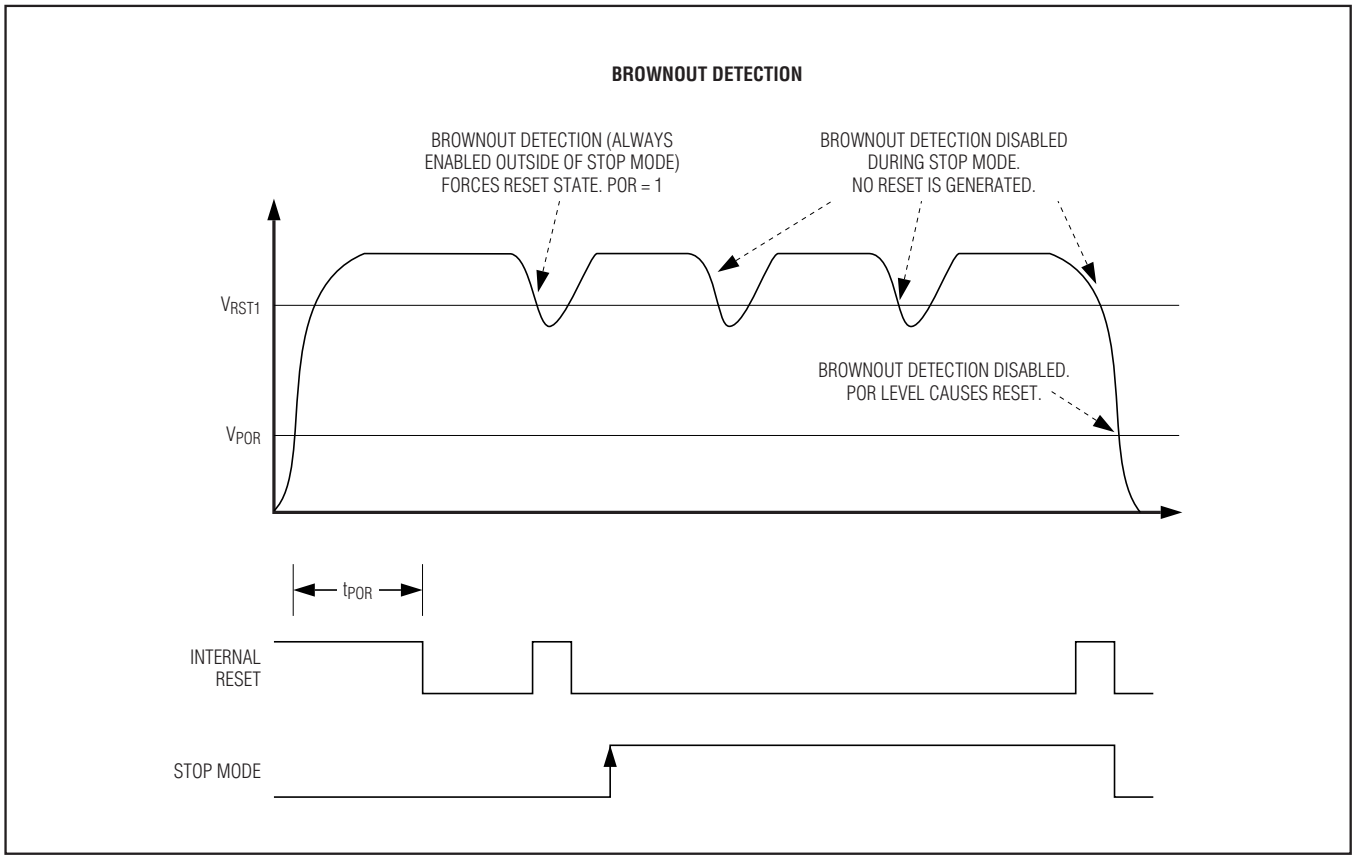

Figure 3. Brownout Reset

error of some kind causes the MAXQ3180 to lock up or enter an endless execution loop, the watchdog timer expires and triggers an automatic hardware reset. There is no register flag to indicate to the master that a watchdog reset has occurred, but the $\overline{\text{RESET}}$ line strobes low briefly. Because the reset causes the MAXQ3180 to re-enter Initialization Mode, the $\overline{\text{IRQ}}$ line drops low.

The watchdog timer does not run during Stop Mode.

Software Reset

A software reset is initiated by the master by setting the RST (STATUS0.4) bit to 1. When a software reset occurs, the MAXQ3180 clears all registers to their default states and returns to Initialization Mode, in the same manner as if an external reset had taken place. Unlike a hardware reset, however, a software reset does not cause the MAXQ3180 to drive the $\overline{\text{RESET}}$ line low.

Power-Supply Monitoring

In addition to the hardware reset provided by the power-on reset and brownout reset circuits, the MAXQ3180 includes the capability to detect a low power supply on the DVDD pin and alert the master through the interrupt ($\overline{\text{IRQ}}$) mechanism before a hardware reset occurs. This function, which is always enabled outside of Stop Mode, causes the RAM status register flag PWRF (STATUS1.1) to be set to 1 whenever DV_{DD} drops below the V_{PFW} trip point. Once PWRF has been set to 1 by hardware, it can only be cleared by the master (or by a system reset). Whenever PWRF = 1, if the EPWRF interrupt masking bit is also set to 1, the MAXQ3180 drives $\overline{\text{IRQ}}$ low to signal to the master that an interrupt condition (in this case, a power-fail warning) exists and requires attention.

Clock Sources

All operations including ADC sampling and SPI communications are synchronized to a single system clock. This clock can be obtained from any one of three selectable sources, as shown in Figure 4.

External High-Frequency Crystal

The default system clock source for the MAXQ3180 is an external high-frequency crystal oscillator circuit connected between XTAL1 and XTAL2. When clocked with an external crystal, a parallel-resonant, AT-cut crystal oscillating in the fundamental mode is required. The typical values of the external load capacitors vary with the type of crystal being used and should be selected based on the load capacitance as suggested by the crystal manufacturer.

When using a high-frequency crystal, the fundamental oscillation mode of the crystal operates as inductive reactance in parallel resonance with external capacitors C1 and C2. The typical values of these external capacitors vary with the type of crystal being used and should be selected based on the load capacitance as suggested by the crystal manufacturer.

Since noise at XTAL1 and XTAL2 can adversely affect device timing, the crystal and capacitors should always be placed as close as possible to the XTAL1 and XTAL2 pins, with connection traces between the crystal and the device kept as short and direct as possible. In multiple layer boards, avoid running other high-speed digital signals underneath the crystal oscillator circuit if possible, as this may inject unwanted noise into the clock circuit.

Following power-up or any system reset, the high-frequency clock is automatically selected as the system clock source. However, before this clock can be used for system execution, a crystal warmup timer must count 65,536 cycles of the high-frequency clock. While this warmup time period is in effect, execution continues using the internal 1MHz oscillator. Once the 65,536-cycle count completes (which requires approximately 8.2ms at 8MHz), the device automatically switches over to the high-frequency clock. This crystal warmup timer is also activated upon exit from Stop Mode, since the high-frequency crystal oscillator is shut down during Stop Mode.

External High-Frequency Clock

Instead of using a crystal oscillator to generate the high-frequency clock, it is also possible to input a high-frequency clock that has been generated by another source (such as a digital oscillator IC) directly into the XTAL1 pin of the MAXQ3180.

To use an external high-frequency clock as the system clock source, the XTAL1 pin should be used as the

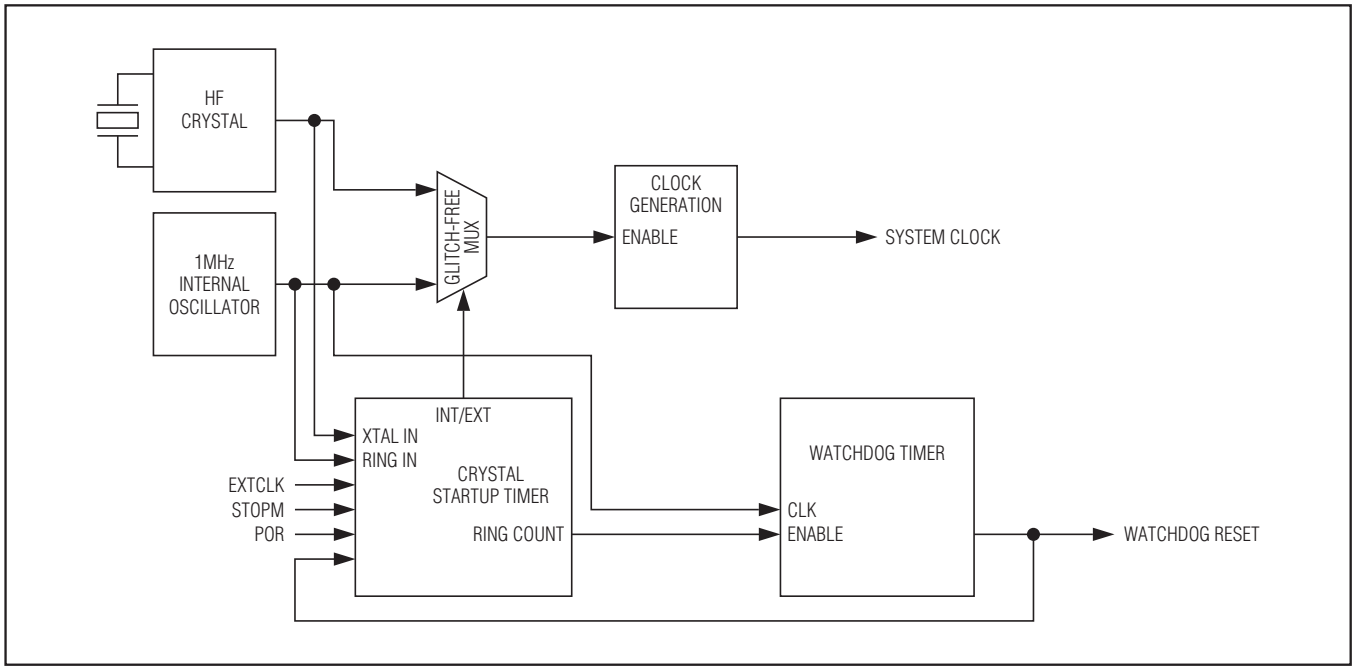

Figure 4. Simplified Clock Sources

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clock input and the XTAL2 pin should be left unconnected. The master should also shut down the internal crystal oscillator circuit by setting the EXTCLK bit (STATUS0.6) to 1. This bit is only cleared by the MAXQ3180 if a power-on or brownout reset occurs and is unaffected by other resets.

When using an external high-frequency clock, the clock signal should be generated by a CMOS driver. If the clock driver is a TTL gate, its output must be connected to DVDD through a pullup resistor to ensure that the correct logic levels are generated. To minimize system noise in the clock circuitry, the external clock source must meet the maximum rise and fall times and the minimum high and low times specified for the clock source in the *Electrical Characteristics* table.

Internal RC Oscillator

When the external high-frequency crystal is warming up, or when the MAXQ3180 is placed into LPMM mode, the system clock is sourced from an internal RC oscillator. This internal oscillator is designed to run at approximately 8MHz, although the exact frequency varies over temperature and supply voltage.

If no external crystal circuit or high-frequency clock will be used, the MAXQ3180 can be forced to operate indefinitely from the internal oscillator by grounding XTAL1. This ensures that the crystal warmup count never completes, so the MAXQ3180 runs from the internal oscillator in all active modes (Initialization Mode, Run Mode, and LPMM Mode).

Master Communications

Before the MAXQ3180 can begin performing electric-metering operations, the master must initialize a number of configuration parameters. Since the MAXQ3180 does not contain internal nonvolatile memory, these parameters (stored in internal registers) must be set by the master each time a power-up or reset cycle occurs, or each time a switch is made between LPMM Mode and Run Mode.

The external master communicates with the MAXQ3180 over a standard SPI bus, using commands to read and write values to internal registers on the MAXQ3180. These registers include, among many other items:

- Operating mode settings (Stop Mode, LPMM Mode, external clock mode, etc.)
- Status and interrupt flags (not initialized, power-supply failure, overcurrent/overvoltage detection)
- Masking control for interrupts to determine which conditions cause $\overline{IRQ}$ to be driven low
- Configuration settings for analog channel scanning
- Power pulse output configuration
- Filter coefficients and configuration
- Read-only registers containing accumulated power and energy data

Once all the configuration registers have been set by the master to their proper values, the master must clear the NOINIT flag (STATUS1.0) to zero. Once this flag has been cleared, the MAXQ3180 exits Initialization Mode and begins execution in either Run Mode or LPMM Mode, depending on the setting of the LOWPM bit.

As the MAXQ3180 obtains voltage and current measurements in Run Mode or LPMM Mode, it accumulates, filters, and performs a number of calculations on the collected data. Many of these operations (including the various filtering stages) are configured by settings in registers written by the master. The output results can then be read by the master from various read-only registers in parallel with the ongoing measurement and processing operations.

SPI Communications Rate and Format

The MAXQ3180 provides an SPI bus for master/slave communications. All communications transfers are initiated by the external master. The interrupt request line $\overline{IRQ}$, while not technically part of the SPI bus interface, is also used for master/slave communications, since it allows the MAXQ3180 to notify the master that an interrupt condition exists.

During an SPI transfer, data is simultaneously transmitted and received over two serial data lines (MISO and MOSI) with respect to a single serial shift clock (SCLK). The polarity and phase of the serial shift clock are the primary components in defining the SPI data transfer format. The polarity of the serial clock corresponds to the idle logic state of the clock line and, therefore, also defines which clock edge is the active edge. To define a serial shift clock signal that idles in a logic-low state (active clock edge = rising), the clock polarity select (CKPOL; SPICF.0) bit should be configured to a 0, while setting CKPOL = 1 causes the shift clock to idle in a logic-high state (active clock edge = falling). The phase of the serial clock selects which edge is used to sample the serial shift data. The clock phase select (CKPHA; SPICF.1) bit controls whether the active or inactive clock edge is used to latch the data. When CKPHA is set to a logic 1, data is sampled on the inactive clock edge (clock returning to the idle state). When CKPHA is set to a logic 0, data is sampled on the active clock edge (clock transition to the active state). Together, the CKPOL and CKPHA bits allow four possible SPI data transfer formats.

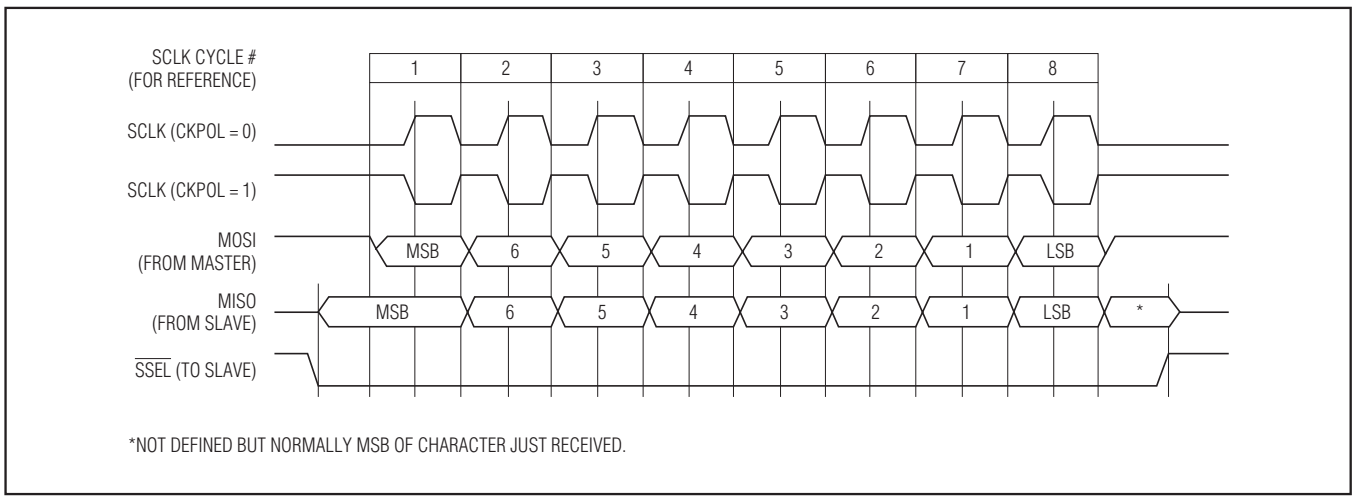

Figure 5a. SPI Interface Timing (CKPHA = 1). With CKPHA = 1 and CKPOL = 1, the SPI interface clocks data into the peripheral device on the clock's rising edge and data out of the peripheral on the clock's falling edge.

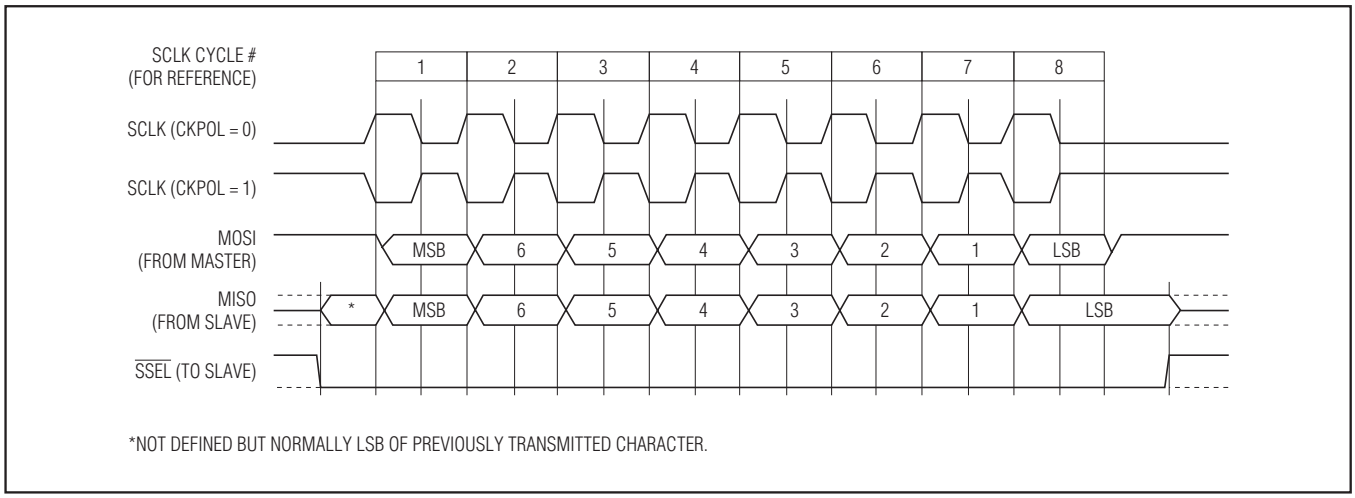

Figure 5b. SPI Interface Timing (CKPHA = 0). With CKHPA = 0 and CKPOL = 1, the SPI interface clocks data into the peripheral device on the clock's falling edge and data out of the peripheral on the clock's rising edge.

Transfers over the SPI interface always start with the most significant bit and end with the least significant bit. All SPI data transfers to and from the MAXQ3180 are always 8 bits (one byte) in length. The MAXQ3180 SPI interface does not support 16-bit character lengths.

The default format (upon power-up or system reset) for the MAXQ3180 SPI interface is represented in Figure 5b (CKPOL = 0; CKPHA = 0). In this format, the SPI clock idle state is low, and data is shifted in and out on the rising edge of SCLK. Once SPI communication with the MAXQ3180 has been established, it is possible to alter the CKPOL and CKPHA format settings (as well as changing the $\overline{SSEL}$ signal from active low to active high) if desired by writing to the R_SPICF mirror register and then reading from the special command register UPD_SFR to copy the R_SPICF value into the internal SPI configuration register.

Whenever the active clock edge is used for sampling (CKPHA = 0), the transfer cycle must be started with assertion of the $\overline{SSEL}$ signal. This requirement means that the $\overline{SSEL}$ signal be deasserted and reasserted between successive transfers. Conversely, when the inactive edge is used for sampling (CKPHA = 1), the $\overline{SSEL}$ signal may remain low through successive

transfers, allowing the active clock edge to signal the start of a new transfer.

The clock rate used for the SPI interface is determined by the bus master, since the MAXQ3180 always operates as an SPI slave device. However, the maximum clock rate is limited by the system clock frequency of the MAXQ3180. For proper communications operation, the SPI clock frequency used by the master must be less than or equal to the MAXQ3180's clock frequency divided by 8. For example, when the MAXQ3180 is running at 8MHz, the SPI clock frequency must be 1MHz or less. And if the MAXQ3180 is running in LPMM Mode (or if the crystal is still warming up), the SPI clock frequency must remain at 125kHz or less for proper communications operation.

In addition to limiting the overall SPI bus clock rate, the master must also include a communications delay following each byte transmit/receive cycle. This delay, which provides the MAXQ3180 with time to process the transmitted byte, should be a minimum of 1 ADC scan slot (time value contained in TIME_FS register, defined as (R_ADCRATE + 1)/(system clock frequency). With default settings and running at 8MHz, this delay time is 25µs. Reducing the system clock frequency to 1MHz (LPMM mode) would increase this delay period by a factor of 8µs to 200µs.

SPI Communications Protocol

All transactions between the master and the MAXQ3180 consist of the master writing to or reading from one of the MAXQ3180's registers. There are several different categories of internal registers on the MAXQ3180.

- **RAM Registers.** The values of these registers are stored in the internal RAM of the MAXQ3180. Some can be read and written by the master, while others are read only. RAM registers are either two or four bytes long (16 or 32 bits), although in some registers not all the bits have defined values. Read/write registers are generally either status/flag registers (which can be written by either the MAXQ3180 or the master), configuration registers (which are written by the master and read by the MAXQ3180 firmware), or data registers (which are read only and are written by the MAXQ3180 firmware and read by the master).
- **Virtual Registers.** These read-only registers are not stored in RAM; instead, they contain values that are calculated on the fly by the MAXQ3180 firmware when the master reads them. These registers are used by the master to obtain values such as phase A, B, and C active, reactive, and apparent power; power factor; and RMS voltage and current, which are calculated from currently collected data on an as-needed basis. All virtual registers are 4 bytes in length.
- **Hardware Registers.** These registers control core functions of the MAXQ3180 including the ADC and the SPI slave bus controller. Each of these registers (R_ACFG, R_ADCRATE, R_ADCADQ, R_SPICF, and STATUS0 (bit 6, EXTCLK only)) has a register location in RAM that "shadows" the value of the hardware register. To read from a hardware register, the master must first read from the special command register UPD_MIR (A00h) to copy the values from the hardware registers to the mirror registers in RAM, and then the mirror register in RAM can be read. To write to a hardware register, the master reverses the process by writing to the mirror RAM register and then reading from the special command register UPD_SFR (900h) to copy the values from the mirror registers to the hardware registers.
- **Special Command Registers.** These registers (UPD_SFR and UPD_MIR) do not return meaningful data when read but instead trigger an operation. Reading UPD_SFR causes values to be copied from the mirror registers to hardware, and reading UPD_MIR causes values to be copied from the hardware to mirror registers.

Every defined register on the MAXQ3180 has a 12-bit address (from 0 to 4095). This address is used when addressing the register for either a read or write operation. Addresses 0 to 1023 (000h to 3FFh) are used to address RAM registers. Registers with addresses from 1024 to 4095 (400h to FFFh) are used for virtual registers and special command registers.

Each command consists of a read/write command code, a data length (1, 2, 4, or 8 bytes), a 12-bit register address, and the specified number of data bytes followed optionally by a CRC. Since SPI is a full-duplex interface, the master and slave must both transmit the same number of bytes during the command. When a multiple-byte register is read or written (2/4/8 byte length), the least significant byte is read or written first in the command.

Table 1. Command Format for SPI Register Read

BYTE	TRANSFERS	BIT	DESCRIPTION
1st byte	Master sends command; Slave sends 0xC1 byte	7:6	Command Code: 00 Read 01 Reserved 10 Write
		5:4	Data Length: 00 1 byte 01 2 bytes 10 4 bytes
		3:0	MSB portion of data address.
2nd byte	Master sends address; Slave sends 0xC2 byte	7:0	LSB portion of data address.
Sync bytes	Master sends dummy; Slave sends ACK (0x41) or NACK (0x4E) byte	7:0	Master sends dummy byte; Slave responds with NACK if busy, or with ACK when processing complete. Master must receive ACK, then receive data.
3rd byte (1st data byte)	Master sends dummy; Slave sends data	7:0	Data, LSB
...	...	...	...
Nth byte (Last data byte)	Master sends dummy; Slave sends data	7:0	Data, MSB
(N + 1) byte	Master sends dummy; Slave sends CRC	7:0	Optional CRC

Table 2. Command Format for SPI Register Write

BYTE	TRANSFERS	BIT	DESCRIPTION
1st byte	Master sends command; Slave sends 0xC1 byte	7:6	Command code: 00 Read 01 Reserved 10 Write
		5:4	Data Length: 00 1 byte 01 2 bytes 10 4 bytes
		3:0	MSB portion of data address.
2nd byte	Master sends address; Slave sends 0xC2 byte	7:0	LSB portion of data address.
3rd byte (1st data byte)	Master sends data; Slave sends ACK (0x41)	7:0	Data, LSB
...	...	...	...
Nth byte (Last data byte)	Master sends data; Slave sends ACK (0x41)	7:0	Data, MSB
(N + 1) byte	Master sends CRC; Slave sends ACK (0x41)	7:0	Optional CRC
Sync bytes	Master sends dummy; Slave sends ACK (0x41) or NACK (0x4E) byte	7:0	Master sends dummy byte; Slave responds with NACK if busy, or with ACK when processing complete. Master must receive ACK before starting the next transaction.

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Optionally, a cyclic redundancy check (CRC) byte can be appended to each transaction. For write commands, the CRC byte is sent by the master, and for read commands the CRC byte is sent by the MAXQ3180. The CRC mode is enabled when the CRCEN bit is set to 1 in STATUS0 register. Otherwise, the MAXQ3180 assumes no CRC byte is used. The 8-bit CRC is calculated for all bytes in a transaction, from the first command byte sent by the master through the last data byte excluding sync bytes, using the polynomial $P = x^8 + x^5 + x^4 + 1$. If the transmitted CRC byte does not match the calculated CRC byte (for a write command), the MAXQ3180 ignores the command.

The length of the transfer is defined by the first command byte and the status of the CRCEN bit in the STATUS0 register. There is no special synchronization mechanism provided in this simple protocol. Therefore, the master is responsible for sending/receiving the correct number of bytes. If the master mistakenly sends more bytes than are required by the current command, the extra bytes are either ignored (if the MAXQ3180 is busy processing the previous command) or are interpreted as the beginning of a new command. If the master sends fewer bytes than are required by the current command, the MAXQ3180 waits for approximately 200ms, then drops the transaction and resets the communication channel. The duration of the timeout can be configured through the COM_TIMO register.

Figures 6 and 7 show typical 2-byte reading and writing transfers (without CRC byte).

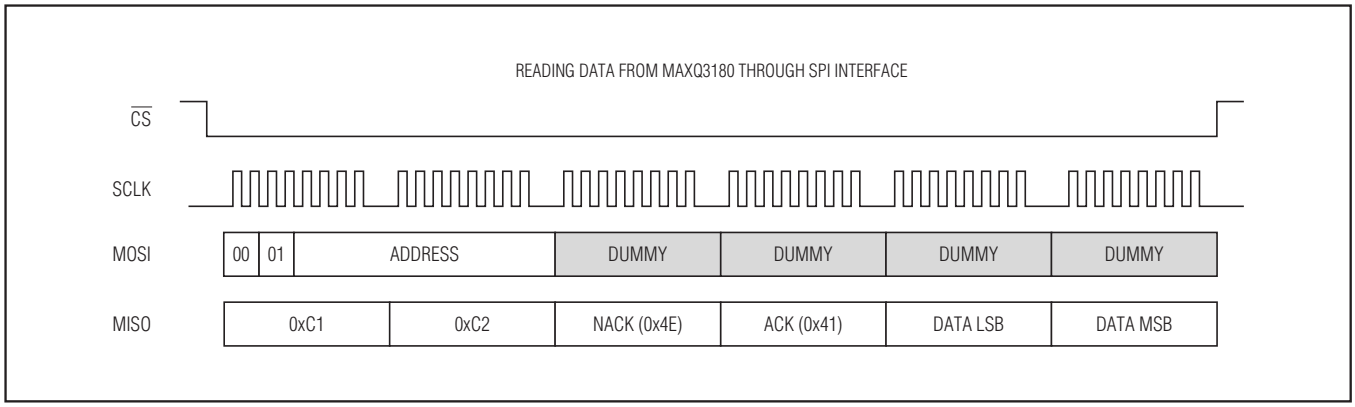

Figure 6. Read SPI Transfer

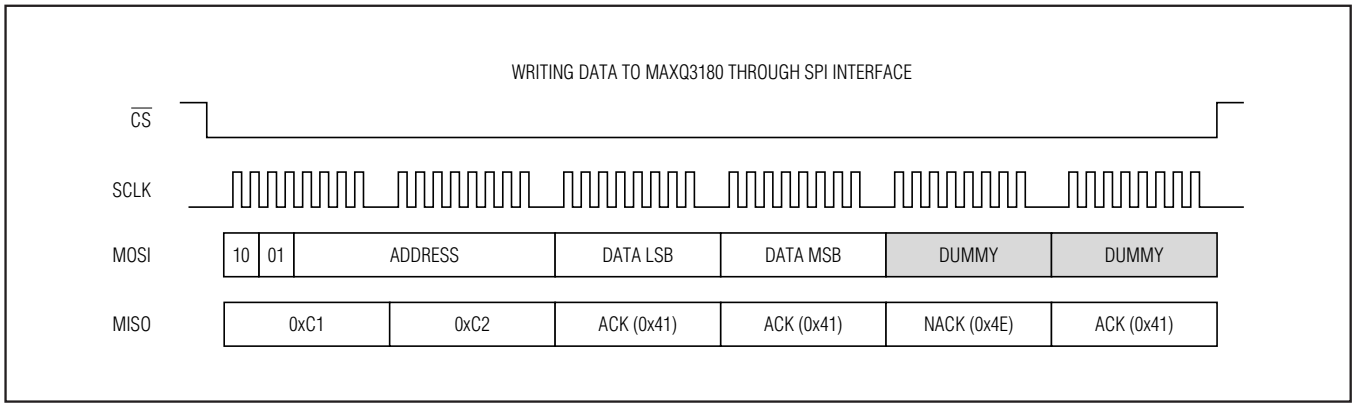

Figure 7. Write SPI Transfer

Table 3. RAM Register Map

	x0h	x1h	x2h	x3h	x4h	x5h	x6h	x7h	x8h	x9h	xAh	xBh	xCh	xDh	xEh	xFh
0xh	STATUS0		OPMODE		STATUS1		INT_MASK		STATUS2		CONNCT					
1xh	SCAN_0		SCAN_1		SCAN_2		SCAN_3		SCAN_4		SCAN_5		SCAN_6		SCAN_7	
2xh	TIME_FS		VOLT_FS		AMP_FS		PWR_FS		KWHT				KAHT			
3xh	CYCNT		PLSCFG		THR1				THR2				PLS1_WD		PLS2_WD	
4xh																
5xh					AVC0		AVC1		LPF_B0FZC		LPF_B0FNS		LPF_B0FSM		HPF_B0F	
6xh	BPF_B0F		BPF_A1F										PKCYC		SAGCYC	
7xh	OCLVL		OVLVL		SAGLVL		IUBLVL		VUBLVL		NZC_TIMO		REV_TIMO		ACC_TIMO	
8xh	COM_TIMO		R_ACFG		R_ADCRATE		R_ADCACQ		R_SPICF		NOLOAD		NS			
9xh	RAW_TEMP															
Axh																
Bxh																
Cxh																
Dxh																
Exh	PHASE_A_ KWHAP		PHASE_A_ KWHAN		PHASE_A_ KWHR1		PHASE_A_ KWHR2		PHASE_A_ KWHR3		PHASE_A_ KWHR4		PHASE_A_ KWHAP		PHASE_A_ KWHIH	
Fxh	PHASE_A_ I_GAIN		PHASE_A_ V_GAIN		PHASE_A_ E_GAIN_HI		PHASE_A_ EOFF_HI		PHASE_A_ E_GAIN_LO		PHASE_A_ EOFF_LO		PHASE_A_ PA_0		PHASE_A_ PA_1	
10xh	PHASE_A_ PA_2		PHASE_A_ PA_3		PHASE_A_ FLAGS		PHASE_A_ EOVFL		PHASE_A_ IPK		PHASE_A_ VPK					
11xh																
12xh																
13xh																
14xh																
15xh																
16xh																
17xh																
18xh																
19xh			PHASE_A_IRMS				PHASE_A_VRMS				PHASE_A_IH				PHASE_A_ ACT	
1Axh	PHASE_A_ ACT		PHASE_A_REA				PHASE_A_APP									
1Bxh																
1Cxh																
1Dxh	PHASE_B_ KWHAP		PHASE_B_ KWHAN		PHASE_B_ KWHR1		PHASE_B_ KWHR2		PHASE_B_ KWHR3		PHASE_B_ KWHR4		PHASE_B_ KWHAP		PHASE_B_ KWHIH	
1Exh	PHASE_B_ I_GAIN		PHASE_B_ V_GAIN		PHASE_B_ E_GAIN_HI		PHASE_B_ EOFF_HI		PHASE_B_ E_GAIN_LO		PHASE_B_ EOFF_LO		PHASE_B_ PA_0		PHASE_B_ PA_1	
1Fxh	PHASE_B_ PA_2		PHASE_B_ PA_3		PHASE_B_ FLAGS		PHASE_B_ EOVFL		PHASE_B_ IPK		PHASE_B_ VPK					
20xh																

Table 3. RAM Register Map (continued)

	x0h	x1h	x2h	x3h	x4h	x5h	x6h	x7h	x8h	x9h	xAh	xBh	xCh	xDh	xEh	xFh
21xh																
22xh																
23xh																
24xh																
25xh																
26xh																
27xh																
28xh			PHASE_B_IRMS				PHASE_B_VRMS				PHASE_B_IH				PHASE_B_ACT	
29xh	PHASE_B_ACT		PHASE_B_REA				PHASE_B_APP									
2Axh																
2Bxh																
2Cxh	PHASE_C_KWHAP		PHASE_C_KWHAN		PHASE_C_KWHR1		PHASE_C_KWHR2		PHASE_C_KWHR3		PHASE_C_KWHR4		PHASE_C_KWHAP		PHASE_C_KWHIH	
2Dxh	PHASE_C_I_GAIN		PHASE_C_V_GAIN		PHASE_C_E_GAIN_HI		PHASE_C_EOFF_HI		PHASE_C_E_GAIN_LO		PHASE_C_EOFF_LO		PHASE_C_PA_0		PHASE_C_PA_1	
2Exh	PHASE_C_PA_2		PHASE_C_PA_3		PHASE_C_FLAGS		PHASE_C_EOVFL		PHASE_C_IPK		PHASE_C_VPK					
2Fxh																
30xh																
31xh																
32xh																
33xh																
34xh																
35xh																
36xh																
37xh			PHASE_C_IRMS				PHASE_C_VRMS				PHASE_C_IH				PHASE_C_ACT	
38xh	PHASE_C_ACT		PHASE_C_REA				PHASE_C_APP									
39xh																
3Axh																
3Bxh	NEUTRAL_KWHIH			NEUTRAL_I_GAIN			NEUTRAL_EOVFL									
3Cxh																
3Dxh																
3Exh					NEUTRAL_IRMS				NEUTRAL_IH							
3Fxh																

Table 4. RAM Register Summary

NAME	ADDRESS (BYTE)	DESCRIPTION	R/W	DEFAULT VALUE (HEX)	BITS	NAME	DESCRIPTION
STATUS0	0 0x000	Status	R/W	0x0000	15:7, 0	—	Reserved. Should be set to 0.
					6	EXTCLK	External clock
					5	ACCEN	Enable energy accumulation
					4	RST	Software reset
					3	CRCEN	Enable CRC
					2	LOWPM	LPMM Mode
					1	STOPM	Stop Mode
OPMODE	2 0x002	Mode of Operation	R/W	0x0000	15:10, 7:6, 2:0	—	Reserved. Should be set to 0.
					9	TMPC1	Temperature (double)
					8	TMPC0	Temperature (single)
					5:4	HRM	00: no filter 01: bandpass filter 1x: bandstop filter
					3	APPSEL	Select apparent energy: 0: sqrt(P^2 + Q^2) 1: I_{RMS} x V_{RMS} Select harmonics filter
STATUS1	4 0x004	Status. Device drives $\overline{IRQ}$ low when any bit in this register is set and not masked.	R/W	0x0001	15	SEQERR	Phase sequence error
					14	VUNBF	Voltage unbalance flag
					13	IUNBF	Current unbalance flag
					12	MISV	Missed voltage detected
					11	NOZC	No zero crossings
					10	SAG	Voltage sag detected
					9	OV	Overvoltage detected
					8	OC	Overcurrent detected
					7:6	—	Reserved
					5	DCH_Q	Pulse 2 direction change
					4	DCH_P	Pulse 1 direction change
					3	EOVF	Energy overflow
					2	TMRD	Temperature reading ready
					1	PWRF	Supply power-fail interrupt
					0	NOINIT	Not initialized
INT_MASK	6 0x006	Interrupt Mask (Enable)	R/W	0x0001	Same as STATUS1		Enable corresponding $\overline{IRQ}$ when set to 1

Table 4. RAM Register Summary (continued)

NAME	ADDRESS (BYTE)	DESCRIPTION	R/W	DEFAULT VALUE (HEX)	BITS	NAME	DESCRIPTION
STATUS2	8 0x008	Status	R/W	0x0000	15:8, 6, 3, 1:0	—	Reserved. Should be set to 0.
					7	PORF	POR flag
					5	REV_Q	Reverse pulse 2
					4	REV_P	Reverse pulse 1
					2	WTRF	Watchdog timer flag
CONNCT	10 0x00A	Connection and Power Calculation Configuration	R/W	0x0000	15:8	—	These bits are reserved and should be set to 0
					7	INTGN	Enable IN integrator (di/dt)
					6	INTGC	Enable IC integrator (di/dt)
					5	INTGB	Enable IB integrator (di/dt)
					4	INTGA	Enable IA integrator (di/dt)
					3	—	Reserved
					2	INEN	Enable neutral current
					1:0	CONNCT [1:0]	00: P1 = VA x IA P2 = VB x IB P3 = VC x IC 01: P1 = VA x IA P2 = -IB x (VA + VC) P3 = VC x IC 1x: P1 = VA x IA P2 = -IB x VA P3 = VC x IC
RESERVED	12–15	—	—	—	—	—	—
SCAN_0	16	Analog Scan Configuration (Slot 0)	R/W	0x0301	15:12	—	These bits are reserved and should be set to 0
					11:8	MUX	Analog mux setting: 0000: V0P–VN 0001: V1P–VN 0010: V2P–VN 0011: I0P–I0N 0100: I1P–I1N 0101: I2P–I2N 0110: INP–VN Other: Reserved
					7	NOCONV	Disable ADC conversion for this slot if set
					6:4	PGA	PGA setting: 000: x1 001: x2 010: x4 011: x8 100: x16 101: x32

Table 4. RAM Register Summary (continued)

NAME	ADDRESS (BYTE)	DESCRIPTION	R/W	DEFAULT VALUE (HEX)	BITS	NAME	DESCRIPTION
SCAN_0	16	Analog Scan Configuration (Slot 0)	R/W	0x0301	3:1	EXCON	External connection: 000: IA 001: VA 010: IC 011: VC 100: IB 101: VB 110: IN
					0	—	Reserved
SCAN_1	18 0x012	Analog Scan Configuration (Slot 1)	R/W	0x0003	Same as SCAN_0		
SCAN_2	20 0x014	Analog Scan Configuration (Slot 2)	R/W	0x0505	Same as SCAN_0		
SCAN_3	22 0x016	Analog Scan Configuration (Slot 3)	R/W	0x0207	Same as SCAN_0		
SCAN_4	24 0x018	Analog Scan Configuration (Slot 4)	R/W	0x0409	Same as SCAN_0		
SCAN_5	26 0x01A	Analog Scan Configuration (Slot 5)	R/W	0x010B	Same as SCAN_0		
SCAN_6	28 0x01C	Analog Scan Configuration (Slot 6)	R/W	0x068D	Same as SCAN_0		
SCAN_7	30 0x01E	Analog Scan Configuration (Slot 7)	R/W	0x08AF	Reserved. Do not modify these bits.		
TIME_FS	32 0x020	Timing Calibration	R/W	0x07D0	15:0		Real-time duration of one scan frame (R_ADCRATE + 1 system clocks) in 0.1µs units
VOLT_FS	34 0x022	Voltage Calibration	R/W	0x81F0	15:0		Voltage conversion coefficient: reported voltage = VOLT_FS x $V_{RMS}/2^{16}$
AMP_FS	36 0x024	Current Calibration	R/W	0x17D8	15:0		Current conversion coefficient: reported current = AMP_FS x $I_{RMS}/2^{16}$

Table 4. RAM Register Summary (continued)

NAME	ADDRESS (BYTE)	DESCRIPTION	R/W	DEFAULT VALUE (HEX)	BITS	NAME	DESCRIPTION
PWR_FS	38 0x026	Power Calibration	R/W	0x3539	15:0		Power conversion coefficient: reported power = PWR_FS x I_{RMS} x $V_{RMS}/2^{26}$
KWHT	40 0x028	kWh Threshold	R/W	0x0084 1C2F	31:0		Defines the LSB of energy accumulators (default 0.0001kWh)
KAHT	44 0x02C	kAh Threshold	R/W	0x1194 0000	31:0		Defines the LSB of Ah accumulators (default 0.0001kAh)
CYCNT	48 0x030	Cycle Count	R/W	0x0001	15:0		Defines how many line cycles to accumulate before calculating energy
PLSCFG	50 0x032	Pulse Output Configuration	R/W	0x1707	15:11	PLS2SEL	Selects the value for pulse 2 output
					10:8	PLS2TRM	Independently selects E1, E2, and E3 for pulse 2
					7:3	PLS1SEL	Selects the value for pulse 1 output
					2:0	PLS1TRM	Independently selects E1, E2, and E3 for pulse 1
THR1	52 0x34	Pulse 1 Threshold	R/W	0x019C D813	31:0		Pulse 1 duration timer (1 LSB = 64SCLK)
THR2	56 0x38	Pulse 2 Threshold	R/W	0x019C D813	31:0		Pulse 2 duration timer (1 LSB = 64SCLK)
PLS1_WD	60 0x3C	Pulse 1 Width	R/W	0x186A	15:0		Downcounter load for pulse 1 duration (default 50ms)
PLS2_WD	62 0x3E	Pulse 2 Width	R/W	0x186A	15:0		Downcounter load for pulse 2 duration (default 50ms)
RESERVED	64–83	System	—	—	—	—	—
AVC0	84 0x054	Allpass Filter Coefficient	R/W	0x3000	15:0		—
AVC1	86 0x056	Allpass Filter Coefficient	R/W	0x5000	15:0		—
LPF_B0FZC	88 0x058	LPF Coefficient for Zero Crossing	R/W	0x1000	15:0		—

Table 4. RAM Register Summary (continued)

NAME	ADDRESS (BYTE)	DESCRIPTION	R/W	DEFAULT VALUE (HEX)	BITS	NAME	DESCRIPTION
LPF_B0FNS	90 0x05A	LPF Coefficient for NS Calculation	R/W	0x0800	15:0		—
LPF_B0FSM	92 0x05C	LPF Coefficient for Samples Calculation	R/W	0x1000	15:0		—
HPF_B0F	94 0x05E	HPF Coefficient	R/W	0x0200	15:0		—
BPF_B0F	96 0x060	BPF and BSF Coefficient	R/W	0x1000	15:0		—
BPF_A1F	98 0x062	BPF and BSF Coefficient	R/W	0x301A	15:0		—
RESERVED	100–107	System	—	—	—	—	—
PKCYC	108 0x06C	Number of Line Cycles for Peak Detection	R/W	0x0032	15:0		—
SAGCYC	110 0x06E	Number of Line Cycles for Sag Detection	R/W	0x0005	15:0		—
OCLVL	112 0x070	Overcurrent Interrupt Threshold	R/W	0x7FFF	15:0		—
OVLVL	114 0x072	Overvoltage Interrupt Threshold	R/W	0x7FFF	15:0		—
SAGLVL	116 0x074	Voltage Sag Interrupt Threshold	R/W	0x0000	15:0		—
IUBLVL	118 0x076	Current Unbalance Interrupt Threshold	R/W	0xFFFF	15:0		—
VUBLVL	120 0x078	Voltage Unbalance Interrupt Threshold	R/W	0xFFFF	15:0		—
NZC_TIMO	122 0x07A	Zero-Crossing Timeout	R/W	0x0640	15:0		Number of frames to detect no-zero crossing

Table 4. RAM Register Summary (continued)

NAME	ADDRESS (BYTE)	DESCRIPTION	R/W	DEFAULT VALUE (HEX)	BITS	NAME	DESCRIPTION
REV_TIMO	124 0x07C	Reverse Pulse Direction Timeout	R/W	0x000B	15:0		Number of line cycles to detect reverse pulse direction
ACC_TIMO	126 0x07E	Energy Accumulation Delay Timeout	R/W	0x0032	15:0		Number of line cycles before starting energy accumulation
COM_TIMO	128 0x080	Communication Timeout	R/W	0x03E8	15:0		Number of frames to reset communication channel
R_ACFG	130 0x082	Analog Control Shadow	R/W	0x0007	15:8	—	These bits are reserved and should be set to 0
					7	ADCASD	Automatic shutdown disable
					6	ADCRY	Sample ready (system)
					5:4	ADCCD [1:0]	ADC clock divider 00: ADC = SYSCLK 01: ADC = SYSCLK/2 10: ADC = SYSCLK/4 11: Reserved
					3	ADCBY	ADC busy (system)
					2	ADCIE	ADC interrupt enable (system)
					1	ARBE	Internal V_{REF} enable
					0	ADCE	ADC enable
R_ADCRATE	132 0x084	Analog Control Shadow	R/W	0x00C7	15:9	—	Reserved. Should be set to 0.
					8:0	R_ADCRATE [8:0]	Number of SYSCLKs between two consecutive ADC conversions minus 1
R_ADCACQ	134 0x086	Analog Control Shadow	R/W	0x002F	15:7	—	Reserved. Should be set to 0.
					6:0	R_ADCACQ [6:0]	Number of SYSCLKs for amplifier to acquire input signal before conversion minus 1
R_SPICF	136 0x088	SPI Control Shadow	R/W	0x0080	15:8, 5:3	—	Reserved. Should be set to 0.
					7	ESPII	SPI interrupt enable (system)
					6	SAS	SSEL active level select 0: $\overline{SSEL}$ active low 1: $\overline{SSEL}$ active high
					5:3	—	These bits are reserved and should be set to 0
					2	CHR	SPI character length bit 0: 8 bits 1: 16 bits
					1	CKPHA	SPI clock phase select
					0	CKPOL	SPI clock polarity select

Table 4. RAM Register Summary (continued)

NAME	ADDRESS (BYTE)	DESCRIPTION	R/W	DEFAULT VALUE (HEX)	BITS	NAME	DESCRIPTION
NOLOAD	138 0x08A	No-Load Threshold	R/W	0x00F0	15:0		No-load threshold. Default setting corresponds to 0.5W
NS	140 0x08C	Raw Line-Cycle Period	R/W	0x00640000	31:0		Number of scan frames per line cycle, LSB = $2^{(-16)}$
RAW_TEMP	144 0x090	Temperature Sample	RO	—	15:4	RAW_TEMP [15:4]	Raw ADC output, proportional to absolute die temperature
					3:0	—	Reserved
RESERVED	146–223	—	—	—	—	—	—
PHASE_A_ KWHAP	224 0x0E0	Active Positive Energy	RO	—	15:0		Accumulated active energy in positive direction. Units defined by KWHT setting.
PHASE_A_ KWHAN	226 0x0E2	Active Negative Energy	RO	—	15:0		Accumulated active energy in negative direction. Units defined by KWHT setting.
PHASE_A_ KWHR1	228 0x0E4	Reactive Q1 Energy	RO	—	15:0		Accumulated reactive energy in quadrant 1. Units defined by KWHT setting.
PHASE_A_ KWHR2	230 0x0E6	Reactive Q2 Energy	RO	—	15:0		Accumulated reactive energy in quadrant 2. Units defined by KWHT setting.
PHASE_A_ KWHR3	232 0x0E8	Reactive Q3 Energy	RO	—	15:0		Accumulated reactive energy in quadrant 3. Units defined by KWHT setting.
PHASE_A_ KWHR4	234 0x0EA	Reactive Q4 Energy	RO	—	15:0		Accumulated reactive energy in quadrant 4. Units defined by KWHT setting.
PHASE_A_ KWHAP	236 0x0EC	Apparent Energy	RO	—	15:0		Accumulated apparent energy. Units defined by KWHT setting.
PHASE_A_ KWHIH	238 0x0EE	Amp-Hours	RO	—	15:0		Accumulated amp-hours. Units defined by KAHT setting.
PHASE_A_I _GAIN	240 0x0F0	Current Gain Coefficient	R/W	0x0000	15:0		Signed two's complement; used to correct I_{RMS}: $Y = X \times (1 + gain/2^{16})$
PHASE_A_V _GAIN	242 0x0F2	Voltage Gain Coefficient	R/W	0x0000	15:0		Signed two's complement; used to correct V_{RMS}: $Y = X \times (1 + gain/2^{16})$
PHASE_A_E _GAIN_HI	244 0x0F4	Power and Energy Gain Coefficient	R/W	0x0000	15:0		Signed two's complement; used to correct pwr: $Y = X \times (1 + gain/2^{16})$

Table 4. RAM Register Summary (continued)

NAME	ADDRESS (BYTE)	DESCRIPTION	R/W	DEFAULT VALUE (HEX)	BITS	NAME	DESCRIPTION
PHASE_A_EOFF_HI	246 0x0F6	Linearity Coefficient: High Range Energy Offset	R/W	0x0000	15:0		Signed two's complement; used to correct energy: Y = X - Eoff_hi
PHASE_A_E_GAIN_LO	248 0x0F8	Linearity Coefficient: Low Range Energy Gain	R/W	0x0000	15:0		Signed two's complement; Used to correct pwr: $Y = X \times (1 + gain/2^{16})$
PHASE_A_EOFF_LO	250 0x0FA	Linearity Coefficient: Low range Energy Offset	R/W	0x0000	15:0		Signed two's complement; Used to correct pwr: Y = X - Eoff_lo
PHASE_A_PA_0	252 0x0FC	Phase Angle Coefficient	R/W	0x0000	15:0		Signed two's complement; $Y = PA\_0 + (PA\_1 \times X) + (PA\_2 \times X^2) + (PA\_3 \times X^3)$
PHASE_A_PA_1	254 0x0FE	Phase Angle Coefficient	R/W	0x0000	15:0		
PHASE_A_PA_2	256 0x100	Phase Angle Coefficient	R/W	0x0000	15:0		
PHASE_A_PA_3	258 0x102	Phase Angle Coefficient	R/W	0x0000	15:0		
PHASE_A_FLAGS	260 0x104	Interrupt Flags	R/W	0x0000	15:13, 7:5	—	Reserved. Should be set to 0.
					12:8	4:0	Mask (enable) bits for flags 4:0, correspondingly
					4	MISVF	Missing voltage flag
					3	NOZCF	No zero-crossing flag
					2	VSAGF	Voltage sag flag
					1	OVF	Overvoltage flag
					0	OCF	Overcurrent flag
PHASE_A_EOVFL	262 0x106	Energy Overflow Flags	R/W	0x0000	7	IHOF	KWHIH overflow
					6	APOF	KWHAP overflow
					5	R4OF	KWHR4 overflow
					4	R3OF	KWHR3 overflow
					3	R2OF	KWHR2 overflow
					2	R1OF	KWHR1 overflow
					1	ANOF	KWHAN overflow
					0	APOF	KWHAP overflow

Table 4. RAM Register Summary (continued)

NAME	ADDRESS (BYTE)	DESCRIPTION	R/W	DEFAULT VALUE (HEX)	BITS	NAME	DESCRIPTION
PHASE_A_IPK	264 0x108	Current Peak	RO	—	15:0		—
PHASE_A_VPK	266 0x10A	Voltage Peak	RO	—	15:0		—
RESERVED	268–401	—	—	—	—	—	—
PHASE_A_IRMS	402 0x192	Raw RMS Current	RO	—	31:0		Per most recent line cycle. Full-scale = 2^{30}
PHASE_A_VRMS	406 0x196	Raw RMS Voltage	RO	—	31:0		Per most recent line cycle. Full-scale = 2^{30}
PHASE_A_IH	410 0x19A	Raw Amp-Hours	RO	—	31:0		Per most recent line cycle. Full-scale = 2^{14} x NS
PHASE_A_ACT	414 0x19E	Raw Active Energy	RO	—	31:0		Per most recent line cycle. Full-scale = 2^{18} x NS
PHASE_A_REA	418 0x1A2	Raw Reactive Energy	RO	—	31:0		Per most recent line cycle. Full-scale = 2^{18} x NS
PHASE_A_APP	422 0x1A6	Raw Apparent Energy	RO	—	31:0		Per most recent line cycle. Full-scale = 2^{18} x NS
RESERVED	426–463	—	—	—	—	—	—
PHASE_B_KWHAP	464 0x1D0	Active Positive Energy	RO	—	15:0		Accumulated active energy in positive direction. Units defined by KWHT setting.
PHASE_B_KWHAN	466 0x1D2	Active Negative Energy	RO	—	15:0		Accumulated active energy in negative direction. Units defined by KWHT setting.
PHASE_B_KWHR1	468 0x1D4	Reactive Q1 Energy	RO	—	15:0		Accumulated reactive energy in quadrant 1. Units defined by KWHT setting.
PHASE_B_KWHR2	470 0x1D6	Reactive Q2 Energy	RO	—	15:0		Accumulated reactive energy in quadrant 2. Units defined by KWHT setting.
PHASE_B_KWHR3	472 0x1D8	Reactive Q3 Energy	RO	—	15:0		Accumulated reactive energy in quadrant 3. Units defined by KWHT setting.
PHASE_B_KWHR4	474 0x1DA	Reactive Q4 Energy	RO	—	15:0		Accumulated reactive energy in quadrant 4. Units defined by KWHT setting.
PHASE_B_KWHAP	476 0x1DC	Apparent Energy	RO	—	15:0		Accumulated apparent energy. Units defined by KWHT setting.

Table 4. RAM Register Summary (continued)

NAME	ADDRESS (BYTE)	DESCRIPTION	R/W	DEFAULT VALUE (HEX)	BITS	NAME	DESCRIPTION
PHASE_B_ KWHIH	478 0x1DE	Amp-Hours	RO	—	15:0		Accumulated amp-hours. Units defined by KAHT setting.
PHASE_B_ I_GAIN	480 0x1E0	Current Gain Coefficient	R/W	0x0000	15:0		Signed two's complement; Used to correct I_{RMS}: $Y = X \times (1 + gain/2^{16})$
PHASE_B_ V_GAIN	482 0x1E2	Voltage Gain Coefficient	R/W	0x0000	15:0		Signed two's complement; Used to correct V_{RMS}: $Y = X \times (1 + gain/2^{16})$
PHASE_B_ E_GAIN_HI	484 0x1E4	Power and Energy Gain Coef	R/W	0x0000	15:0		Signed two's complement; Used to correct pwr: $Y = X \times (1 + gain/2^{16})$
PHASE_B_ EOFF_HI	486 0x1E6	Linearity Coefficient: High Range Energy Offset	R/W	0x0000	15:0		Signed two's complement; Used to correct energy: Y = X - Eoff_hi
PHASE_B_ E_GAIN_LO	488 0x1E8	Linearity Coefficient: Low Range Energy Gain	R/W	0x0000	15:0		Signed two's complement; Used to correct pwr: $Y = X \times (1 + gain/2^{16})$
PHASE_B_ EOFF_LO	490 0x1EA	Linearity Coefficient: Low Range Energy Offset	R/W	0x0000	15:0		Signed two's complement; Used to correct pwr: Y = X - Eoff_lo
PHASE_B_ PA_0	492	Phase Angle Coefficient	R/W	0x0000	15:0		Signed two's complement; $Y = PA\_0 + (PA\_1 \times X) + (PA\_2 \times X^2) + (PA\_3 \times X^3)$
PHASE_B_ PA_1	494	Phase Angle Coefficient	R/W	0x0000	15:0		
PHASE_B_ PA_2	496	Phase Angle Coefficient	R/W	0x0000	15:0		
PHASE_B_ PA_3	498	Phase Angle Coefficient	R/W	0x0000	15:0		

Table 4. RAM Register Summary (continued)

NAME	ADDRESS (BYTE)	DESCRIPTION	R/W	DEFAULT VALUE (HEX)	BITS	NAME	DESCRIPTION
PHASE_B_ FLAGS	500	Interrupt Flags	R/W	0x0000	15:13, 7:5	—	Reserved
					12:8	4:0	Mask (enable) bits for flags 4:0, correspondingly
					4	MISVF	Missing voltage flag
					3	NOZCF	No zero-crossing flag
					2	VSAGF	Voltage sag flag
					1	OVF	Overvoltage flag
					0	OCF	Overcurrent flag
PHASE_B_ EOVFL	502	Energy Overflow Flags	R/W	0x0000	7	IHOF	KWHIH overflow
					6	APOF	KWHAP overflow
					5	R4OF	KWHR4 overflow
					4	R3OF	KWHR3 overflow
					3	R2OF	KWHR2 overflow
					2	R1OF	KWHR1 overflow
					1	ANOF	KWHAN overflow
					0	APOF	KWHAP overflow
PHASE_B_ IPK	504	Current Peak	RO	—	15:0		—
PHASE_B_ VPK	506	Voltage Peak	RO	—	15:0		—
RESERVED	508–641	—	—	—	—	—	—
PHASE_B_ IRMS	642	Raw RMS Current	RO	—	31:0		Per most recent line cycle. Full-scale = 2^{30}
PHASE_B_ VRMS	646	Raw RMS Voltage	RO	—	31:0		Per most recent line cycle. Full-scale = 2^{30}
PHASE_B_ IH	650	Raw Amp-Hours	RO	—	31:0		Per most recent line cycle. Full-scale = 2^{14} x NS
PHASE_B_ ACT	654	Raw Active Energy	RO	—	31:0		Per most recent line cycle. Full-scale = 2^{18} x NS
PHASE_B_ REA	658	Raw Reactive Energy	RO	—	31:0		Per most recent line cycle. Full-scale = 2^{18} x NS
PHASE_B_ APP	662	Raw Apparent Energy	RO	—	31:0		Per most recent line cycle. Full-scale = 2^{18} x NS
RESERVED	666–703	—	—	—	—	—	—
PHASE_C_ KWHAP	704	Active Positive Energy	RO	—	15:0		Accumulated active energy in positive direction. Units defined by KWHT setting.
PHASE_C_ KWHAN	706	Active Negative Energy	RO	—	15:0		Accumulated active energy in negative direction. Units defined by KWHT setting.

Table 4. RAM Register Summary (continued)

NAME	ADDRESS (BYTE)	DESCRIPTION	R/W	DEFAULT VALUE (HEX)	BITS	NAME	DESCRIPTION
PHASE_C_KWHR1	708	Reactive Q1 Energy	RO	—	15:0		Accumulated reactive energy in quadrant 1. Units defined by KWHT setting.
PHASE_C_KWHR2	710	Reactive Q2 Energy	RO	—	15:0		Accumulated reactive energy in quadrant 2. Units defined by KWHT setting.
PHASE_C_KWHR3	712	Reactive Q3 Energy	RO	—	15:0		Accumulated reactive energy in quadrant 3. Units defined by KWHT setting.
PHASE_C_KWHR4	714	Reactive Q4 Energy	RO	—	15:0		Accumulated reactive energy in quadrant 4. Units defined by KWHT setting.
PHASE_C_KWHAP	716	Apparent Energy	RO	—	15:0		Accumulated apparent energy. Units defined by KWHT setting.
PHASE_C_KWHIH	718	Amp-Hours	RO	—	15:0		Accumulated amp-hours. Units defined by KAHT setting.
PHASE_C_I_GAIN	720	Current Gain Coefficient	R/W	0x0000	15:0		Signed two's complement; Used to correct I_{RMS}: $Y = X \times (1 + gain/2^{16})$
PHASE_C_V_GAIN	722	Voltage Gain Coefficient	R/W	0x0000	15:0		Signed two's complement; Used to correct V_{RMS}: $Y = X \times (1 + gain/2^{16})$
PHASE_C_E_GAIN_HI	724	Power and Energy Gain Coefficient	R/W	0x0000	15:0		Signed two's complement; Used to correct pwr: $Y = X \times (1 + gain/2^{16})$
PHASE_C_EOFF_HI	726	Linearity Coefficient: High Range Energy Offset	R/W	0x0000	15:0		Signed two's complement; Used to correct energy: Y = X - Eoff_hi
PHASE_C_E_GAIN_LO	728	Linearity Coefficient: Low Range Energy Gain	R/W	0x0000	15:0		Signed two's complement; Used to correct pwr: $Y = X \times (1 + gain/2^{16})$
PHASE_C_EOFF_LO	730	Linearity Coefficient: Low Range Energy Offset	R/W	0x0000	15:0		Signed two's complement; Used to correct pwr: Y = X - Eoff_lo

Table 4. RAM Register Summary (continued)

NAME	ADDRESS (BYTE)	DESCRIPTION	R/W	DEFAULT VALUE (HEX)	BITS	NAME	DESCRIPTION
PHASE_C_PA_0	732	Phase Angle Coefficient	R/W	0x0000	15:0		Signed two's complement; $Y = PA\_0 + (PA\_1 \times X) + (PA\_2 \times X^2) + (PA\_3 \times X^3)$
PHASE_C_PA_1	734	Phase Angle Coefficient	R/W	0x0000	15:0		
PHASE_C_PA_2	736	Phase Angle Coefficient	R/W	0x0000	15:0		
PHASE_C_PA_3	738	Phase Angle Coefficient	R/W	0x0000	15:0		
PHASE_C_FLAGS	740	Interrupt Flags	R/W	0x0000	15:13, 7:5	—	Reserved
					12:8		Mask (enable) bits for flags 4:0, correspondingly
					4	MISVF	Missing voltage flag
					3	NOZCF	No zero-crossing flag
					2	VSAGF	Voltage sag flag
					1	OVF	Overvoltage flag
					0	OCF	Overcurrent flag
PHASE_C_EOVFL	742	Energy Overflow Flags	R/W	0x0000	7	IHOF	KWHIH overflow
					6	APOF	KWHAP overflow
					5	R4OF	KWHR4 overflow
					4	R3OF	KWHR3 overflow
					3	R2OF	KWHR2 overflow
					2	R1OF	KWHR1 overflow
					1	ANOF	KWHAN overflow
					0	APOF	KWHAP overflow
PHASE_C_IPK	744	Current Peak	RO	—	15:0		—
PHASE_C_VPK	746	Voltage Peak	RO	—	15:0		—
RESERVED	748–881	—	—	—	—	—	—
PHASE_C_IRMS	882	Raw RMS Current	RO	—	31:0		Per most recent line cycle. Full-scale = 2^{30}
PHASE_C_VRMS	886	Raw RMS Voltage	RO	—	31:0		Per most recent line cycle. Full-scale = 2^{30}
PHASE_C_IH	890	Raw Amp-Hours	RO	—	31:0		Per most recent line cycle. Full-scale = $2^{14} \times NS$

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Table 4. RAM Register Summary (continued)

NAME	ADDRESS (BYTE)	DESCRIPTION	R/W	DEFAULT VALUE (HEX)	BITS	NAME	DESCRIPTION
PHASE_C_ACT	894	Raw Active Energy	RO	—	31:0		Per most recent line cycle. Full-scale = 2^{18} x NS
PHASE_C_REA	898	Raw Reactive Energy	RO	—	31:0		Per most recent line cycle. Full-scale = 2^{18} x NS
PHASE_C_APP	902	Raw Apparent Energy	RO	—	31:0		Per most recent line cycle. Full-scale = 2^{18} x NS
RESERVED	906–943	—	—	—	—	—	—
NEUTRAL_KWHIH	944	Amp-Hours	RO	—	15:0		Accumulated amp-hours. Units defined by KAHT setting.
NEUTRAL_I_GAIN	946	Current Gain Coefficient	R/W	0x0000	15:0		Signed two's complement; Used to correct I_{RMS}: $Y = X \times (1 + gain/2^{16})$
NEUTRAL_EOVFL	948	Energy Overflow Flags	R/W	0x0000	0	IHOF	KWHIH overflow
RESERVED	950–995	—	—	—	—	—	—
NEUTRAL_IRMS	996	Raw RMS Current	RO	—	31:0		Per most recent line-cycle. Full-scale = 2^{30}
NEUTRAL_IH	1000	Raw Amp-Hours	RO	—	31:0		Per most recent line cycle. Full-scale = 2^{14} x NS
RESERVED	1004–1023	—	—	—	—	—	—

Virtual Registers

Some register values are not stored in RAM, but instead are calculated at the master's request when needed. These registers, which include power (kW), voltage (V), and current (A) values, can be read by the master through the virtual registers listed in Table 5. The addresses of all virtual registers have the most significant bit (bit 11) set to 1. All virtual registers are read only.

Table 5. Virtual Registers

NAME	ADDRESS	DESCRIPTION	DATA LENGTH (BYTES)
PWRP.A	0x801	Phase A Active Power. Units defined by PWR_FS setting.	4
PWRP.B	0x802	Phase B Active Power. Units defined by PWR_FS setting.	4
PWRP.C	0x804	Phase C Active Power. Units defined by PWR_FS setting.	4
PWRP.T	0x807	Total A + B + C Active Power. Units defined by PWR_FS setting.	4
PWRQ.A	0x811	Phase A Reactive Power. Units defined by PWR_FS setting.	4
PWRQ.B	0x812	Phase B Reactive Power. Units defined by PWR_FS setting.	4
PWRQ.C	0x814	Phase C Reactive Power. Units defined by PWR_FS setting.	4
PWRQ.T	0x817	Total A + B + C Reactive Power. Units defined by PWR_FS setting.	4
PWRS.A	0x821	Phase A Apparent Power. Units defined by PWR_FS setting.	4
PWRS.B	0x822	Phase B Apparent Power. Units defined by PWR_FS setting.	4

Table 5. Virtual Registers (continued)

NAME	ADDRESS	DESCRIPTION	DATA LENGTH (BYTES)
PWRS.C	0x824	Phase C Apparent Power. Units defined by PWR_FS setting.	4
PWRS.T	0x827	Total A + B + C Apparent Power. Units defined by PWR_FS setting.	4
V.A	0x831	Phase A RMS-Voltage. Units defined by VOLT_FS setting.	4
V.B	0x832	Phase B RMS-Voltage. Units defined by VOLT_FS setting.	4
V.C	0x834	Phase C RMS-Voltage. Units defined by VOLT_FS setting.	4
I.A	0x841	Phase A RMS-Current. Units defined by AMP_FS setting.	4
I.B	0x842	Phase B RMS-Current. Units defined by AMP_FS setting.	4
I.C	0x844	Phase C RMS-Current. Units defined by AMP_FS setting.	4
LINEFREQ	0x851	Line Frequency; LSB = 0.001Hz.	4
VBPH	0x852	Voltage B Phase Delay to Voltage A; LSB = 0.01°.	4
VCPH	0x854	Voltage C Phase Delay to Voltage A; LSB = 0.01°.	4
PF.A	0x861	Phase A Power Factor; Two's Complement, LSB = 0.00001.	4
PF.B	0x862	Phase B Power Factor; Two's Complement, LSB = 0.00001.	4
PF.C	0x864	Phase C Power Factor; Two's Complement, LSB = 0.00001.	4
PF.T	0x867	Total A + B + C Power Factor; Two's Complement, LSB = 0.00001.	4

Table 6. Virtual Register with Special Commands

NAME	ADDRESS	DESCRIPTION	DATA LENGTH (BYTES)
UPD_SFR	0x900	Copy mirror registers (R_ADCF, R_ADCRATE, R_ADCACQ, R_SPICF) into hardware SFR registers. Read dummy data.	1
UPD_MIR	0xA00	Copy hardware SFR registers into mirror registers (R_ADCF, R_ADCRATE, R_ADCACQ, R_SPICF). Read dummy data.	1

Special Commands

Some virtual registers trigger special commands when read by the master (Table 6). Writing these registers has no effect. All reads from these registers return dummy data.

Analog Front-End Processing

Whenever the MAXQ3180 is in one of the active operating modes (Run Mode or LPMM Mode), the analog front-end operates continuously, scanning through up to eight scan slots depending on the selected front-end configuration. For each analog scan slot that is enabled, one of the eight differential input pairs is measured.

The SCAN_0 to SCAN_7 registers contain the settings for each slot, which include whether the slot is enabled, the differential input pair to measure during that scan slot, and the logical mapping of that slot. One typical configuration might be:

- Slot 0—Phase A Current (IA)
- Slot 1—Phase A Voltage (VA)
- Slot 2—Phase C Current (IC)
- Slot 3—Phase C Voltage (VC)
- Slot 4—Phase B Current (IB)
- Slot 5—Phase B Voltage (VB)
- Slot 6—Neutral Current (IN)—disabled by default
- Slot 7—Temperature Measurement—normally disabled, activated when TMPC0 or TMPC1 is set

Table 7. Analog Scan Slot Time Selection

ADCCD1	ADCCD0	ADC CLOCK DIVISION RATE	ANALOG SCAN SLOT TIME (t_C)
0	0	Divide by 1 (default)	$1/f_{CLK}$ x (R_ADCRATE[8:0] + 1)
0	1	Divide by 2	$2/f_{CLK}$ x (R_ADCRATE[8:0] + 1)
1	0	Divide by 4	$4/f_{CLK}$ x (R_ADCRATE[8:0] + 1)

Note that analog scan slot 7 is reserved for temperature measurements. There is no need to explicitly enable this measurement slot, since it is automatically activated when either the TMPC0 (single temperature measurement command) or TMPC1 (double temperature measurement command) bits are set by the master.

The required time for a each analog scan slot measurement (t_C) is determined by the MAXQ3180 system clock frequency, the setting of the ADC clock division bits (ADCCD0 and ADCCD1) in the R_ACFG hardware register, and the setting of the R_ADCRATE hardware register, as shown in Table 7.

Using the default register settings (ADCCD[1:0] = 00b and ADCRATE = C7h = 199d), the time for each analog slot measurement (t_C) is 25µs when the MAXQ3180 is running at 8MHz. Since there are eight analog scan slots in the measurement frame, the total time for all measurements (t_F) is t_C x 8. Using the default settings with the MAXQ3180 running at 8MHz, the entire sequence of measurements takes 200µs to complete, which, in turn, means that 200µs will elapse, for example, between one phase A current measurement and the next.

Even if some of the analog measurement slots (such as neutral current or temperature measurement) are skipped by setting the NOCONV bit in that slot's SCAN_x register to 1, the time period for that slot will remain in the frame, ensuring that the total frame time is always t_C x 8, regardless of which individual slots are enabled or disabled.

Digital Processing

As voltage and current samples are collected, the MAXQ3180 performs a variety of digital filtering, accumulation, and processing calculations to arrive at meter-reading values (such as line frequency, RMS voltage and current, and active and reactive power) that can then be read by the master. The MAXQ3810 calculates and detects values and conditions including the following:

- Zero-crossing detection
- Line frequency and line period calculation
- RMS voltage (phase A, phase B, phase C)
- RMS current (phase A, phase B, phase C, neutral current)
- Power (active, reactive, and apparent) for each phase
- Energy accumulation (including energy pulse output function)
- Peak voltage (phase A, phase B, phase C)
- Peak current (phase A, phase B, phase C)
- Voltage sag condition
- Tamper condition detection

Voltage Zero-Crossing Detection

The MAXQ3180 monitors each of the three voltage input signals (from phase A, phase B, and phase C) and detects zero-crossing events on each of them individually. The sequence of the detected zero crossings and the intervals between them are then used to calculate additional data.

Before zero-crossing detection is performed, each of the three voltage inputs (VA, VB, and VC) are passed through a first-order lowpass filter (LPF) with a cutoff frequency near 50Hz to reduce harmonics, which can trigger false zero-crossing events. The master can configure this LPF by setting the register LPF_B0FZC. The equation for the zero-crossing LPF (for all three voltage phase inputs) is as follows:

$$Y_n = Y_p + (X_n - Y_p) \times LPF\_B0FZC/2^{16}$$

Although the filtered waveform output is not a perfect sine wave, the LPF ensures that the output has no more than one ascending zero crossing per line period. Following the LPF filter processing stage, the MAXQ3180 scans the voltage signals to detect ascending zero-crossing events for each voltage phase.

Line Frequency and Period Measurement

For each phase A, B, and C, the MAXQ3180 counts the number of scan frames (NS) between two consecutive zero crossings. The NS is a global value, common for all three phases, and is located in RAM at address 0x08C. Each individual phase A, B, or C zero-crossing event contributes raw NS count, which plugs as input to the LPF.

$$Y_n = Y_{n-1} + (lpf\_b0fns/65,536) \times (X_n - Y_{n-1})$$

Filter coefficient (lpf_b0fns) is a signed 16-bit value and can be configured by the master. In the previous equation, Y denotes the global NS value, and X denotes individual NS measurements produced by zero-crossing events detected on phase A, B, or C voltage channel. Note that if all three phase voltages are present, the filter above receives three inputs each line cycle. The global NS value is used to generate line-cycle trigger for DSP processing. Note that value NS can be configured by the master, which may be necessary if all three voltage signals are lost and no zero crossings are detected. The line period is then calculated as a product of NS and the scan slot period t_C (stored in the timing calibration register TIME_FS). The reciprocal of this value is the line frequency, which can be obtained as a fixed-point value with 1 LSB = 0.001Hz by reading the virtual register LINEFREQ.

No-Zero-Crossing Detection

The MAXQ3180 monitors the voltage signal on each phase for zero-crossing events. If no ascending zero crossings are detected within a specified number of analog scan frame periods, the NOZC (STATUS1.11) flag is set by the MAXQ3180 to notify the master of this condition. If the interrupt enable bit INT_MASK.11 is set to 1, the interrupt signal $\overline{IRQ}$ is driven low by the MAXQ3180 whenever NOZC = 1. The master can clear NOZC back to 0 to remove the interrupt condition.

Phase Sequence Errors

A phase sequence error occurs when zero-crossing events occur on all three phases, but they do not occur in the expected order. Normally, a zero-crossing event should occur on the phase A voltage signal, followed by phase B, phase C, and then phase A again. If a zero crossing on phase A is then followed immediately by a zero crossing on phase C (and not by phase B as expected), this is registered by the MAXQ3180 as a phase sequence error.

When a phase sequence error occurs, the MAXQ3180 sets the phase sequence error flag SEQERR (STATUS1.15) to 1. If the corresponding interrupt enable bit (INT_MASK.15) is also set to 1, the interrupt signal $\overline{IRQ}$ is driven low by the MAXQ3180 whenever SEQERR = 1. The master can clear SEQERR back to 0 to remove the interrupt condition.

RMS Voltage, RMS Current, and Energy Calculation

For each of the three phases, the MAXQ3180 calculates RMS voltage and RMS current values, as well as determines active and reactive energy, using a line-cycle-based integration process.

Power Calculation (Active, Reactive, Apparent)

The power, energy, and RMS calculation process consists of two tasks: continuous accumulation and post-processing triggered every CYCNT line cycles. The accumulation task accumulates raw data obtained from the AFE during CYCNT line cycles. This task is performed continuously in the background by the MAXQ3180. When a CYCNT line cycles accumulation stage has completed, which is determined by a dedicated frame counter exceeding the CYCNT x NS level, the raw integral accumulator values are saved for post-processing and cleared, beginning the next cycle of accumulation task. Then, the DSP postprocessing is triggered to process saved integrals and calculate energy, power, etc., values. Note that the background accumulation task continues while foreground postprocessing is taking place, i.e., both tasks are executed simultaneously sharing CPU time. It is essential that the DSP postprocessing calculations be completed before the next DSP trigger to avoid losing accumulated data. The master should allow enough processing time by adjusting the R_ADCRATE register. Default settings provide plenty of CPU time for both tasks.

The MAXQ3180 accumulates raw sums and calculates line-cycle integrals for each voltage-current pair separately. The individual power accumulators are:

- P1 = (VA x IA)
- P2 = (VB x IB) or -IB x (VA + VC) or -IB x VA
- P3 = (VC x IC)

The P1 and P3 accumulators always operate in a single mode: (VA x IA) for the P1 accumulator, (VC x IC) for the P3 accumulator. Alternately, the operating mode of the P2 accumulator is defined by setting bits 0 and 1 in the CONNCT register as shown in Table 8.

Table 8. P2 Power Accumulator Modes

CONNCT[1:0]	P2 OPERATING MODE	WIRING CONFIGURATIONS
00b	(VB x IB)	5S/13S 3-Wire Delta, 9S/16S 4-Wire Wye
01b	-IB x (VA + VC)	6S/14S 4-Wire Wye
10b, 11b	-IB x VA	8S/15S 4-Wire Delta

If the CONNCT bits are set to 01b, then the P2 (phase B) input voltage sample is calculated using an allpass filter described as:

$$(VA + VC)_n = (AVCO/2^{16})(VC_n + VA_{n-1}) + (AVC1/2^{16})(VC_{n-1} + VA_n)$$

Low-Power, Multifunction, Polyphase AFE

Highpass Filter (HPF)

A simple first-order highpass filter (HPF) is used.The filter formula is:

$$Y_n = (1 - hpf\_b0f/2^{16}) \times (Y_{n-1} + X_n - X_{n-1})$$

The filter coefficient (hpf_b0f) is a signed 16-bit value and can be configured by the master.

Integrator

The digital integrator block can be engaged separately for each current phase (IA, IB, IC) and for neutral current (IN) by setting configuration bits INTGA, INTGB, INTGC, and INTGN in the CONNCT register. When enabled, the digital integrator block calculates the integral of the input current signal (i.e., sum of samples) and then feeds this integral into the processing path instead of the current sample. This sum can produce a DC offset that must be removed by an additional HPF stage. The HPF can be combined with the integrator in a single formula:

$$Y_n = (1 - hpf\_b0f/2^{16}) \times (Y_{n-1} + X_n)$$

where hpf_b0f is the same coefficient used in the stand-alone HPF stage. The integrator increases the amplitude of accumulation by approximately ($NS/2\pi$), where NS is the number of samples per line cycle (factor approximately 16 for 50Hz signal and 200µs sampling rate). The output of the integrator is scaled down by factor 16 in the MAXQ3180.

The HPF, when combined with the digital integrator, introduces an additional phase shift into the current channel. To compensate for this, the second HPF stage is automatically engaged in the voltage processing path when the current integrator is active.

Fundamental and Harmonics Modes

The power calculation engine can work in one of three modes: full, fundamental, and harmonics. The mode of operation is selected by the HRM configuration bits.

- HRM = 00b—Full mode. Neither the bandpass or the bandstop filters are applied.
- HRM = 01b—Fundamental mode. The voltage channel signal is put through the bandpass filter (BPF). This BPF is centered on the fundamental frequency, so only fundamental power is measured.
- HRM = 10b—Harmonics mode. The voltage channel signal is put through the bandstop filter (BSF). That BSF is centered on the fundamental frequency, so fundamental power is removed and only harmonics power is measured.

Both filters, the BPF and BSF, are second-order filters and use the same set of coefficients. The filter formulas are:

BPF:

$$Y_n = 2Y_{n-1} - Y_{n-2} + (bpf\_b0f/2^{20}) \times (2Y_{n-2} + X_n - X_{n-2}) - (bpf\_a1f/2^{20}) \times Y_{n-1}$$

BSF:

$$Y_n = 2Y_{n-1} - Y_{n-2} + X_n - 2X_{n-1} - X_{n-2} + (bpf\_b0f/2^{20}) \times (2Y_{n-2} - X_n - X_{n-2}) + (bpf\_a1f/2^{20}) \times (X_{n-1} - Y_{n-1})$$

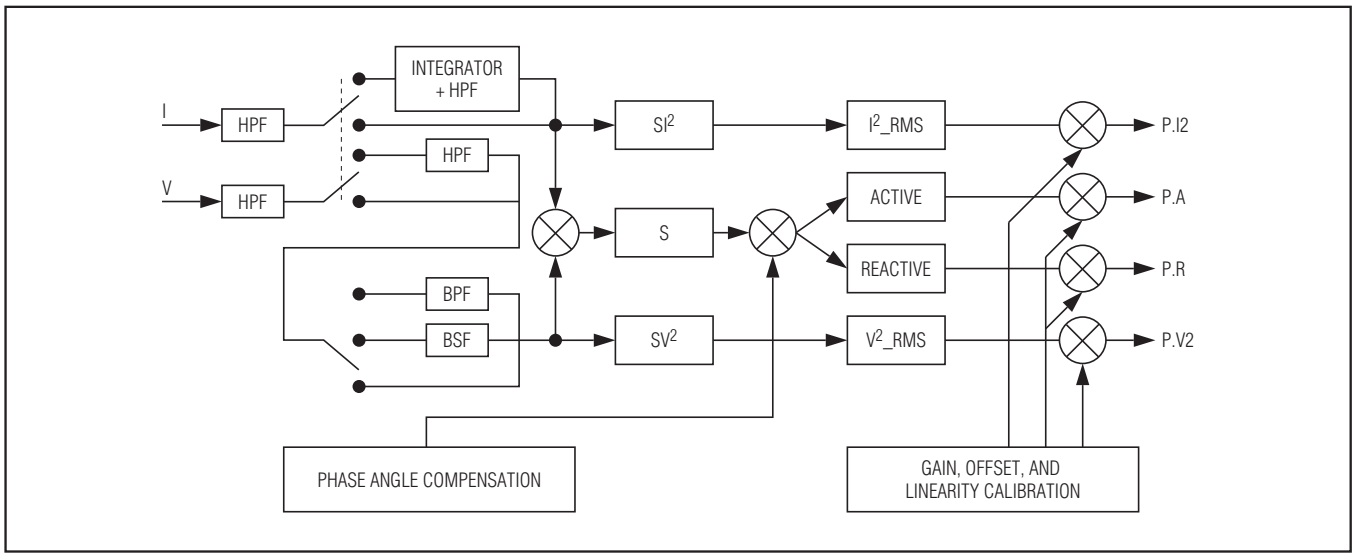

Figure 8. DSP Flow

Filter coefficients (bpf_b0f and bpf_a1f) are signed 16-bit values and can be configured by the master. By default they are tuned to 50Hz frequency, provided that all other parameters are also set to default values. The coefficients of the filters should be updated periodically by the master to track the actual line frequency that may deviate from the preset value. It is usually enough to update only one coefficient (bpf_a1) to change the filter's peak frequency slightly.

The same mechanism of BPF can be used for a special feature—measuring individual harmonics. The BPF coefficients can be set to values that pass only the Nth-order harmonics on the voltage channel. Then, the V_{RMS} output produces the Nth harmonics voltage and the power output produces the Nth harmonics power. The current I_{RMS} can then be calculated by the master as I_{RMS} = Power/V_{RMS}.

Phase Angle Compensation

Phase angle compensation requires two coefficients—cosine and sine of the phase angle PA. The phase compensation angle PA is calculated based on the logarithm of the raw RMS-current values using 3rd-order curve fitting:

$$PA \times 2^{16} = PA\_0 + (PA\_1 \times X) + (PA\_2 \times X^2) + (PA\_3 \times X^3)$$

Where

$$X = \frac{([(2^{12}) \times \ln([IRMS/2^{16}])] - ln\_off)}{2^{16}}$$

Where brackets [ ] denote the integer and ln_off is the hard-coded value 6100h.

Curve-fitting coefficients are usually obtained during the calibration process and loaded into RAM registers upon initialization. Once the phase angle PA has been calculated, the MAXQ3180 calculates SIN(PA) and COS(PA) and performs phase compensation for active and reactive energy. By default, all curve-fitting coefficients are zeros: PA_0 = PA_1 = PA_2 = PA_3 = 0. The calibration procedure is discussed in the *Typical Calibration Procedure for MAXQ3180* section.

Apparent Power

Apparent power is then calculated. The method used is selectable using the APPSEL (OPMODE.3) bit. If APPSEL = 0 (the default mode), then

$$Pwr\_S = sqrt(Pwr\_A^2 + Pwr\_R^2)$$

If APPSEL = 1, then

$$Pwr\_S = V_{RMS} \times I_{RMS} \times NS,$$

and scaled by shifting in order to produce the same magnitude as the square-root method (APPSEL = 0).

Linearity Correction

The MAXQ3180 applies linearity compensation to active, reactive, and apparent energy based on whether input current signal level is in high range or in low range. The signal is considered high range if the voltage across the analog input pins is greater than approximately 48mV_{P-P}; otherwise the signal is considered low range. For high range, offset correction is applied to the apparent power value:

$$Pwr\_S\_corr = Pwr\_S - Eoff\_hi \times K$$

For low range, both offset and gain correction factors are applied to the apparent power value:

$$Pwr\_S\_corr = (1 + Gain\_lo/2^{16}) \times (Pwr\_S - Eoff\_lo \times K)$$

The factor K accounts for possible voltage and line frequency changes:

$$K = [NS/2^{16}] \times [VRMS/2^{16}]/2^{16}$$

Separate linearity compensation coefficients (Eoff_hi, Eoff_lo, Gain_lo) are used for each phase. Initial values of those coefficients are loaded upon default initialization; the master can then overwrite coefficients if necessary.

Once the corrected apparent power has been calculated, the MAXQ3180 applies proportional correction to active and reactive power, and applies common power gain to all power samples:

$$Pwr\_A\_corr = (1 + E\_gain/2^{16}) \times Pwr\_A \times Pwr\_S\_corr/Pwr\_S,$$

$$Pwr\_R\_corr = (1 + E\_gain/2^{16}) \times Pwr\_R \times Pwr\_S\_corr/Pwr\_S,$$

$$Pwr\_S\_corr = (1 + E\_gain/2^{16}) \times Pwr\_S\_corr$$

The calibration procedure is discussed in the *Typical Calibration Procedure for MAXQ3180* section.

Energy Accumulation Start Delay

All filters have a certain settling time before accurate energy readings can be accumulated. To avoid accumulation of invalid data from filters that are still settling, an energy accumulation timeout period can be set in the ACC_TIMO register. Together with the accumulation enable (ACC_EN) bit, this provides a means to control the preaccumulation delay. After reset, ACC_EN = 0 and no energy is accumulated. After the ACC_TIMO scan slots have elapsed, the MAXQ3180 sets ACC_EN = 1 and energy accumulation begins.

No-Load Feature

To avoid meter creep, no energy accumulation should take place when calculated apparent power is less than a certain threshold. The NOLOAD register can be

programmed to enable and configure this feature. If the measured E_VA value for a phase (A, B, or C) falls below the NOLOAD threshold, the energy accumulators for this phase are not incremented. Setting NOLOAD = 0 disables this feature.

Energy Pulse Output

The two pulse output pins, CFP and CFQ, have associated accumulators PLS1, PLS2 and configurable thresholds THR1, THR2. The MAXQ3180 issues a pulse on the output pin when the pulse accumulator exceeds the threshold level (e.g., PLS1 > THR1), then continues accumulation from the level PLS1 = PLS1 - THR1.

Each pulse output accumulator can be configured to include energy accumulators E1, E2, or E3 (typically corresponding to phase A, B, C) as independent terms, and to output various quantities, by setting the PLSCFG register:

PLSCFG = (qqqqqmmm ppppppnnn) binary

Bits [2:0] (nnn) and [10:8] (mmm) specify which phase(s) are included in the pulse output.

Bits [7:3] (ppppp) specify the quantity that is directed into the pulse 1 output; bits [15:11] (qqqqq) specify the quantity that is directed into the pulse 2 output.

Both PLS1 and PLS2 accumulators accumulate only absolute values of selected quantity. If the selected pulse-output quantity changes sign, the PLS1 or PLS2 accumulator is cleared and starts accumulation over.

The REV_P (reverse power) bit is set in the STATUS2 register if the PLS1 input stays negative for REV_TIMO consecutive line cycles; the bit is cleared when the PLS1 input stays positive for REV_TIMO consecutive line cycles. Additionally, the direction change DCH_P status bit is set whenever the direction bit REV_P changes its state. The DCH_P bit causes an interrupt request to the master if enabled (unmasked).

Similarly, the REV_Q bit is set in the STATUS2 register if the PLS2 input stays negative for REV_TIMO consecutive line cycles; the bit is cleared when the PLS2 input stays positive for REV_TIMO consecutive line cycles. Additionally, the DCH_Q status bit is set whenever the direction bit REV_Q changes its state. The DCH_Q bit causes an interrupt request to the master if enabled (unmasked).

Table 9. Pulse Output Configuration

nnn BITS	PLS1 INCLUDE	mmm BITS	PLS2 INCLUDE
000	0	000	0
001	E1	001	E1
010	E2	010	E2
011	E1 + E2	011	E1 + E2
100	E3	100	E3
101	E1 + E3	101	E1 + E3
110	E2 + E3	110	E2 + E3
111	E1 + E2 + E3	111	E1 + E2 + E3

Table 10. Pulse Output Quantity Selection

ppppp OR qqqqq	ACCUMULATED VALUE	DESCRIPTION
00000	AP - AN	True active energy (may be negative)
00001	AP + AN	Absolute active energy
00010	R1 + R2 - R3 - R4	True reactive energy (may be negative)
00011	R1 + R2 + R3 + R4	Absolute reactive energy
00100	VA	Apparent energy
00101	IH	Amp-hours
00110	I_{RMS}	I_{RMS} (for calibration purposes)
00111	V_{RMS}	V_{RMS} (for calibration purposes)
01000	AP	Active positive energy
01001	AN	Active negative energy

Table 10. Pulse Output Quantity Selection (continued)

ppppp OR qqqqq	ACCUMULATED VALUE	DESCRIPTION
01010	R1	Reactive quadrant 1 energy
01011	R2	Reactive quadrant 2 energy
01100	R3	Reactive quadrant 3 energy
01101	R4	Reactive quadrant 4 energy
01110	R1 + R3	Absolute inductive energy
01111	R2 + R4	Absolute capacitive energy
Other	Reserved	—

Peak Voltage and Current Detection

The MAXQ3180 records peak current and voltage levels for phase A, phase B, and phase C as follows. The peak RMS values of the current and voltage within a fixed number of accumulation cycles are stored in the IPK and VPK registers for each phase. The values stored in IPK and VPK represent only the 16 most significant bits of the raw RMS registers, i.e., bits 31:16. The PKCYC register specifies the number of accumulation cycles. Figure 9 illustrates the timing behavior of the peak current detection; peak voltage detection works the same way.

Overvoltage and Overcurrent Detection

The MAXQ3180 detects overvoltage and overcurrent events and can issue interrupt request signals to the master when these events occur. The overvoltage level can be programmed into the OVLVL register, while the overcurrent level is determined by the OCLVL register. Both OVLVL and OCLVL registers represent the 16 most significant bits of the VRMS or IRMS registers. Any time the MAXQ3180 detects the RMS-value exceeding a threshold level, the OV or OC interrupt flag is set. If enabled, any of these flags issues an interrupt request. All interrupt flags are “sticky” bits—the

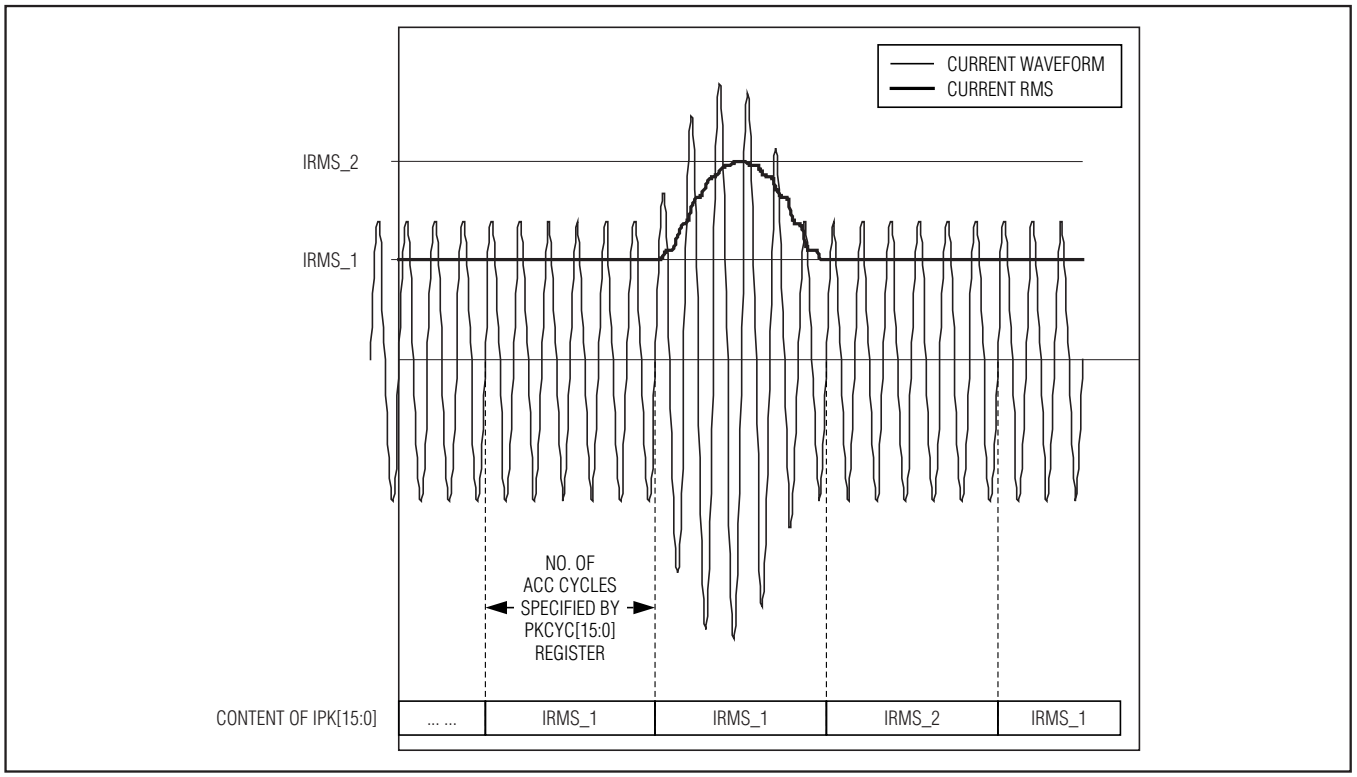

Figure 9. Peak Current-Detection Timing

MAXQ3180 never clears them on its own unless a reset occurs. The interrupt flags should be cleared by the master by writing the appropriate register.

The configuration bits OVEN and OCEN allow enable- or disable-monitoring the overvoltage and overcurrent events on each phase independently.

Voltage Sag Detection

The MAXQ3180 detects voltage sag events and can issue interrupt request signals to the master when these events occur. The sag level threshold is determined by the setting of the SAGLVL register. The SAGLVL register represents the 16 most significant bits of a raw VRMS register. A voltage sag event is detected if the RMS-voltage value remains below the SAGLVL threshold for the number of line cycles specified in the SAGCYC register. The flags SAGA, SAGB, and SAGC are set when voltage sag is detected on phase A, B, or C, respectively. If enabled, any of these flags issues an interrupt request when they are set to 1.

Tamper Condition Detection

The MAXQ3180 detects and reports the following tamper conditions:

- **Missing Potential.** The MAXQ3180 detects a missing potential condition if a phase voltage waveform either has a magnitude less than 10% of the full-scale range or has no zero crossings, i.e., the entire waveform lies above or below zero. The MISVF bit is set in the FLAGS status register for phase A, B, or C to report a missing potential condition. Also, the MISV flag bit is set in the STATUS1 register, which can cause an interrupt request signal if enabled.
- **Voltage Unbalance.** The MAXQ3180 detects a voltage unbalance condition if the sum of all three voltage signals (e.g., VA + VB + VC) has a magnitude greater than VUBLVL/2. The VUBLVL register represents the 16 most significant bits of the raw VRMS register. The VUNBF flag is set in the STATUS1 register to report voltage unbalance. This can cause an interrupt request signal if enabled.
- **Current Unbalance.** The MAXQ3180 detects a current unbalance condition if the sum of current signals IA + IB + IC has a magnitude greater than IUBLVL/2. The IUBLVL register represents the 16 most significant bits of a raw IRMS register. The IUNBF flag is set in the STATUS1 register to report a current unbalance.

Meter Units to Real Units Conversion

All energy calculations, including various threshold checks, are performed internally in fixed format in meter units. Therefore, the threshold values must be supplied by the user in meter units as well. This section describes how to convert real units (V, A, kWh, etc.) into meter units and vice versa.

The conversion factors are based on the settings shown in Table 11, defined by the user's design.

Meter units are defined with respect to the base parameters in Table 11 as shown in Table 12.

Table 11. Meter to Real Units Conversion

NAME	DESCRIPTION	DEFAULT VALUE
t_{FR}	Analog scan frame timing. This parameter is defined by the R_ADCRATE setting and system clock frequency f_{SYS}: $t_{FR} = (R\_ADCRATE + 1) \times 8/f_{SYS}$ Default conditions are R_ADCRATE = 199, f_{SYS} = 8MHz.	200µs/frame
NS	Number of frames per line cycle. This parameter is defined by nominal line frequency f_{LINE} and frame timing t_{FR}: $NS = 1/(t_{FR} \times f_{LINE})$ Default conditions are t_{FR} = 200µs, f_{LINE} = 50Hz.	100 frames/ line cycle
VFS	Full-scale voltage. This is the input voltage that produces full-scale ADC output: 2048 LSB for positive or -2048 LSB for negative, total 12-bit range. This parameter is defined by the hardware voltage transducer ratio V_{TR} and ADC full-scale input voltage V_{FSADC}: $VFS = V_{FSADC} \times V_{TR}$ Default conditions are V_{FSADC} = 1V, V_{TR} = 545V/V (for reference meter design).	545V
IFS	Full-scale current. This is the input current that produces full-scale ADC output: 2048 LSB for positive or -2048 LSB for negative, total 12-bit range. This parameter is defined by the hardware current transducer ratio I_{TR} and ADC full-scale input voltage V_{FSADC}: $IFS = V_{FSADC} \times I_{TR}$ Default conditions are V_{FSADC} = 1V, I_{TR} = 100A/V (for reference meter design).	100A

Table 12. Meter Unit Definitions

REGISTER OR ACCUMULATOR	RAM ADDRESS (BYTE)	LENGTH AND FORMAT	METER UNIT (1 LSB)	DEFAULT METER UNIT (1 LSB)	DEFAULT MAX LEVEL OR ACCUMULATOR CAPACITY
Raw IRMS Sample	402, 642, 882, 996	32-bit unsigned	$IFS/2^{30}$	93.13nA	400A
Raw VRMS Sample	406, 646, 886	32-bit unsigned	$VFS/2^{30}$	0.5076µV	2180V
Raw IH Sample	410, 650, 890, 1000	32-bit unsigned	$IFS \times t_{FR}/2^{14}$	0.3391nAh	1.456Ah
Raw Act, Rea, App as Energy Sample	414, 418, 422, 654, 658, 662, 894, 898, 902	32-bit signed (act, rea), unsigned (app)	$IFS \times VFS \times t_{FR}/2^{18}$	11.55nWh	49.61Wh unsigned, 24.80Wh signed
Raw Act, Rea, App as Power Sample	414, 418, 422, 654, 658, 662, 894, 898, 902	32-bit signed (act, rea), unsigned (app)	$IFS \times VFS/(NS \times 2^{18})$	2.079mW	8.929MW unsigned, 4.465MW signed
Hidden Energy Accumulators	System	32-bit unsigned	$IFS \times VFS \times t_{FR}/2^{18}$	11.55nWh	49.61Wh
Hidden Ah Accumulators	System	32-bit unsigned	$IFS \times t_{FR}/2^{14}$	0.3391nAh	1.456Ah
KWHT	40	32-bit unsigned	$IFS \times VFS \times t_{FR}/2^{18}$	11.55nWh	49.61Wh
KAHT	44	32-bit unsigned	$IFS \times t_{FR}/2^{14}$	0.3391nAh	1.456Ah
THR1, THR2 (when pulse output energy)	52, 56	32-bit unsigned	$IFS \times VFS \times t_{FR}/2^{18}$	11.55nWh	49.61Wh
THR1, THR2 (when pulse output Ah)	52, 56	32-bit unsigned	$IFS \times t_{FR}/2^{14}$	0.3391nAh	1.456Ah
THR1, THR2 (when pulse output I_{RMS})	52, 56	32-bit unsigned	$IFS/2^{30}$	93.13nA	400A
THR1, THR2 (when pulse output V_{RMS})	52, 56	32-bit unsigned	$VFS/2^{30}$	0.5076µV	2180V
IPK	264, 504, 744	16-bit unsigned	$IFS/2^{14}$	6.104mA	400A
VPK	266, 506, 746	16-bit unsigned	$VFS/2^{14}$	33.26mV	2180V
OCLVL	112	16-bit unsigned	$IFS/2^{14}$	6.104mA	400A
OVLVL	114	16-bit unsigned	$VFS/2^{14}$	33.26mV	2180V
SAGLVL	116	16-bit unsigned	$VFS/2^{14}$	33.26mV	2180V
IUBLVL	118	16-bit unsigned	$IFS/2^{14}$	6.104mA	400A
VUBLVL	120	16-bit unsigned	$VFS/2^{14}$	33.26mV	2180V
NZC_TIMO	122	16-bit unsigned	t_{FR}	200µs	13.12s
REV_TIMO	124	16-bit unsigned	$t_{FR} \times NS$	0.02s	21.85 minutes
ACC_TIMO	126	16-bit unsigned	$t_{FR} \times NS$	0.02s	21.85 minutes
COM_TIMO	128	16-bit unsigned	t_{FR}	200µs	13.12s
NOLOAD	138	16-bit signed	$IFS \times VFS \times t_{FR}/2^{18}$ per line-cycle; or $IFS \times VFS/(NS \times 2^{18})$	11.55nWh per line cycle, or 2.079mW	0.3785mWh per line cycle, or 136.25W

Table 13. Virtual Register Coefficients

VIRTUAL REGISTER	INPUT RESOLUTION IN METER UNITS (1 LSB)	OUTPUT RESOLUTION (1 LSB), DEFINED BY USER	COEFFICIENT	DEFAULT OUTPUT RESOLUTION (1 LSB)	DEFAULT COEFFICIENT
Power, 0x 801–827	E_res = IFS x VFS/2^{18}	P_res	PWR_FS = 2^{16} x E_res/P_res	1W	PWR_FS = 0x3539
Voltage, 0x 831–834	Vrms_res = VFS/2^{30}	V_res	VOLT_FS = 2^{16} x V_res/Vrms_res	1µV	VOLT_FS = 0x81F0
Current, 0x 831–834	Irms_res = IFS/2^{30}	I_res	AMP_FS = 2^{16} x I_res/Irms_res	1µA	AMP_FS = 0x17D8

When reading virtual registers, the MAXQ3180 uses the configurable coefficients TIME_FS, VOLT_FS, AMP_FS, and PWR_FS to return meaningful data. However, the user must first configure these coefficients. Table 13 describes how to set the coefficients.

Temperature Measurement

The MAXQ3180 only measures the die temperature when commanded by the master. To activate temperature measurement, the master must write one of the TMPC[1:0] bits in the OPMODE register. When TMPC0 is set to 1, the MAXQ3180 performs a single temperature conversion by forcing bias currents 1µA and 16µA through a pair of diode stacks, placing the result in the RAW_TEMP register and automatically clearing the TMPC0 bit to 0. When TMPC1 is written to 1, the MAXQ3180 performs two consecutive temperature conversions. The first conversion is the same as previously stated with 1µA and 16µA bias currents, and the second conversion uses reversed 16µA and 1µA bias currents. The average of the two measurements is placed in the RAW_TEMP register, and then both TMPC bits are cleared. Double measurement cancels possible offset incidental to single measurement and thus improves accuracy. The RAW_TEMP register returns raw ADC sample proportional to absolute temperature. Conversion to meaningful scale (°F, °C, or °K) should be done by the master as needed. When finished, the MAXQ3180 sets the temperature ready flag, TMRD, in the STATUS1 register. This flag signals an interrupt request to the master if enabled. The master can then read the TEMP register and clear the TMRD status flag.

Typical Calibration Procedure for MAXQ3180

The MAXQ3180 should be calibrated at the user's factory and the calibration constants stored in nonvolatile memory by the host microcontroller. Upon any reset or loss of power, the host microcontroller must reload the MAXQ3180 with the calibration constants.

The calibration procedure consists of three passes, one per each phase A, B, and C. Each pass applies the same calibration procedure to a single phase, consisting of the following items:

- Current Gain Calibration
- Voltage Gain Calibration
- Power Gain Calibration
- Power Linearity Calibration
- Phase Angle Calibration

Each item requires one or more signals be applied to the meter's inputs, then the output to be measured. The calibration coefficients are then calculated, verified, and loaded into the MAXQ3180's RAM registers. The power linearity calibration and the phase angle calibration can be performed in any order.

Current Gain Calibration

To perform the current gain calibration, all three phase voltages 220V should be applied. Only one current signal of max amplitude (I_{MAX}) is applied to the phase input being calibrated. From the view of the MAXQ3180 pins, the other current inputs should be grounded or

connected together to result in zero current. **Note:** All intermediate calculations should be performed with double precision, and the last result rounded to the nearest integer.

1) Clear I_gain coefficient that is being calibrated to 0x0000.
2) Measure average raw IRMS by reading the RAM register several times.
3) Calculate expected raw RMS value using the following proportion:

   Full_scale_current: produces FS_raw_rms = 2^{30}
   I_input_current: produces Expected_raw_rms

   Here, Full_scale_current is the input current that is transformed into $1V_{RMS}$ at the input pins. That Full_scale_current value depends on the transducer chosen for meter design. For example, if current sensor is a transformer 10A to 5mA with 20Ω load resistor, then Full_scale_current = 100A, because it is transformed to 50mA x 20Ω = 1V.
4) Calculate I_gain coefficient:

   I_gain = [Expected_raw_rms/ Measured_raw_rms) - 1] x 2^{16}

Voltage Gain Calibration

To perform the voltage gain calibration, all three phase voltages 220V should be applied. Current inputs should be zero. **Note:** All intermediate calculations should be performed with double precision, the last result rounded to the nearest integer.

1) Clear V_gain coefficient being calibrated to 0x0000.
2) Measure average raw VRMS by reading the RAM register several times.
3) Calculate expected raw RMS value using the following proportion:

   Full_scale_voltage: produces FS_raw_rms = 2^{30}
   V_input_voltage: produces Expected_raw_rms

   Here, Full_scale_voltage is the input voltage that is transformed into $1V_{RMS}$ at the input pins. That Full_scale_voltage value depends on the transducer chosen for meter design. For example, if voltage sensor is a divider with a 544:1 resistor ratio, then Full_scale_voltage = 545V, because it is transformed to 1V.
4) Calculate V_gain coefficient:

   V_gain = [(Expected_raw_rms/ Measured_raw_rms) - 1] x 2^{16}

Power Gain Calibration

To perform the power gain calibration, all three phase voltages 220V must be applied. Only one current signal of max amplitude (I_{MAX}) is applied to the phase input being calibrated. The current sine wave should be in phase with the corresponding voltage sine wave, i.e., power factor 1. Other current inputs should be zero.

1) Clear the E_gain coefficient being calibrated to 0x0000.
2) Measure the power output of the meter. This can be done in two ways: (a) by reading raw RAM registers from the MAXQ3180, or (b) by measuring pulse output error. The following procedure depends on the way of measuring power output.
   a) Measure average raw apparent energy by reading the RAM register several times.
   b) Pulse output error is typically measured by the tester equipment. The pulse output parameters in the MAXQ3180 must be properly configured before pulse output error can be measured.

      The PLSCFG register should be set to output apparent energy of one phase being calibrated. That setting is:

      If measuring pulse 1 output on the CFP pin:
      PLSCFG = 0x0021 for phase A
      PLSCFG = 0x0022 for phase B
      PLSCFG = 0x0024 for phase C

      or

      If measuring pulse 2 output on the CFQ pin:
      PLSCFG = 0x2100 for phase A
      PLSCFG = 0x2200 for phase B
      PLSCFG = 0x2400 for phase C
   c) Then, the corresponding pulse threshold register should be set to the proper value; that is, THR1 register if measure pulse 1 output on the CFP pin, or THR2 register if measure pulse 2 output on the CFQ pin. The value for the threshold register defines the pulse output rate and should match the rate expected by tester equipment. The tester typically expresses pulse output rate as a meter constant (MC) indicating the number of pulses per kWh. The proper threshold value is then calculated as:

      (THR1 or THR2) = 2^{18} x 10^3/(MC x IFS x VFS x t_{FR})

      In this formula IFS is the Full_scale_current described in the *Current Gain Calibration* section, VFS is the Full_scale_voltage described in

the *Voltage Gain Calibration* section, and t_{FR} is the sampling time that depends on the MAXQ3180 system clock frequency and sampling rate register setting (ADCRATE):

$$t_{FR} = (ADCRATE + 1) \times 8/f_{SYS}$$

For example, for the default conditions ADCRATE = 199 and f_{SYS} = 8MHz, then t_{FR} = 200µs = 55.55nh. Using typical example values IFS = 100A and VFS = 545V, the formula for the threshold can be transformed into the following:

Typical (THR1 or THR2) = 86,579,669,725/MC

Note: Threshold is a 32-bit register, which imposes a limitation on the minimal meter constant to avoid overflow.

When the PLSCFG and THR1 (or THR2) registers are set, the pulse output error can be measured by tester equipment. That error is usually expressed as % of the expected power.

3) If choice 2a was made (apparent energy by reading RAM register), then perform step 3. Calculate expected raw energy value using the following proportion:

   Full_scale voltage x Full_scale_current: produce FS_raw_pwr = $2^{18}/(f_{LINE} \times t_{FR})$
   V_input_voltage x I_input_current: produce Expected_raw_pwr

   Here, Full_scale_voltage, Full_scale_current, and t_{FR} are the same as described above, f_{LINE} is the line frequency of the input voltage, typically 50Hz or 60Hz.

4) Calculate E_gain coefficient:

   a) If output was measured by reading RAM register:

   $$E\_gain = [(Expected\_raw\_pwr/Measured\_raw\_pwr) - 1] \times 2^{16}$$

   b) If output was measured through pulse output error:

   $$E\_gain = (2^{16}) \times (-Measured\_Error\%)/(100\% + Measured\_Error\%)$$

   Note: All intermediate calculations should be performed with double precision, the last result rounded to the nearest integer.

Power Linearity Calibration

This calibration compensates for nonlinearity over the range and requires at least four power measurements at different loads. To perform the power linearity calibration, all three phase voltages 220V must be applied. Only one current signal is applied to the phase input being calibrated. The current sine wave should be in phase with the corresponding voltage sine wave, i.e., power factor 1. Other current inputs should be 0.

1) Clear the Eoff_hi, Gain_lo, and Eoff_lo coefficients being calibrated to 0x0000.

2) Make power measurements.

   a) First power measurement. Apply current input signal of the RMS value close to $IFS/2^{1.5}$ to the phase input being calibrated. For example, typical target value is $100/2^{1.5}$ = 35.36A, so reasonable input current is 30A or 40A. Measure average raw apparent energy by reading the RAM register several times. Denote applied current as I1 and measured power as P1 for future reference.

   b) Second power measurement. Apply current input signal of the RMS value close to $IFS/2^{4.5}$ to the phase input being calibrated. For example, typical target value is $100/2^{4.5}$ = 4.42A, so reasonable input current is 4A or 5A. Measure average raw apparent energy by reading the RAM register several times. Denote applied current as I2 and measured power as P2 for future reference.

   c) Third power measurement. Apply current input signal of the RMS value close to $IFS/2^{6.5}$ to the phase input being calibrated. For example, typical target value is $100/2^{6.5}$ = 1.10A, so reasonable input current is 1A. Measure average raw apparent energy by reading the RAM register several times. Denote applied current as I3 and measured power as P3 for future reference.

   d) Fourth power measurement. Apply current input signal of the RMS value close to $IFS/2^{9.5}$ to the phase input being calibrated. For example, typical target value is $100/2^{9.5}$ = 0.14A, so reasonable input current is 0.1A or 0.2A. Measure average raw apparent energy by reading the RAM register several times. Denote applied current as I4 and measured power as P4 for future reference.

3) Measure average raw VRMS by reading the RAM register several times.
4) Measure average NS by reading the RAM register several times.
5) Calculate coefficient K = [NS/2^{16}] x [VRMS/2^{16}]/2^{16}.
6) Calculate Eoff_hi coefficient:

$$Eoff\_hi = [(P2 \times I1 - P1 \times I2)/(I1 - I2)])/K.$$

7) Calculate Eoff_lo coefficient:

$$Eoff\_lo = [(P4 \times I3 - P3 \times I4)/(I3 - I4)]/K.$$

8) Calculate Gain_lo coefficient (using calculated above Eoff_hi, Eoff_lo, and K):

$$Gain\_lo = (\{(I3/I1) \times (P1 + K \times Eoff\_hi)/(P3 + K \times Eoff\_lo)\} - 1) \times 2^{16}$$

Note: All intermediate calculations should be performed with double precision, the last result rounded to the nearest integer. Eoff_hi, Gain_lo, and Eoff_lo are 16-bit signed coefficients. If a calculated value exceeds 16 bits, the part cannot be calibrated. In this case, assign the largest possible value, i.e., 0x7FFF for positive overflow or 0x8000 for negative overflow.

Phase Angle Calibration

This calibration is intended to compensate for phase angle errors across the range of input loads. The MAXQ3180 uses four PA_n coefficients to calculate the compensation phase angle as a 3rd-order polynomial:

$$compensation\_phase\_angle = PA\_0 + (PA\_1 \times X) + (PA\_2 \times X^2) + (PA\_3 \times X^3)$$

Where X is proportional to the logarithm of raw IRMS. Full calibration of all four coefficients requires at least four measurements of the phase angle across the range. However, in most cases, only one coefficient PA_0 is needed that requires at least one phase angle measurement.

For input signals, all three phase nominal voltages 220V should be applied. Only one current signal is applied to the phase input being calibrated. Other current inputs should be 0.

Phase Angle Error Measurement

This calibration procedure requires measuring the phase angle error of the meter's output at the given current input level I_in. This can be done in two ways: (I) by reading raw RAM registers, or (II) by measuring pulse output errors at different power factors.

Measurement Technique I: Measure Output Phase Angle Error by Reading RAM Registers

1) Measure average raw active power by reading the RAM registers several times.
2) Measure average raw reactive power by reading the RAM registers several times.
3) Calculate output phase angle:

$$output\_PA = atan(Reactive\_raw\_pwr/Active\_raw\_pwr)$$

4) Calculate output phase angle error:

$$output\_PA\_error = output\_PA - input\_PA$$

Measurement Technique II: Measure Output Phase Angle Using Pulse Output

Before the pulse output can be measured, the pulse configuration registers PLSCFG and THR1 (or THR2) must be properly configured. The pulse output should be set to active power. For details on how to set those registers, see the *Power Gain Calibration* section.

1) Apply input signal with power factor 1 (input phase angle 0°) to the meter's inputs. Measure pulse output error for active power, in percent. Denote it as Err00 for future reference.
2) Apply input signal with power factor 0.5L (input phase angle 60°) to the meter's inputs. Measure pulse output error for active power, in percent. Denote it as Err60 for future reference.
3) Calculate output phase angle error:

$$output\_PA\_error = atan\{(1/sqrt(3)) \times (Err00 - Err60)/(100\% + Err00)\}$$

Phase Angle Calibration Procedure

1) Clear PA_0, PA_1, PA_2, PA_3 coefficients being calibrated to 0x0000.
2) Phase angle error measurement.
   a) Apply current input signal of the RMS value close to IFS/$2^{1.5}$ to the phase input being calibrated. For example, typical target value is 100/$2^{1.5}$ = 35.36A, so reasonable input current is 30A or 40A. Measure the output phase angle error as described above. Denote applied current as I1 and measured phase angle error expressed in radians as PAerr1 for future reference.
   b) Measure average raw IRMS by reading the RAM register several times. Denote this as I1_raw for future reference.

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c) Calculate pair of coordinates (x1,y1):

$$x1 = (\ln(I1\_raw/2^{16}) - 6.0625)/16$$
$$y1 = (-PAerr1) \times 2^{16}$$

3) Repeat the phase angle error measurement across the range.

Repeat steps 2a to 2c using other input currents across the range. It is recommended to spread input current points uniformly in logarithmic scale, resulting in a set of point coordinates:

$$(x1,y1), (x2,y2), \ldots (xN,yN)$$

The number of points N is not limited.

4) Calculate the coefficients (PA_n) of best fit polynomial curve.

The calculation recipe depends on the order of polynomial.

a) For zero-order curve (requires at least one point):

$$PA\_0 = average(y1,y2, \ldots yN)$$
$$PA\_1 = PA\_2 = PA\_3 = 0$$

5) For first-order curve (requires at least two points):

$$PA\_1 = \{\sum (xi-x\_avg)(yi-y\_avg)\}/\{\sum (xi-x\_avg)^2\}$$
$$PA\_0 = y\_avg - PA\_1 \times x\_avg$$
$$PA\_2 = PA\_3 = 0$$

where $x\_avg = average (x1,x2, \ldots xN)$,
$y\_avg = average (y1,y2, \ldots yN)$

These two cases cover the majority of practical situations. For higher order curves, the formulas are more complex, and the calculations can be performed using built-in functions of Microsoft Excel® or MATLAB® from The MathWorks, Inc.

Note that all intermediate calculations should be performed with double precision, the last result rounded to the nearest integer. Also note that PA_n are 16-bit signed coefficients. If the calculated value exceeds 16 bits, the phase angle cannot be calibrated. In this case, assign the largest possible value, i.e., 0x7FFF for positive overflow or 0x8000 for negative overflow.

Application Information

Grounds and Bypassing

Careful PCB layout significantly minimizes noise on the analog inputs, resulting in less noise on the digital I/O that could cause improper operation. The use of multilayer boards is essential to allow the use of dedicated power planes. The area under any digital components should be a continuous ground plane if possible. Keep any bypass capacitor leads short for best noise rejection and place the capacitors as close to the leads of the devices as possible.

The MAXQ3180 must have separate ground areas for the analog (AGND) and digital (DGND) portions, connected together at a single point.

CMOS design guidelines for any semiconductor require that no pin be taken above DVDD or below DGND. Violation of this guideline can result in a hard failure (damage to the silicon inside the device) or a soft failure (unintentional modification of memory contents). Voltage spikes above or below the device's absolute maximum ratings can potentially cause a devastating IC latchup.

Microcontrollers commonly experience negative voltage spikes through either their power pins or general-purpose I/O pins. Negative voltage spikes on power pins are especially problematic as they directly couple to the internal power buses. Devices such as keypads can conduct electrostatic discharges directly into the microcontroller and seriously damage the device. System designers must protect components against these transients that can corrupt system memory.

Specific Design Considerations for MAXQ3180-Based Systems

To reduce the possibility of coupling noise into the microcontroller, the system should be designed with a crystal or oscillator in a metal case that is grounded to the digital plane. Doing so reduces the susceptibility of the design to fast transient noise.

Because the MAXQ3180 is designed for use in systems where high voltages are present, care must be taken to route all signal paths, both analog and digital, as far away as possible from the high-voltage components.

It is possible to construct more elaborate metering designs using multiple MAXQ3180 devices. This can be accomplished by using a single SPI bus to connect all the MAXQ3180 devices together but using separate slave select lines to individually select each MAXQ3180.

Additional Documentation

Designers must ensure they have the latest MAXQ3180 errata documents. Errata sheets contain deviations from published specifications. A MAXQ3180 errata sheet for any specific device revision is available at **www.maxim-ic.com/errata**.

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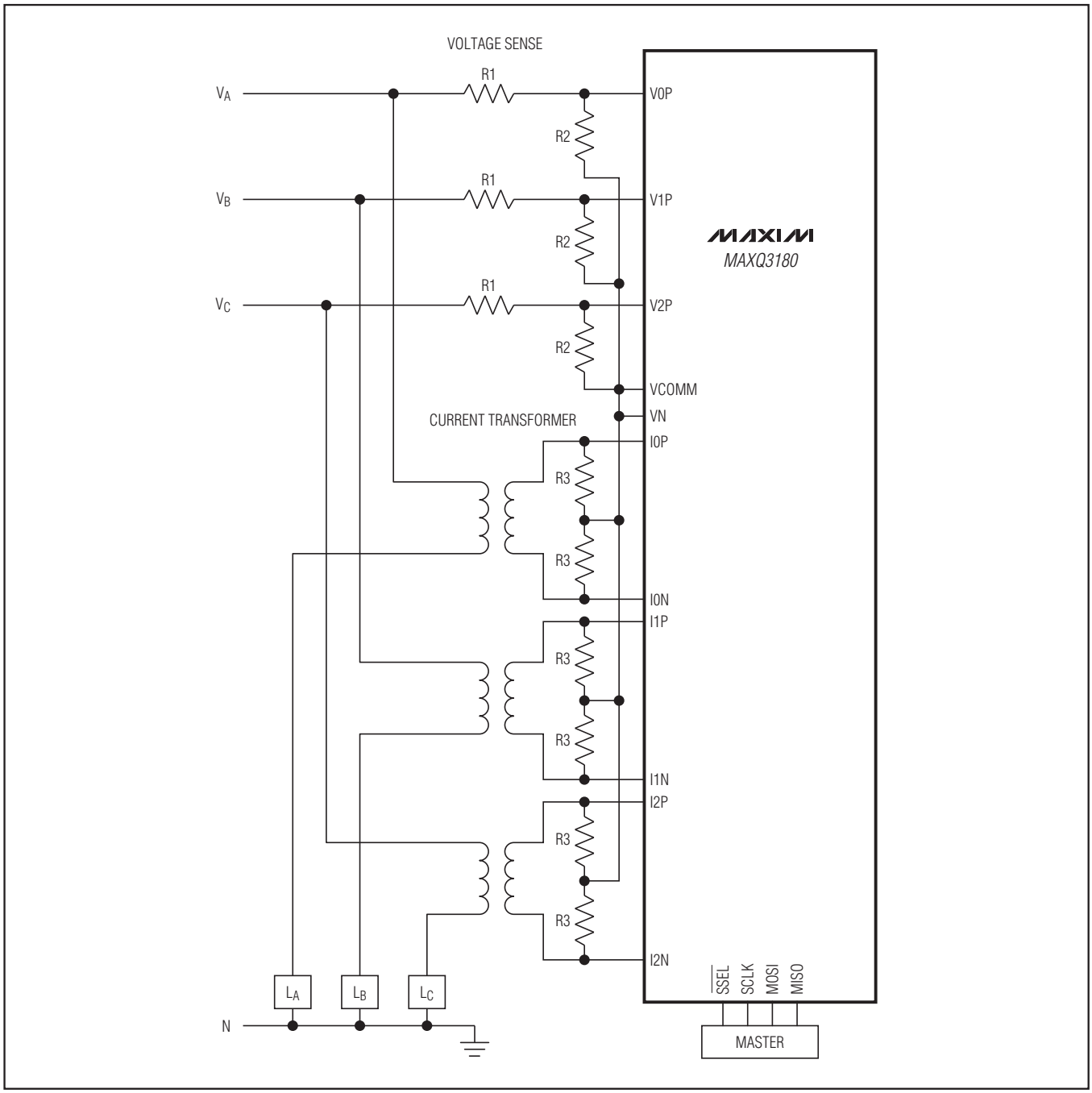
Typical Application Circuit



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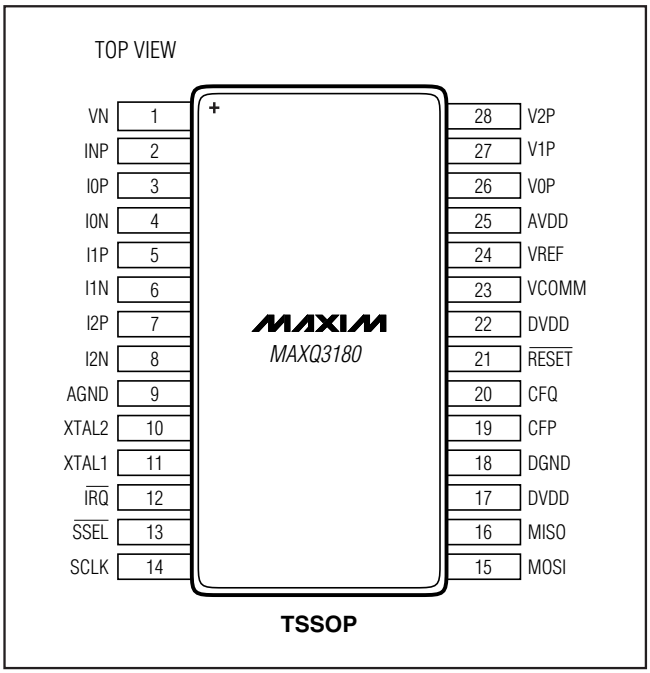
Pin Configuration



Package Information

(For the latest package outline information, go to **www.maxim-ic.com/packages**.)

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
28 TSSOP	U28+2	**21-0066**