

TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

4,194,304-WORD BY 16-BIT CMOS PSEUDO STATIC RAM

DESCRIPTION

The TC51WKM616AXBN is a 67,108,864-bit pseudo static random access memory(PSRAM) organized as 4,194,304 words by 16 bits. Using Toshiba's CMOS technology and advanced circuit techniques, it provides high density, high speed and low power. The device uses dual power supplies(2.6 to 3.3 V for core and 1.7 to 2.2 V for output buffer). The device also features SRAM-like W/R timing whereby the device is controlled by $\overline{CE1}$, \overline{OE} , and \overline{WE} on asynchronous. The device has the page access operation. Page size is 8 words. The device also supports deep power-down mode, realizing low-power standby.

FEATURES

- Organized as 4,194,304 words by 16 bits
- Dual power supplies(2.6 to 3.3 V for core and 1.7 to 2.2 V for output buffer)
- Direct TTL compatibility for all inputs and outputs
- Deep power-down mode: Memory cell data invalid
- Page operation mode:
 - Page read operation by 8 words
- Logic compatible with SRAM R/W (\overline{WE}) pin
- Standby current
 - Standby 100 μ A
 - Deep power-down standby 5 μ A

Access Times:

Access Time	75 ns
$\overline{CE1}$ Access Time	75 ns
\overline{OE} Access Time	25 ns
Page Access Time	30 ns

Package:

P-TFBGA48-0811-0.75BZ (Weight: g typ.)

PIN ASSIGNMENT (TOP VIEW)

	1	2	3	4	5	6
A	\overline{LB}	\overline{OE}	A0	A1	A2	CE2
B	I/O9	\overline{UB}	A3	A4	$\overline{CE1}$	I/O1
C	I/O10	I/O11	A5	A6	I/O2	I/O3
D	VSS	I/O12	A17	A7	I/O4	VDD
E	VDDQ	I/O13	A21	A16	I/O5	VSS
F	I/O15	I/O14	A14	A15	I/O6	I/O7
G	I/O16	A19	A12	A13	\overline{WE}	I/O8
H	A18	A8	A9	A10	A11	A20

(FBGA48)

PIN NAMES

A0 to A21	Address Inputs
A0 to A2	Page Address Inputs
I/O1 to I/O16	Data Inputs/Outputs
$\overline{CE1}$	Chip Enable Input
CE2	Chip select Input
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
\overline{LB} , \overline{UB}	Data Byte Control Inputs
VDD	Power Supply for Core
VDDQ	Power Supply for Output Buffer
GND	Ground

ABSOLUTE MAXIMUM RATINGS (See Note 1)

SYMBOL	RATING	VALUE	UNIT
V _{DD}	Power Supply Voltage	-1.0 to 3.6	V
V _{DDQ}	Output Buffer Power Supply Voltage	-1.0 to V _{DD} + 0.5 (3.6 V Max)	V
V _{IN}	Input Voltage for Address and Control Pins	-1.0 to 3.6	V
V _{I/O}	Input/Output Voltage for I/O Pins	-1.0 to V _{DDQ} + 0.5	V
T _{opr.}	Operating Temperature	-25 to 85	°C
T _{strg.}	Storage Temperature	-55 to 150	°C
T _{solder}	Soldering Temperature (10 s)	260	°C
P _D	Power Dissipation	0.6	W
I _{OUT}	Short Circuit Output Current	50	mA

DC RECOMMENDED OPERATING CONDITIONS (Ta = -25°C to 85°C)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
V _{DD}	Power Supply Voltage	2.6	2.75	3.3	V
V _{DDQ}	Output Buffer Power Supply Voltage	1.7	1.8	2.2	
V _{IH}	Input High Voltage for Address and Control Pins	1.6	—	V _{DD} + 0.3*	
	Input High Voltage for I/O Pins	1.6	—	V _{DDQ} + 0.3*	
V _{IL}	Input Low Voltage	-0.3*	—	0.4	

* : V_{IH}(Max) V_{DD}+1.0 V/ V_{DDQ}+1.0 V with 10 ns pulse width
V_{IL}(Min) -1.0 V with 10 ns pulse width

DC CHARACTERISTICS (Ta = -25°C to 85°C, V_{DD} = 2.6 to 3.3 V, V_{DDQ} = 1.7 to 2.2 V) (See Note 3 to 4)

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP.	MAX	UNIT
I _{IL}	Input Leakage Current	V _{IN} = 0 V to V _{DDQ}	-1.0	—	+1.0	μA
I _{LO}	Output Leakage Current	Output disable, V _{OUT} = 0 V to V _{DD}	-1.0	—	+1.0	μA
V _{OH}	Output High Voltage	I _{OH} = -100 μA	V _{DDQ} - 0.2	—	—	V
V _{OL}	Output Low Voltage	I _{OL} = 100 μA	—	—	0.2	V
I _{DDO1}	Operating Current	CE1 = V _{IL} CE2 = V _{IH} , I _{OUT} = 0 mA	t _{RC} = min	—	—	50 mA
I _{DDO2}	Page Access Operating Current	CE1 = V _{IL} , CE2 = V _{IH} , Page add. cycling, I _{OUT} = 0 mA	t _{PC} = min	—	—	25 mA
I _{DDS}	Standby Current(MOS)	CE1 = V _{DD} - 0.2 V, CE2 = V _{DD} - 0.2 V	—	—	70	μA
I _{DDSD}	Deep Power-down Standby Current	CE2 = 0.2 V	—	—	5	μA

CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C _{IN}	Input Capacitance	V _{IN} = GND	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = GND	10	pF

Note: This parameter is sampled periodically and is not 100% tested.

AC CHARACTERISTICS AND OPERATING CONDITIONS

(Ta = -25°C to 85°C, VDD = 2.6 to 3.3 V, VDDQ = 1.7 to 2.2 V) (See Note 5 to 11)

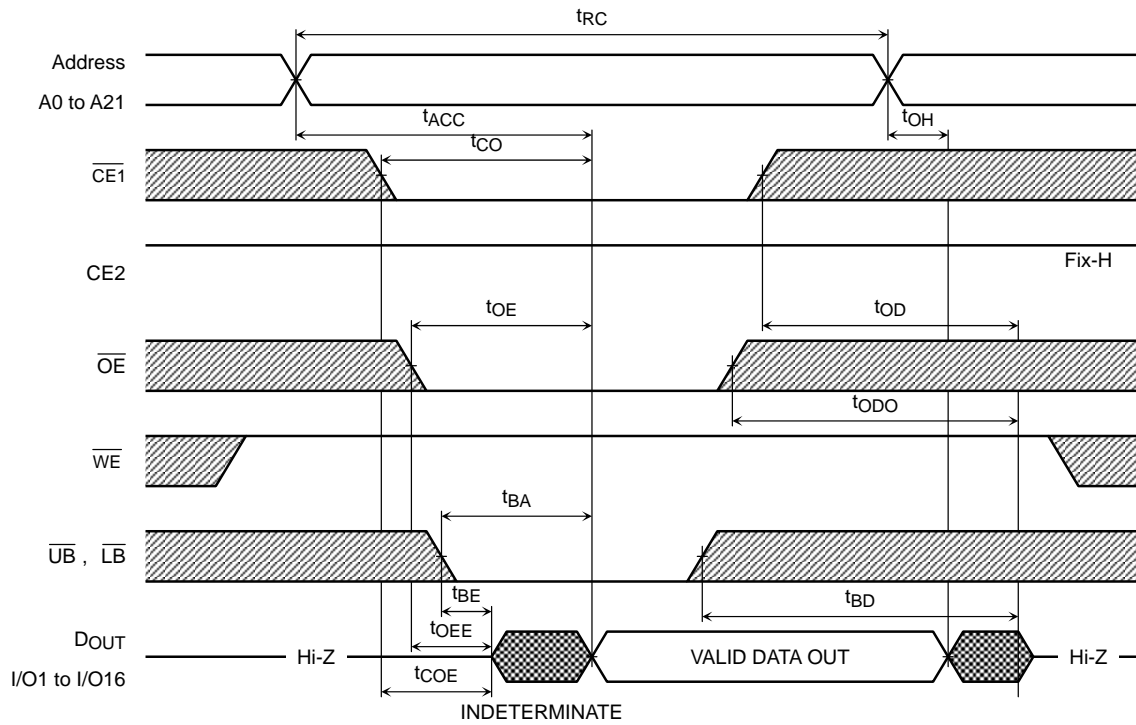
SYMBOL	PARAMETER	MIN	MAX	UNIT
t _{RC}	Read Cycle Time	75	10000	ns
t _{ACC}	Address Access Time	—	75	ns
t _{CO}	Chip Enable ($\overline{CE1}$) Access Time	—	75	ns
t _{OE}	Output Enable Access Time	—	25	ns
t _{BA}	Data Byte Control Access Time	—	25	ns
t _{COE}	Chip Enable Low to Output Active	10	—	ns
t _{OEE}	Output Enable Low to Output Active	0	—	ns
t _{BE}	Data Byte Control Low to Output Active	0	—	ns
t _{OD}	Chip Enable High to Output High-Z	—	20	ns
t _{ODO}	Output Enable High to Output High-Z	—	20	ns
t _{BD}	Data Byte Control High to Output High-Z	—	20	ns
t _{OH}	Output Data Hold Time	10	—	ns
t _{PM}	Page Mode Time	75	10000	ns
t _{PC}	Page Mode Cycle Time	30	—	ns
t _{AA}	Page Mode Address Access Time	—	30	ns
t _{AOH}	Page Mode Output Data Hold Time	10	—	ns
t _{WC}	Write Cycle Time	75	10000	ns
t _{WP}	Write Pulse Width	50	—	ns
t _{CW}	Chip Enable to End of Write	75	—	ns
t _{BW}	Data Byte Control to End of Write	60	—	ns
t _{AW}	Address Valid to End of Write	60	—	ns
t _{AS}	Address Set-up Time	0	—	ns
t _{WR}	Write Recovery Time	0	—	ns
t _{ODW}	\overline{WE} Low to Output High-Z	—	20	ns
t _{OEW}	\overline{WE} High to Output Active	0	—	ns
t _{DS}	Data Set-up Time	30	—	ns
t _{DH}	Data Hold Time	0	—	ns
t _{CS}	CE2 Set-up Time	0	—	ns
t _{CH}	CE2 Hold Time	300	—	μs
t _{DPD}	CE2 Pulse Width	10	—	ms
t _{CHC}	CE2 Hold from $\overline{CE1}$	0	—	ns
t _{CHP}	CE2 Hold from Power On	30	—	μs

AC TEST CONDITIONS

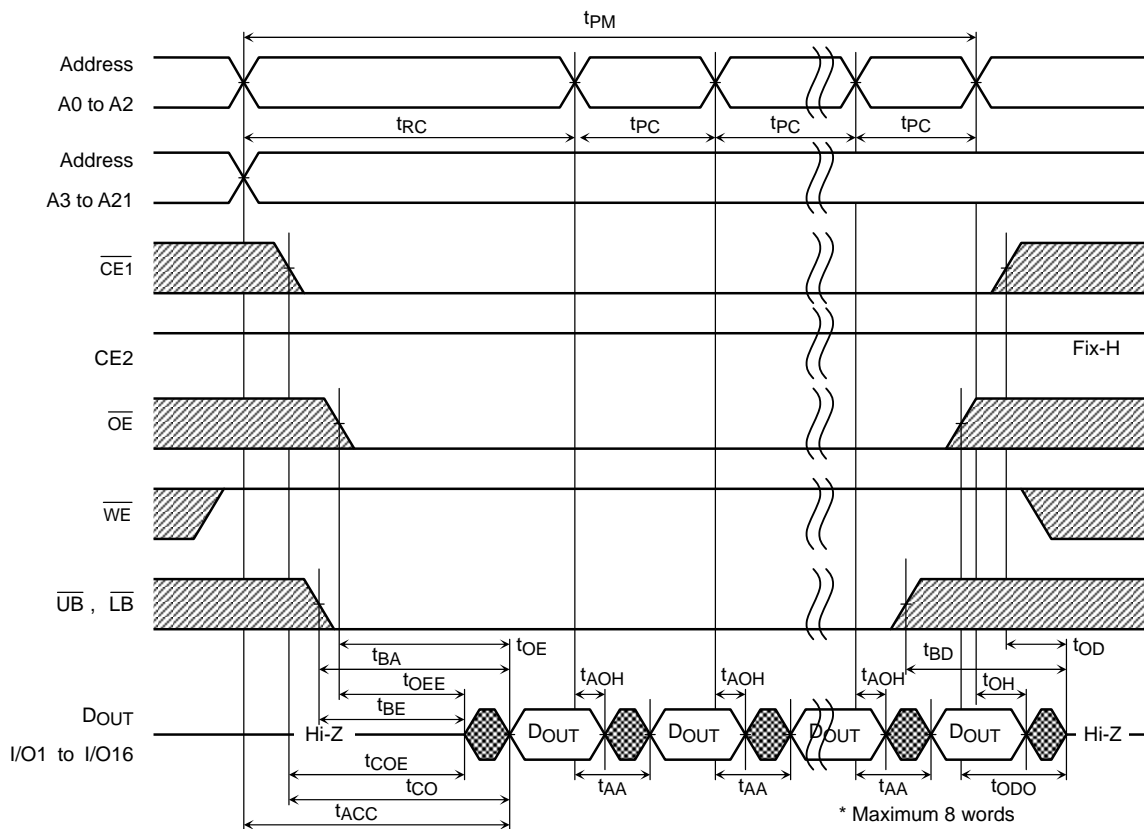
PARAMETER	CONDITION
Output load	30 pF + 1 TTL Gate
Input pulse level	V _{DDQ} - 0.2 V, 0.2 V
Timing measurements	V _{DDQ} × 0.5
Reference level	V _{DDQ} × 0.5
t _R , t _F	5 ns

TIMING DIAGRAMS

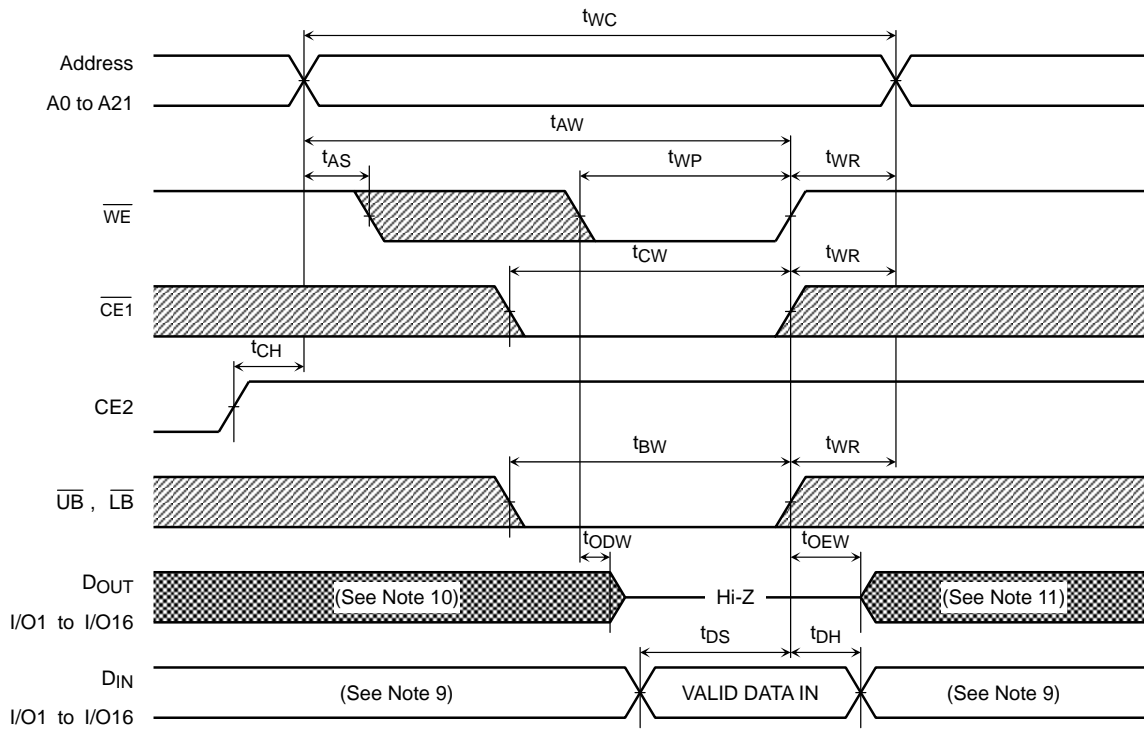
READ CYCLE



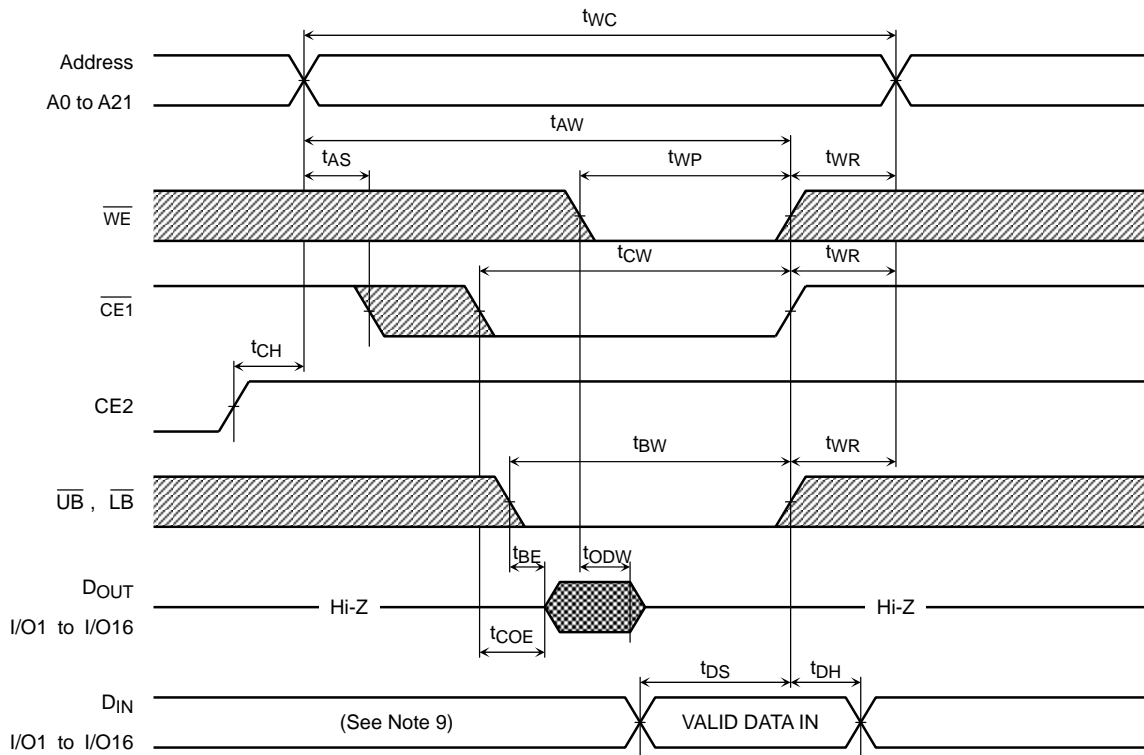
PAGE READ CYCLE (8 words access)



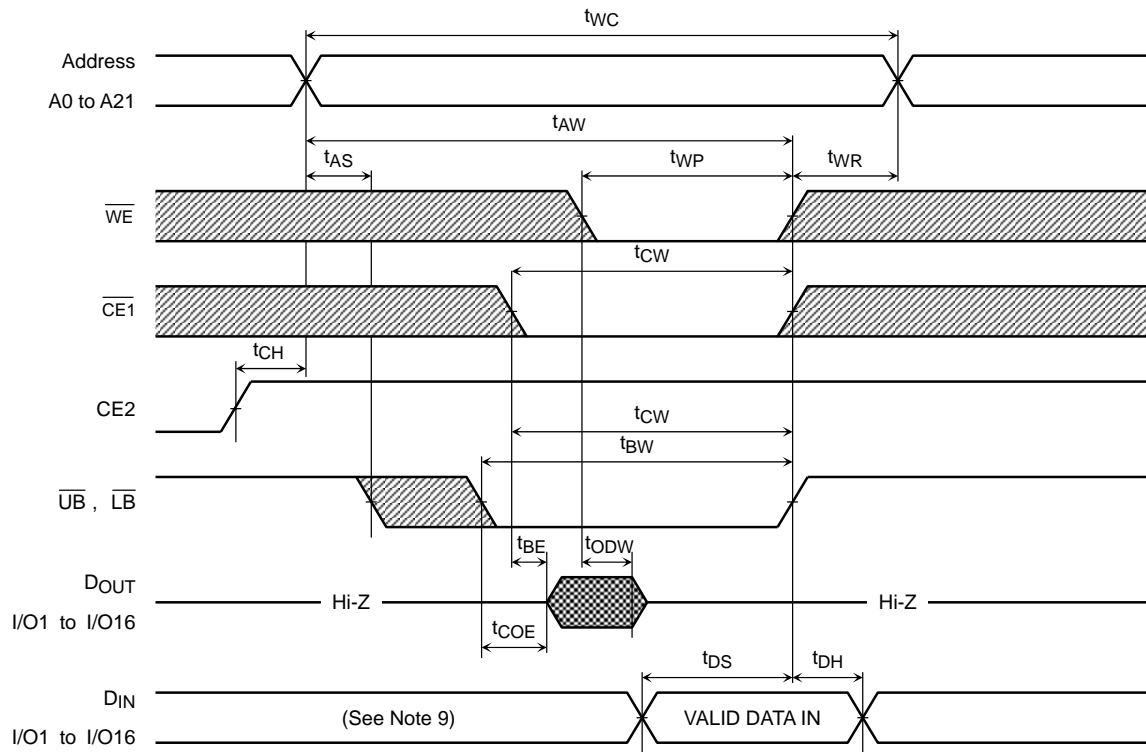
WRITE CYCLE 1 (\overline{WE} CONTROLLED) (See Note 8)



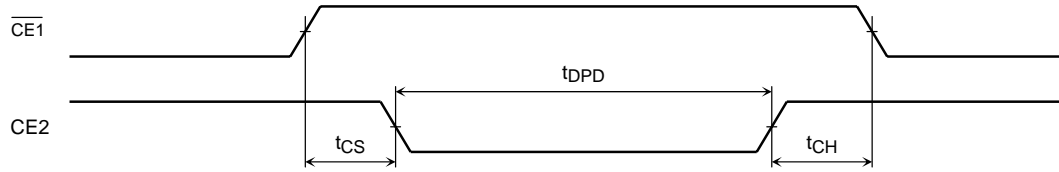
WRITE CYCLE 2 (\overline{CE} CONTROLLED) (See Note 8)



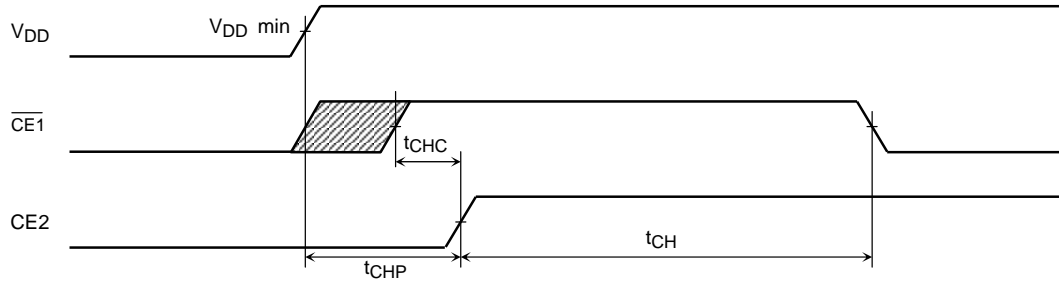
WRITE CYCLE 3 (\overline{UB} , \overline{LB} CONTROLLED) (See Note 8)



Deep Power-down Timing



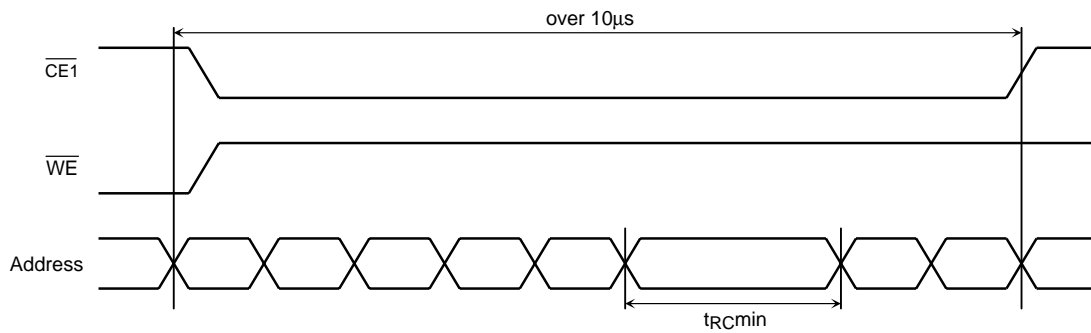
Power-on Timing



Provisions of Address Skew

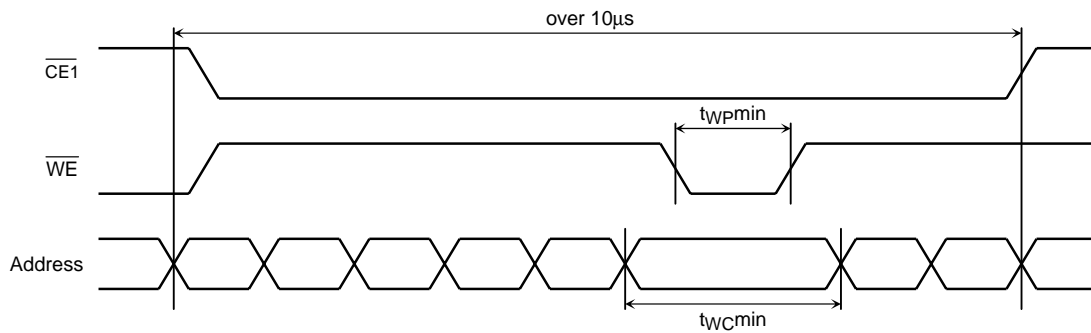
Read

In case, multiple invalid address cycles shorter than t_{RCmin} sustain over $10\mu s$ in a active status, as least one valid address cycle over t_{RCmin} must be needed during $10\mu s$.



Write

In case, multiple invalid address cycles shorter than t_{WCmin} sustain over $10\mu s$ in a active status, as least one valid address cycle over t_{WCmin} with t_{WPmin} must be needed during $10\mu s$.



Notes:

- (1) Stresses greater than listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
- (2) All voltages are reference to GND.
- (3) I_{DDO} depends on the cycle time.
- (4) I_{DDO} depends on output loading. Specified values are defined with the output open condition.
- (5) AC measurements are assumed $t_R, t_F = 5$ ns.
- (6) Parameters t_{OD}, t_{ODO}, t_{BD} and t_{ODW} define the time at which the output goes the open condition and are not output voltage reference levels.
- (7) Data cannot be retained at deep power-down stand-by mode.
- (8) If \overline{OE} is high during the write cycle, the outputs will remain at high impedance.
- (9) During the output state of I/O signals, input signals of reverse polarity must not be applied.
- (10) If $\overline{CE1}$ or $\overline{LB}/\overline{UB}$ goes LOW coincident with or after \overline{WE} goes LOW, the outputs will remain at high impedance.
- (11) If $\overline{CE1}$ or $\overline{LB}/\overline{UB}$ goes HIGH coincident with or before \overline{WE} goes HIGH, the outputs will remain at high impedance.

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