19-4058; Rev 0; 3/08

Digitally Programmable LCD Gamma Reference Generator with Digital Voltage Reference

General Description

The MAX5679 digitally programmable LCD gamma reference generator provides 18 buffered channels for biasing LCD column drivers. The device provides 14 outputs of 8-bit programmable gamma reference voltage derived from four externally applied reference voltages, and four buffered outputs of the same externally applied reference voltages. An I²C serial interface programs the 14 upper and lower range gamma buffer outputs independently.

The MAX5679 features a digitally programmable voltage reference (DVR) with 7-bit adjustable current sink to set the LCD common backplane (VCOM) voltage. The MAX5679 includes a power-on reset (POR) function that configures all 14 programmable gamma outputs to predetermined levels upon initial power-up.

The MAX5679 is available in a 5mm x 5mm, 32-pin TQFN package and is specified over the -40°C to +85°C extended temperature range.

Applications

TFT-LCD Panels for Flat Screen TVs

TFT-LCD Panels for Desktop Monitors

Features

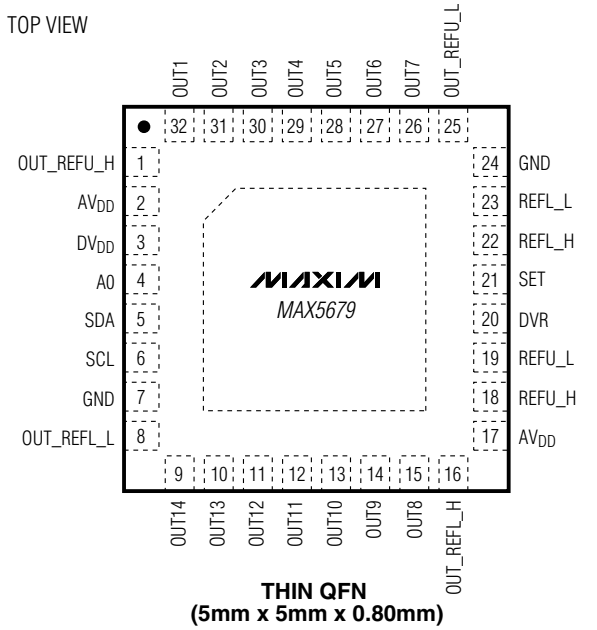
- **7-Bit Adjustable VCOM Calibrator (DVR)**
- **14 Programmable Gamma Outputs for LCD Column Driver ICs**
  - **8-Bit DAC Resolution for Upper and Lower Range Outputs**
  - **Maximum Output Swing of (AV_{DD} - 0.2V) (OUT1–OUT7)**
  - **Minimum Output Swing of (GND + 0.2V) (OUT8–OUT14)**
- **Four Independent Reference Inputs**
- **Four Independent Buffered Reference Outputs**
- **9V to 16.5V Analog Supply**
- **2V to 5.5V Digital Supply**
- **400kHz I²C-Compatible Serial Interface**
- **Pin-Selectable I²C Address Bit Allows Two Slave IDs**
- **Backward Compatible with the MAX5678**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX5679ETJ+	-40°C to +85°C	32 TQFN-EP* (5mm x 5mm)	T3255+4

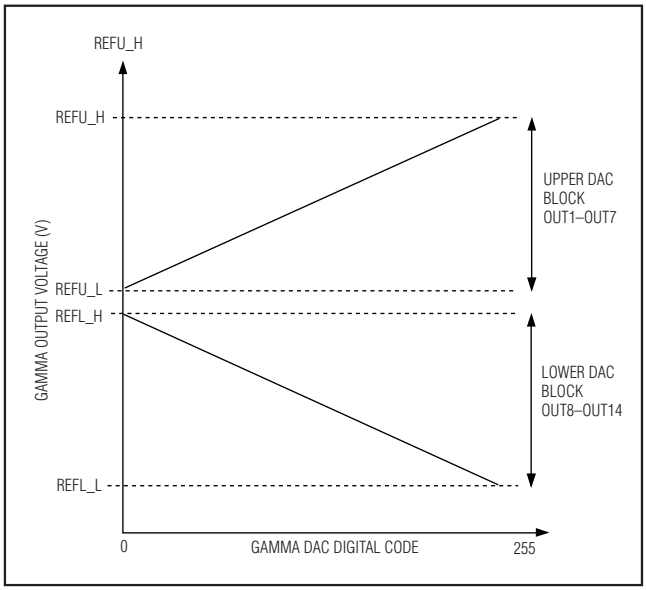
+Denotes a lead-free package.
**EP = Exposed pad.*

Pin Configuration



THIN QFN (5mm x 5mm x 0.80mm)

Gamma DAC Transfer Function



Functional Diagram appears at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Digitally Programmable LCD Gamma Reference Generator with Digital Voltage Reference

ABSOLUTE MAXIMUM RATINGS

AV_{DD} to GND .....-0.3V to +22V
DV_{DD} to GND .....-0.3V to +6.0V
SET to GND .....-0.3V to +6.0V
DVR to GND .....-0.3V to (AV_{DD} + 0.3V)
OUT_REF_ _ _, OUT_ to GND .....-0.3V to (AV_{DD} + 0.3V)
REF_ _ _ to GND .....-0.3V to (AV_{DD} + 0.3V)
SCL, SDA, A0 to GND .....-0.3V to (DV_{DD} + 0.3V)
Maximum Current Into Any Input .....±50mA
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Continuous Power Dissipation (T_A = +70°C)
32-Pin TQFN (derate 21mW/°C above +70°C) 1700mW
Lead temperature (soldering, 10s) .....+300°C
Junction Temperature .....+150°C
ESD Protection
SCL, SDA to GND, DV_{DD} (Human Body Model).....±4kV
All Other Pins (Human Body Model, JESD22-A114D).....±2kV

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{DD} = 9V to 16.5V, DV_{DD} = 2V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GAMMA OUTPUTS						
DAC Resolution			8			Bits
Differential Nonlinearity				±0.05	±1	LSB
Integral Nonlinearity					±2	LSB
Power-On Reset (POR) Gamma Codes		OUT1		246D		Decimal
		OUT2		148D		
		OUT3		118D		
		OUT4		87D		
		OUT5		67D		
		OUT6		55D		
		OUT7		7D		
		OUT8		7D		
		OUT9		55D		
		OUT10		67D		
		OUT11		87D		
		OUT12		118D		
		OUT13		148D		
		OUT14		246D		
Absolute Accuracy		(Note 2)		±13	±70	mV
Channel-to-Channel Matching		(Note 2)		±18	±70	mV
Gamma Output Voltage Range (Note 3)		OUTREFU_H, I_{OUT} = I10mAI	1/2 x AV_{DD} - 0.5		AV_{DD} - 0.2	V
		OUT1–OUT7, OUTREFU_L, I_{OUT} = I20mAI	1/2 x AV_{DD} + 0.5		AV_{DD} - 0.5	
		OUTREFL_L, I_{OUT} = I10mAI	GND + 0.2		1/2 x AV_{DD} + 0.5	
		OUTREFL_H, OUT8–OUT14, I_{OUT} = I20mAI	GND + 0.5		1/2 x AV_{DD} + 0.5	

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = 9V to 16.5V, DV_{DD} = 2V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Stability		R_S = 0Ω, no sustained oscillations		200		pF
Slew Rate	SR	OUT1–OUT14, REFU_L, REFL_H, no load		15		V/µs
		REFU_H, REFL_L, no load		10		
Load Regulation	V_{REG}	OUTREFU_H, I_{OUT} = ±10mA, V_{OUT} = AV_{DD} - 0.2V		±5		mV
		OUT1–OUT7, OUTREFU_L, I_{OUT} = ±20mA, V_{OUT} = AV_{DD} - 0.5V		±5		
		OUT7–OUT14, OUTREFL_H, I_{OUT} = ±20mA, V_{OUT} = GND + 0.5V		±5		
		OUTREFL_L, I_{OUT} = ±10mA, V_{OUT} = GND + 0.2V		±5		
Output Short-Circuit Current		OUT1–OUT14, $V_{OUT\_}$ = AV_{DD}/2		±200		mA
		OUTREFU_L, OUTREFL_H, OUTREFL_L, $V_{OUT\_\_}$ = AV_{DD}/2		±200		
		OUTREFU_H sourcing		200		
		OUTREFU_H sinking		20		
Gamma Output Load	R_L	Referenced to nominal DC output voltage		1000		Ω
Gamma Output Load Capacitance		Referenced to nominal DC output voltage		200		pF
		R_S = 5Ω (Note 4)		1		µF
REFU_H, REFU_L, REFL_H, REFL_L						
Input Voltage Range		REFU_H, REFU_L	AV_{DD}/2 + 0.5		AV_{DD}	V
		REFL_H, REFL_L	GND		AV_{DD}/2 + 0.5	
Input Resistance	R_{IN}	Measured from $V_{REF\_}$ to GND		3.3		MΩ
Input Current	I_{IN}	Measured from $V_{REF\_}$ to GND with $V_{REF\_\_}$ = +16.5V		5		µA
Reference Feedthrough Bandwidth	BW_{REF}	From any REF_ _ _ input to any reference or gamma output		40		kHz
VCOM CALIBRATOR (DVR)						
Power-On Reset VCOM Code					64	Decimal
Adjustment Steps		(Note 5)			125	Steps
SET Current		(Note 6)	20		250	µA
SET External Resistance (Note 6)		To GND, AV_{DD} = 16.5V		3.3		kΩ
		To GND, AV_{DD} = 9V		1.8		
SET Maximum External Capacitance				30		pF

Digitally Programmable LCD Gamma Reference Generator with Digital Voltage Reference

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = 9V to 16.5V, DV_{DD} = 2V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SET Differential Nonlinearity					±0.5	LSB
SET Zero-Scale Error				±2	±21	mV
V_{SET}/AV_{DD} Ratio		DAC at full scale		0.05		V/V
V_{SET}/AV_{DD} Ratio POR		At power-up		0.0254		V/V
DVR Compliance Range		DVR compliance measured at midscale	V_{SET} + 0.5		AV_{DD}	V
POWER SUPPLY						
Analog Supply Voltage	AV_{DD}	(Note 7)	9.0		16.5	V
AV_{DD} High-Voltage Stress		(Note 7)			20	V
Digital Supply Voltage	DV_{DD}		2.0	3.3	5.5	V
Analog Supply Current	I_S			12.5	18	mA
Digital Supply Current	I_{SD}			0.01	1	mA
DIGITAL INPUTS (A0, SDA, SCL)						
Input-Logic High Voltage	V_{IH}			0.7 x DV_{DD}		V
Input-Logic Low Voltage	V_{IL}			0.3 x DV_{DD}		V
Input Leakage Current	I_{IN}	V_{IN} = 0 or DV_{DD}		±0.1	±1	µA
Input Hysteresis	V_{HYST}			0.05 x DV_{DD}		V
Input Capacitance	C_{IN}			6		pF
SDA Output-Logic Low Voltage	V_{OL}	I_{SINK} = 3mA			0.4	V
SERIAL-INTERFACE TIMING						
Serial-Clock Frequency	f_{SCL}				400	kHz
Bus Free Time	t_{BUF}	Between STOP and START	1.3			µs
REPEATED START Hold Time	$t_{HD:STA}$	After this period, the first clock pulse is generated	0.6			µs
SCL Pulse-Width Low	t_{LOW}		1.3			µs
SCL Pulse-Width High	t_{HIGH}		0.6			µs
REPEATED START Setup Time	$t_{SU:STA}$		0.6			µs

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = 9V to 16.5V, DV_{DD} = 2V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Hold Time	$t_{HD;DAT}$		0		900	ns
Data Setup Time	$t_{SU;DAT}$		100			ns
SDA/SCL Receiving Rise Time	t_r		20 + Cb/10		300	ns
SDA/SCL Receiving Fall Time	t_f		20 + Cb/10		300	ns
SDA Transmitting Fall Time	t_f		20 + Cb/10		250	ns
STOP Setup Time	$t_{SU;STO}$		0.6			µs
Bus Capacitance	C_b	DV_{DD} = 2V to 2.7V	10		100	pF
		DV_{DD} = 2.7V to 5.5V	10		400	
Suppressed Spike Pulse Width	t_{sp}			50		ns

Note 1: Specifications at T_A = +85°C are guaranteed by production testing. Specifications at T_A = -40°C and T_A = +25°C are guaranteed by design and characterization.

Note 2: Error from the ideal output defined by the transfer function in the *Gamma DAC Transfer Functions* section.

Note 3: Due to power dissipation limits, not all outputs can source/sink I_{OUT} (max) simultaneously.

Note 4: R_S is a series resistor between the amplifier output and C_L. The amplifier should be stable under this condition.

Note 5: The lower three codes, 0–2, are hardwired to give the same value as code two. This eliminates a zero-current condition in the DVR output.

Note 6: Keep the minimum current into DVR > 10µA, and maximum current into DVR < 250µA over all codes.

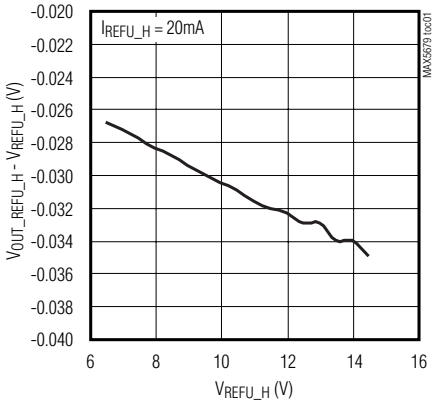
Note 7: AV_{DD} > 20V is a stress test. Functionality and spec compliance not guaranteed above 16.5V.

Digitally Programmable LCD Gamma Reference Generator with Digital Voltage Reference

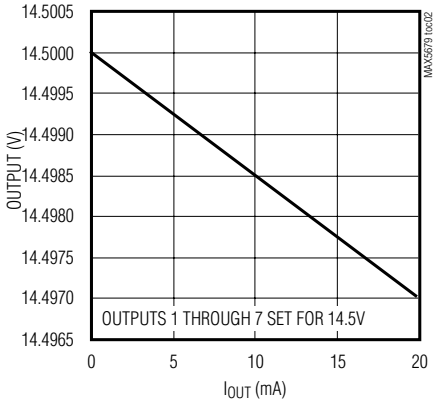
Typical Operating Characteristics

(AV_{DD} = +16.5V, DV_{DD} = +3.3V, performance of the *Typical Operating Circuit*, T_A = +25°C, unless otherwise noted.)

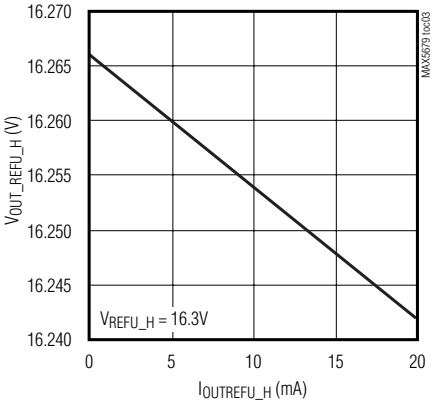
OUT_REFU_H OFFSET



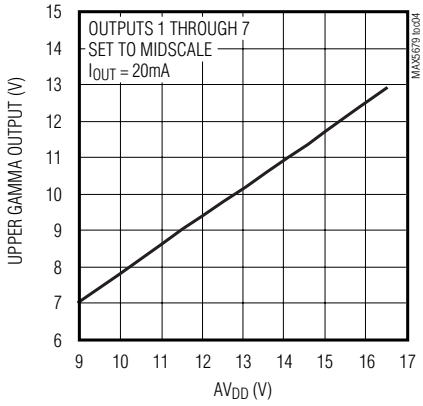
UPPER GAMMA LOAD REGULATION



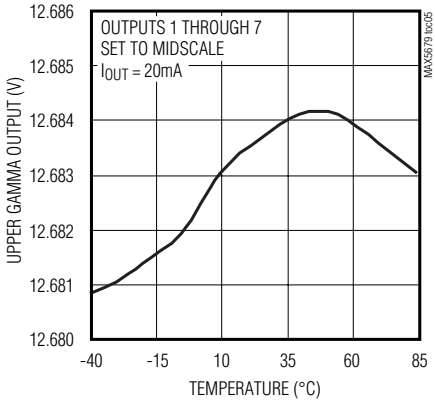
OUT_REFU_H LOAD REGULATION



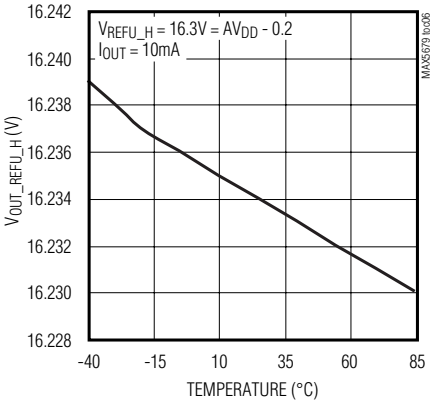
UPPER GAMMA OUTPUT vs. AV_{DD}



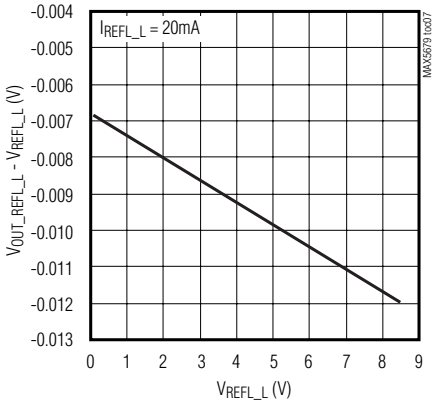
UPPER GAMMA OUTPUT vs. TEMPERATURE



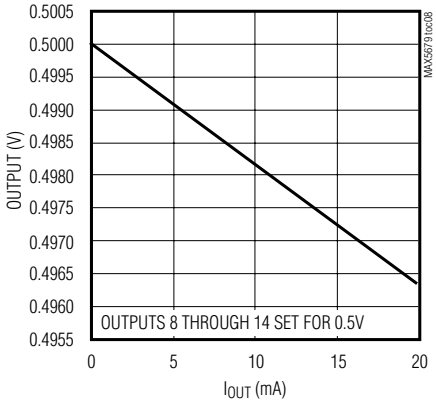
OUT_REFU_H vs. TEMPERATURE



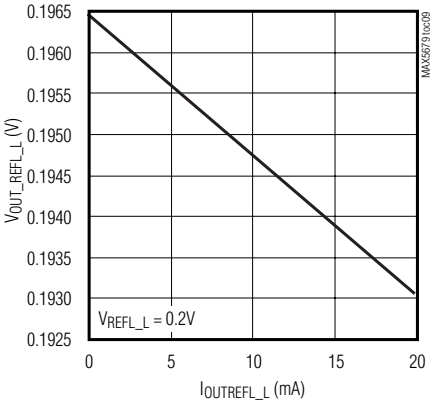
OUT_REFL_L OFFSET



LOWER GAMMA LOAD REGULATION



OUT_REFL_L LOAD REGULATION

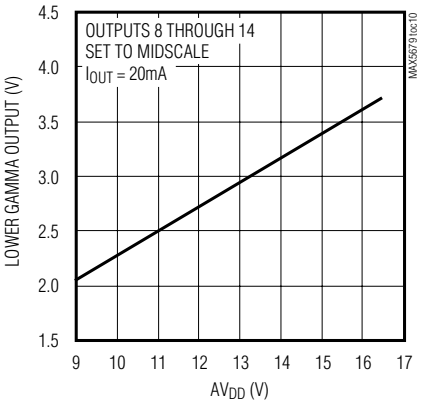


Digitally Programmable LCD Gamma Reference Generator with Digital Voltage Reference

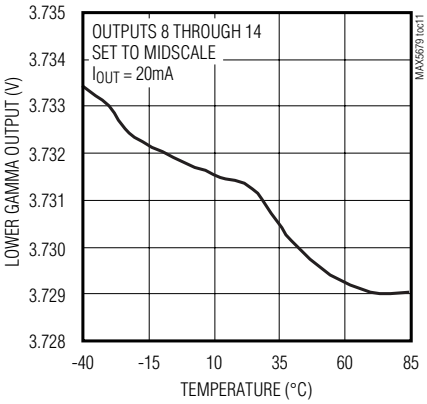
Typical Operating Characteristics (continued)

(AV_{DD} = +16.5V, DV_{DD} = +3.3V, performance of the *Typical Operating Circuit*, T_A = +25°C, unless otherwise noted.)

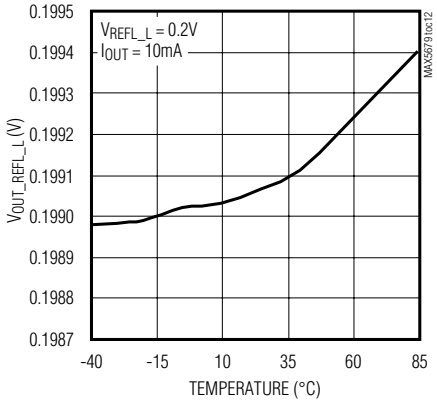
LOWER GAMMA OUTPUT vs. ANALOG SUPPLY VOLTAGE



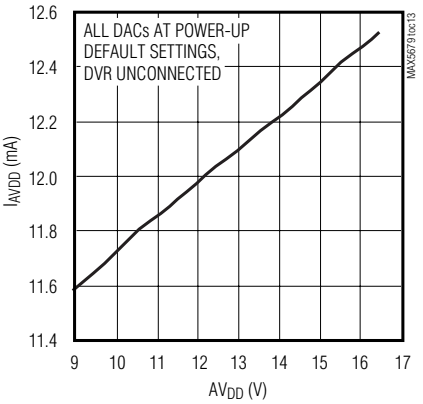
LOWER GAMMA OUTPUT vs. TEMPERATURE



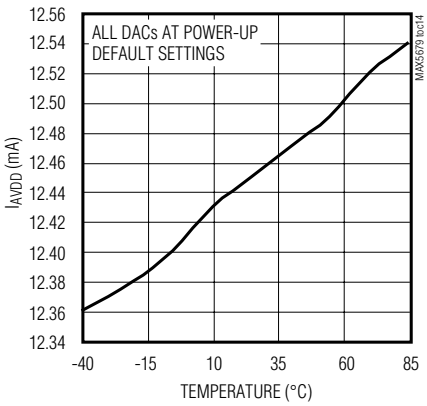
OUT_REFL_L vs. TEMPERATURE



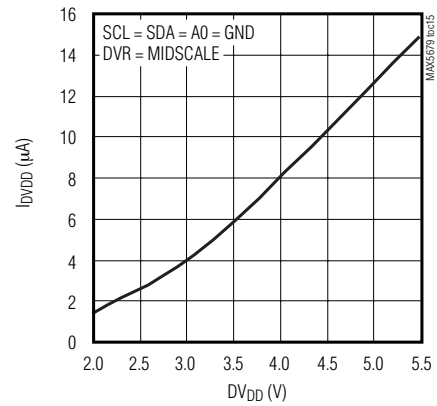
ANALOG SUPPLY CURRENT vs. ANALOG SUPPLY VOLTAGE



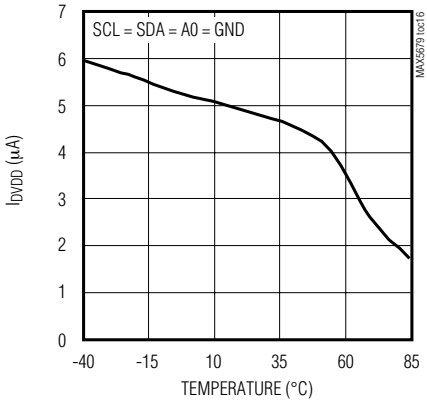
ANALOG SUPPLY CURRENT vs. TEMPERATURE



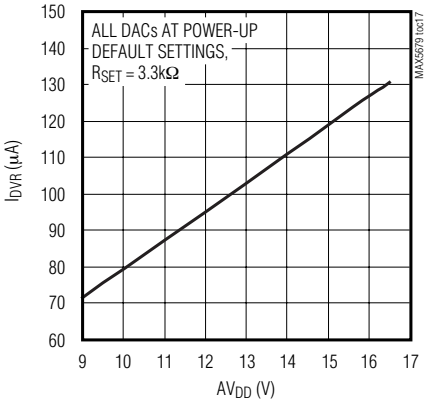
DIGITAL SUPPLY CURRENT vs. DIGITAL SUPPLY VOLTAGE



DIGITAL SUPPLY CURRENT vs. TEMPERATURE



DVR CURRENT vs. ANALOG SUPPLY VOLTAGE



Digitally Programmable LCD Gamma Reference Generator with Digital Voltage Reference

Pin Description

PIN	NAME	FUNCTION
1	OUT_REFU_H	Analog Output. Upper gamma reference high output.
2, 17	AV_{DD}	Analog Power Supply
3	DV_{DD}	Digital Power Supply
4	A0	Address Bit 0
5	SDA	Serial-Data Input
6	SCL	Serial-Clock Input
7, 24	GND	Ground
8	OUT_REFL_L	Lower Gamma Reference Low Output
9	OUT14	Gamma Reference 14 Output
10	OUT13	Gamma Reference 13 Output
11	OUT12	Gamma Reference 12 Output
12	OUT11	Gamma Reference 11 Output
13	OUT10	Gamma Reference 10 Output
14	OUT9	Gamma Reference 9 Output
15	OUT8	Gamma Reference 8 Output
16	OUT_REFL_H	Lower Gamma Reference High Output
18	REFU_H	Upper Reference High Input
19	REFU_L	Upper Reference Low Input
20	DVR	Sink Current Output
21	SET	Sink Current Set
22	REFL_H	Lower Reference High Input
23	REFL_L	Lower Reference Low Input
25	OUT_REFU_L	Upper Gamma Reference Low Output
26	OUT7	Gamma Reference 7 Output
27	OUT6	Gamma Reference 6 Output
28	OUT5	Gamma Reference 5 Output
29	OUT4	Gamma Reference 4 Output
30	OUT3	Gamma Reference 3 Output
31	OUT2	Gamma Reference 2 Output
32	OUT1	Gamma Reference 1 Output
—	EP	Exposed Pad. Internally connected to GND. Connect to large ground plane for maximum thermal dissipation. Do not use as primary ground connection.

Digitally Programmable LCD Gamma Reference Generator with Digital Voltage Reference

Detailed Description

The MAX5679 provides 18 buffered outputs for biasing LCD column drivers. Fourteen outputs are 8-bit programmable voltages derived from four externally applied reference voltages, and four are buffered outputs of the externally applied reference voltages. Additionally, the MAX5679 features a DVR, using a 7-bit adjustable current sink to set the VCOM voltage.

The MAX5679 includes a POR function that configures all programmable outputs to predetermined levels upon initial power-up. See the *Power-On Reset* section for more information.

An I^2C serial interface programs the internal DACs to set the 14 upper/lower range gamma buffer outputs and DVR's sink current.

I^2C Serial Interface

The MAX5679 operates as an I^2C slave device that sends and receives data through an I^2C-compatible 2-wire interface. The interface uses a serial-data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the MAX5679 and generates the SCL clock that synchronizes the data transfer (Figure 1). A slave issues an acknowledge bit after it recognizes its address and again after each data byte is read and recognized.

SDA operates as both an input and an open-drain output. Install a pullup resistor, R_P, between SDA and DV_{DD}. The value of R_P depends on the DV_{DD} supply voltage and bus capacitance. SCL operates only as an input. Install a pullup resistor, R_{PC}, on SCL if there are multiple masters on the 2-wire interface, or if the master

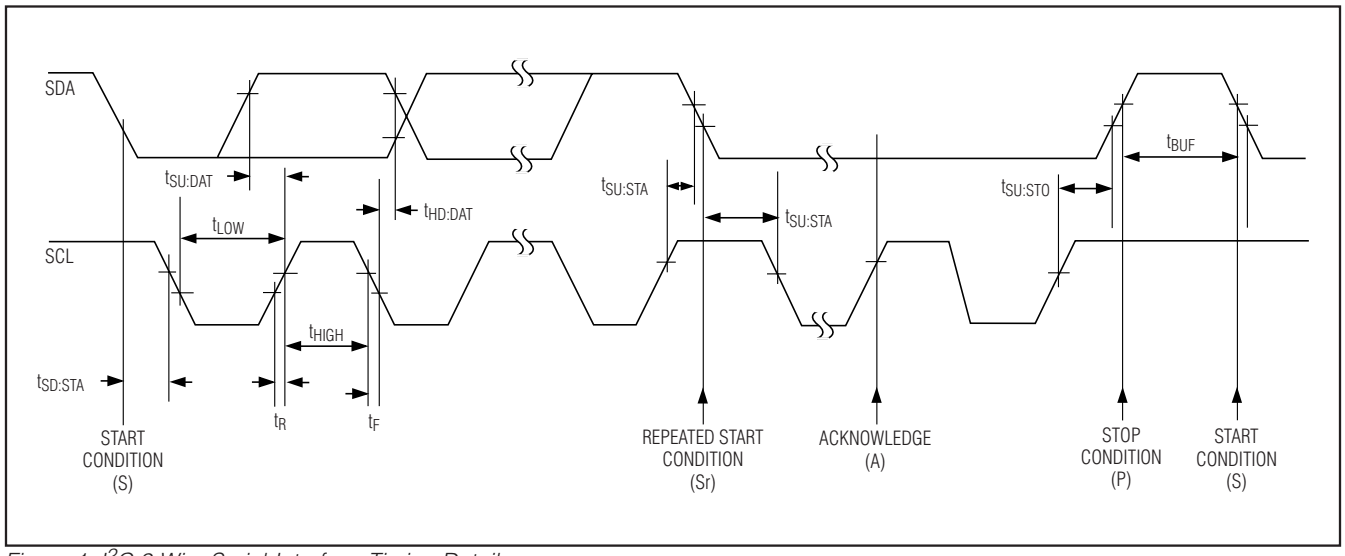


Figure 1. I^2C 2-Wire Serial-Interface Timing Details

Digitally Programmable LCD Gamma Reference Generator with Digital Voltage Reference

in a single-master system has an open-drain SCL output. Each communication with the MAX5679 contains a START (S) condition sent by a master, the 7-bit MAX5679 slave address plus a read/write (R/W) bit, an acknowledge bit, a series of data bytes each followed by an acknowledge bit, and finally a STOP (P) condition. Figure 2 shows how each communication is framed by START and STOP conditions.

START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission (Figure 1).

Early STOP Conditions

The MAX5679 recognizes a STOP condition at any point in a transmission even when the STOP condition occurs in the same SCL high pulse as the START condition (Figure 3).

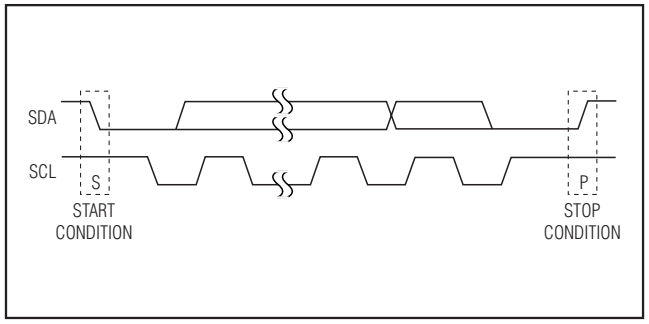


Figure 2. START and STOP Conditions

REPEATED START (Sr) Conditions

A REPEATED START (Sr) condition on the bus is when a START condition occurs without a prior STOP condition. An Sr condition terminates any previous operation on the bus, and should be followed by the slave address, which starts a new session. Usually Sr is issued after the acknowledge bit. Issuing Sr in between acknowledge bits prevents completion of the ongoing byte transmission.

Bit Transfer

One data bit is transferred during each clock pulse. The data on SDA must remain stable while SCL is high (Figure 4).

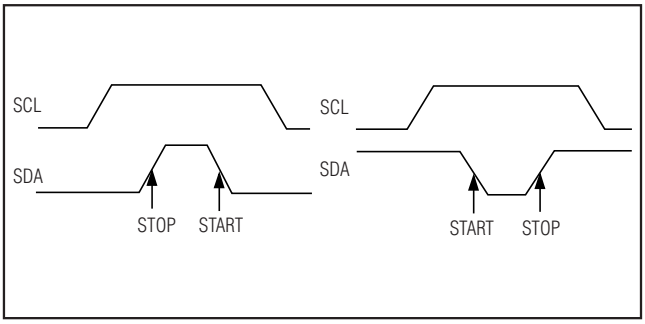


Figure 3. Valid START/STOP Conditions

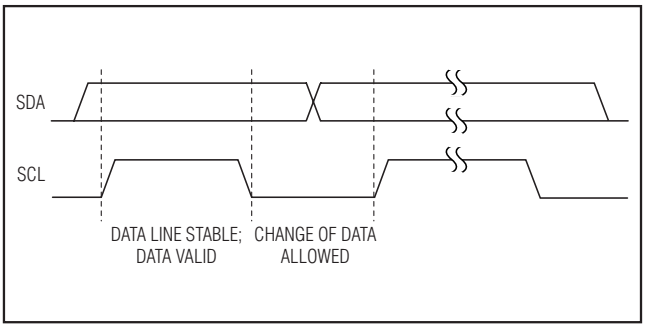


Figure 4. Bit Transfer

Digitally Programmable LCD Gamma Reference Generator with Digital Voltage Reference

Acknowledge

The acknowledge bit is a clocked 9th bit that the recipient uses to signal the receipt of its address and each byte of data (Figure 5). Each byte transferred thus effectively requires nine clock pulses. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, ensuring the SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX5679, the device generates the acknowledge bit because the MAX5679 is the recipient. When the MAX5679 is transmitting to the master, the master generates the acknowledge bit because the master is the recipient. If the master fails to provide an acknowledge bit during a read from the MAX5679, the MAX5679 interface ceases to provide data and waits for a new START condition and a valid address. Not acknowledging by the master is a legitimate way to terminate reading from the MAX5679; no STOP condition is necessary afterwards.

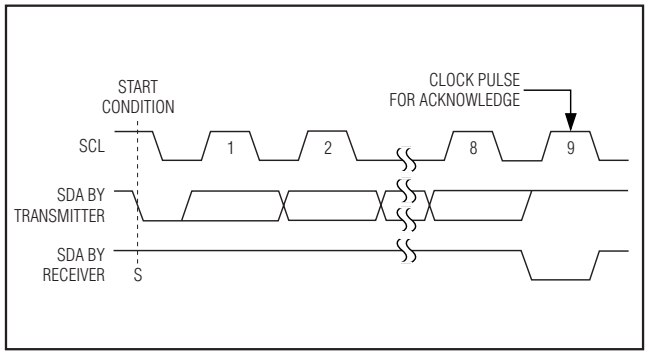


Figure 5. Acknowledge

I²C Compatibility

The MAX5679 is fully compatible with existing I²C systems. The interface supports both standard (100kHz) and fast (400kHz) data-transfer modes. The MAX5679 does not respond to a general call address.

Slave Address

The MAX5679 has a 7-bit long slave address (Table 1). The 8th bit following the 7-bit slave address is the R/$\overline{W}$ bit. The R/$\overline{W}$ bit is low for a write command or high for a read command.

Bits B7 through B2 of the MAX5679 slave address are set to 111010. Address input, A0, controls the slave address bit, B1. Connect A0 to DV_{DD} or GND. The MAX5679 provides two possible slave addresses (Table 1). An interface can control two MAX5679 devices independently.

The address input A0 can be driven dynamically. Ensure that the bit value is stable in the address sequence. The MAX5679 interface compares each address value bit-by-bit to allow the interface to power down in the event of a bus cycle that does not address the MAX5679.

Write Data Format

Send a START condition followed by the 7-bit slave address of the device with the R/$\overline{W}$ bit reset to 0 and one or more data bytes to initiate a write command. The MAX5679 supports two timing modes referred to as

Table 1. Slave Address

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	0	1	0	A0	R/$\overline{W}$

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mode 1 and mode 2. See Figures 6a and 6b. In mode 1, the data received by the MAX5679 consists of 9 bytes defined as follows: slave address, DVR data, and gamma 1 data though gamma 7 data. The DVR data is stored in the DVR DAC register, while the gamma data is stored in the gamma DAC registers as defined in Table 2a. A STOP condition after gamma 7 data is received determines the mode to be mode 1 (MAX5678 compatible mode).

If no STOP condition is detected after gamma 7 data and additional data are received, the mode is determined to be mode 2. In mode 2, additional data is sent in the form of gamma 8 data through gamma 14 data. After the gamma 14 data is received a STOP condition should be asserted by the master. The data received after gamma 7 data (i.e. gamma 8 data through gamma 14 data) is stored in the gamma DAC registers according to Table 2b.

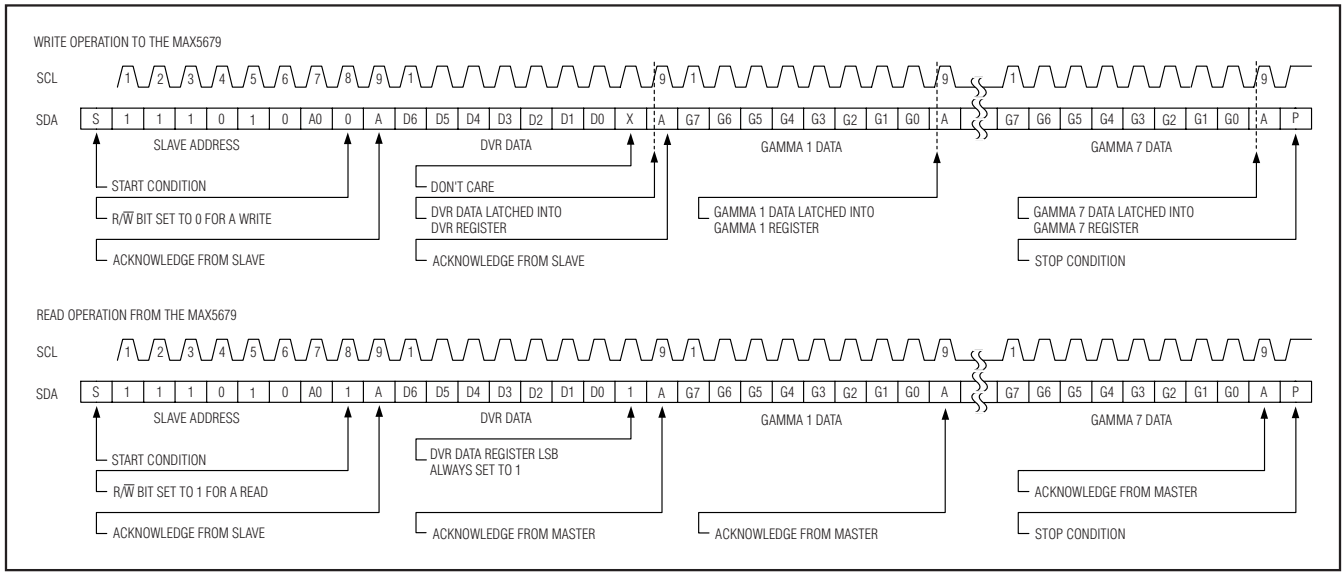

Figure 6a. Mode 1 (MAX5678 Compatible Mode)

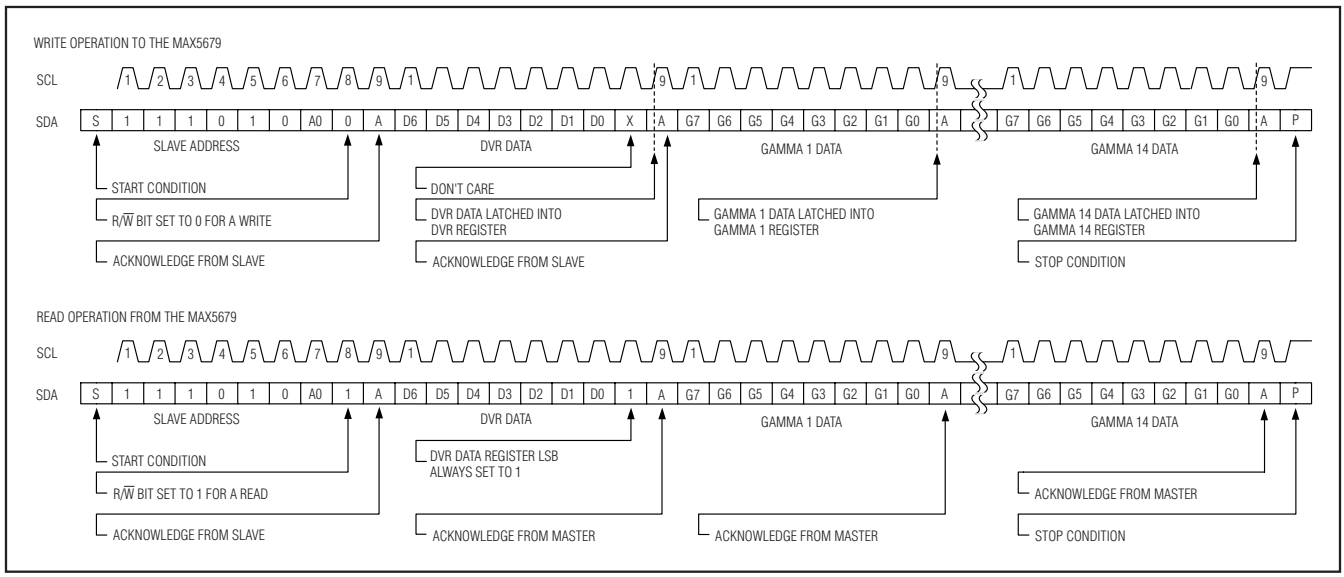

Figure 6b. Mode 2

Table 2a. Mode 1 (MAX5678 Compatible Mode)

GAMMA DATA BYTE	WRITE OPERATION REGISTER		READ OPERATION REGISTER READ
1	Register 1	Register 14	Register 1
2	Register 2	Register 13	Register 2
3	Register 3	Register 12	Register 3
4	Register 4	Register 11	Register 4
5	Register 5	Register 10	Register 5
6	Register 6	Register 9	Register 6
7	Register 7	Register 8	Register 7

Table 2b. Mode 2

GAMMA REGISTER BYTE	WRITE OPERATION REGISTER DATA STORED	READ OPERATION REGISTER DATA READ
1	Data 1	Data 1
2	Data 2	Data 2
3	Data 3	Data 3
4	Data 4	Data 4
5	Data 5	Data 5
6	Data 6	Data 6
7	Data 7	Data 7
8	Data 8	Data 8
9	Data 9	Data 9
10	Data 10	Data 10
11	Data 11	Data 11
12	Data 12	Data 12
13	Data 13	Data 13
14	Data 14	Data 14

Read Data Format

Send a START condition followed by the 7-bit slave address of the device with the R/$\overline{W}$ bit set to 1 to initiate a read command to the MAX5679. The MAX5679 then sequentially outputs 8 bytes of data if operating in mode 1 or 15 bytes if in mode 2 that correspond to the values stored in its internal registers. The first data byte represents the contents of the DVR register. The following 7 or 14 bytes of data represent the gamma DAC settings.

DVR Register

The DVR register stores the 1st data byte transmitted to the MAX5679 following a START condition and the device slave address when a write operation is performed (Figures 6a and 6b). The DVR register sets the code for the DVR DAC and controls the operation of the SET and DVR outputs. The DVR DAC is a 7-bit DAC with the least significant bit (LSB) of this register as a don't-care bit (Table 3). When performing a read from the MAX5679, the DVR register data is the first byte to be output by the device following a START condition and the slave address. A read from the DVR register always returns an LSB value of 1.

Gamma Register

The MAX5679 includes a total of 14 gamma registers that store the digital codes for the gamma DACs, which control outputs OUT1–OUT14. When writing to the MAX5679, the first data byte transmitted after the DVR data is stored in the first gamma register and subsequent bytes of data are stored in the remaining gamma registers until either seven or all 14 have been written, depending on the mode (Tables 2a and 2b). Each gamma register controls an upper and a lower DAC output. The upper and lower DACs share the same digital code in mode 1. See the *Gamma DAC Transfer Functions* section. When a read from the MAX5679 is performed, the contents of the gamma registers are output sequentially after the DVR register data (Figures 6a and 6b). If the MAX5679 is operating in mode 1, issue a stop condition after receiving the 7th gamma byte. If the device is operating in mode 2, issue a stop condition after receiving the 14th gamma byte.

Register Update

The registers of the MAX5679 are updated on the rising edge of SCL during the acknowledge bit. All bus cycles require each 8-bit byte to be followed by an acknowledge bit. If a write sequence is aborted before its respective acknowledge bit, the data values are not updated and the MAX5679 waits for a new START condition and a valid slave address. For the MAX5679, a write operation from the master may contain additional data beyond what is required to program all the internal registers. In this situation, the MAX5679 ignores any data beyond the 15th data byte (DVR plus 14 gamma bytes). The MAX5679 also accepts write commands with fewer than 8 bytes. In this case, the number of registers that are updated corresponds to the number of bytes sent. If there are more registers than bytes sent, the remaining registers contain their previous values. If multiple write operations are performed by the master, each operation is performed on the MAX5679 data registers as requested.

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Power-On Reset

On power-up, all internal registers of the MAX5679 (DVR register and 14 gamma registers) are initiated to a preset series of values (Table 3). Use the I²C interface to overwrite these values at any point after initial power-up.

Applications Information

Digital Variable Reference (DVR)

DVR sinks a programmable current set by an internal 7-bit DAC from an external resistive voltage-divider. The DAC is ratiometric relative to AV_{DD} and monotonic over all operating conditions. The combination of the resistive voltage-divider (R1 and R2), the external SET resistor (R_{SET}), and the AV_{DD} supply determine the maximum and minimum values of the DVR output (Figure 7).

DVR DAC Transfer Function and Offset

An I²C interface controls the DVR 7-bit DAC through the DVR register. The DVR DAC determines the voltage at SET as well as the current that DVR can sink. Figure 7 shows the transfer function of the DVR DAC. Calculate the voltage at SET with the following sequation:

$$V_{SET} = \left\{\frac{DVR\_Code + 1}{128}\right\} \times \left(\frac{AV_{DD}}{20}\right)$$

where DVR_Code is any integer from 0 to 127. The DVR DAC provides two codes of offset by making the first three DVR codes correspond to the same SET voltage (Figure 8). DVR codes 0, 1, and 2 yield the same output voltage as if DVR code 2 is written to the DVR DAC. The previous equation is valid for codes 2 to 127. For DVR codes 0 to 2, calculate SET voltage with the following equation:

$$V_{SET} = \left\{\frac{3}{128}\right\} \times \left(\frac{AV_{DD}}{20}\right)$$

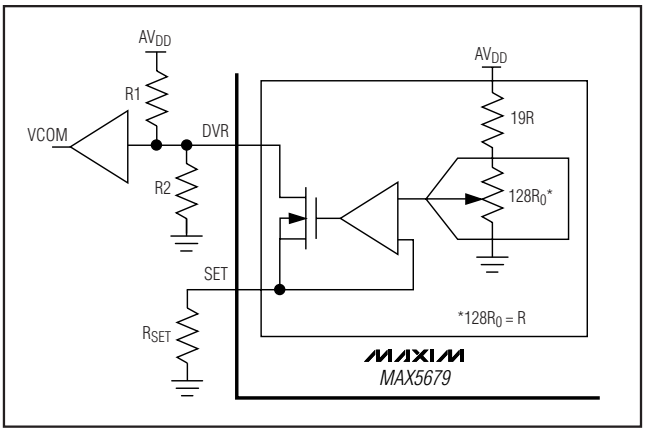

Figure 7. DVR Circuit

Table 3. Power-On Reset Values

REGISTER	OUTPUT	POWER-ON RESET VALUE								
		B7	B6	B5	B4	B3	B2	B1	B0	DECIMAL VALUE
DVR	SET/DVR	1	0	0	0	0	0	0	X	64
Gamma 1	OUT1	1	1	1	1	0	1	1	0	246
Gamma 2	OUT2	1	0	0	1	0	1	0	0	148
Gamma 3	OUT3	0	1	1	1	0	1	1	0	118
Gamma 4	OUT4	0	1	0	1	0	1	1	1	87
Gamma 5	OUT5	0	1	0	0	0	0	1	1	67
Gamma 6	OUT6	0	0	1	1	0	1	1	1	55
Gamma 7	OUT7	0	0	0	0	0	1	1	1	7
Gamma 8	OUT8	0	0	0	0	0	1	1	1	7
Gamma 9	OUT9	0	0	1	1	0	1	1	1	55
Gamma 10	OUT10	0	1	0	0	0	0	1	1	67
Gamma 11	OUT11	0	1	0	1	0	1	1	1	87
Gamma 12	OUT12	0	1	1	1	0	1	1	0	118
Gamma 13	OUT13	1	0	0	1	0	1	0	0	148
Gamma 14	OUT14	1	1	1	1	0	1	1	0	246

X = Don't care.

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Setting the DVR Adjustment Range (R_{SET})

An external resistive divider (R1 and R2) in conjuction with R_{SET}, set DVR's adjustment range (Figure 7). The value of R_{SET} controls the range of currents (I_{DVR}) that DVR can sink. Large R_{SET} values decrease LSB size and decrease DVR's adjustment range. Calculate R1, R2, and R_{SET} using the following procedure:

1) Choose the maximum DVR output level (V_{MAX}), the minimum DVR output level (V_{MIN}), and the AV_{DD} supply voltage (AV_{DD}).

2) Calculate the R1/R2 ratio:

$$\frac{R1}{R2} = \left\{\frac{AV_{DD}}{V_{MAX}}\right\} - 1$$

3) Calculate the R1/R_{SET} ratio:

$$\frac{R1}{R_{SET}} = \left\{\frac{20 \times (V_{MAX} - V_{MIN})}{V_{MAX}}\right\}$$

4) Choose a R_{SET} of approximately the value shown in the *Electrical Characteristics* table and calculate the values for R1 and R2.

5) DVR's LSB size is:

$$LSB = \left\{\frac{V_{MAX} - V_{MIN}}{128}\right\}$$

After selecting the values of R1 and R2, calculate the DVR voltage and I_{DVR} with the following equations:

$$V_{DVR} = \left(\frac{R2}{R1 + R2}\right) \times \left\{1 - \left(\frac{DVR\_Code + 1}{128}\right) \times \left(\frac{R1}{20 \times R_{SET}}\right)\right\} \times AV_{DD}$$

$$I_{DVR} = \left\{\frac{V_{SET}}{R_{SET}}\right\}$$

Gamma DAC Transfer Functions

The MAX5679 contains two sets of gamma DAC blocks; an upper gamma DAC block and a lower gamma DAC block (see the *Functional Diagram*). Each DAC block comprises seven independent identical DACs that control seven independent outputs and each DAC block uses a seperate pair of reference inputs that determine its transfer function.

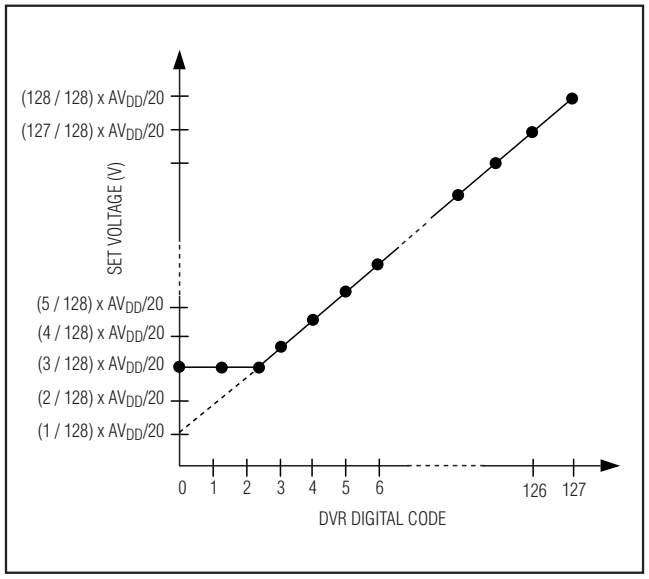


Figure 8. DVR DAC Transfer Function

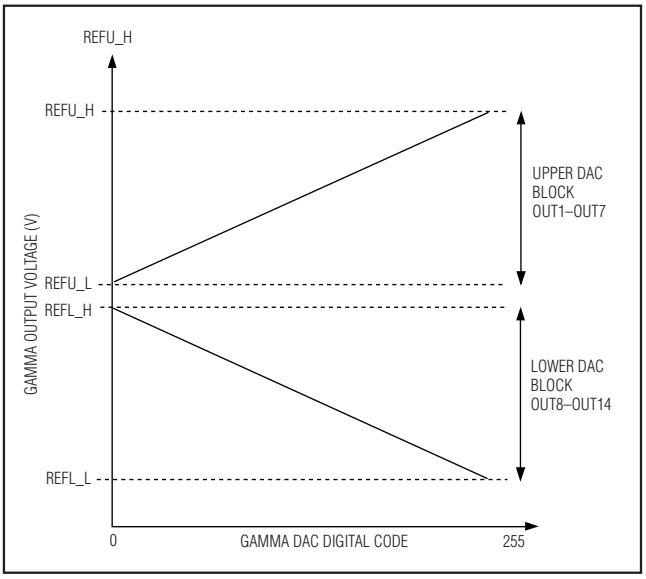


Figure 9. Gamma DAC Transfer Function

Digitally Programmable LCD Gamma Reference Generator with Digital Voltage Reference

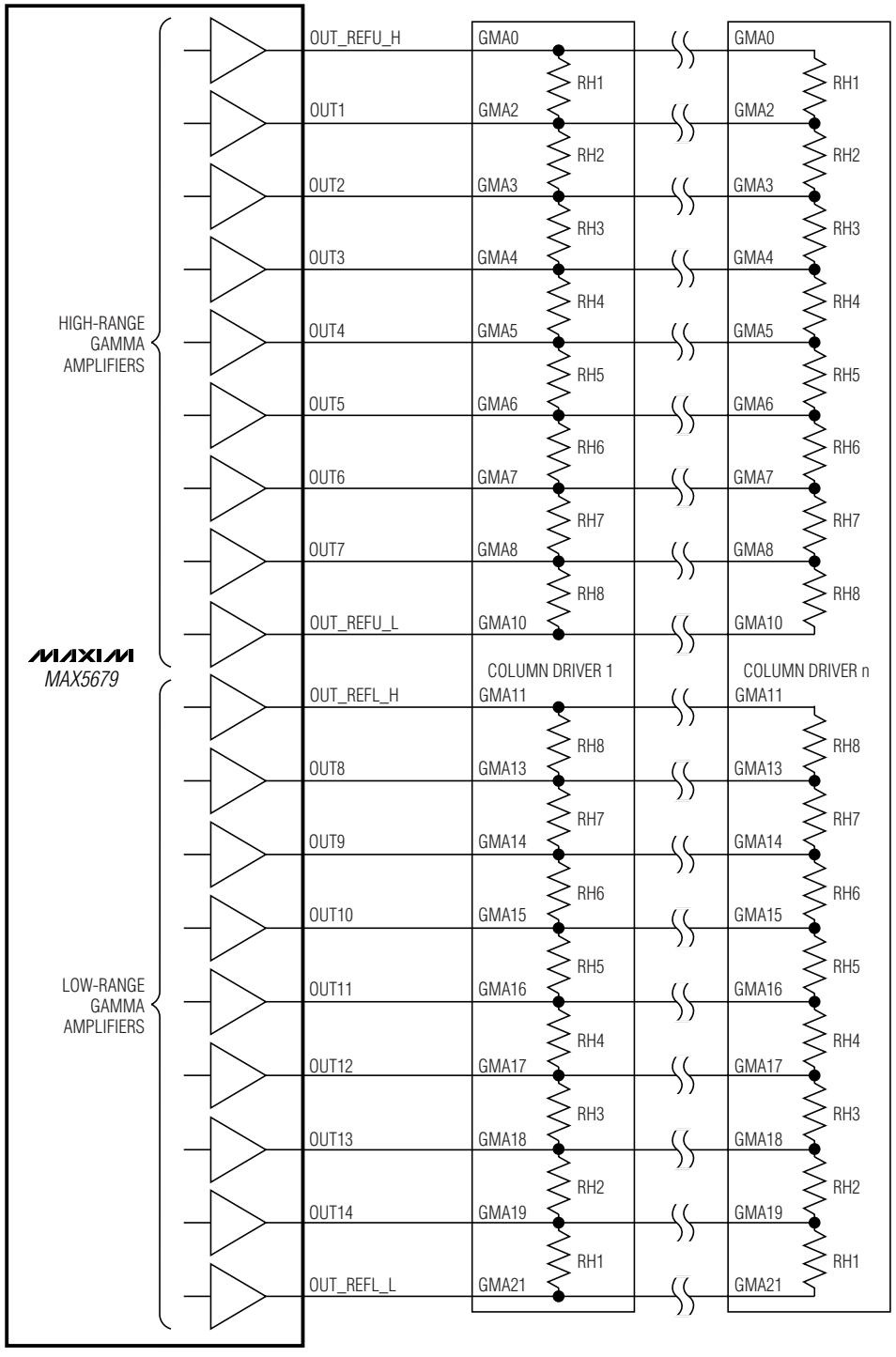


Figure 10. Typical LCD Application

Digitally Programmable LCD Gamma Reference Generator with Digital Voltage Reference

Upper Block DAC Transfer Function

The transfer function (see Figure 9) of each of the DACs in the upper DAC block (OUT1–OUT7) is:

$$V_{OUT\_} = V_{REFU\_L} + \left\{\frac{DAC\_Code}{256}\right\} \times \left(V_{REFU\_H} - V_{REFU\_L}\right)$$

where:

$V_{OUT\_}$ is the output voltage of the respective upper DAC (OUT1–OUT7).

The DAC code is the decimal equivalent of the code written to the gamma register that controls the respective output (see Table 2), 0 ≤ DAC_Code ≤ 255.

V_{REFU_H} is the high reference for the upper DACs.

V_{REFU_L} is the low reference for the upper DACs.

See Figure 10 for a typical LCD application and Figure 11 for a typical LCD gamma curve.

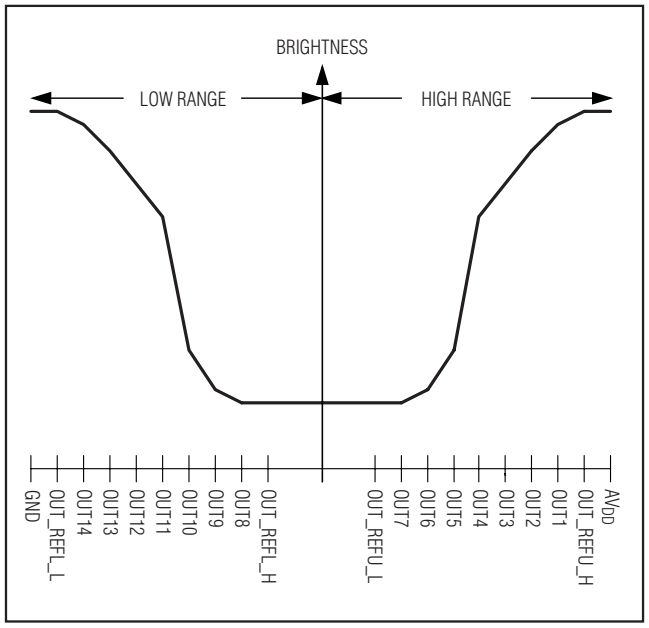


Figure 11. Typical LCD Gamma Curve

Lower Block DAC Transfer Function

The transfer function (see Figure 9) of each of the DACs in the lower DAC block (OUT8–OUT14) is:

$$V_{OUT\_} = V_{REFL\_H} - \left\{\frac{DAC\_Code}{256}\right\} \times \left(V_{REFL\_H} - V_{REFL\_L}\right)$$

where:

$V_{OUT\_}$ is the output voltage of the respective lower DAC (OUT8–OUT14).

The DAC code is the decimal equivalent of the code written to the gamma register that controls the respective output (see Table 2), 0 ≤ DAC code ≤ 255.

V_{REFL_H} is the high reference for the lower DACs.

V_{REFL_L} is the low reference for the lower DACs.

See Figure 10 for a typical LCD application and Figure 11 for a typical LCD gamma curve.

Layout Information

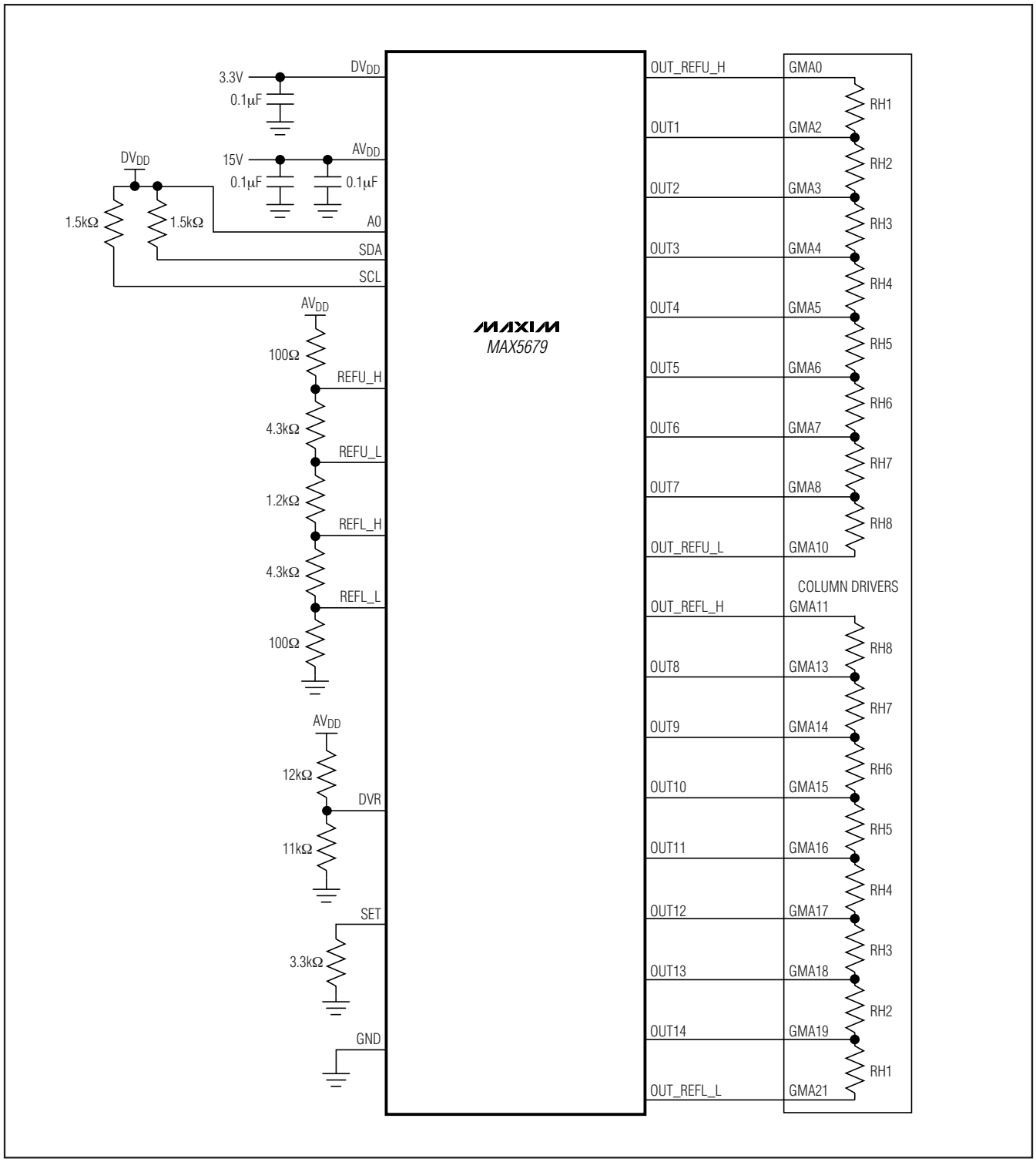
Place the resistor-divider close to the DVR output. Place R_{SET} close to SET. Use bypass capacitors on DV_{DD} and AV_{DD}. Keep all bypass capacitors close to the IC with short connections to the inputs.

Chip Information

PROCESS: BiCMOS

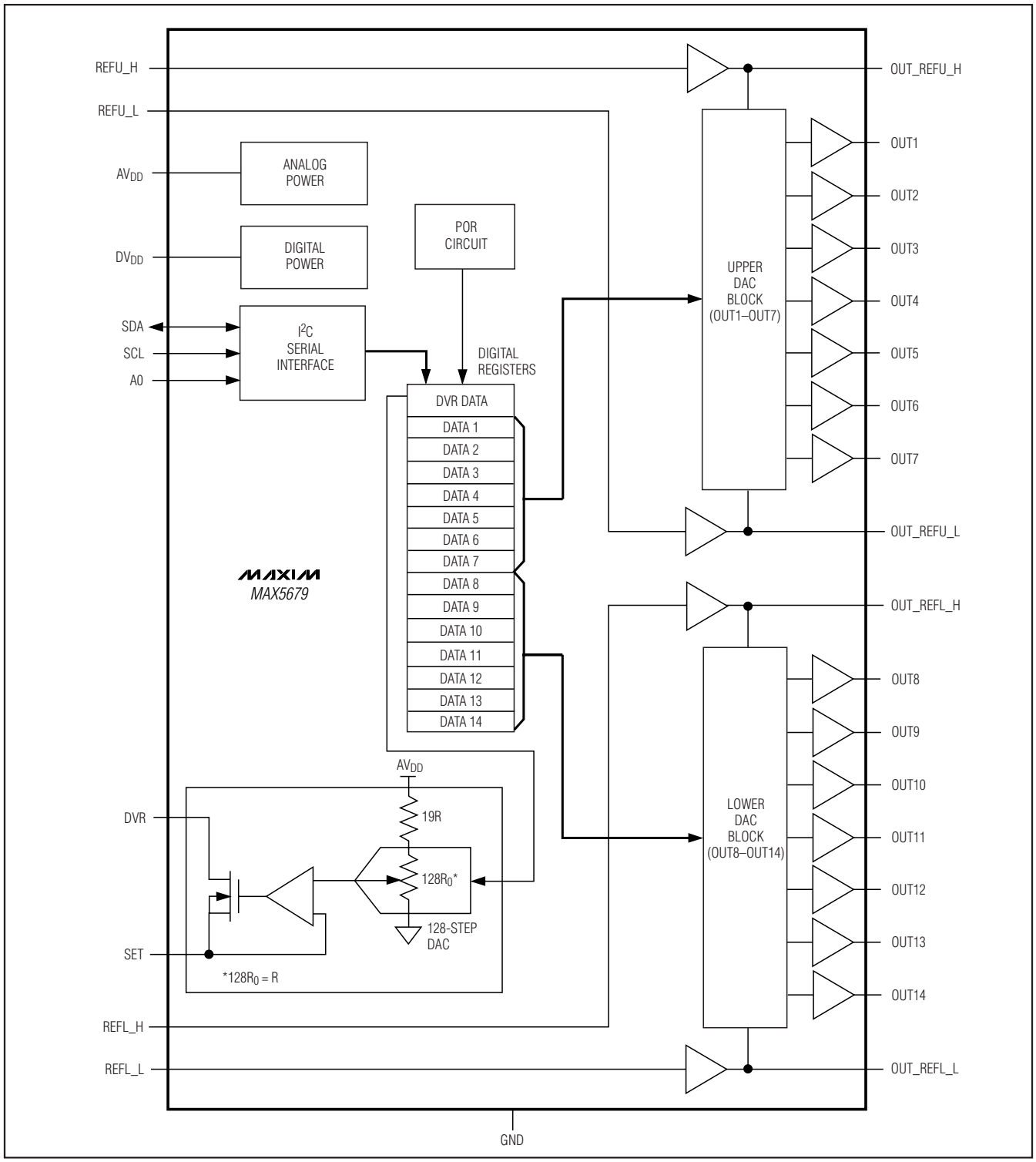
Digitally Programmable LCD Gamma Reference Generator with Digital Voltage Reference

Typical Operating Circuit



Digitally Programmable LCD Gamma Reference Generator with Digital Voltage Reference

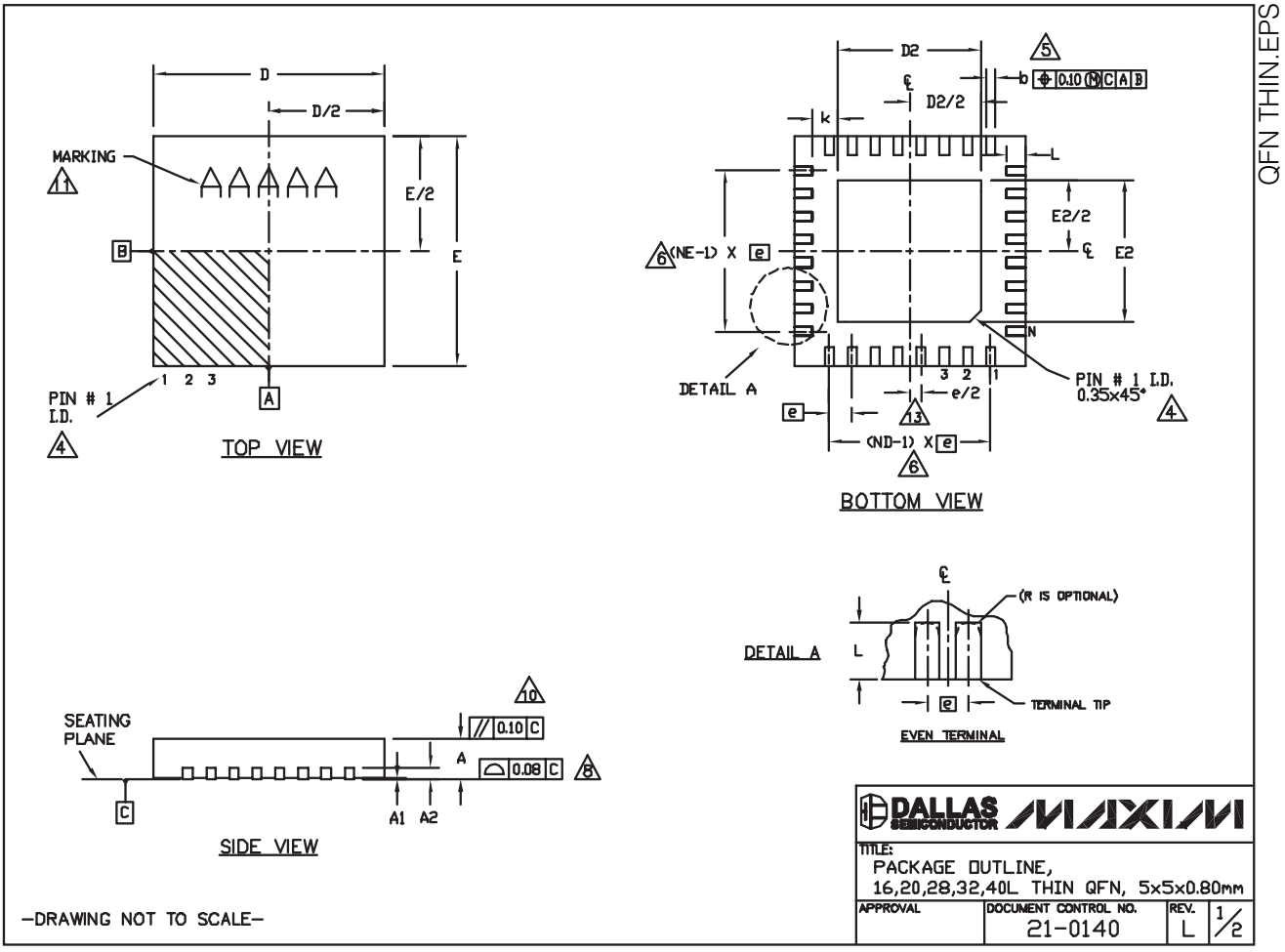
Functional Diagram



Digitally Programmable LCD Gamma Reference Generator with Digital Voltage Reference

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



Digitally Programmable LCD Gamma Reference Generator with Digital Voltage Reference

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS																
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5			
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25	
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.			
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50	
N	16			20			28			32			40			
ND	4			5			7			8			10			
NE	4			5			7			8			10			
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----			

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2055MN-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255M-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60
T4055MN-1	3.40	3.50	3.60	3.40	3.50	3.60

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
14. ALL DIMENSIONS APPLY TO BOTH LEADED AND PbFREE PARTS.

–DRAWING NOT TO SCALE–

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16,20,28,32,40L THIN QFN, 5x5x0.80mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	L	2/2