

NBXDDA016, NBXDDB016

3.3 V, 133.33 MHz /137.93 MHz Dual Frequency CML Clock Oscillator

The NBXDDB016/NBXDDA016 dual frequency crystal oscillator (XO) is designed to meet today's requirements for 3.3 V CML clock generation applications. The device uses a high Q fundamental crystal and Phase Lock Loop (PLL) multiplier to provide selectable 133.33 MHz or 137.93 MHz, ultra low jitter and phase noise CML differential output.

This device is a member of ON Semiconductor's PureEdge™ clock family that provides accurate and precision clock solutions.

Available in 5 mm x 7 mm SMD (CLCC) package on 16 mm tape and reel in quantities of 1,000. Frequency stability options available as either 50 PPM NBXDDB016 or 20 PPM NBXDDA016.

Features

- CML Differential Output
- Uses High Q Fundamental Mode Crystal and PLL Multiplier
- Ultra Low Jitter and Phase Noise - 0.4 ps (12 kHz - 20 MHz)
- Selectable Output Frequency - 133.33 MHz (default)/137.93 MHz
- Hermetically Sealed Ceramic SMD Package
- RoHS Compliant
- Operating Range 3.3 V \pm 10%
- Total Frequency Stability - \pm 20 PPM or \pm 50 PPM

Applications

- High-End Servers
- Basestation
- General Purpose Clock Generation and Margining

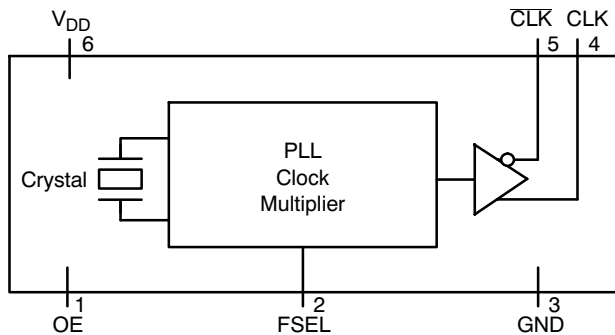
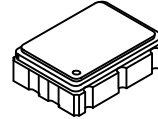


Figure 1. Simplified Logic Diagram



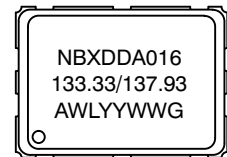
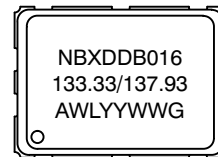
ON Semiconductor®

<http://onsemi.com>



6 PIN CLCC
LN SUFFIX
CASE 848AB

MARKING DIAGRAMS



NBXDDA016 = NBXDDA016 (\pm 50 PPM)
 NBXDDB016 = NBXDDB016 (\pm 20 PPM)
 133.33/137.93 = Output Frequency (MHz)
 A = Assembly Location
 WL = Wafer Lot
 YY = Year
 WW = Work Week
 G = Pb-Free Package

ORDERING INFORMATION

| Device | Package | Shipping† |
|------------------|------------------|----------------------|
| NBXDDB016LN1TAG* | CLCC-6 (Pb-Free) | 1000/ Tape & Reel |
| NBXDDA016LN1TAG | CLCC-6 (Pb-Free) | 1000/ Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

* Please contact sales office for availability

NBXDDA016, NBXDDDB016

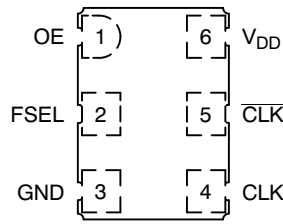


Figure 2. Pin Connections (Top View)

Table 1. PIN DESCRIPTION

| Pin No. | Symbol | I/O | Description |
|---------|-------------------------|-----------------------------|--|
| 1 | OE | LVTTTL/LVCMOS Control Input | Output Enable Pin. When left floating pin defaults to logic HIGH and output is active. See OE pin description Table 2. |
| 2 | FSEL | Control Input | Output Frequency Select Pin. Pin will default LOW when left open. See Output Frequency Select Table 3. |
| 3 | GND | Power Supply | Ground 0 V. |
| 4 | CLK | CML Output | Non-Inverted Clock Output. Typically loaded with 50 Ω receiver termination resistor to $V_{TT} = V_{DD}$. |
| 5 | $\overline{\text{CLK}}$ | CML Output | Inverted Clock Output. Typically loaded with 50 Ω receiver termination resistor to $V_{TT} = V_{DD}$. |
| 6 | V_{DD} | Power Supply | Positive power supply voltage. Voltage should not exceed 3.3 V \pm 10%. |

Table 2. OUTPUT ENABLE TRI-STATE FUNCTION

| OE Pin | Output Pins |
|------------|-------------|
| Open | Active |
| High Level | Active |
| Low Level | High Z |

Table 3. OUTPUT FREQUENCY SELECT

| FSEL Pin | Output Frequency (MHz) |
|------------------------------|------------------------|
| Open (pin will float Low) | 133.33 |
| High Level | 137.93 |
| Low Level | 133.33 |

Table 4. ATTRIBUTES

| Characteristic | Value |
|--|--|
| Input Default State Resistor | 170 k Ω |
| ESD Protection | Human Body Model Machine Model 2 kV 200 V |
| Meets or Exceeds JEDEC Standard EIA/JESD78 IC Latchup Test | |

1. For additional Moisture Sensitivity information, refer to Application Note AND8003/D.

Table 5. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Units |
|-----------|-----------------------------|--------------|-------------|-------------|--------------------|
| V_{DD} | Positive Power Supply | GND = 0 V | | 4.6 | V |
| T_A | Operating Temperature Range | | | -40 to +85 | $^{\circ}\text{C}$ |
| T_{stg} | Storage Temperature Range | | | -55 to +120 | $^{\circ}\text{C}$ |
| T_{sol} | Wave Solder | See Figure 6 | | 260 | $^{\circ}\text{C}$ |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NBXDDA016, NBXDDB016

Table 6. DC CHARACTERISTICS ($V_{DD} = 3.3\text{ V} \pm 10\%$, $GND = 0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$) (Note 2)

| Symbol | Characteristic | Conditions | Min. | Typ. | Max. | Units |
|-------------|-----------------------------------|------------|--------------|--------------|--------------|---------------|
| I_{DD} | Power Supply Current (Note 2) | | | 70 | 100 | mA |
| V_{IH} | OE Input HIGH Voltage | | 2000 | | V_{DD} | mV |
| V_{IL} | OE Input LOW Voltage | | $GND - 300$ | | 800 | mV |
| I_{IH} | Input HIGH Current | OE FSEL | -100 -100 | | +100 +100 | μA |
| I_{IL} | Input LOW Current | OE FSEL | -100 -100 | | +100 +100 | μA |
| V_{IH} | FSEL Input HIGH Voltage | | 2000 | | V_{DD} | mV |
| V_{IL} | FSEL Input LOW Voltage | | 0 | | 800 | mV |
| V_{OH} | Output HIGH Voltage (Note 2) | | $V_{DD}-40$ | | V_{DD} | mV |
| V_{OL} | Output LOW Voltage (Note 2) | | $V_{DD}-450$ | $V_{DD}-380$ | $V_{DD}-300$ | mV |
| V_{OUTPP} | Output Voltage Amplitude (Note 2) | | | 380 | | mV |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

2. Measurement taken with outputs terminated with 50 ohm to V_{DD} . See Figure 5.

NBXDDA016, NBXDDB016

Table 7. AC CHARACTERISTICS ($V_{DD} = 3.3\text{ V} \pm 10\%$, $GND = 0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$) (Note 3)

| Symbol | Characteristic | Conditions | Min. | Typ. | Max. | Units |
|--------------------------|---|----------------------------------|------|--------|----------------------|--------|
| f_{CLKOUT} | Output Clock Frequency | FSEL = HIGH | | 137.93 | | MHz |
| | | FSEL = LOW | | 133.33 | | |
| Δf | Frequency Stability - NBXDDB016 - NBXDDA016 | (Note 4) | | | ± 20 ± 50 | ppm |
| Φ_{NOISE} | Phase-Noise Performance $f_{\text{CLKout}} = 133.33\text{ MHz}/137.93\text{ MHz}$ (See Figures 3 and 4) | 100 Hz of Carrier | | -102 | | dBc/Hz |
| | | 1 kHz of Carrier | | -120 | | dBc/Hz |
| | | 10 kHz of Carrier | | -126 | | dBc/Hz |
| | | 100 kHz of Carrier | | -126 | | dBc/Hz |
| | | 1 MHz of Carrier | | -134 | | dBc/Hz |
| | | 10 MHz of Carrier | | -162 | | dBc/Hz |
| $t_{\text{jit}}(\Phi)$ | RMS Phase Jitter | 12 kHz to 20 MHz | | 0.4 | 0.9 | ps |
| t_{jitter} | Cycle to Cycle, RMS | 1000 Cycles | | 1.5 | 8 | ps |
| | Cycle to Cycle, Peak-to-Peak | 1000 Cycles | | 10 | 30 | ps |
| | Period, RMS | 10,000 Cycles | | 0.8 | 4 | ps |
| | Period, Peak-to-Peak | 10,000 Cycles | | 7 | 20 | ps |
| $t_{\text{OE/OD}}$ | Output Enable/Disable Time | | | | 200 | ns |
| $t_{\text{DUTY_CYCLE}}$ | Output Clock Duty Cycle (Measured at Cross Point) | | 48 | 50 | 52 | % |
| t_{R} | Output Rise Time (20% and 80%) | | | 160 | 300 | ps |
| t_{F} | Output Fall Time (80% and 20%) | | | 160 | 300 | ps |
| t_{start} | Start-up Time | | | 1 | 5 | ms |
| | Aging | 1 st Year | | | 3 | ppm |
| | | Every Year After 1 st | | | 1 | ppm |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. Measurement taken with outputs terminated with 50 ohm to V_{DD} . See Figure 5.

4. Parameter guarantees 10 years of aging. Includes initial stability at 25°C, shock, vibration, and first year aging.

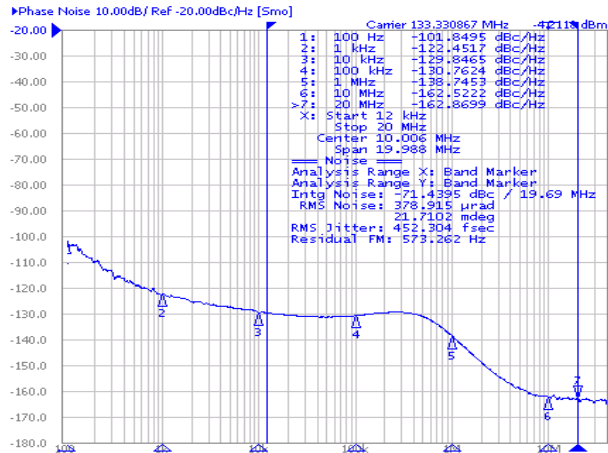


Figure 3. Typical Phase Noise Plot @ 133.33 MHz

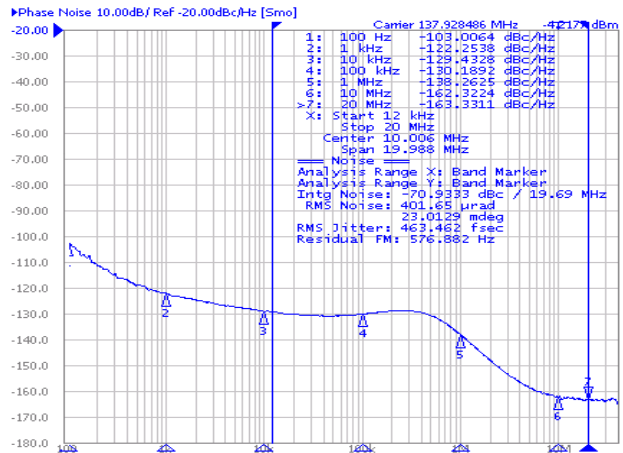


Figure 4. Typical Phase Noise Plot @ 137.93 MHz

NBXDDA016, NBXDDB016

Table 8. RELIABILITY COMPLIANCE

| Parameter | Standard | Method |
|----------------------------|-------------|---------------------------------------|
| Shock | Mechanical | MIL-STD-833, Method 2002, Condition B |
| Solderability | Mechanical | MIL-STD-833, Method 2003 |
| Vibration | Mechanical | MIL-STD-833, Method 2007, Condition A |
| Solvent Resistance | Mechanical | MIL-STD-202, Method 215 |
| Thermal Shock | Environment | MIL-STD-833, Method 1011, Condition A |
| Moisture Level Sensitivity | Environment | MSL1 260°C per IPC/JEDEC J-STD-020D |

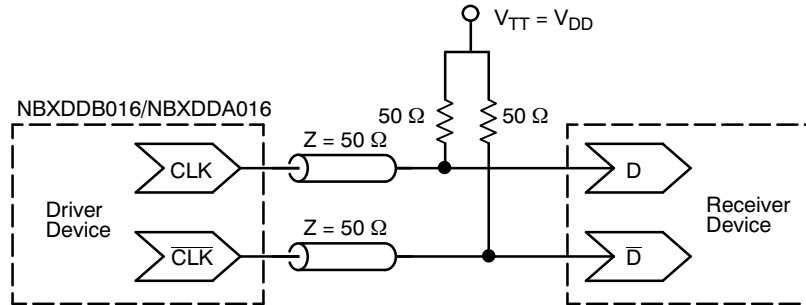


Figure 5. Typical CML Termination for Output Driver and Device Evaluation
(See Application Note AND8173 – Termination of CML Devices)

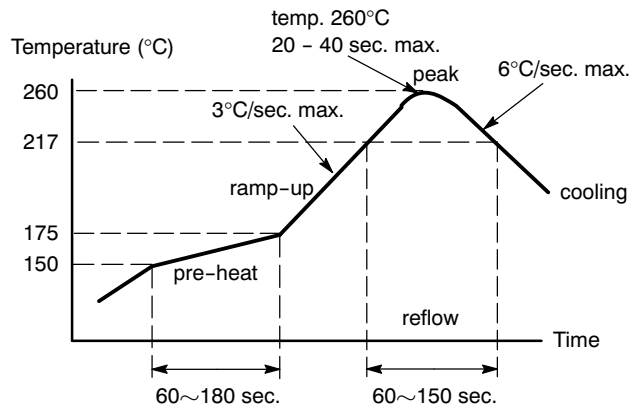
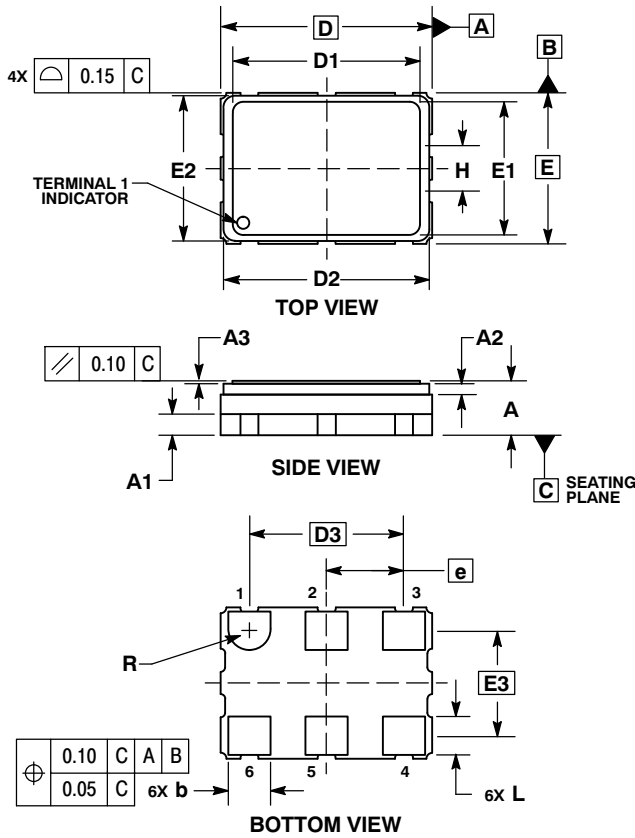


Figure 6. Recommended Reflow Soldering Profile

NBXDDA016, NBXDDB016

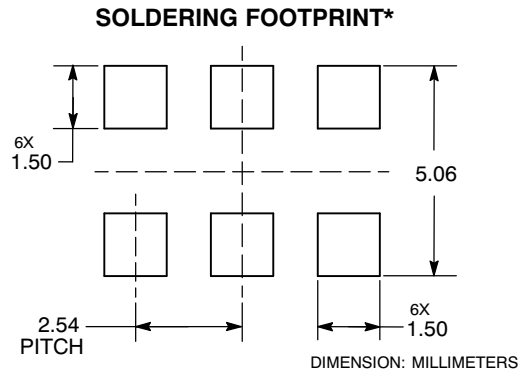
PACKAGE DIMENSIONS

6 PIN CLCC, 7x5, 2.54P
CASE 848AB-01
ISSUE C



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.

| DIM | MILLIMETERS | | |
|-----|-------------|------|------|
| | MIN | NOM | MAX |
| A | 1.70 | 1.80 | 1.90 |
| A1 | 0.70 REF | | |
| A2 | 0.36 REF | | |
| A3 | 0.08 | 0.10 | 0.12 |
| b | 1.30 | 1.40 | 1.50 |
| D | 7.00 BSC | | |
| D1 | 6.17 | 6.20 | 6.23 |
| D2 | 6.66 | 6.81 | 6.96 |
| D3 | 5.08 BSC | | |
| E | 5.00 BSC | | |
| E1 | 4.37 | 4.40 | 4.43 |
| E2 | 4.65 | 4.80 | 4.95 |
| E3 | 3.49 BSC | | |
| e | 2.54 BSC | | |
| L | 1.17 | 1.27 | 1.37 |
| R | 0.70 REF | | |



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local Sales Representative

NBXDDA016/D