

Decimating Digital Filter

The HSP43220/883 Decimating Digital Filter is a linear phase low pass decimation filter which is optimized for filtering narrow band signals in a broad spectrum of a signal processing applications. The HSP43220/883 offers a single chip solution to signal processing application which have historically required several boards of ICs. This reduction in component count results in faster development times, as well as reduction of hardware costs.

The HSP43220/883 is implemented as a two stage filter structure. As seen in the Block Diagram, the first stage is a High Order Decimation Filter (HDF) which utilizes an efficient decimation (sample rate reduction) technique to obtain decimation up to 1024 through a coarse low-pass filtering process. The HDF provides up to 96dB aliasing rejection in the signal pass band. The second stage consists of a Finite Impulse Response (FIR) decimation filter structured as a transversal FIR filter with up to 512 symmetric taps which can implement filters with sharp transition regions. The FIR can perform further decimation by up to 16 if required, while preserving the 96dB aliasing attenuation obtained by the HDF. The combined total decimation capability is 16,384.

The HSP43220/883 accepts 16-bit parallel data in 2's complement format at sampling rates up to 30MSPS. It provides a 16-bit microprocessor compatible interface to simplify the task of programming and three-state outputs to allow the connection of several ICs to a common bus. The HSP43220/883 also provides the capability to bypass either the HDF or the FIR for additional flexibility.

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Single Chip Narrow Band Filter with up to 96dB Attenuation
- DC to 25.6MHz Clock Rate
- 16-Bit 2's Complement Input
- 20-Bit Coefficients in FIR
- 24-Bit Extended Precision Output
- Programmable Decimation up to a Maximum of 16,384
- Standard 16-Bit Microprocessor Interface
- Filter Design Software Available DECI•MATE™

Applications

- Very Narrow Band Filters
- Zoom Spectral Analysis
- Channelized Receivers

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HSP43220GM-15/883	-55 to 125	84 Ld PGA	G84.A
HSP43220GM-25/883	-55 to 125	84 Ld PGA	G84.A

Block Diagram

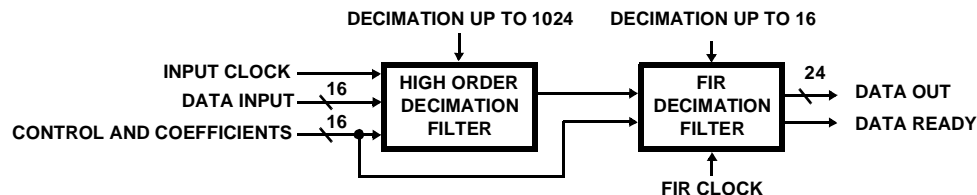


TABLE 2. AC ELECTRICAL PERFORMANCE SPECIFICATIONS

Devices Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES) (NOTE 5)	GROUP A SUB- GROUPS	TEMP (°C)	-15 (15MHz)		-25 (25.6MHz)		UNITS
					MIN	MAX	MIN	MAX	
Input Clock Period	t _{CK}		9, 10, 11	-55 ≤ T _A ≤ 125	66	-	39	-	ns
FIR Clock Period	t _{FIR}		9, 10, 11	-55 ≤ T _A ≤ 125	66	-	39	-	ns
Clock Pulse Width Low	t _{SPWL}		9, 10, 11	-55 ≤ T _A ≤ 125	26	-	16	-	ns
Clock Pulse Width High	t _{SPWH}		9, 10, 11	-55 ≤ T _A ≤ 125	26	-	16	-	ns
Clock Skew Between FIR_CLK and CK_IN	t _{SK}		9, 10, 11	-55 ≤ T _A ≤ 125	0	T _{FIR} -25	0	T _{FIR} -19	ns
RESET Pulse Width Low	t _{RSPW}		9, 10, 11	-55 ≤ T _A ≤ 125	4 T _{CK}	-	4 T _{CK}	-	ns
Recovery Time On RESET	t _{RTRS}		9, 10, 11	-55 ≤ T _A ≤ 125	8 T _{CK}	-	8 T _{CK}	-	ns
ASTARTIN Pulse Width Low	t _{AST}		9, 10, 11	-55 ≤ T _A ≤ 125	T _{CK} +10	-	T _{CK} +10	-	ns
STARTOUT Delay From CK_IN	t _{STOD}		9, 10, 11	-55 ≤ T _A ≤ 125	-	35	-	20	ns
STARTIN Setup to CK_IN	t _{STIC}		9, 10, 11	-55 ≤ T _A ≤ 125	25	-	15	-	ns
Setup Time on DATA_IN	t _{SET}		9, 10, 11	-55 ≤ T _A ≤ 125	20	-	16	-	ns
Hold Time on All Inputs	t _{HOLD}		9, 10, 11	-55 ≤ T _A ≤ 125	0	-	0	-	ns
Write Pulse Width Low	t _{WL}		9, 10, 11	-55 ≤ T _A ≤ 125	26	-	15	-	ns
Write pulse Width High	t _{WH}		9, 10, 11	-55 ≤ T _A ≤ 125	26	-	20	-	ns
Setup Time on Address Bus Before the Rising Edge of Write	t _{STADD}		9, 10, 11	-55 ≤ T _A ≤ 125	28	-	24	-	ns
Setup Time on Chip Select Before the Rising Edge of Write	t _{STCS}		9, 10, 11	-55 ≤ T _A ≤ 125	28	-	24	-	ns
Setup Time on Control Bus Before the Rising Edge of Write	t _{STCB}		9, 10, 11	-55 ≤ T _A ≤ 125	28	-	24	-	ns
DATA_RDY Pulse Width Low	t _{DRPWL}		9, 10, 11	-55 ≤ T _A ≤ 125	2T _{FIR} -20	-	2T _{FIR} -10	-	ns
DATA_OUT Delay Relative to FIR_CLK	t _{FIRDV}		9, 10, 11	-55 ≤ T _A ≤ 125	-	50	-	35	ns
DATA_RDY Valid Delay Relative to FIR_CLK	t _{FIRDR}		9, 10, 11	-55 ≤ T _A ≤ 125	-	35	-	25	ns
DATA_OUT Delay Relative to OUT_SELH	t _{OUT}		9, 10, 11	-55 ≤ T _A ≤ 125	-	30	-	25	ns
Output Enable to Data Out Valid	t _{OEV}	Note 6	9, 10, 11	-55 ≤ T _A ≤ 125	-	20	-	20	ns

NOTES:

- AC Testing: V_{CC} = 4.5V and 5.5V. Inputs are driven at 3.0V for a Logic "1" and 0.0V for a Logic "0". Input and output timing measurements are made at 1.5V for both a Logic "1" and "0". CLK is driven at 4.0V and 0V and measured at 2.0V.
- Transition is measured at ±200mV from steady state voltage with loading as specified by test load circuit and C_L = 40pF.

TABLE 3. ELECTRICAL PERFORMANCE SPECIFICATIONS

Devices Guaranteed and 100% Tested

PARAMETER	SYMBOL	TEST CONDITIONS	NOTES	TEMP (°C)	-15 (15MHz)		-25 (25.6MHz)		UNITS
					MIN	MAX	MIN	MAX	
CK_IN Pulse Width Low	t _{CH1L}		7, 9	-55 ≤ T _A ≤ 125	29	-	19	-	ns
CK_IN Pulse Width High	t _{CH1H}		7, 9	-55 ≤ T _A ≤ 125	29	-	19	-	ns
CK_IN Setup to FIR_CK	t _{CIS}		7, 9	-55 ≤ T _A ≤ 125	27	-	17	-	ns
CK_IN Hold from FIR_CK	t _{CIH}		7, 9	-55 ≤ T _A ≤ 125	2	-	2	-	ns
Input Capacitance	C _{IN}	V _{CC} = Open, f = 1MHz, All measurements are referenced to device GND	7	T _A = 25°C	-	12	-	12	pF
Output Capacitance	C _{OUT}	V _{CC} = Open, f = 1MHz, All measurements are referenced to device GND	7	T _A = 25°C	-	10	-	10	pF
Output Disable Delay	t _{OEZ}		7, 8	-55 ≤ T _A ≤ 125	-	20	-	20	ns
Output Rise Time	t _{OR}		7, 8	-55 ≤ T _A ≤ 125	-	8	-	8	ns
Output Fall Time	t _{OF}		7, 8	-55 ≤ T _A ≤ 125	-	8	-	8	ns

NOTES:

7. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.
8. Loading is as specified in the test load circuit with C_L = 40pF.
9. Applies only when H_BYP = 1 or H_DRATE = 0.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	-
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C and D	Samples/5005	1, 7, 9

HSP43220/883

Burn-In Circuit

HSP43220/883
TOP VIEW
PINS DOWN

	1	2	3	4	5	6	7	8	9	10	11
A	GND	DATA_IN 1	DATA_IN 2	DATA_IN 4	DATA_IN 7	DATA_IN 8	DATA_IN 11	DATA_IN 14	VCC	GND	GND
B	START_IN	START_OUT	DATA_IN 0	DATA_IN 3	DATA_IN 6	DATA_IN 13	DATA_IN 12	DATA_IN 15	CLK_IN	VCC	DATA_OUT 1
C	ASTART_IN	VCC			DATA_IN 0	DATA_IN 9	DATA_IN 10			DATA_OUT 0	DATA_OUT 2
D	A1	RESET								DATA_OUT 3	DATA_OUT 4
E	CS	WR	A0						DATA_OUT 5	DATA_OUT 3	DATA_OUT 7
F	C_BUS 10	C_BUS 15	C_BUS 14						DATA_OUT 9	VCC	DATA_OUT 8
G	C_BUS 12	C_BUS 11	C_BUS 13						DATA_OUT 10	GND	DATA_OUT 11
H	C_BUS 9	VCC								DATA_OUT 13	DATA_OUT 12
J	GND	C_BUS 7			OUT_SELH	GND	FIR_CK			DATA_OUT 16	DATA_OUT 14
K	C_BUS 8	C_BUS 5	C_BUS 4	C_BUS 1	OUT_EMP	VCC	GND	DATA_OUT 22	DATA_OUT 19	DATA_OUT 17	DATA_OUT 15
L	C_BUS 6	C_BUS 3	C_BUS 2	C_BUS 0	OUT_ENX	DATA_RDY	VCC	DATA_OUT 23	DATA_OUT 21	DATA_OUT 20	DATA_OUT 18

BURN-IN CIRCUIT SIGNALS

PIN LEAD	PIN NAME	BURN-IN SIGNAL	PIN LEAD	PIN NAME	BURN-IN SIGNAL	PIN LEAD	PIN NAME	BURN-IN SIGNAL
A1	GND	GND	C1	ASTARTIN	F15	F11	DATA_OUT 3	VCC/2
A2	DATA_IN 1	F2	C2	VCC	VCC	G1	C_BUS 12	F5
A3	DATA_IN 2	F3	C5	DATA_IN 5	F6	G2	C_BUS 11	F4
A4	DATA_IN 4	F5	C6	DATA_IN 9	F2	G3	C_BUS 13	F6
A5	DATA_IN 7	F8	C7	DATA_IN 10	F3	G9	DATA_OUT 10	VCC/2
A6	DATA_IN 8	F1	C10	DATA_OUT 0	VCC/2	G10	GND	GND
A7	DATA_IN 11	F4	C11	DATA_OUT 2	VCC/2	G11	DATA_OUT 11	VCC/2
A8	DATA_IN 14	F7	D1	A1	F14	H1	C_BUS 9	F2
A9	VCC	VCC	D2	RESET	F16	H2	VCC	VCC
A10	GND	GND	D10	DATA_OUT 3	VCC/2	H10	DATA_OUT 13	VCC/2
A11	GND	GND	D11	DATA_OUT 4	VCC/2	H11	DATA_OUT 12	VCC/2
B1	STARTIN	F15	E1	CS	F11	J1	GND	GND
B2	STARTOUT	VCC/2	E2	WR	F11	J2	C_BUS 7	F8
B3	DATA_IN 0	F1	E3	A0	F13	J5	OUT_SEL	F10
B4	DATA_IN 3	F4	E9	DATA_OUT 5	VCC/2	J6	GND	GND
B5	DATA_IN 6	F7	E10	DATA_OUT 6	VCC/2	J8	FIR_CK	F0

BURN-IN CIRCUIT SIGNALS (CONTINUED)

PIN LEAD	PIN NAME	BURN-IN SIGNAL	PIN LEAD	PIN NAME	BURN-IN SIGNAL	PIN LEAD	PIN NAME	BURN-IN SIGNAL
B6	DATA_IN 13	F6	E11	DATA_OUT 7	V _{CC} /2	J10	DATA_OUT 16	V _{CC} /2
B7	DATA_IN 12	F5	F1	C_BUS 10	F3	J11	DATA_OUT 14	V _{CC} /2
B8	DATA_IN 15	F8	F2	C_BUS 15	F8	K1	C_BUS 8	F1
B9	CK_IN	F0	F3	C_BUS 14	F7	K2	C_BUS 5	F6
B10	V _{CC}	V _{CC}	F9	DATA_OUT 9	V _{CC} /2	K3	C_BUS 4	F5
B11	DAT_OUT 1	V _{CC} /2	F10	V _{CC}	V _{CC}	K4	C_BUS 1	F2
K5	OUT_ENP	F9	K11	DATA_OUT 15	V _{CC} /2	L6	DATA_RDY	V _{CC} /2
K6	V _{CC}	V _{CC}	L1	C_BUS 6	F7	L7	V _{CC}	V _{CC}
K7	GND	GND	L2	C_BUS 3	F4	L8	DATA_OUT 23	V _{CC} /2
K8	DATA_OUT 22	V _{CC} /2	L3	C_BUS 2	F3	L9	DATA_OUT 21	V _{CC} /2
K9	DATA_OUT 19	V _{CC} /2	L4	C_BUS 0	F1	L10	DATA_OUT 20	V _{CC} /2
K10	DATA_OUT 17	V _{CC} /2	L5	OUT_ENX	F9	L11	DATA_OUT 18	V _{CC} /2

NOTES:

10. V_{CC}/2 (2.7 ±10%) used for outputs only.
11. 47kΩ (±20%) resistor connected to all pins except V_{CC} and GND.
12. V_{CC} = 5.5 ±0.5V.
13. 0.1μF (minimum) capacitor between V_{CC} and GND per position.
14. F0 = 100kHz ±10%, F1 = F0/2, F2 = F1/2....F16 = F15/2, 40% - 60% duty cycle.
15. Input voltage limits: V_{IL} = 0.8 maximum, V_{IH} = 4.5V ±10%.

Metal Topology

DIE DIMENSIONS:

348 x 349.2 x 19 ±1 mils

METALLIZATION:

Type: Si - Al, or Si - Al - Cu
 Thickness: 8kÅ

WORST CASE CURRENT DENSITY:

1.18 x 10⁵A/cm²

GLASSIVATION:

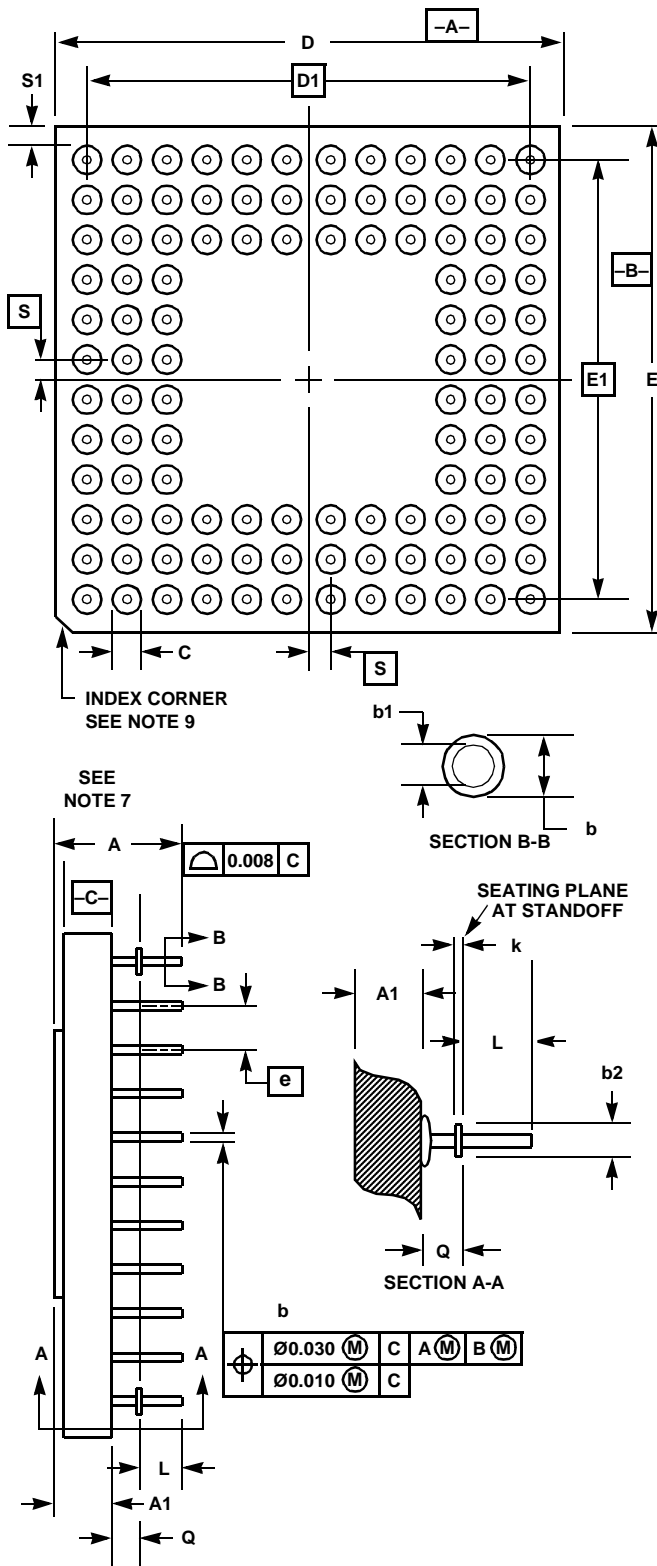
Type: Nitrox
 Thickness: 10kÅ

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Ceramic Pin Grid Array Packages (CPGA)



G84.A MIL-STD-1835 CMGA3-P84C (P-AC)
84 LEAD CERAMIC PIN GRID ARRAY PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.215	0.345	5.46	8.76	-
A1	0.070	0.145	1.78	3.68	3
b	0.016	0.0215	0.41	0.55	8
b1	0.016	0.020	0.41	0.51	-
b2	0.042	0.058	1.07	1.47	4
C	-	0.080	-	2.03	-
D	1.140	1.180	28.96	29.97	-
D1	1.000 BSC		25.4 BSC		-
E	1.140	1.180	28.96	29.97	-
E1	1.000 BSC		25.4 BSC		-
e	0.100 BSC		2.54 BSC		6
k	0.008 REF		0.20 REF		-
L	0.120	0.140	3.05	3.56	-
Q	0.040	0.060	1.02	1.52	5
S	0.000 BSC		0.00 BSC		10
S1	0.003	-	0.08	-	-
M	11		11		1
N	-	121	-	121	2

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NOTES:

1. "M" represents the maximum pin matrix size.
2. "N" represents the maximum allowable number of pins. Number of pins and location of pins within the matrix is shown on the pinout listing in this data sheet.
3. Dimension "A1" includes the package body and Lid for both cavity-up and cavity-down configurations. This package is cavity up. Dimension "A1" does not include heatsinks or other attached features.
4. Standoffs are intrinsic and shall be located on the pin matrix diagonals. The seating plane is defined by the standoffs at dimensions Q.
5. Dimension "Q" applies to cavity-up configurations only.
6. All pins shall be on the 0.100 inch grid.
7. Datum C is the plane of pin to package interface for both cavity up and down configurations.
8. Pin diameter includes solder dip or custom finishes. Pin tips shall have a radius or chamfer.
9. Corner shape (chamfer, notch, radius, etc.) may vary from that shown on the drawing. The index corner shall be clearly unique.
10. Dimension "S" is measured with respect to datums A and B.
11. Dimensioning and tolerancing per ANSI Y14.5M-1982.
12. Controlling dimension: INCH.