14-Bit, Dual Channel Resolver-to-Digital Converter

AD2S34

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FEATURES

- 1 in², 32-Pin Flatpack
- 2.6 Arc Minute Accuracy
- 14-Bit Resolution
- On-Board Oscillator
- Independent Reference Inputs
- Independent Velocity Outputs
- High Tracking Rate

APPLICATIONS

- Gimbal/Gyro Control Systems
- Radar/Sonar
- Engine Controllers
- Coordinate Conversion
- Military Servo Control Systems
- Fire Control Systems
- Avionic Systems
- Missile Systems
- Antenna Monitoring
- CNC Machine Tools

GENERAL DESCRIPTION

The AD2S34 series are 14-bit dual channel, continuous tracking resolver-to-digital converters. They have been designed specifically for applications where space and weight are at a premium. Each 32-pin hybrid device contains two independent Type II servo loop tracking converters and a power oscillator suitable for exciting resolvers. The ratiometric conversion technique employed by the converters provides excellent noise immunity, repeatability and tolerance of long lead lengths. The core of each conversion is performed by state-of-the-art monolithic integrated circuits manufactured in Analog Devices' proprietary BiMOS II process which combines the advantages of low power CMOS digital logic with bipolar linear circuits. The use of these ICs keeps the internal component count low and ensures high reliability.

The converter interfaces directly to 2 V rms output resolvers. A simple voltage divider circuit of resistors can be used to derive the 2 V rms from other standard resolver voltages.

An on-board oscillator provides a reference excitation for resolvers operating at either 400 Hz, 2.6 kHz or 4 kHz. Each channel has an independent reference input, allowing the user to compensate for any resolver phase shift between induced signals (sin, cos) and reference.

The converter output is via a tristate transparent latch allowing data to be read without interruption of converter operation. The $\overline{\text{SEL A}}$ and $\overline{\text{SEL B}}$ control lines select the channel and present the digital position to the common data output pins. A $\overline{\text{DATA VALID}}$ flag is provided to assist with data transfer.

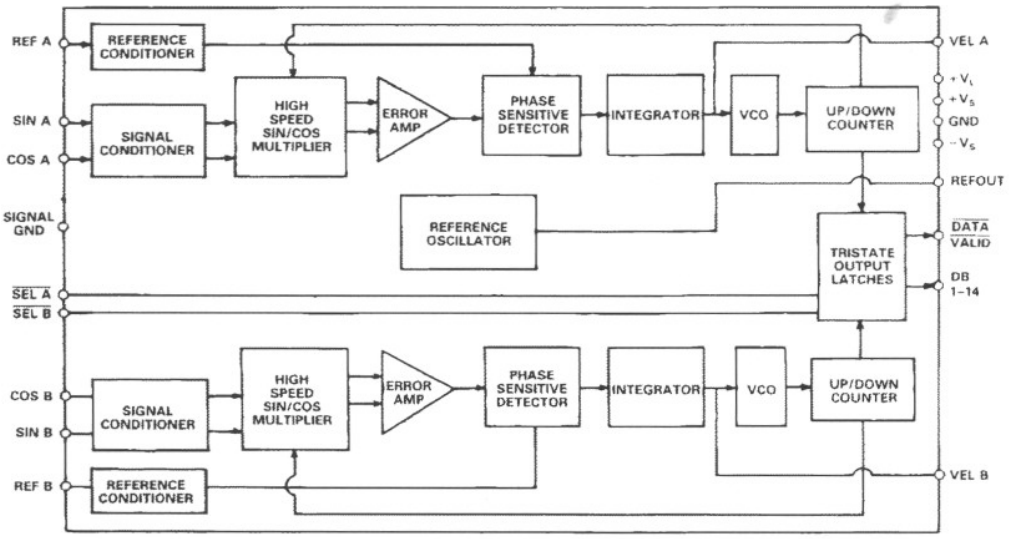
The AD2S34 also features two velocity outputs, one for each channel; these continuously generate analog signals proportional to the rotational velocity of the resolver shafts. These signals can be used in place of velocity transducers in many applications to provide loop stabilization and velocity feedback data.

MODELS AVAILABLE

The AD2S34 series is available in 2 accuracy grades:

AD2S34TZ	14-Bits	2.6 arc mins	−55°C to +125°C
AD2S34SZ	14-Bits	4.0 arc mins	−55°C to +125°C

FUNCTIONAL BLOCK DIAGRAM



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AD2S34—SPECIFICATIONS (typical at +25°C unless otherwise specified)

Parameter	AD2S34 Min	Typ	Max	Units	Comments
PERFORMANCE					
Accuracy[1]					
AD2S34TZ			±2.6	arc min	−55°C to +125°C
AD2S34SZ			±4.0	arc min	−55°C to +125°C
Max Tracking Rate					
AD2S34xZ10	20			revs/s	
AD2S34xZ40	48			revs/s	
AD2S34xZ60	20			revs/s	
Resolution			14	Bits	Output Coding Parallel
	(1 LSB = 1.3 arc min)				Natural Binary
Repeatability			1	LSB	
Signal/Reference Frequency					
AD2S34xZ10	360	400	440	Hz	
AD2S34xZ40	2340	2600	2860	Hz	
AD2S34xZ60	3600	4000	4400	Hz	
Tracking Bandwidth					
AD2S34xZ10	90			Hz	
AD2S34xZ40	370			Hz	
AD2S34xZ60	650			Hz	
SIGNAL INPUTS (SIN, COS)					
Signal Voltage	1.8	2.0	2.2	V rms	
Allowable Phase Shift					
(Signal to Reference)			±10	Degrees	
Input Impedance	1			MΩ	
REFERENCE INPUTS (REF A, REF B)					
Reference Voltage	1.8	2.0	2.2	V rms	
Tolerance	1.4		8.0	V peak	
Input Impedance	1			MΩ	
ACCELERATION CONSTANT					
AD2S34xZ10	53000			sec^{-2}	
AD2S34xZ40	695000			sec^{-2}	
AD2S34xZ60	2164000			sec^{-2}	
STEP RESPONSE					
Large Step[1]					
AD2S34xZ10		60	72	ms	179° to 1 LSB
AD2S34xZ40		30	36	ms	of Error
AD2S34xZ60		22.5	30	ms	
POWER LINES (No Load on REF OUT)					
$+V_S$ = +15 V dc[1]		40	55	mA	
$-V_S$ = −15 V dc[1]		30	45	mA	
$+V_L$ = +5 V dc[1]		1	5	mA	Quiescent Condition
Power Dissipation[1]		1.06	1.53	W	Quiescent Condition
DIGITAL INPUTS ($\overline{SEL\ A}$, $\overline{SEL\ B}$)					
V_{IL}			0.8	V dc	
V_{IH}	2.0			V dc	
I_{IL}			±100	μA	V_{IL} = 0 V
I_{IH}			±100	μA	V_{IH} = 5 V
DIGITAL OUTPUTS (DB1–DB14, $\overline{DATA\ VALID}$)					
V_{OL}[1]			0.4	V dc	I_{OL} = 1.2 mA
V_{OH}[1]	2.4			V dc	I_{OH} = 100 μA
Tristate Leakage Current[1]			±100	μA	
Drive Capability			3	LSTTL Loads	

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Parameter	AD2S34 Min	Typ	Max	Units	Comments
VELOCITY OUTPUTS (VEL A, VEL B)					
Voltage[1]	±7.5			V dc	At Max Tracking Rate
Linearity[1]					
AD2S34xZ10			±1	% of Output	
AD2S34xZ40			±3	% of Output	
AD2S34xZ60			±1	% of Output	
Reversion Error[1]			±3	%	
DC Zero Offset @ +25°C					
AD2S34xZ10		22	55	mV	
AD2S34xZ40		9	23	mV	
AD2S34xZ60		22	55	mV	
DC Zero Offset Temperature Coefficient					
AD2S34xZ10			−100	μV/°C	
AD2S34xZ40			−42	μV/°C	
AD2S34xZ60			−100	μV/°C	
Gain Scaling Accuracy			±10	% of FSD	
Noise and Ripple at LSB Rate			2	mV	
Dynamic Ripple (Peak)			1.5	% of Mean Output	
REFERENCE OUTPUT (REF OUT)					
Frequency[1]					
AD2S34xZ10	360	400	440	Hz	
AD2S34xZ40	2340	2600	2860	Hz	
AD2S34xZ60	3600	4000	4400	Hz	
Voltage[1]	5.5	6.0	6.5	V rms @ 50 mA	Min 120 Ω Load
DATA TRANSFER (See Figure 3)					
Time to Data Stable (After Negative Edge of $\overline{SEL\ A}$ or $\overline{SEL\ B}$)			1000	ns	t_Q
Time to Data in High Impedance State (After Positive Edge of SEL A or SEL B)			50	ns	t_R
Time to DATA VALID High (After Negative Edge of $\overline{SEL\ A}$ or $\overline{SEL\ B}$)	1050			ns	t_P
Time to DATA VALID Low (After Positive Edge of $\overline{SEL\ A}$ or $\overline{SEL\ B}$)	40			ns	t_Q
DIMENSIONS	1.00 × 1.00 × 0.155 25.4 × 25.4 × 3.9			inch mm	See Package Information
WEIGHT			0.254 7.2	oz grams	
THERMAL RESISTANCE[2]					
θ_{JC} Worst Case Component			35	°C/W	
θ_{CA}			31	°C/W	

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NOTES

[1]Specified over temperature range, −55°C to +125°C, and for: (a) 10% signal and reference amplitude variation; (b) 10% signal and reference harmonic distortion; (c) 5% power supply variation; (d) 10% variation in reference frequency.

[2]To ensure that the junction temperature of the hottest component within the hybrid does not exceed the rated maximum of 150°C, the case temperature must not exceed 130°C.

Boldface type indicates parameters which are 100% tested at nominal values of power supplies, input signal voltages, and operating frequency. All other parameters are guaranteed by design, not tested.

Specifications subject to change without notice.

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ABSOLUTE MAXIMUM RATINGS

$+V_S$ to GND	+17.25 V dc
$-V_S$ to GND	−17.25 V dc
$+V_L$ to GND	0 to +7.0 V dc
Any Logic Input to GND (max)	+7.0 V dc
Any Logic Input to GND (min)	−0.4 V dc
SIN, COS to SIGNAL GND	±12 V dc
REF A, REF B to SIGNAL GND	±12 V dc
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C

CAUTION

1. Absolute maximum ratings are the limits beyond which damage to the device may occur.
2. Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.

ORDERING INFORMATION

When ordering, the converter part numbers should be suffixed by a two letter code defining the accuracy grade, and a two digit numeric code defining the signal/reference frequency and voltage. All the standard options and their option codes are shown below. For options not shown, please contact Analog Devices.

AD2S34 x Z y 0 B

- B = High-Reliability Processing (Optional)
- 0 = Signal 2 V Reference 2 V Resolver
- y = Base Part Number
  - y = 1 400 Hz Reference Frequency
  - y = 4 2.6 kHz Reference Frequency
  - y = 6 4.0 kHz Reference Frequency
- Z = Leaded Chip Carrier
- x = "T" −55°C to +125°C Operating Temperature Range 2.6 Arc Min Accuracy
- x = "S" −55°C to +125°C Operating Temperature Range 4.0 Arc Min Accuracy

For example, the correct part number for a component to operate with 400 Hz reference frequency and have a 2.6 arc minute accuracy over the −55°C to +125°C temperature range and processed to high reliability standards would be AD2S34TZ10B.

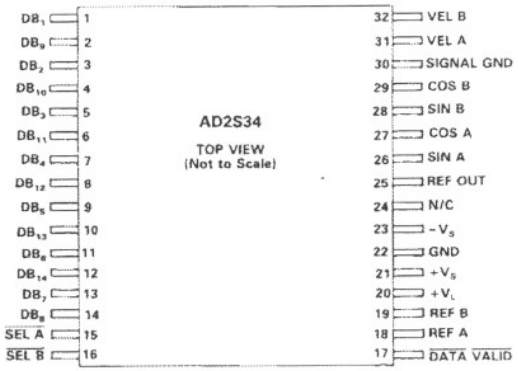
All components are 100% tested at −55°C, +25°C and +125°C. Devices processed to high reliability screening standards (Suffix B) receive further levels of testing and screening to ensure high levels of reliability.

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage ($+V_S$ to GND)	+15 V dc ±5%
Power Supply Voltage ($-V_S$ to GND)	−15 V dc ±5%
Power Supply Voltage V_L	+5 V dc ±5%
Analog Input Voltage (SIN, COS to SIGNAL GND)	2 V rms ±10%
Analog Input Voltage (REF A, REF B to SIGNAL GND)	1.0 V to 8.0 V Peak
Signal and Reference Harmonic Distortion	±10%
Phase Shift Between Signal and Reference	±10 Degrees
Ambient Operating Temperature Range	−55°C to +125°C

PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1–14	DB1–DB14	PARALLEL OUTPUT DATA
15	$\overline{\text{SEL A}}$	SELECT CHANNEL A
16	$\overline{\text{SEL B}}$	SELECT CHANNEL B
17	$\overline{\text{DATA VALID}}$	DATA VALID
18	REF A	REFERENCE INPUT CHANNEL A
19	REF B	REFERENCE INPUT CHANNEL B
20	$+V_L$	LOGIC POWER SUPPLY
21	$+V_S$	POSITIVE POWER SUPPLY
22	GND	POWER SUPPLY GROUND (NOTE: THIS PIN IS ELECTRICALLY CONNECTED TO CASE.)
23	$-V_S$	NEGATIVE POWER SUPPLY
24	N/C	NOT CONNECTED
25	REF OUT	REFERENCE OUTPUT
26	SIN A	SINE INPUT CHANNEL A
27	COS A	COSINE INPUT CHANNEL A
28	SIN B	SINE INPUT CHANNEL B
29	COS B	COSINE INPUT CHANNEL B
30	SIGNAL GND	GROUND PIN FOR SIGNALS FROM RESOLVERS
31	VEL A	VELOCITY OUTPUT CHANNEL A
32	VEL B	VELOCITY OUTPUT CHANNEL B



AD2S34 Terminal Connections

ESD SENSITIVITY

The AD2S34 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (human body model) and fast, low energy pulses (charged device model).

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. For further information on ESD precautions, refer to Analog Devices' *ESD Prevention Manual*.

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PRINCIPLES OF OPERATION

The AD2S34 series operate on a Type 2 tracking closed-loop principle. The output digital word continually tracks the position of the resolver shaft without the need for external convert commands and wait states. As the transducer moves through a position equivalent to the least significant bit weighting, the output digital word is updated by one LSB.

Each channel is identical in operation, sharing power supply and digital position output pins.

Both channels operate continuously and independently of each other. The shared digital output from either channel is available as selected by switching the channel select inputs.

To illustrate the conversion process, the resolver format input signals are represented by:

$$V_1 = K E_0 \sin \omega t \sin \theta$$
$$V_2 = K E_0 \sin \omega t \cos \theta$$

where θ is the angle of the resolver shaft.

Assume that the current word state of the up-down counter is ϕ. V1 is multiplied by cos ϕ and V2 is multiplied by sin ϕ to give:

$$K E_0 \sin \omega t \sin \theta \cos \phi$$
$$K E_0 \sin \omega t \cos \theta \sin \phi$$

These signals are subtracted by the error amplifier to give:

$$K E_0 \sin \omega t (\sin \theta \cos \phi - \cos \theta \sin \phi)$$

or

$$K E_0 \sin \omega t \sin (\theta - \phi)$$

A phase sensitive detector, integrator and voltage controlled oscillator (VCO) form a closed-loop system which seeks to null sin $(\theta - \phi)$. When this is accomplished, the word state of the up-down counter, ϕ, equals, to within the rated accuracy of the converter, the resolver shaft angle, θ.

CONNECTING THE CONVERTER

The power supply voltages connected to $+V_S$ and $-V_S$ pins should be +15 V dc and −15 V dc, respectively, and must not be reversed. The voltage applied to V_L should be +5 V nominally. It is suggested that a parallel combination of a 100 nF (ceramic) and a 6.8 μF (tantalum) capacitor be placed from each of the three supply pins to GND.

The pin marked GND is connected electrically to the case and should be taken to the zero volt potential in the system.

The digital output is taken from Pins 1–14. Pin 1 is the MSB, Pin 12 the LSB. Please see terminal connections diagram.

The internal oscillator output (REF OUT) should be connected to each resolver and via an optional phase shift compensation circuit to the reference inputs (REF A & REF B). See Figure 1 for suitable phase compensation circuits.

The signals applied to REF A and REF B should be ac coupled as shown in Figure 1. This ac coupling can be included in the optional phase compensation circuit.

NOTE: For the 400 Hz option (AD2S34xZ10), in addition to the phase shift compensation referred to above, an extra 3.8 degrees of phase lead should be included to compensate for the internal phase shift within the hybrid. For higher frequency options this extra lead is not necessary as the internal phase shift does not affect the stated accuracy.

The signals are connected to sin and cos according to the following convention:

$$E_{SIN} = E_{RLO-RHI} \sin \omega t \sin \theta$$
$$E_{COS} = E_{RLO-RHI} \sin \omega t \cos \theta$$

The two signal ground wires from each resolver should be connected at the SIGNAL GND pin of the converter to minimize the coupling between the sine and cosine signals. For the same reason it is also recommended that the resolvers are connected using individual twisted pair cables with the sine, cosine and reference signals twisted separately.

See Figure 1 for the recommended connection circuit.

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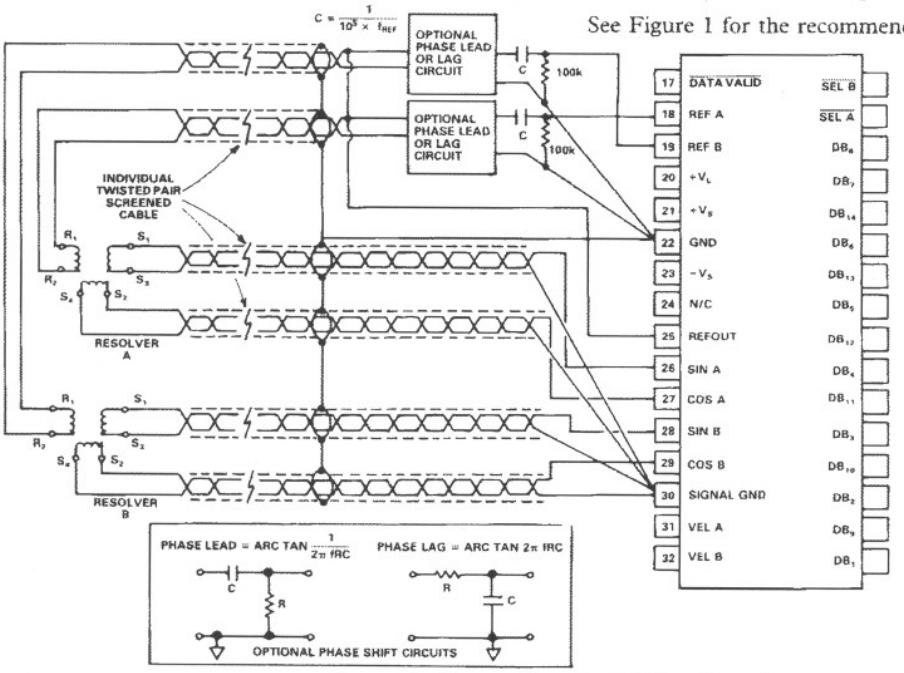

Figure 1. Connecting the 2S34 to Resolvers

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SCALING FOR NONSTANDARD SIGNALS

A feature of these converters is that the signal and reference inputs can be resistively scaled to accommodate nonstandard input signal and reference voltages which are outside the nominal ±10% limits of the converter. Using this technique, it is possible to use a standard converter with a "personality card" in systems where a wide range of input and reference voltages are encountered.

NOTE: The accuracy of the converter will be affected by the matching accuracies of resistors used for external scaling. It is critical that the value of the resistors on the sine signals be precisely matched to the cosine signals. In general, a 0.1% mismatch between resistor values will contribute an additional 1.7 arc minutes of error to the conversion. In addition, imbalances in resistor values can greatly reduce the common-mode rejection ratio of the signal inputs.

CHANNEL SELECT $\overline{\text{SEL A}}$, $\overline{\text{SEL B}}$

$\overline{\text{SEL A}}$ and $\overline{\text{SEL B}}$ are the channel select inputs. A logic low on $\overline{\text{SEL A}}$ selects Channel A and a logic low on $\overline{\text{SEL B}}$ selects Channel B. Both channels must not be selected at the same time.

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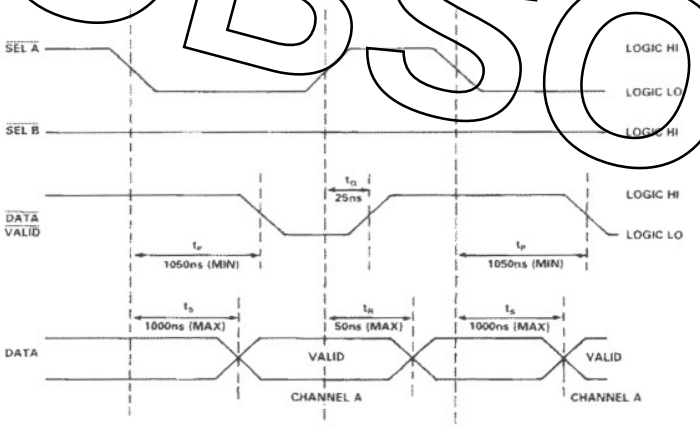

Figure 2a. Timing Diagram for Repetitive Reading of One Channel

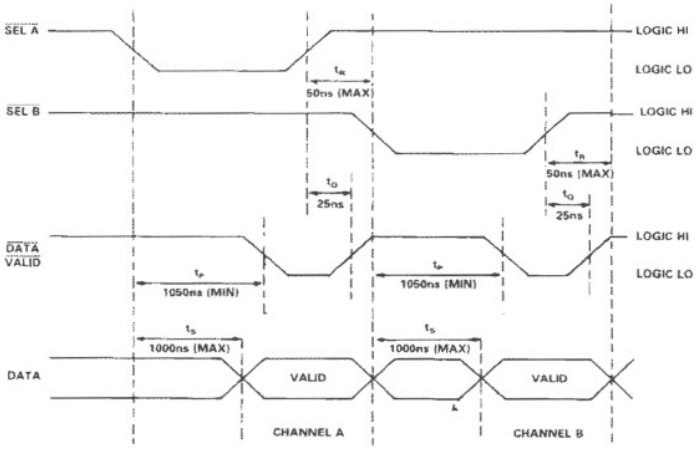

Figure 2b. Timing Diagram for Alternate Reading of Each Channel

Data becomes valid 1 µs after the negative edge of $\overline{\text{SEL A}}$ or $\overline{\text{SEL B}}$. Timing information is shown in Figure 2.

$\overline{\text{DATA VALID}}$

The $\overline{\text{DATA VALID}}$ output is a logic output which switches low 1 µs after the negative edge of either channel select indicating that the output latches have valid data for transfer.

REFERENCE OUTPUT REF OUT

The reference output provides a 6 V rms reference signal of 400 Hz, 2.6 kHz or 4.0 kHz frequency which can be used to excite the two resolvers and also to be used as the reference to the converter.

CAUSES OF ERROR

Differential Phase Shift

Phase shift between the sine and the cosine signals from the resolver is known as differential phase shift and can cause static error. Some differential phase shift will be present on all resolvers being a transducer characteristic. A small resolver residual voltage (quadrature voltage) indicates a small differential phase shift. Additional phase shift can be introduced if the sine channel wires and the cosine channel wires are routed differently. For instance, different cable lengths or different capacitive loads could cause differential phase shift.

The additional error caused by differential phase shift on the input signals approximates to

$$Error = 0.53 \times a \times b \text{ arc minutes}$$

where a = differential phase shift in degrees and b = signal to reference phase shift in degrees.

This error can be minimized by choosing a resolver with a small residual voltage, ensuring that the sine and cosine signals are handled identically and removing the reference phase shift (see section on "CONNECTING THE CONVERTER"). By taking these precautions, the extra error can be made insignificant.

Resolver Phase Shift

Under static operating conditions phase shift between the reference and the signal lines alone will not theoretically affect the converter's stated accuracy. However, most resolvers exhibit a phase shift between the signal and the reference. This phase shift will give rise under dynamic conditions to an additional error defined by:

$$\frac{Shaft\ Speed\ (rps) \times Phase\ Shift\ (degrees)}{Reference\ Frequency}$$

This effect can be eliminated by placing a phase shift in the reference to the converter equivalent to the phase shift in the resolver (see section "CONNECTING THE CONVERTER").

NOTE: Capacitive and inductive crosstalk in the signal and reference leads and wiring can cause similar problems.

VELOCITY OUTPUT VEL A, VEL B

The signals on these pins are analogue voltages proportional to the rate of change of the respective input angle. These signals are available regardless of the state of the channel selects $\overline{\text{SEL A}}$ and $\overline{\text{SEL B}}$.

A better quality of velocity signal will be achieved if the following points are considered.

1. Protection. For loads greater than 5 pF or 10 kΩ the velocity signal should be buffered before use.
2. Ripple and noise. Noise on the input signals to the converter is the major cause of noise on the velocity signal. This can be reduced to a minimum if the following precautions are taken:

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The resolvers are connected to the converter using separate screened twisted pair cable of equal lengths for the sine, cosine and reference signals.

Care is taken to reduce the external noise wherever possible.

A resolver with low residual voltage is chosen, i.e., one with small quadrature signals.

Feedthrough of the reference frequency can be removed by a filter on the velocity signal. Care must to be taken when setting the filter not to impede speed loop bandwidth.

Reference to signal phase shift should be minimized to reduce quadrature effects and larger ripple.

If the above precautions are taken, a very good noise and ripple performance can be achieved allowing the AD2S34 velocity signals to be used in very noisy environments.

DYNAMIC PERFORMANCE

The transfer function of the converter is given below.

Figure 3. Transfer Function of AD2S34

Open-loop transfer function:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{K_A\ (1 + sT_1)}{s^2\ (1 + sT_2)}$$

Closed-loop transfer function:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{1 + sT_1}{1 + sT_1 + s^2/K_A + s^3\ T_2/K_A}$$

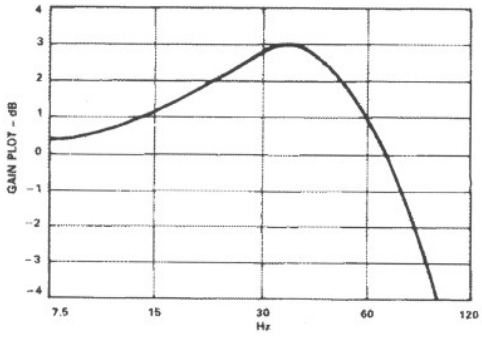

Figure 4. AD2S34xZ10 Gain Plot

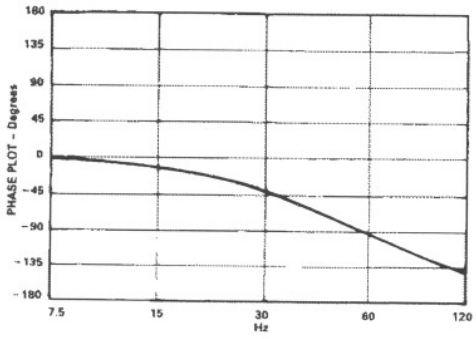

Figure 5. AD2S34xZ10 Phase Plot

Where:

Option xZ10	Option xZ40	Option xZ60
K_A = 53000 sec^{-2}	K_A = 695000 sec^{-2}	K_A = 2164000 sec^{-2}
T_1 = 0.0062 sec	T_1 = 0.0019 sec	T_1 = 0.0011 sec
T_2 = 0.00079 sec	T_2 = 0.0003 sec	T_2 = 0.00017 sec

The gain and phase diagrams are shown in Figures 4 through 9.

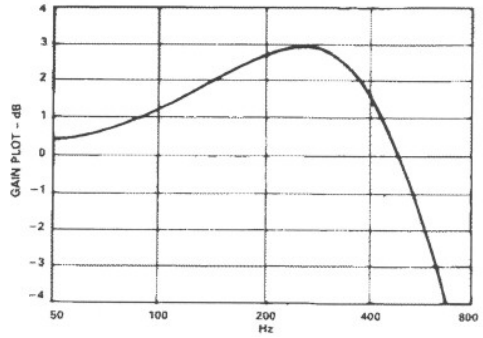

Figure 6. AD2S34xZ40 Gain Plot

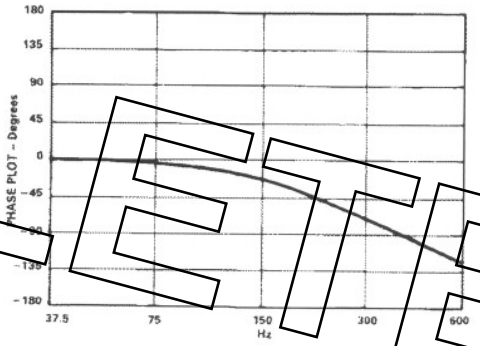

Figure 7. AD2S34xZ40 Phase Plot

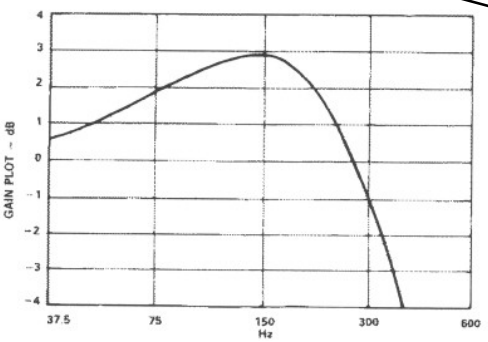

Figure 8. AD2S34xZ60 Gain Plot

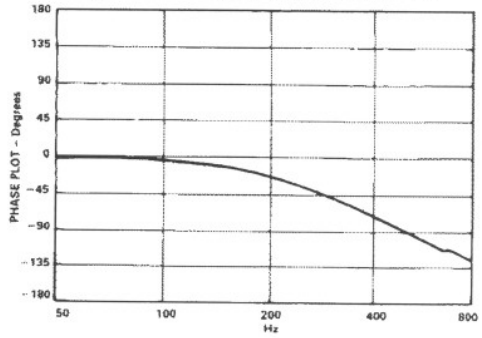

Figure 9. AD2S34xZ60 Phase Plot

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AD2S34

ACCELERATION ERROR

A tracking converter employing a Type 2 servo loop does not suffer any velocity lag, however, there is an additional error due to acceleration.

This additional error can be defined using the acceleration constant K_A of the converter.

$$K_A = \frac{Input\ Acceleration}{Error\ in\ Output\ Angle}$$

The numerator and denominator must have consistent angular units. For example, if K_A is in sec^{-2}, then the input acceleration may be specified in degrees/sec^2 and the error in output angle in degrees. Alternatively, the angular unit of measure may be in radians, minutes of arc, LSBs, etc.

K_A does not define maximum acceleration, only the error due to acceleration. The maximum acceleration for which the AD2S34 will not lose track is of the order of $5° \times K_A = 265000$ °/sec^2 or about 730 revolutions/sec^2 for the 400 Hz option.

K_A can be used to predict the output position error due to input acceleration. For example, for an acceleration of 50 revolutions/sec^2 with $K_A = 53000$,

$$\text{Error in LSBs} = \frac{\text{Input Acceleration [LSB/sec}^2\text{]}}{K_A\ [sec^{-2}]}$$

$$= \frac{50\ [rev/sec^2] \cdot 2^{14}\ [LSB/rev]}{53000\ [sec^{-2}]} = 15.5\ LSBs$$

RELIABILITY

The reliability of these products is very high due to the extensive use of custom chip circuits that decrease the active component count. Calculations of the MTBF figure under various environmental conditions are available on request.

Figure 10 shows the MTBF in years vs. case temperature for Naval Sheltered and Airborne Uninhabited Attack conditions calculated in accordance with MIL-HDBK-217E.

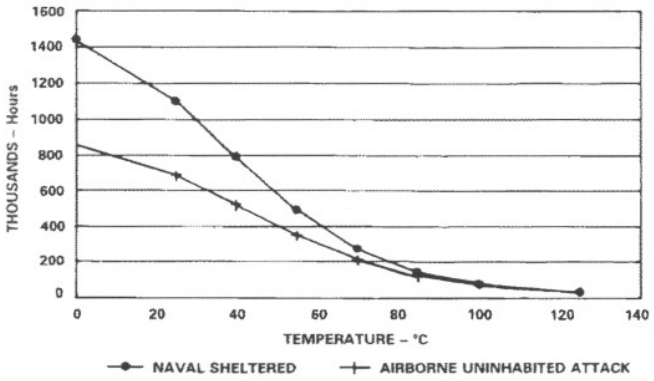


Figure 10. AD2S34 MTBF vs. Temperature

OTHER PRODUCTS

The AD2S44 is a low cost dual channel synchro or resolver converter with independent reference inputs and a built in test feature. The AD2S44 contains all the necessary front end electronics to interface directly to popular synchro and resolver options.

The AD2S80A/AD2S81A/AD2S82A are monolithic resolver-to-digital converters. The AD2S80A/AD2S82A offer selectable 10–16 bits of resolution. The AD2S81A has 12-bit resolution. All devices have user selectable dynamics. The AD2S80A is available in 40-pin DIP, 44-pin LCC and is qualified to MIL-STD-883B, Rev C. The 2S82A is available in a 44-pin PLCC, and the AD2S81A in a 28-pin DIP.

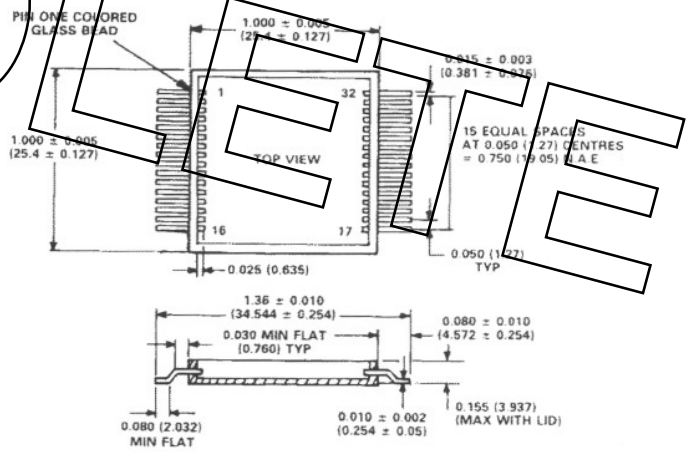
The AD2S46 is a highly integrated hybrid resolver/synchro-to-digital converter packaged in a 28-pin DIP. The part offers the user 1.3 arc minutes of accuracy over the full military temperature range.

The 1740/41/42 are hybrid resolver/synchro-to-digital converters which incorporate pico transformer isolated input signal conditioning.

OBSOLETE

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



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