Universal Synchro/Resolver Transformer Isolated Interface

AD2S75

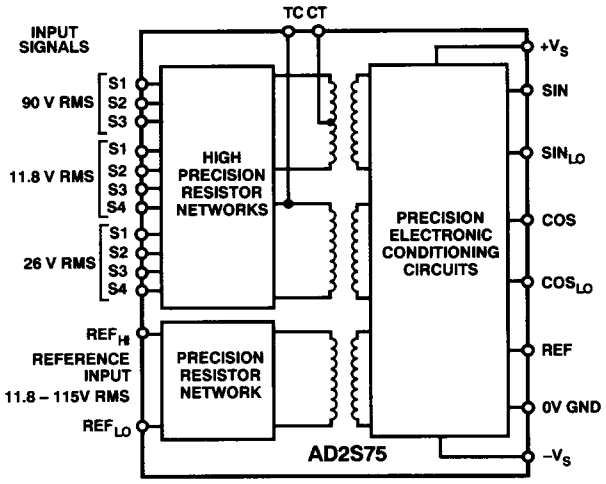
FEATURES

Universal Transformer Isolated Synchro/Resolver Interface
Supports All the Standard Synchro/Resolver Voltages
High Accuracy over Full Military Temperature Range
Wideband Performance: 56 Hz to 20,000 Hz
Not Achievable with Conventional Transformers
Wide Power Supply Range: ±5 to ±15 V dc
1000 V dc Transformer Isolation
Dimensions: 1.37 × 1.1 × 0.3 inch (35 × 27.7 × 7.6 mm)

APPLICATIONS

Universal Synchro/Resolver Interface
Military Systems/Equipment
Avionics
Factory Automation
Interfaces to Most R/DCs Including AD2S80A/81A/82A, AD2S83, AD2S90
Transformer Isolator, Signal Buffer, Signal Conditioning

BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD2S75 is a functionally complete, analog signal conditioning transformer interface for all the standard synchro/resolver format signals.

The AD2S75 performs synchro-to-resolver and resolver-to-resolver signal transformations. The device features signal inputs for 90 V rms, 26 V rms and 11.8 V rms, and outputs 2 V rms resolver format signals (sine and cosine). The reference frequency input accepts sinusoidal signals in the range 11.8 V rms to 115 V rms and outputs a nominal voltage of 2 V rms with enhanced zero crossing definition.

All inputs are isolated from the outputs and power supply lines by use of patent design miniature transformers thus providing true galvanic isolation. On the secondary (low side) of the isolation transformers, analog signal conditioning circuits are used to sustain the performance and stabilize the device over the wide operating temperature range as well as over the broad range of reference frequency.

The AD2S75 is a wide bandwidth device which operates over a reference frequency range of 56 Hz to 20,000 Hz. This covers the majority of commercially available synchros and resolvers for military and industrial use, thus providing the isolated interface for these types of transducers. The AD2S75 operates over the wide range of ±5 V dc to ±15 V dc nominal power supplies without degradation in accuracy or a reduction in the range of reference frequency.

The AD2S75AM operates over the industrial temperature range of −40°C to +85°C. The AD2S75SMB is designed to operate over the full military temperature range of −55°C to +125°C.

PRODUCT HIGHLIGHTS

Complete Synchro/Resolver Interface. The AD2S75 is a universal synchro/resolver interface for resolver-to-digital converters that accept 2 V rms resolver format signals. All the standard synchro/resolver voltages are catered for, thus eliminating the need for different voltage option devices to be ordered and to be held in stock.

1000 V dc Transformer Isolation. The AD2S75 continues the transformer isolated SDC/RDC tradition from Analog Devices. The internal miniature transformers present a balanced input regardless of other equipment that may be connected to the synchro, or resolver.

True Galvanic Isolation. 1000 V dc input to output isolation regardless of input voltage amplitude level. The galvanic isolation completely eliminates ground loops between the transducer and the converter, thus minimizing errors.

High Common-Mode Voltage consistent across all input voltage ranges. Electronic solid state conditioning circuits are input voltage amplitude dependent.

Ratiometric Inputs. Eliminate errors due to parasitic capacitance effects and enhance the accuracy performance of synchros and resolvers.

REV. A

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AD2S75—SPECIFICATIONS (typical at +25°C, $\pm V_S$ = ±15 V and nominal input voltages unless specified otherwise)

Parameter	Min	Typ	Max	Units	Comments/Test Conditions
ACCURACY					
60 Hz, 400 Hz		0.33	**1.32**	arc min	Reference Frequency, Accuracy Tested at 60,
2600 Hz		0.66	**1.98**	arc min	400, and 2600.
ACCURACY T_{MIN} to T_{MAX}			**2.5**	arc min	
SIGNAL INPUT FORMAT[1]					Either Synchro or Resolver
SIGNAL INPUTS[1, 2]					
90 V Synchro S1, S2, S3	81	90	99	V rms	Line to Line
90 V Synchro Input Impedance		200.0		kΩ	Resistive, Tolerance ±0.1% (Including Transformer Winding Resistance)
11.8 V Synchro S1, S2, S3	10.6	11.8	13	V rms	Line to Line
11.8 V Synchro Input Impedance		26.25		kΩ	Resistive, Tolerance ±0.1% (Including Transformer Winding Resistance)
26 V Resolver S1, S2, S3, S4	23.4	26	28.6	V rms	Line to Line
26 V Resolver Input Impedance		57.8		kΩ	Resistive, Tolerance ±0.1% (Including Transformer Winding Resistance)
11.8 V Resolver S1, S2, S3, S4	10.6	11.8	13	V rms	Line to Line
11.8 V Resolver Input Impedance		26.25		kΩ	Resistive Tolerance ±0.1% (Including Transformer Winding Resistance)
OUTPUT SIGNAL FORMAT					Resolver Format 2 V rms
Output Signals (SIN to SIN_{LO}, COS to COS_{LO})	**1.980**	2	**2.020**	V rms	Tested with Nominal Input Voltage at 400 Hz
SIGNAL OUTPUT IMPEDANCE		100		mΩ	
SIGNAL OUTPUT DRIVE CAPABILITY		100		pF	
SIGNAL CURRENT OUTPUT DRIVE	**4.3**	20		mA peak	Minimum Refers to Operation with Supplies $\pm V_S$ = ±5 V dc
SIGNAL OUTPUT OFFSET SIN, COS		2	**10**	mV	Measured across SIN, SIN_{LO} and COS, COS_{LO}
OUTPUT SIGNAL PHASE SHIFT					SIN, COS with Respect to Reference,
60 Hz, 400 Hz		0.66		degrees	Measured at Zero Crossings,
2600 Hz		0.25		degrees	Average of Both Alignments.
OUTPUT SIGNALS DIFFERENTIAL PHASE SHIFT					SIN with Respect to COS, Measured at
60 Hz, 400 Hz		0.66		degrees	Zero Crossings, Average of Both
2600 Hz		0.25		degrees	Alignments.
REFERENCE INPUT SIGNAL VOLTAGE[1, 2]		11.8–115		V rms	Reference Frequency = 60 Hz to 20000 Hz
Reference Input Impedance		81		kΩ	Resistive, Tolerance ±2%
REFERENCE OUTPUT VOLTAGE SIGNAL					Zero Crossing Transition Enhanced Waveform
I/P 11.8 V rms	0.8	1.2	1.4	V rms	Output Signal Consists of a 1.1 V Square Wave
I/P 26 V rms	1.1	1.4	1.7	V rms	(at Reference Frequency) on Which Is Super-
I/P 115 V rms	2.0	2.3	2.6	V rms	imposed a Sinusoid of Amplitude 1/50 of Reference Frequency.
REFERENCE OUTPUT IMPEDANCE		400		mΩ	
REFERENCE OUTPUT DRIVE CAPACITANCE		100		pF	See Load Considerations
REFERENCE CURRENT OUTPUT DRIVE	3	10		mA peak	Minimum Refers to Operation with Supplies $\pm V_S$ = ±5 V dc
TRANSFORMER ISOLATION					
Input to Output	±1000			V dc	With Respect to Grounded Secondary
Common-Mode Range		600		V rms	400 Hz
Input to Case (GND)		±1000		V dc	
POWER SUPPLIES					
Voltage Levels					
$+V_S$	+4.75		+15.75	V dc	
$-V_S$	−4.75		−15.75	V dc	
$+I_S$		13	**18**	mA	$+V_S$ = +5 V dc
$-I_S$		13	**18**	mA	$-V_S$ = −5 V dc
$+I_S$		15	**20**	mA	$+V_S$ = +15 V dc
$-I_S$		15	**20**	mA	$-V_S$ = −15 V dc
Power Dissipation			**180**	mW	$\pm V_S$ = ±5 V dc
			600	mW	$\pm V_S$ = ±15 V dc

Parameter	Min	Typ	Max	Units	Comments/Test Conditions
POWER SUPPLY SENSITIVITY		0.05	0.2	arc min	$\pm V_S$ = ±5 V dc to ±15 V dc
DIMENSIONS					See Outline Dimension
WEIGHT		20		gm	

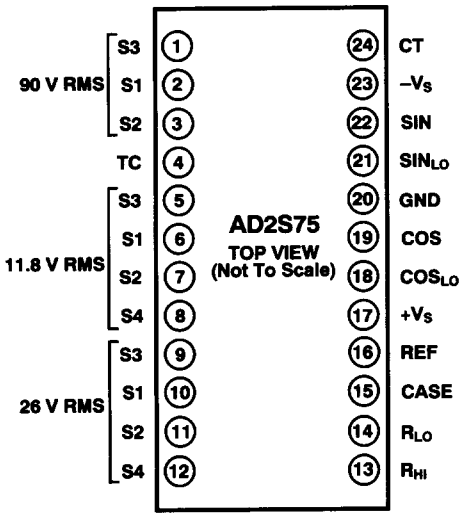
NOTES
[1]Specified for: (a) ±10% signal and reference amplitude variation; (b) 10% reference harmonic distortion; (c) ±5% power supply variation; (d) ±10% variation in reference frequency.
[2]For power supply voltages $\pm V_S$ less than ±6 V dc, signal and reference input voltage overdrive should be constrained to ±5% maximum.
Boldface type indicates parameters which are 100% tested at nominal values of power supplies, input signal and reference voltage amplitude and operating frequency. All other parameters are guaranteed by design and are not tested.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

$+V_S$ to GND[2] . . . . . +17.25 V dc
$-V_S$ to GND[2] . . . . . −17.25 V dc
Reference Input Signal Voltage . . . . . 130 V rms
Case Operating Temperature Range . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability Only one Absolute Maximum Rating may be applied at any time.
[2]Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins and must not be reversed.

PIN CONFIGURATION



ORDERING GUIDE

Model	Operating Temperature Range	Package Option
AD2S75AM	−40°C to +85°C	M-24
AD2S75SMB	−55°C to +125°C	M-24

PIN DESCRIPTION

Pin	Mnemonic	Description
1, 2, 3	S3, S1, S2	90 V rms Synchro Signal Inputs
4	TC	"TEASER" winding-connect to CT, Pin 24, for Synchro input signals. Do not connect for Resolver signals.
5 6 7 8	S3 S1 S2 S4	11.8 V rms Synchro signal inputs to S3, S1, S2. (S4 not connected) 11.8 V rms Resolver signal inputs (SINE) to S3, S1, (COSINE) to S2, S4. For Resolver, S3–S1 is the effective SINE signal, S2–S4 is the effective COSINE signal.
9 10 11 12	S3 S1 S2 S4	26 V rms Resolver signal inputs (SINE) to S3, S1, (COSINE), to S2, S4. For Resolver, S3–S1 is the effective SINE signal, S2–S4 is the effective COSINE signal. 26 V rms Synchro signal inputs (non standard) to S3, S1, S2, do not connect S4.
13	R_{HI}	Reference Input HI Synchro and Resolver.
14	R_{LO}	Reference Input LO Synchro and Resolver.
15	CASE	Connect to 0 V, GND Pin 20.
16	REF	Reference output signal connect to R/DC. Reference output measured with respect to 0 V, GND Pin 20.
17	$+V_S$	Positive power supply line +5 V dc to +15 V dc
18	COS_{LO}	Cosine output signal return.
19	COS	Cosine output signal. Connect to COS Input of R/DC.
20	GND	Analog ground, 0 V power supplies common.
21	SIN_{LO}	Sine output signal return.
22	SIN	Sine output signal. Connect to SIN input of R/DC.
23	$-V_S$	Negative power supply line −5 V dc to −15 V dc.
24	CT	Center tap of primary windings. Synchro input signals only—connect to TC Pin 4. Resolver signals do not connect. See connection diagrams.

SYNCHRO FORMAT SIGNALS

A synchro is an electromagnetic rotational transducer (forerunner of the resolver) that detects angular displacement. The synchro consists of a fixed stator, which houses three pickup windings which are star connected, 120° apart. The rotor contains the ac excitation (Reference) winding which is connected to terminals via slip rings and brushes.

The voltage induced in any stator winding, by the rotor, will be proportional to the sine of the angle θ between the rotor coil axis and the stator coil axis.

The voltage induced across any pair of stator terminals will be the sum or the difference, depending on the phase of the voltages across the two coils concerned.

The excitation voltage of the rotor, applied across R1 and R2, is of the form:

A sin ωt

The voltages which would appear across the stator terminals will be:

S3 to S1 = AR sin ωt sin θ
S2 to S3 = AR sin ωt sin (θ + 120°)
S1 to S2 = AR sin ωt sin (θ + 240°)

where:

R = transformation ratio of the transducer.
A = amplitude of the excitation voltage signal.
sin ωt = excitation frequency.
θ = the synchro shaft angle.

Note: The S1, S2 and S3 outputs for synchros are **phase coherent signals**.

An equivalent electrical representation and diagram of the typical output signal formats for a synchro are shown in Figure 1.

Note: Standard notation for the rotation of synchros is counter clockwise (CCW) shaft movement for an increasing angle as viewed from the transducer shaft end.

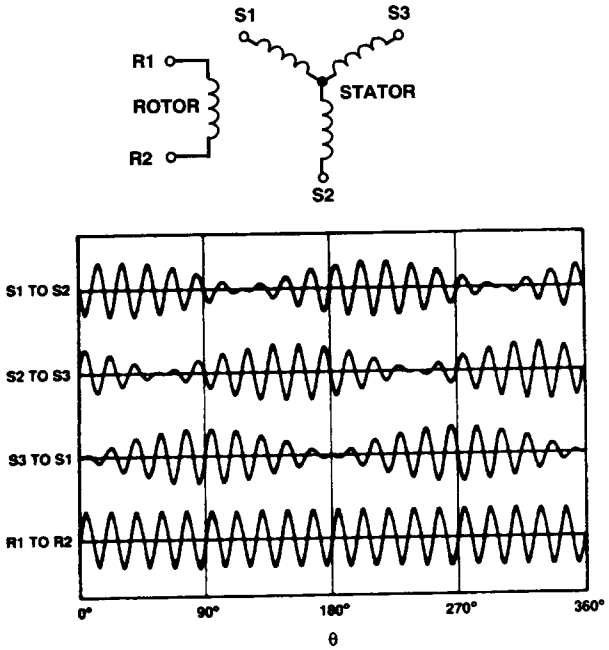


Figure 1. Electrical Representation and Typical Synchro Signals

RESOLVER FORMAT SIGNALS

A resolver is an electromagnetic, rotational transducer that detects angular displacement. Most modern resolvers are "brushless." An ac excitation (reference) signal is applied to the stator (primary reference winding); in turn a voltage is induced in the rotor which subsequently induces a voltage in two pickup windings sine and cosine, which are also located in the stator (secondaries), spaced 90° apart.

The induced voltages (secondaries) ratios are amplitude modulated by the sine and the cosine of the angle θ of the rotor relative to the stator.

The excitation voltage is of the form:

A sin ωt

The voltages which would appear across the stator terminals will be:

Sine: S3 to S1 = AR sin ωt sin θ
Cosine: S2 to S4 = AR sin ωt cos θ

where:

A = amplitude of the excitation voltage signal
R = transformation ratio of the transducer
sin ωt = excitation frequency
θ = the resolver shaft angle

Note: the S1, S2, S3 and S4 outputs for resolvers are **phase coherent signals**.

An equivalent electrical representation and diagram of the typical output signals format for a resolver are shown in Figure 2.

Note: Standard notation for the rotation of resolvers is clockwise (CW) shaft movement for an increasing angle as viewed from the transducer shaft end.

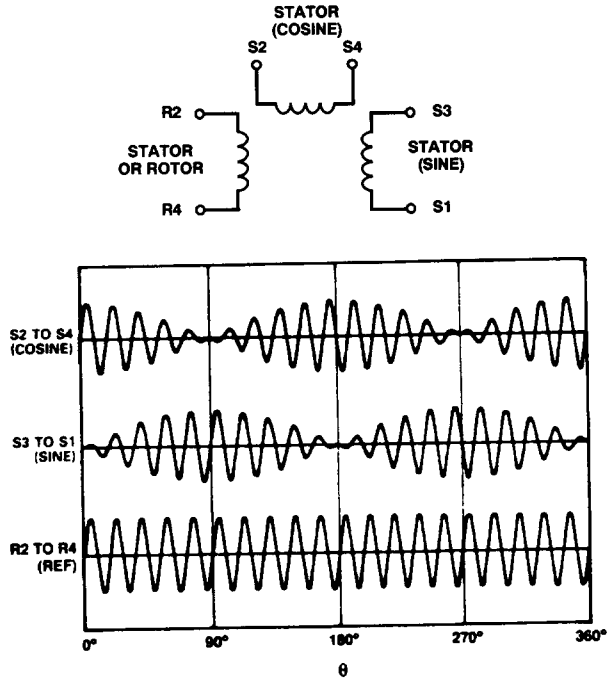


Figure 2. Electrical Representation and Typical Resolver Signals

AD2S75 USER BENEFITS

The AD2S75 is a user friendly interface device which minimizes many potential sources of error. However errors can occur due to the nonideal generation of the transducer signals and their subsequent distribution, limitations such as:

- Finite output impedance of the transducer.
- Imbalance between transducer impedances.
- Imbalance in chassis wiring impedances.

These errors are minimized by the use of the AD2S75 which employs balanced, high precision, high impedance, transformer isolated, input networks. This allows system accuracies to be maintained, even when long chassis wiring runs are required between synchro/resolver transducer and the AD2S75. Accuracy is maintained by the simple control of resistive balance of the transducer signals. This overall balance requirement is dominated by the precision input resistor network; which greatly reduces the balance requirements placed on the transducer and associated chassis wiring. When using the AD2S75, the sensitivities to signal distribution imbalance (mismatch) are of the order:

Synchro	90 V	87.3 Ω/arc min or 28.8 Ω/bit in 16
	11.8 V	11.4 Ω/arc min or 3.8 Ω/bit in 16
Resolver	26 V	16.8 Ω/arc min or 5.5 Ω/bit in 16
	11.8 V	7.6 Ω/arc min or 2.5 Ω/bit in 16

Thus 22 AWG wire at 17 mΩ per foot and PCB tracking using 0.012 inch 1 oz. Cu at 400 mΩ per foot will not introduce significant errors provided simple control of resistive balance is maintained.

The use of the AD2S75 eliminates errors due to ill defined ground loop currents. This is achieved by the galvanic isolation of the internal transformers and strict adherence to analog star point sensing internal to the AD2S75, and between the AD2S75 and the RDC as shown in the following connection diagrams.

Errors due to signal loading effects on the SIN and COS outputs are minimized by providing balanced, low output impedances, together with distinct and separate four wire transmission for SIN, SIN_{LO} and COS, COS_{LO}. Full angular accuracy is maintained from zero to maximum output current drive capability.

Capacitive loading considerations (100 pF maximum) indicate that the AD2S75 should be sited close to its load, often a AD2S80A. Provided the capacitive loading limits are met, then the AD2S75 can be sited in accordance with user preference.

CONNECTING THE TRANSDUCERS TO THE AD2S75 INTERFACE

Synchro

Synchros are available in two standard voltage ranges:

(a) 90 V rms line-to-line signals, 115 V rms reference, nominal frequency 400 Hz or 60 Hz.

(b) 11.8 V rms line-to-line signals, 26 V rms reference, nominal frequency 400 Hz.

For nonstandard voltages, please see section "Resistive Scaling of Inputs."

The signals from the synchro should be connected to the appropriate inputs. Refer to pin configuration diagram.

90 V: connect S3 to Pin 1, S1 to Pin 2, S2 to Pin 3.
11.8: connect S3 to Pin 5, S1 to Pin 6, S2 to Pin 7.

Note: S4 (Pin 8) should be left unconnected for synchro signals and connected for use with 11.8 V resolver signals only.

TC, Pin 4 should be connected to CT, Pin 24.

The reference input signal, either 115 V or 26 V, should be connected to R_{HI} and R_{LO}, Pins 13 and 14, respectively.

After the synchro output signals have been connected and the devices have been powered up, the synchro signals transformed to resolver signals should be as shown in Figures 1 and 2, respectively.

Note that the standard notation for the rotation of a synchro, for increasing angle is counter clockwise (CCW) as viewed from the transducer's shaft end.

Resolver

Resolvers are available in a variety of voltages. The three standard voltage ranges (most common) are:

(a) 11.8 V rms, line-to-line signals, 11.8 V rms reference, various frequencies between 400 Hz to 10,000 Hz.

(b) 26 V rms, line-to-line signals, 26 V rms reference, various frequencies between 400 Hz to 10,000 Hz.

(c) 11.8 V rms, line-to-line signals, 26 V rms reference, various frequencies between 400 Hz to 10,000 Hz.

For nonstandard voltages, please refer to section "Resistive Scaling of Inputs."

The signals from the resolver should be connected to appropriate inputs. Refer to pin configuration diagram.

11.8 V: Connect the Sine signal to S3, S1, Pins 5 and 6, S1 being the voltage measurement reference point. Connect the Cosine signal to S2, S4, Pins 7 and 8, S4 being the voltage measurement reference point.

26 V: Connect the Sine signal to S3, S1, Pins 9 and 10, S1 being the voltage measurement reference point. Connect the Cosine signal to S2, S4, Pins 11 and 12, S4 being the voltage measurement reference point.

TC Pin 4 and CT Pin 24 should not be connected.

The reference input signal should be connected to R_{HI} and R_{LO}, Pins 13 and 14, respectively.

After the connections have been completed and the devices have been powered up, the output signals from the AS2S75 should be as shown in Figure 2.

Note that the standard notation for the rotation of a resolver, for increasing angle is clockwise (CW), as viewed from the transducer's shaft end.

GENERAL GOOD ENGINEERING PRACTICE

The AD2S75 offers the user numerous benefits. This section describes techniques which will enable the user to achieve the specified performance of the device.

Wiring Practice

The recommended cable for interconnecting synchros to equipment is a three-way twisted cable. Such a cable will eliminate any radiated electromagnetic interference, and will have minimum capacitance as there is no need for an earthed screen. This will also present a balanced load to the transducer.

The recommended cable for interconnecting resolvers to equipment would be three separate screened twisted pair cables for the sine, cosine and reference signals. Further information should be obtained by consulting with the synchro and resolver suppliers.

Layout Considerations

The high voltage input signals, including reference, should be kept physically remote from the precision low voltage output signals.

Input signal track pairs, i.e., S3, S1 should be routed using parallel, physically adjacent PCB tracks that employ the same PCB layer. This minimizes external radiation that could corrupt low level precision analog signals. Distinct signal track pairs, i.e., R_{HI}–R_{LO} and S3–S1 should be routed physically separate. This minimizes mutual interference coupling whereby large amplitude signals can corrupt low level signals. This is angle dependent as shown in Figures 1 and 2, e.g., Cosine or Reference coupling to Sine at 0° (Figure 2).

A ground/power plane should not be sited underneath these high voltage input signal tracks as these signals can corrupt the noise integrity of the plane.

Errors due to ill defined ground loop currents should be avoided. The use of the AD2S75 enables the complete elimination of these errors using galvanic isolation within the internal transformers while retaining rigid adherence to analog star point sensing internal to the AD2S75 and between the AD2S75 and the RDC, as shown in the following connection diagrams. Note that the signal grounds have been connected to 0 V at the source of the signal.

CONNECTING THE AD2S75 TO A RESOLVER-TO-DIGITAL CONVERTER

The power supply voltages connected to $+V_S$ and $-V_S$, Pins 17 and 23, should be within the range of +5 V dc to +15 V dc and −5 V dc to −15 V dc, respectively, with respect to 0 V, (GND Pin 20), and must not be reversed.

It is recommended that a 100 nF (ceramic) decoupling capacitor should be connected between each of the supply pins and GND. The decoupling capacitors should be placed as near to the device as possible.

The metal package CASE, Pin 15, should be connected to 0 V, GND, Pin 20, to screen the internal circuits from any external noise and aid the operation of the magnetic circuits within the device.

The AD2S75 is a universal synchro/resolver interface for resolver-to-digital converters that accept 2 V rms input signals. The following converters from the Analog Devices range can be used directly with the AD2S75 and benefit from the transformer isolated interface:

AD2S80A series—monolithic, variable resolution RDC all accuracy grades, including the AD2S81A, AD2S82A, AD2S83 and AD2S90. For connections, please see Figure 3.

General

The Sine signal output from the AD2S75 is from SIN and SIN_{LO}, Pins 22 and 21, respectively.

The Cosine signal output from the AD2S75 is from COS and COS_{LO}, Pins 19 and 18, respectively.

The Reference signal output from the AD2S75 is from REF and GND, Pins 16 and 20 respectively.

The above signals should be connected to the appropriate input pins of the RDC.

The following should be noted:

Place the AD2S75 near to the RDC to minimize any external noise pickup.

Connect the signals from the AD2S75 to the RDC using equal lengths of pcb track so as to minimize differential phase shifts. The tracks should be routed in close proximity, parallel to each other on the same side of the pcb. Avoid the use of ground/power planes near the route of the ac signals so to avoid ac coupling and phase shifts caused by parasitic capacitance.

Connecting the AD2S75 to AD2S80A Series of RDCs
The following information also applies to AD2S81A, AD2S82A, AD2S83, and AD2S90.

The above resolver-to-digital converters (RDCs) have single ended amplifier inputs for the SIN and COS signals. It is recommended that SIN_{LO} and COS_{LO} are connected individually to a "star" point at SIGNAL GND, Pin 6 of the RDC. This eliminates any errors due to movement of the measurement reference point (SIGNAL GND).

The above is particularly important when the RDC is used at 14- to 16-bit resolution, medium to high accuracy applications.

For detailed information on the AD2S80A series of RDC, please see the relevant data sheets.

Please see Figure 3.

RESISTIVE SCALING OF INPUTS

The AD2S75 signal and reference inputs can be scaled by using resistors to accommodate any voltage input (above 10.6 V rms).

Note: The accuracy of the interface and subsequently the accuracy of an R/DC, will be affected by the matching accuracies of the resistors used for the external scaling.

The current into any of the S1, S2, S3 and S4 inputs is very precisely controlled to 0.450 mA.

The total resistance in series with the signal inputs should be 2.222 kΩ per extra volt of signal. To calculate the values of the external scaling input resistors, add 1.111 kΩ per extra volt of input signal in series with S1, S2, S3 for a synchro, and S1, S2, S3, S4 for a resolver. For example to interface a 57.5 V rms line to line Magslip to the AD2S75 either:

(a) Into 26 V Inputs; use 35,000 Ω in series with each input; S1 Pin 10, S2 Pin 11 and S3 Pin 9. Leave S4 Pin 12 unconnected.

or

(b) Into 11.8 V Inputs; use 50,777.8 Ω in series with each input; S1 Pin 6, S2 Pin 7, S3 Pin 5. Leave S4 Pin 8 unconnected.

For example to interface a 48 V rms line-to-line resolver to the AD2S75 either:

(a) Into 26 V Inputs; use 24,444.4 Ω in series with S1 Pin 10, S2 Pin 11, S3 Pin 9 and S4 Pin 12.

or

(b) Into 11.8 V Inputs; use 40,222.2 Ω in series with S1 Pin 6, S2 Pin 7, S3 Pin 5 and S4 Pin 8.

The current into the reference input is controlled to 1.42 mA. For reference signals in excess of 115 V rms, please add 707 Ω per extra volt of input signal in series with R_{HI}, Pin 13, and R_{LO}, Pin 14.

External Resistor tolerance requirements are reduced by employing the highest standard internal voltage input available.

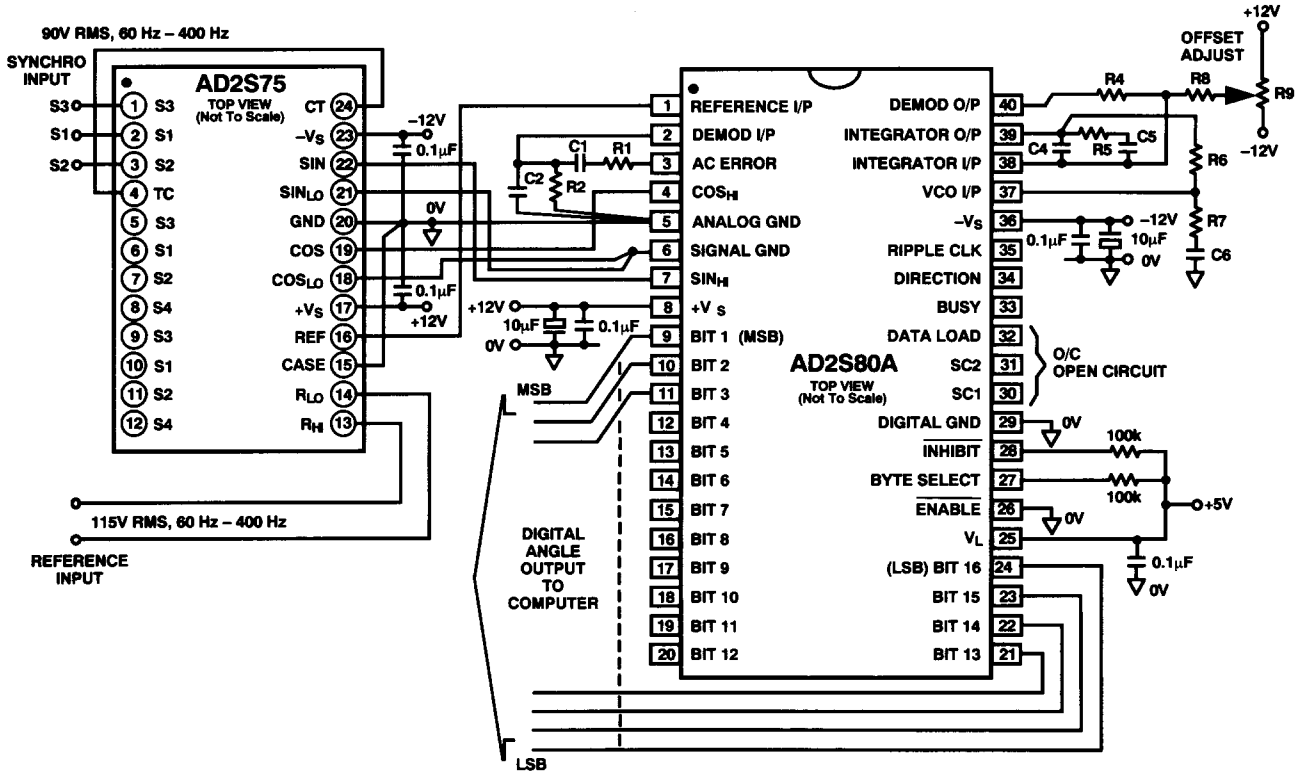


Figure 3. Using the AD2S75 to Interface a 90 V Signal, 115 V Reference, 60 Hz–400 Hz, Synchro to AD2S80A Resolver-to-Digital Converter

DYNAMIC PERFORMANCE

The closed-loop frequency response of the AD2S75 is shown below:

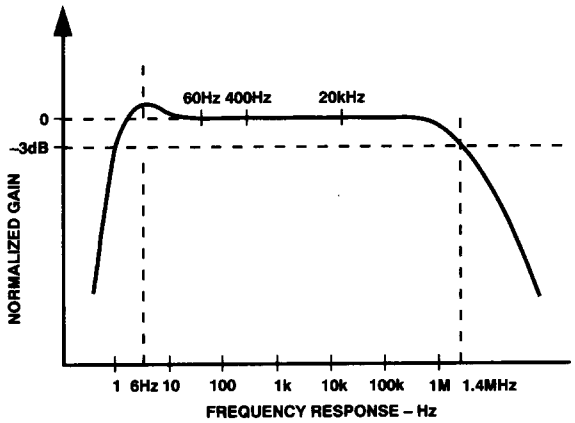


Figure 4. AD2S75 Closed-Loop Frequency Response

The reference output waveform is shown below.

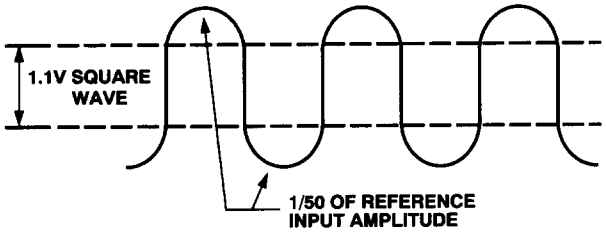


Figure 5. AD2S75 Reference Output Waveform

RELIABILITY

Figure 6 shows the MTBF in years versus case temperature for conditions, calculated in accordance with MIL-HDBK-217E.

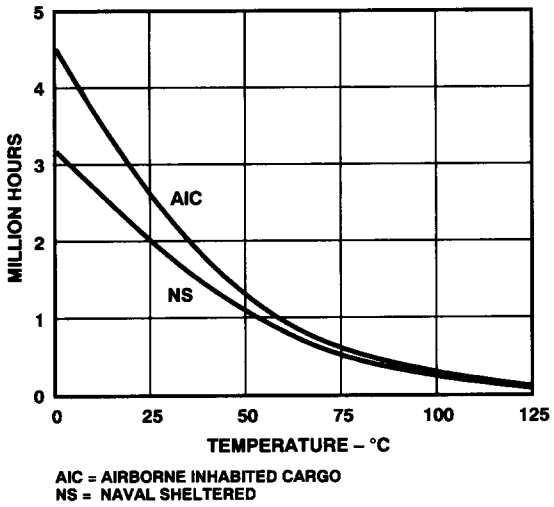
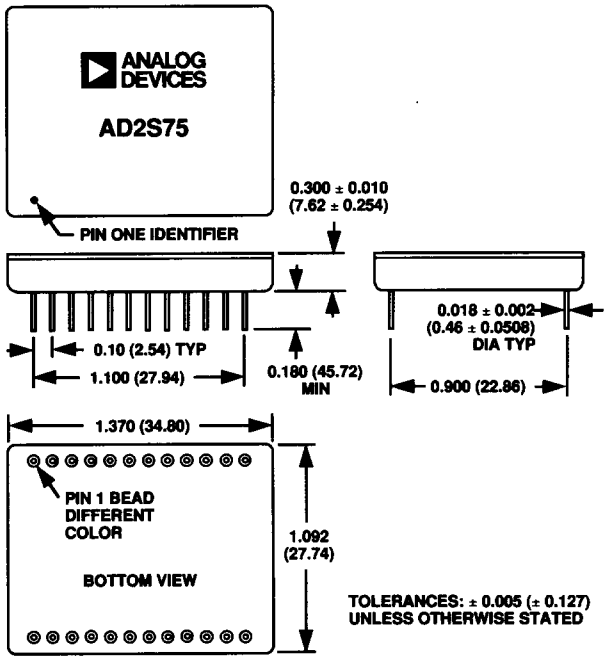


Figure 6. 2S75 vs. Temperature

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



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