

# 74LVU04

## Hex inverter

Rev. 06 — 20 December 2007

Product data sheet

## 1. General description

---

The 74LVU04 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HCU04.

The 74LVU04 is a general purpose hex inverter. Each of the six inverters is a single stage with unbuffered outputs.

## 2. Features

---

- Wide operating voltage: 1.0 V to 5.5 V
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Typical output ground bounce < 0.8 V at  $V_{CC} = 3.3$  V and  $T_{amb} = 25$  °C
- Typical HIGH-level output voltage ( $V_{OH}$ ) undershoot: > 2 V at  $V_{CC} = 3.3$  V and  $T_{amb} = 25$  °C
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

## 3. Applications

---

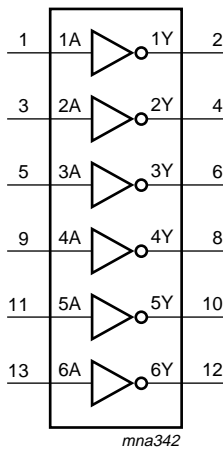
- Linear amplifier
- Crystal oscillator
- Astable multivibrator

### 4. Ordering information

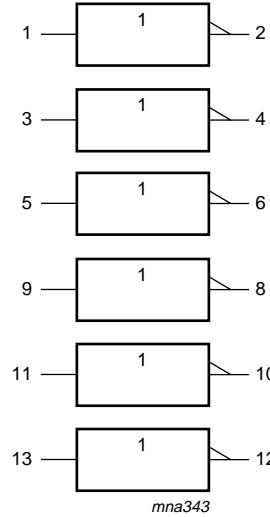
Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVU04N	-40 °C to +125 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74LVU04D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVU04DB	-40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LVU04PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LVU04BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

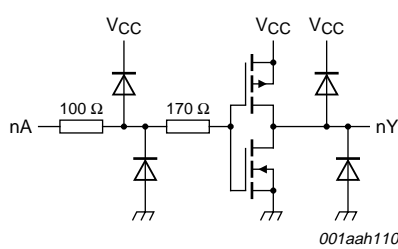
### 5. Functional diagram



**Fig 1. Logic symbol**



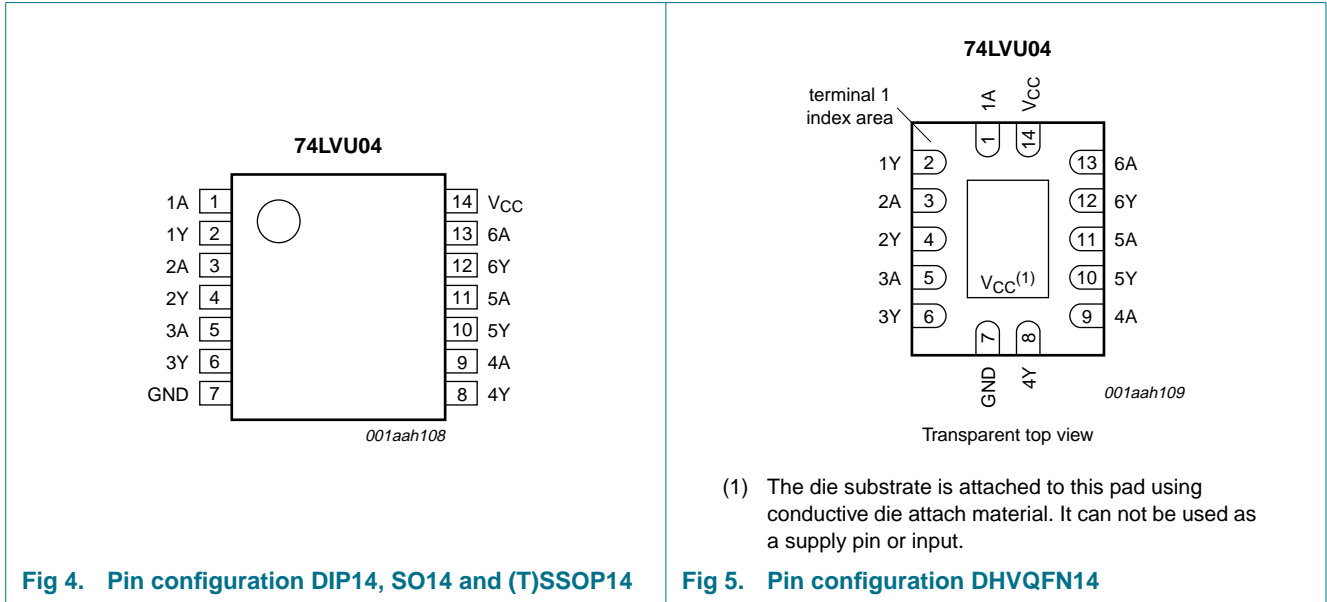
**Fig 2. IEC logic symbol**



**Fig 3. Circuit diagram (one inverter)**

## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A	1	data input
1Y	2	data output
2A	3	data input
2Y	4	data output
3A	5	data input
3Y	6	data output
GND	7	ground (0 V)
4Y	8	data output
4A	9	data input
5Y	10	data output
5A	11	data input
6Y	12	data output
6A	13	data input
V <sub>CC</sub>	14	supply voltage

## 7. Functional description

**Table 3. Function table**<sup>[1]</sup>

Input nA	Output nY
L	H
H	L

[1] H = HIGH voltage level;  
L = LOW voltage level.

## 8. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	[1] -	±20	mA
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	[1] -	±50	mA
$I_O$	output current	$V_O = -0.5\text{ V}$ to $(V_{CC} + 0.5\text{ V})$	-	±25	mA
$I_{CC}$	supply current		-	50	mA
$I_{GND}$	ground current		-50	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$			
		DIP14 package	[2] -	750	mW
		SO14 package	[3] -	500	mW
		(T)SSOP14 package	[4] -	500	mW
		DHVQFN14 package	[5] -	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- [2]  $P_{tot}$  derates linearly with 12 mW/K above 70 °C.
- [3]  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.
- [4]  $P_{tot}$  derates linearly with 5.5 mW/K above 60 °C.
- [5]  $P_{tot}$  derates linearly with 4.5 mW/K above 60 °C.

## 9. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		[1] 1.0	3.3	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.0\text{ V to }2.0\text{ V}$	-	-	500	ns/V
		$V_{CC} = 2.0\text{ V to }2.7\text{ V}$	-	-	200	ns/V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	-	100	ns/V
		$V_{CC} = 3.6\text{ V to }5.5\text{ V}$	-	-	50	ns/V

[1] The static characteristics are guaranteed from  $V_{CC} = 1.2\text{ V}$  to  $V_{CC} = 5.5\text{ V}$ , but LV devices are guaranteed to function down to  $V_{CC} = 1.0\text{ V}$  (with input levels GND or  $V_{CC}$ ).

## 10. Static characteristics

**Table 6. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 1.2\text{ V}$	1.0	-	-	1.0	-	V
		$V_{CC} = 2.0\text{ V}$	1.6	-	-	1.6	-	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2.4	-	-	2.4	-	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$0.8V_{CC}$	-	-	$0.8V_{CC}$	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 1.2\text{ V}$	-	-	0.2	-	0.2	V
		$V_{CC} = 2.0\text{ V}$	-	-	0.4	-	0.4	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	-	0.5	-	0.5	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	$0.2V_{CC}$	-	$0.2V_{CC}$	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$						
		$I_O = -100\ \mu\text{A}; V_{CC} = 1.2\text{ V}$	-	1.2	-	-	-	V
		$I_O = -100\ \mu\text{A}; V_{CC} = 2.0\text{ V}$	1.8	2.0	-	1.8	-	V
		$I_O = -100\ \mu\text{A}; V_{CC} = 2.7\text{ V}$	2.5	2.7	-	2.5	-	V
		$I_O = -100\ \mu\text{A}; V_{CC} = 3.0\text{ V}$	2.8	3.0	-	2.8	-	V
		$I_O = -100\ \mu\text{A}; V_{CC} = 4.5\text{ V}$	4.3	4.5	-	4.3	-	V
		$I_O = -6\text{ mA}; V_{CC} = 3.0\text{ V}$	2.4	2.82	-	2.2	-	V
$I_O = -12\text{ mA}; V_{CC} = 4.5\text{ V}$	3.6	4.2	-	3.5	-	V		

**Table 6. Static characteristics ...continued**  
 Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.2 V	-	0	-	-	-	V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 2.0 V	-	0	0.2	-	0.2	V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 2.7 V	-	0	0.2	-	0.2	V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 3.0 V	-	0	0.2	-	0.2	V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 4.5 V	-	0	0.2	-	0.2	V
		I <sub>O</sub> = 6 mA; V <sub>CC</sub> = 3.0 V	-	0.25	0.40	-	0.50	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 4.5 V	-	0.35	0.55	-	0.65	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	1.0	-	1.0	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	20.0	-	40	μA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C.

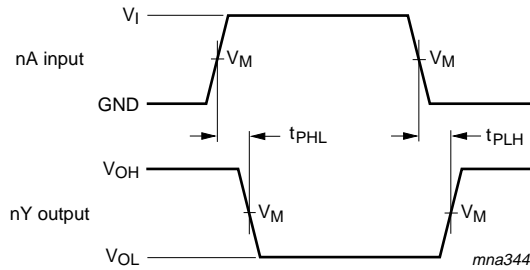
## 11. Dynamic characteristics

**Table 7. Dynamic characteristics**  
 GND = 0 V; For test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
t <sub>pd</sub>	propagation delay	nA, nB to nY; see <a href="#">Figure 6</a> <sup>[2]</sup>						
		V <sub>CC</sub> = 1.2 V	-	35	-	-	-	ns
		V <sub>CC</sub> = 2.0 V	-	12	14	-	17	ns
		V <sub>CC</sub> = 2.7 V	-	9	10	-	13	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V; C <sub>L</sub> = 15 pF <sup>[3]</sup>	-	6	-	-	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[3]</sup>	-	7	8	-	10	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	7	-	9	ns
C <sub>PD</sub>	power dissipation capacitance	C <sub>L</sub> = 50 pF; f <sub>i</sub> = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> <sup>[4]</sup>	-	18	-	-	-	pF

- [1] All typical values are measured at T<sub>amb</sub> = 25 °C.
- [2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.
- [3] Typical values are measured at nominal supply voltage (V<sub>CC</sub> = 3.3 V).
- [4] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:  
 f<sub>i</sub> = input frequency in MHz, f<sub>o</sub> = output frequency in MHz  
 C<sub>L</sub> = output load capacitance in pF  
 V<sub>CC</sub> = supply voltage in V  
 N = number of inputs switching  
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

12. Waveforms



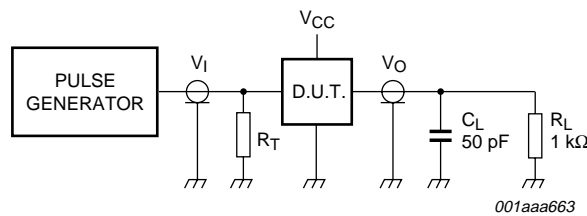
Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

Fig 6. The input (nA) to output (nY) propagation delays

Table 8. Measurement points

Supply voltage	Input	Output
$V_{CC}$	$V_M$	$V_M$
< 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$
2.7 V to 3.6 V	1.5 V	1.5 V
$\geq 4.5$ V	$0.5V_{CC}$	$0.5V_{CC}$



Test data is given in [Table 9](#).

Definitions test circuit:

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

Fig 7. Load circuit for switching times

Table 9. Test data

Supply voltage	Input	$t_r, t_f$
$V_{CC}$	$V_I$	$t_r, t_f$
< 2.7 V	$V_{CC}$	$\leq 2.5$ ns
2.7 V to 3.6 V	2.7 V	$\leq 2.5$ ns
$\geq 4.5$ V	$V_{CC}$	$\leq 2.5$ ns

13. Transfer characteristics

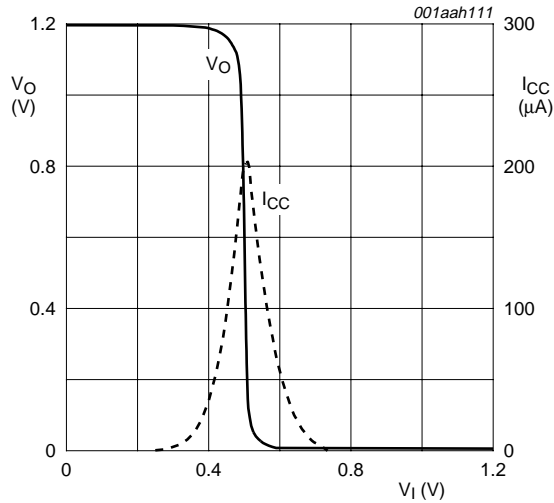


Fig 8.  $V_{CC} = 1.2\text{ V}; I_O = 0\text{ A}$   
 $T_{amb} = 25\text{ }^\circ\text{C}.$

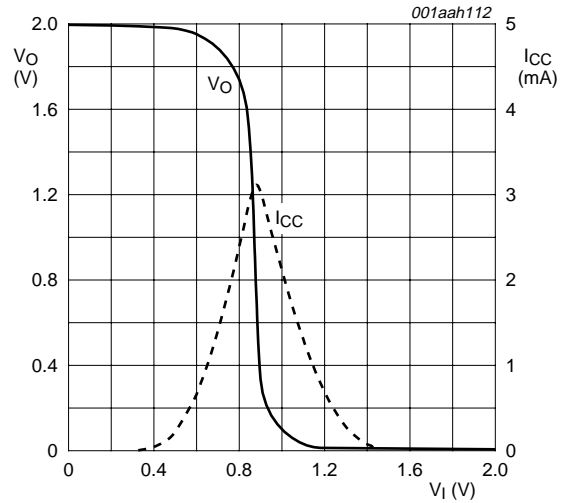


Fig 9.  $V_{CC} = 2.0\text{ V}; I_O = 0\text{ A}$   
 $T_{amb} = 25\text{ }^\circ\text{C}.$

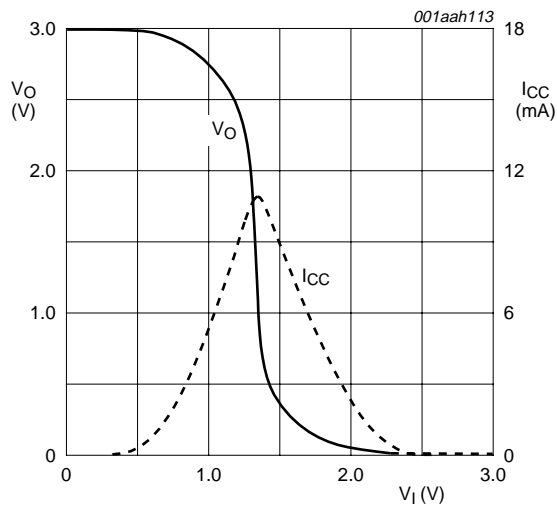
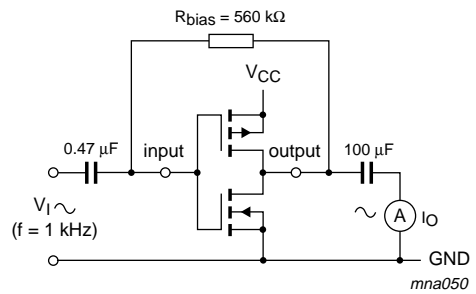


Fig 10.  $V_{CC} = 3.0\text{ V}; I_O = 0\text{ A}$   
 $T_{amb} = 25\text{ }^\circ\text{C}.$

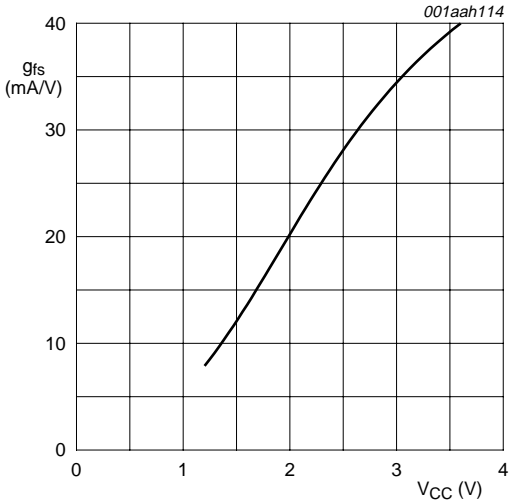


$$g_{fs} = \frac{\Delta I_O}{\Delta V_I}$$

$f_i = 1\text{ kHz}$  at  $V_O$  is constant

Fig 11. Test set-up for measuring forward transconductance





T<sub>amb</sub> = 25 °C.

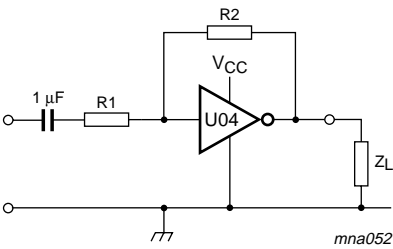
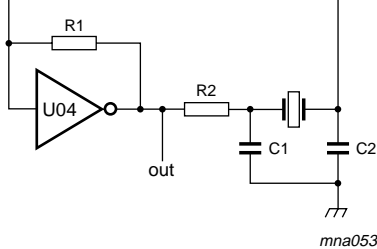
Fig 12. Forward transconductance as a function of the supply voltage

### 14. Application information

Some applications are:

- Linear amplifier (see [Figure 13](#))
- In crystal oscillator design (see [Figure 14](#))
- Astable multivibrator (see [Figure 15](#))

**Remark:** All values given are typical unless otherwise specified.

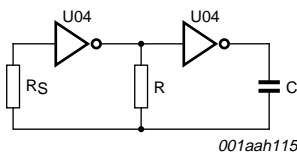
 <p>Maximum <math>V_{o(p-p)} = V_{CC} - 1.5 \text{ V}</math> centered at <math>0.5V_{CC}</math>.</p> $G_v = -\frac{G_{ol}}{1 + \frac{R1}{R2}(1 + G_{ol})}$ <p><math>G_{ol}</math> = open loop gain  <math>G_v</math> = voltage gain  <math>C_i</math>, see <a href="#">Figure 16</a>  <math>R1 \geq 3 \text{ k}\Omega</math>, <math>R2 \leq 1 \text{ M}\Omega</math>  <math>Z_L &gt; 10 \text{ k}\Omega</math>; <math>G_{ol} = 20</math> (typical)          Typical unity gain bandwidth product is 5 MHz.</p> <p><b>Fig 13. Linear amplifier</b></p>	 <p><math>C1 = 47 \text{ pF}</math> (typical)  <math>C2 = 22 \text{ pF}</math> (typical)  <math>R1 = 1 \text{ M}\Omega</math> to <math>10 \text{ M}\Omega</math> (typical)  <math>R2</math> optimum value depends on the frequency and required stability against changes in <math>V_{CC}</math> or average minimum <math>I_{CC}</math> (<math>I_{CC}</math> is typically 2 mA at <math>V_{CC} = 3 \text{ V}</math> and <math>f_i = 1 \text{ MHz}</math>).          See <a href="#">Table 10</a> and <a href="#">Table 11</a></p> <p><b>Fig 14. Crystal oscillator</b></p>
--	--

**Table 10. External components for oscillator (f < 1 MHz)**  
 All values given are typical and must be used as an initial set-up.

Frequency	R1	R2	C1	C2
10 kHz to 15.9 kHz	2.2 MΩ	220 kΩ	56 pF	20 pF
16 kHz to 24.9 kHz	2.2 MΩ	220 kΩ	56 pF	10 pF
25 kHz to 54.9 kHz	2.2 MΩ	100 kΩ	56 pF	10 pF
55 kHz to 129.9 kHz	2.2 MΩ	100 kΩ	47 pF	5 pF
130 kHz to 199.9 kHz	2.2 MΩ	47 kΩ	47 pF	5 pF
200 kHz to 349.9 kHz	2.2 MΩ	47 kΩ	47 pF	5 pF
350 kHz to 600 kHz	2.2 MΩ	47 kΩ	47 pF	5 pF

Table 11. Optimum value for R2

Frequency	R2	Optimum for
3 kHz	2.0 kΩ	minimum required I <sub>CC</sub>
	8.0 kΩ	minimum influence due to change in V <sub>CC</sub>
6 kHz	1.0 kΩ	minimum required I <sub>CC</sub>
	4.7 kΩ	minimum influence due to change in V <sub>CC</sub>
10 kHz	0.5 kΩ	minimum required I <sub>CC</sub>
	2.0 kΩ	minimum influence due to change in V <sub>CC</sub>
14 kHz	0.5 kΩ	minimum required I <sub>CC</sub>
	1.0 kΩ	minimum influence due to change in V <sub>CC</sub>
>14 kHz	-	replace R2 by C3 with a typical value of 35 pF

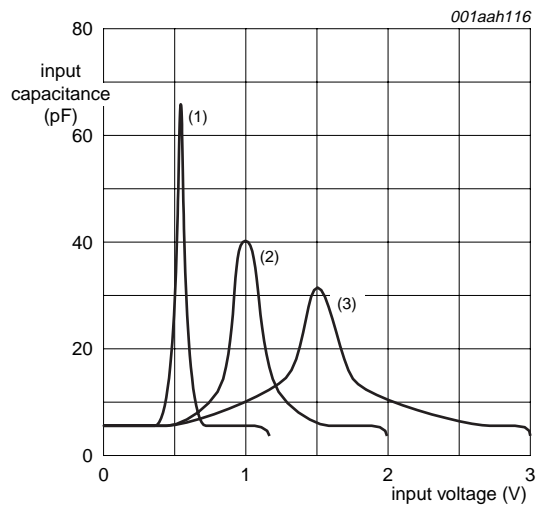


$$f = \frac{1}{T} \approx \frac{1}{2.2RC}$$

$$R_S \approx 2 \times R$$

The average I<sub>CC</sub> (mA) is approximately 3.5 + 0.05 x f (MHz) x C (pF) at V<sub>CC</sub> = 3.0 V.

Fig 15. Astable multivibrator



V<sub>CC</sub> = 1.2 V  
 V<sub>CC</sub> = 2.0 V  
 V<sub>CC</sub> = 3.0 V  
 T<sub>amb</sub> = 25 °C.

Fig 16. Input capacitance as function of input voltage

15. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1

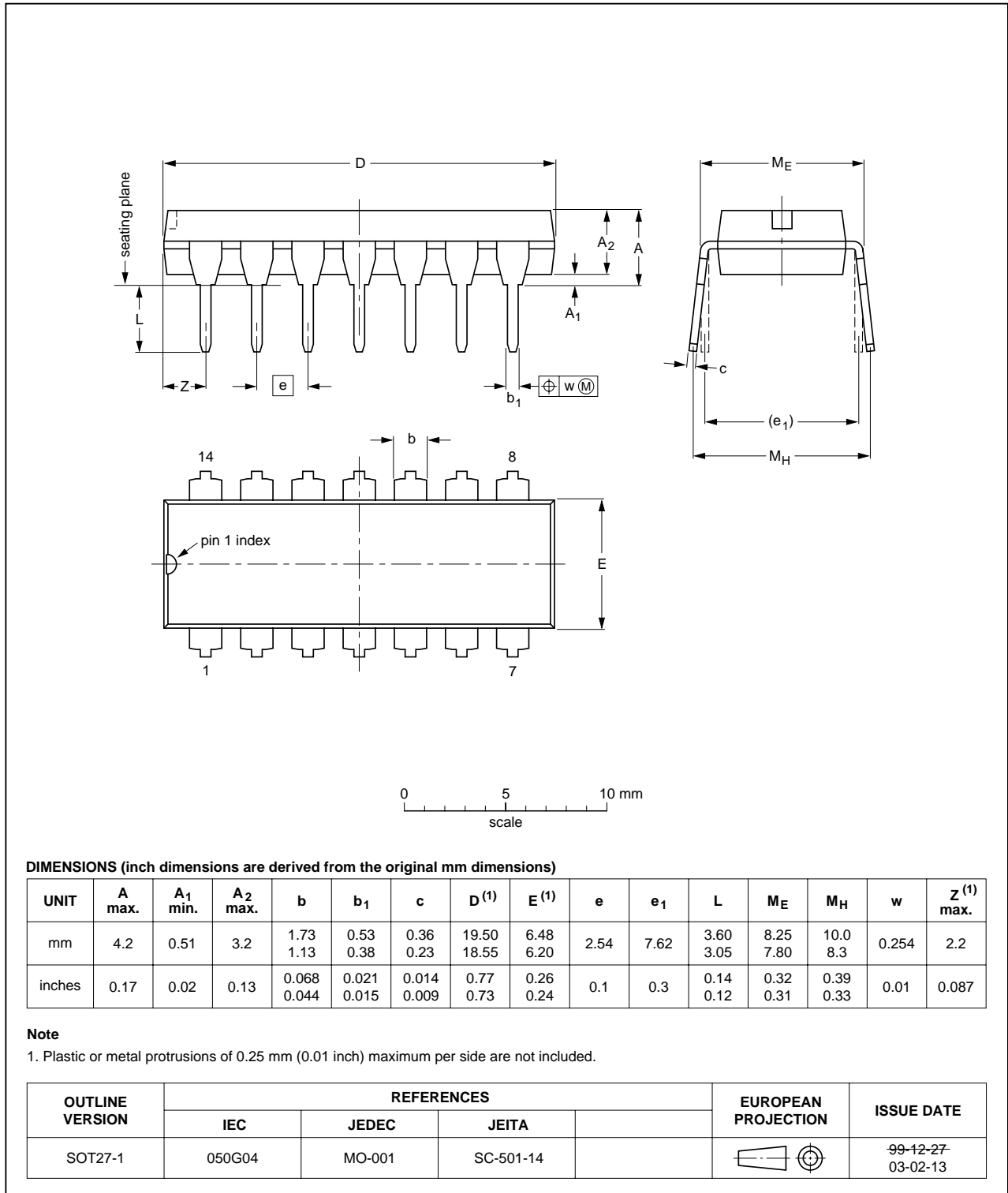


Fig 17. Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

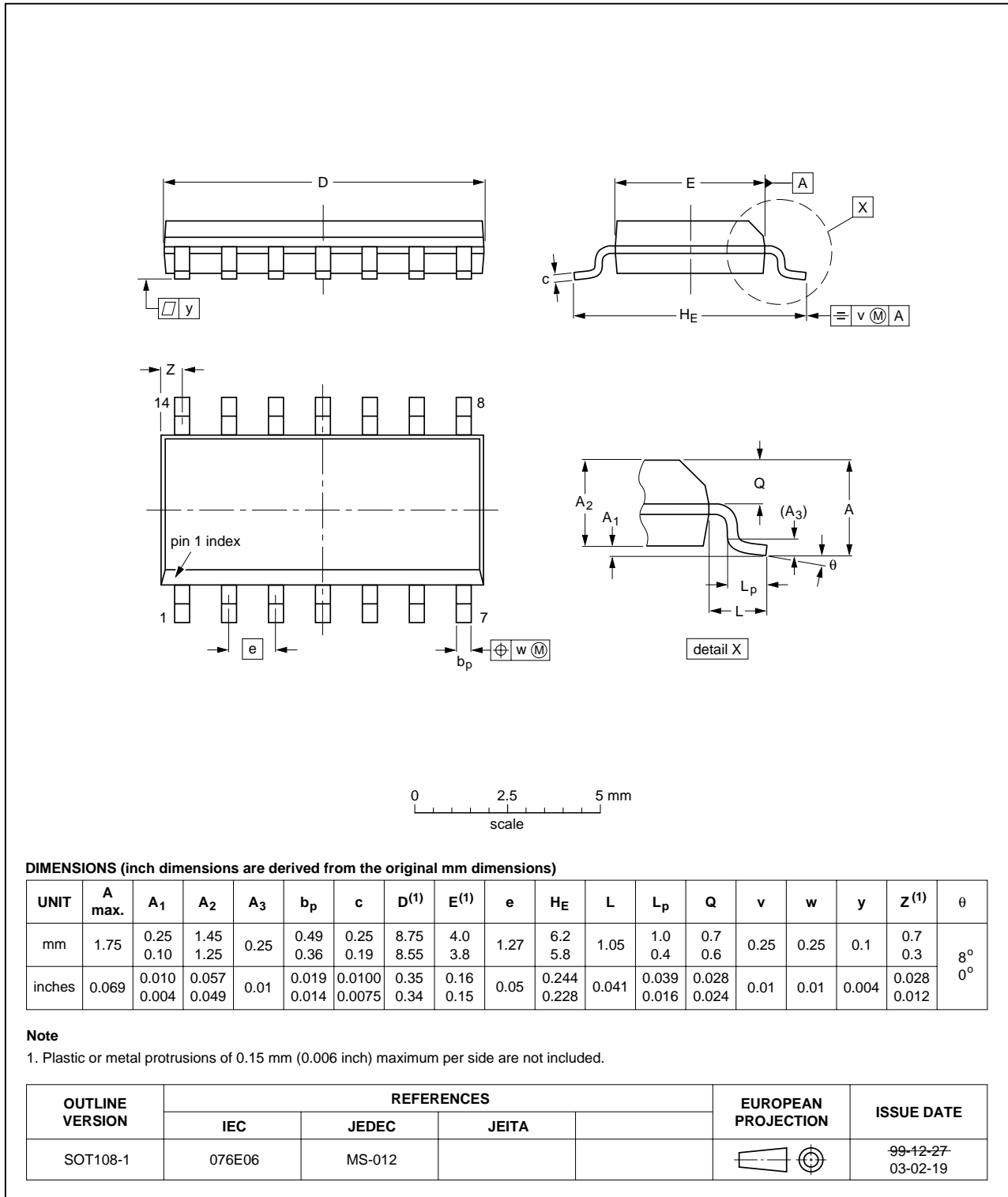


Fig 18. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

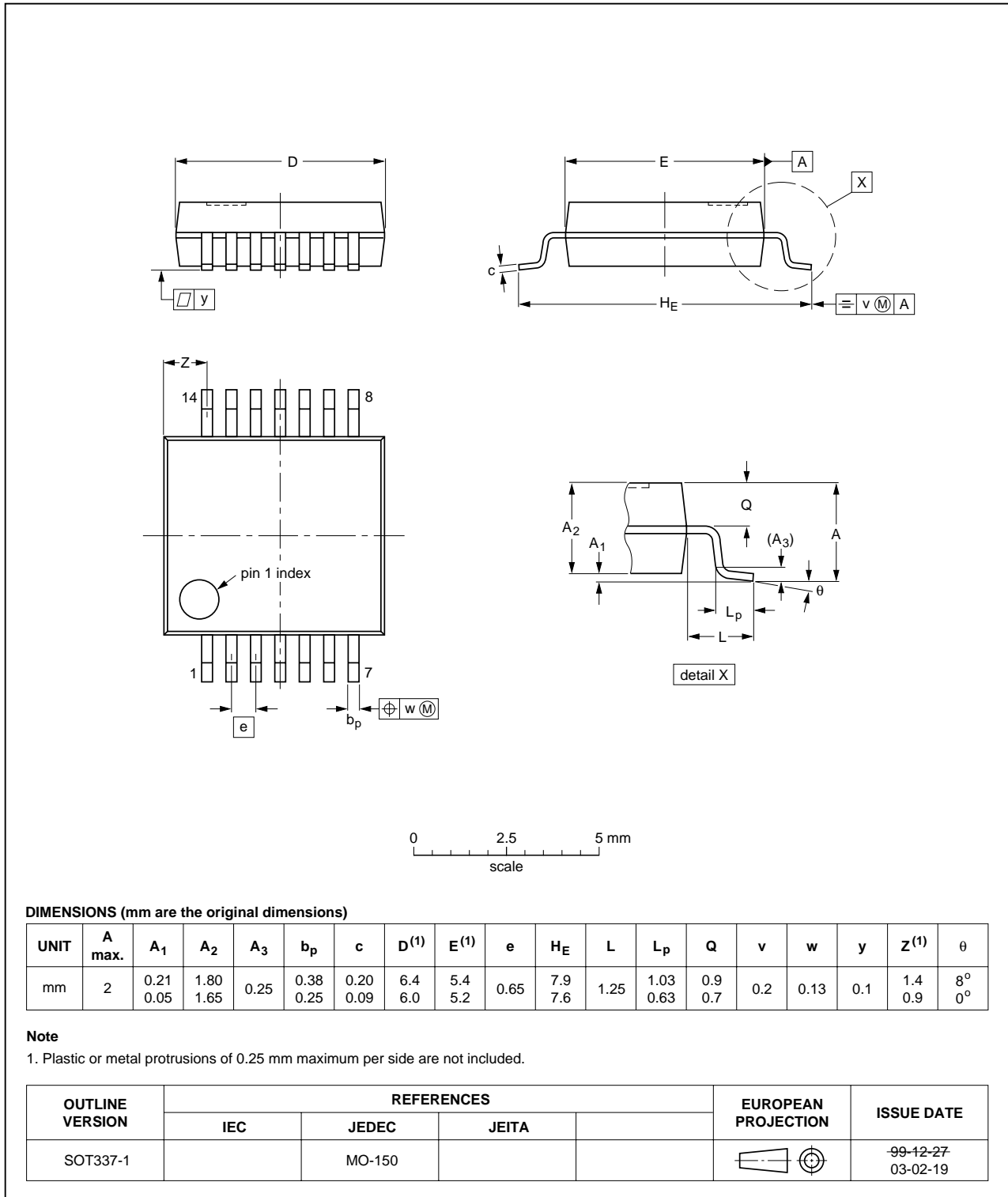


Fig 19. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

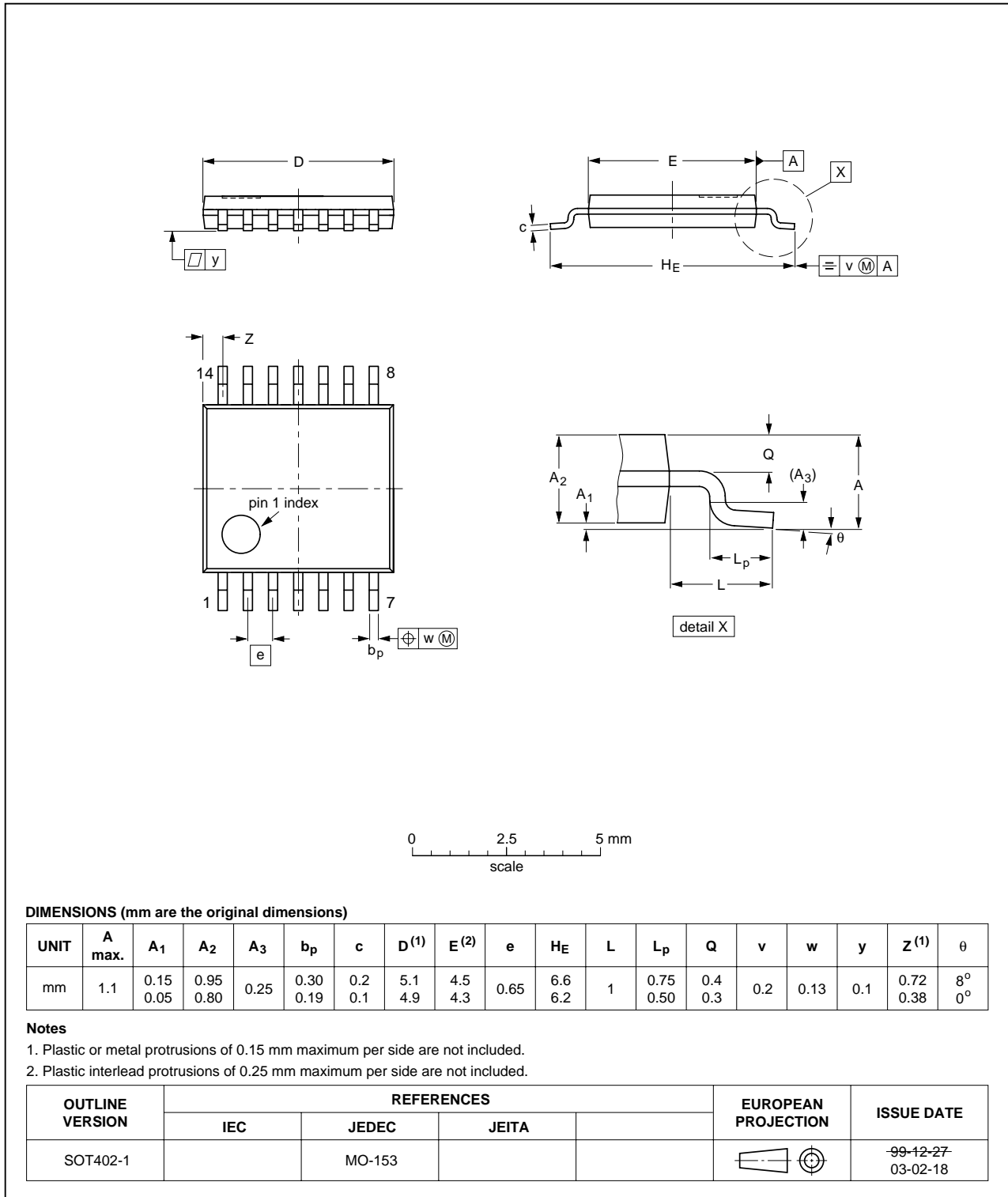


Fig 20. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

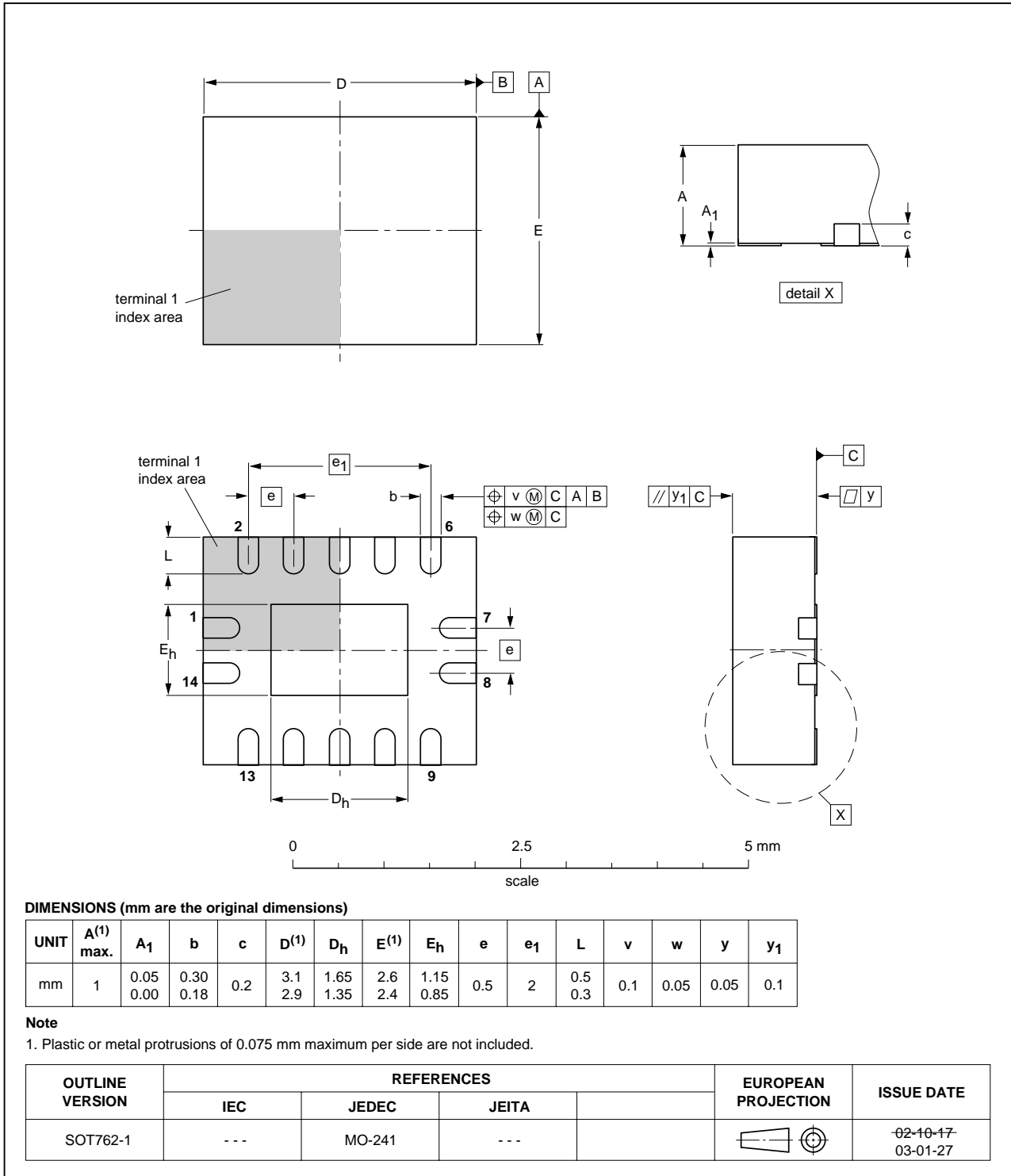


Fig 21. Package outline SOT762-1 (DHVQFN14)



## 16. Abbreviations

Table 12. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 17. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVU04_6	20071220	Product data sheet	-	74LVU04_5
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Section 4</a>: DHVQFN14 package added.</li> <li><a href="#">Section 8</a>: derating values added for DHVQFN14 package.</li> <li><a href="#">Section 15</a>: outline drawing added for DHVQFN14 package.</li> </ul>			
74LVU04_5	20010111	Product specification	-	74LVU04_4
74LVU04_4	20001218	Product specification	-	74LVU04_3
74LVU04_3	19980420	Product specification	-	74LVU04_1
74LVU04_1	19970212	Product specification	-	-

## 18. Legal information

### 18.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 18.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

### 18.3 Disclaimers

**General** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Terms and conditions of sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

### 18.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 19. Contact information

For additional information, please visit: <http://www.nxp.com>

For sales office addresses, send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

20. Contents

1 General description . . . . . 1

2 Features . . . . . 1

3 Applications . . . . . 1

4 Ordering information . . . . . 2

5 Functional diagram . . . . . 2

6 Pinning information . . . . . 3

6.1 Pinning . . . . . 3

6.2 Pin description . . . . . 3

7 Functional description . . . . . 4

8 Limiting values . . . . . 4

9 Recommended operating conditions . . . . . 5

10 Static characteristics . . . . . 5

11 Dynamic characteristics . . . . . 6

12 Waveforms . . . . . 7

13 Transfer characteristics . . . . . 8

14 Application information . . . . . 10

15 Package outline . . . . . 12

16 Abbreviations . . . . . 17

17 Revision history . . . . . 17

18 Legal information . . . . . 18

18.1 Data sheet status . . . . . 18

18.2 Definitions . . . . . 18

18.3 Disclaimers . . . . . 18

18.4 Trademarks . . . . . 18

19 Contact information . . . . . 18

20 Contents . . . . . 19

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

