74LV4094

8-stage shift-and-store bus register

Rev. 02 — 29 June 2006 Product data sheet

1. General description

The 74LV4094 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC4094, 74HCT4094.

The 74LV4094 is an 8-stage serial shift register having a storage latch associated with each stage for strobing data from the serial input (D) to the parallel buffered 3-state outputs (QP0 to QP7). The parallel outputs may be connected directly to the common bus lines. Data is shifted on the positive-going clock (CP) transitions. The data in each shift register is transferred to the storage register when the strobe input (STR) is HIGH. Data in the storage register appears at the outputs whenever the output enable input (OE) signal is HIGH. Two serial outputs (QS1 and QS2) are available for cascading a number of 74LV4094 devices. Data is available at QS1 on the positive-going clock edges to allow high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information is available at QS2 on the next negative going clock edge and is for cascading 74LV4094 devices when the clock rise time is slow.

2. Features

- Optimized for low voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C
- Typical V_{OHV} (V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C
- ESD protection:
  - HBM EIA/JESD22-A114-C exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
- Specified from –40 °C to +85 °C and –40 °C to +125 °C

3. Applications

- Serial-to-parallel data conversion
- Remote control holding register

PHILIPS

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV4094N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74LV4094D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LV4094DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74LV4094PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

5. Functional diagram

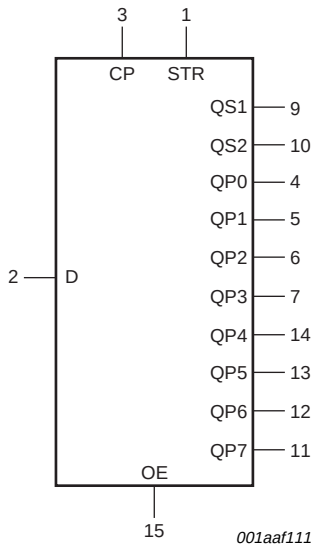


Fig 1. Logic symbol

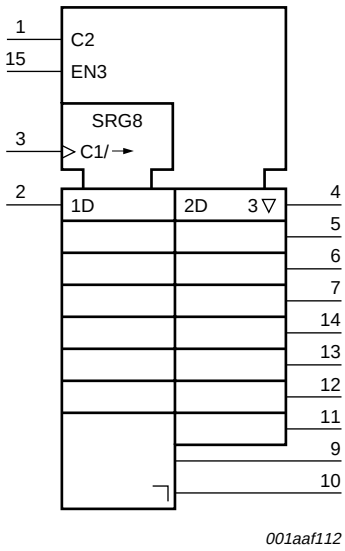


Fig 2. IEC logic symbol

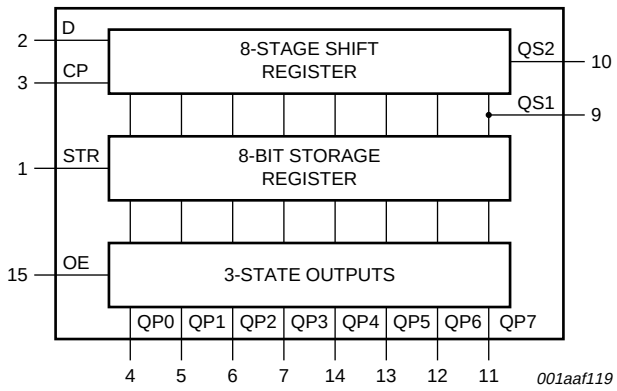


Fig 3. Functional diagram

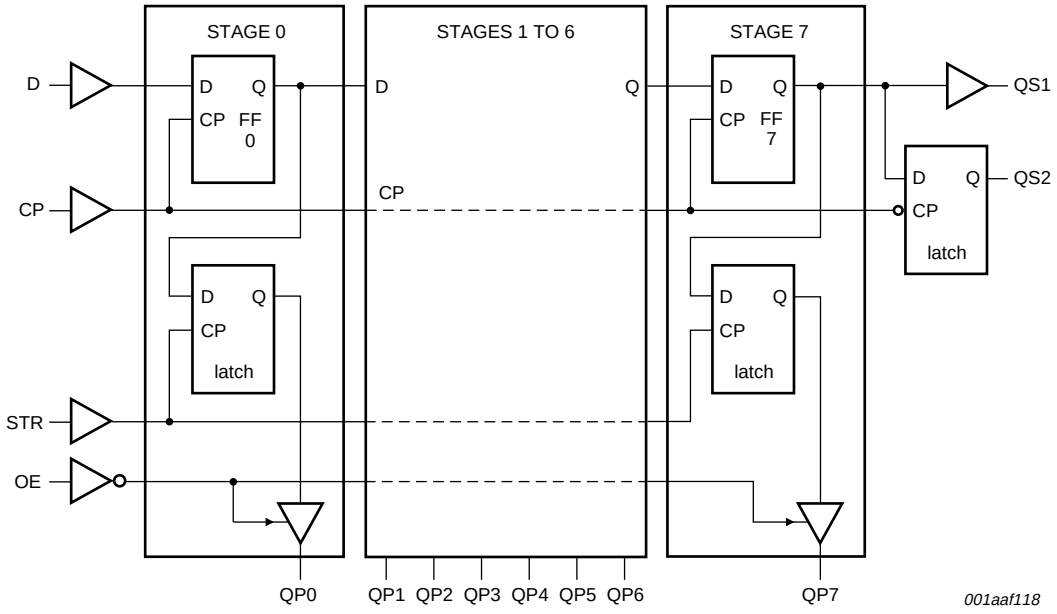


Fig 4. Logic diagram

6. Pinning information

6.1 Pinning

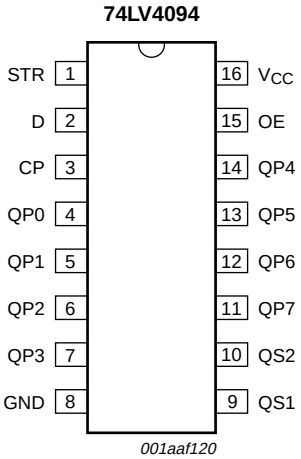


Fig 5. Pin configuration DIP16, SO16 and (T)SSOP16

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
STR	1	data strobe input
D	2	data serial input
CP	3	clock input (edge triggered LOW-to-HIGH)
QP0	4	data parallel output 0
QP1	5	data parallel output 1
QP2	6	data parallel output 2
QP3	7	data parallel output 3
GND	8	ground (0 V)
QS1	9	data serial output 1
QS2	10	data serial output 2
QP7	11	data parallel output 7
QP6	12	data parallel output 6
QP5	13	data parallel output 5
QP4	14	data parallel output 4
OE	15	output enable input
V_{CC}	16	supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state; n.c. = no change;
↑ = LOW-to-HIGH clock transition; ↓ = HIGH-to-LOW clock transition.

Input				Parallel output		Serial output	
CP	OE	STR	D	QP0	QPn	QS1[1]	QS2
↑	L	X	X	Z	Z	QS6	n.c.
↓	L	X	X	Z	Z	n.c.	QP7
↑	H	L	X	n.c.	n.c.	QS6	n.c.
↑	H	H	L	L	QPn–1	QS6	n.c.
↑	H	H	H	H	QPn–1	QS6	n.c.
↓	H	H	H	n.c.	n.c.	n.c.	QP7

[1] QS6 = the information in the 7th register stage is transferred to the 8th register stage and QS1, QS2 clock edge.

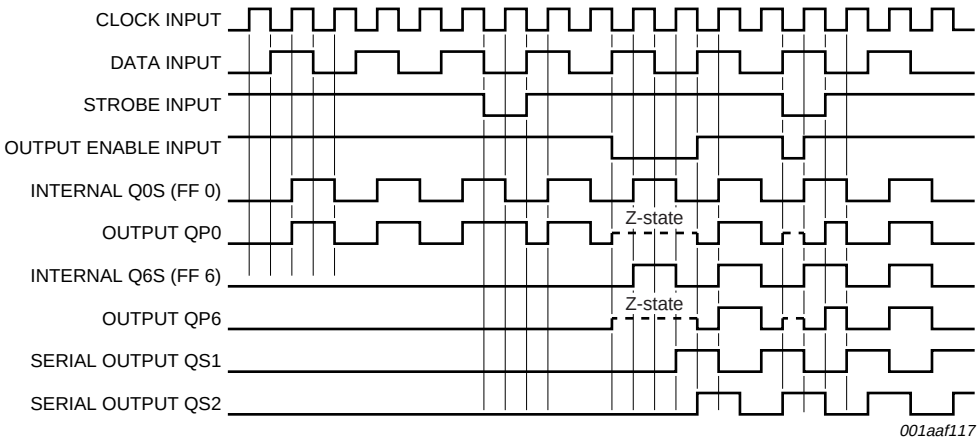


Fig 6. Timing diagram

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V		-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V		-	±50	mA
I_O	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5$ V)	[1]	-	±25	mA
I_{CC}	quiescent supply current			-	50	mA
I_{GND}	ground current			-	–50	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C				
	DIP16 package		[2]	-	750	mW
	SO16 package		[3]	-	500	mW
	(T)SSOP16 package		[4]	-	400	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[3] SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

[4] (T)SSOP16 package: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage		[1]	1.0	3.3	3.6	V
V_I	input voltage			0	-	V_{CC}	V
V_O	output voltage			0	-	V_{CC}	V
T_{amb}	ambient temperature	in free air		–40	-	+125	°C
t_r, t_f	input rise and fall time	V_{CC} = 1.0 V to 2.0 V		-	-	500	ns/V
		V_{CC} = 2.0 V to 2.7 V		-	-	200	ns/V
		V_{CC} = 2.7 V to 3.6 V		-	-	100	ns/V

[1] The static characteristics are guaranteed from V_{CC} = 1.2 V to V_{CC} = 5.5 V, but LV devices are guaranteed function down to V_{CC} = 1.0 V (with input levels GND or V_{CC}).

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C[1]						
V_{IH}	HIGH-state input voltage	V_{CC} = 1.2 V	V_{CC}	0.6	-	V
		V_{CC} = 2.0 V	1.4	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 1.2 V	-	0.4	GND	V
		V_{CC} = 2.0 V	-	-	0.6	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V
V_{OH}	HIGH-state output voltage	V_I = V_{IH} or V_{IL}; all pins				
		I_O = –100 µA; V_{CC} = 1.2 V	-	1.2	-	V
		I_O = –100 µA; V_{CC} = 2.0 V	1.8	2.0	-	V
		I_O = –100 µA; V_{CC} = 2.7 V	2.5	2.7	-	V
		I_O = –100 µA; V_{CC} = 3.0 V	2.8	3.0	-	V
		V_I = V_{IH} or V_{IL}; pins QPn				
		I_O = –6 mA; V_{CC} = 3.0 V	2.40	2.82	-	V
V_{OL}	LOW-state output voltage	V_I = V_{IH} or V_{IL}; all pins				
		I_O = 100 µA; V_{CC} = 1.2 V	-	0	-	V
		I_O = 100 µA; V_{CC} = 2.0 V	-	0	0.2	V
		I_O = 100 µA; V_{CC} = 2.7 V	-	0	0.2	V
		I_O = 100 µA; V_{CC} = 3.0 V	-	0	0.2	V
		V_I = V_{IH} or V_{IL}; pins QPn				
		I_O = 6 mA; V_{CC} = 3.0 V	-	0.25	0.40	V
I_{LI}	input leakage current	V_I = V_{CC} or GND; V_{CC} = 3.6 V	-	-	1.0	µA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND; V_{CC} = 3.6 V	-	-	5	µA

Table 6. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 3.6$ V	-	-	20.0	µA
ΔI_{CC}	additional quiescent supply current	per input; $V_I = V_{CC} - 0.6$ V; $V_{CC} = 2.7$ V to 3.6 V	-	-	500	µA
C_i	input capacitance		-	-	3.5	pF
$T_{amb} = -40$ °C to +125 °C						
V_{IH}	HIGH-state input voltage	$V_{CC} = 1.2$ V	V_{CC}	-	-	V
		$V_{CC} = 2.0$ V	1.4	-	-	V
		$V_{CC} = 2.7$ V to 3.6 V	2.0	-	-	V
V_{IL}	LOW-state input voltage	$V_{CC} = 1.2$ V	-	-	GND	V
		$V_{CC} = 2.0$ V	-	-	0.6	V
		$V_{CC} = 2.7$ V to 3.6 V	-	-	0.8	V
V_{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}; all pins				
		$I_O = -100$ µA; $V_{CC} = 1.2$ V	-	-	-	V
		$I_O = -100$ µA; $V_{CC} = 2.0$ V	1.8	-	-	V
		$I_O = -100$ µA; $V_{CC} = 2.7$ V	2.5	-	-	V
		$I_O = -100$ µA; $V_{CC} = 3.0$ V	2.8	-	-	V
		$V_I = V_{IH}$ or V_{IL}; pins QPn				
		$I_O = -6$ mA; $V_{CC} = 3.0$ V	2.20	-	-	V
V_{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}; all pins				
		$I_O = 100$ µA; $V_{CC} = 1.2$ V	-	-	-	V
		$I_O = 100$ µA; $V_{CC} = 2.0$ V	-	-	0.2	V
		$I_O = 100$ µA; $V_{CC} = 2.7$ V	-	-	0.2	V
		$I_O = 100$ µA; $V_{CC} = 3.0$ V	-	-	0.2	V
		$V_I = V_{IH}$ or V_{IL}; pins QPn				
		$I_O = 6$ mA; $V_{CC} = 3.0$ V	-	-	0.50	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 3.6$ V	-	-	1.0	µA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND; $V_{CC} = 3.6$ V	-	-	10	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 3.6$ V	-	-	160	µA
ΔI_{CC}	additional quiescent supply current	per input; $V_I = V_{CC} - 0.6$ V; $V_{CC} = 2.7$ V to 3.6 V	-	-	850	µA

[1] All typical values are measured at $T_{amb} = 25$ °C.

11. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 11.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C [1]							
t_{PHL}, t_{PLH}	propagation delay CP to QS1	see Figure 7					
		V_{CC} = 1.2 V		-	90	-	ns
		V_{CC} = 2.0 V		-	31	58	ns
		V_{CC} = 2.7 V		-	23	43	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	-	17	34	ns
		V_{CC} = 3.3 V; C_L = 15 pF		-	14	-	ns
t_{PHL}, t_{PLH}	propagation delay CP to QS2	see Figure 7					
		V_{CC} = 1.2 V		-	80	-	ns
		V_{CC} = 2.0 V		-	27	51	ns
		V_{CC} = 2.7 V		-	20	38	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	-	14	30	ns
		V_{CC} = 3.3 V; C_L = 15 pF		-	13	-	ns
t_{PHL}, t_{PLH}	propagation delay CP to QPn	see Figure 7					
		V_{CC} = 1.2 V		-	115	-	ns
		V_{CC} = 2.0 V		-	39	75	ns
		V_{CC} = 2.7 V		-	29	55	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	-	22	44	ns
		V_{CC} = 3.3 V; C_L = 15 pF		-	18	-	ns
t_{PHL}, t_{PLH}	propagation delay STR to QPn	see Figure 8					
		V_{CC} = 1.2 V		-	105	-	ns
		V_{CC} = 2.0 V		-	36	68	ns
		V_{CC} = 2.7 V		-	26	50	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	-	20	40	ns
		V_{CC} = 3.3 V; C_L = 15 pF		-	17	-	ns
t_{PZH}, t_{PZL}	3-state output enable time OE to QPn	see Figure 9					
		V_{CC} = 1.2 V		-	100	-	ns
		V_{CC} = 2.0 V		-	34	65	ns
		V_{CC} = 2.7 V		-	25	48	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	-	19	38	ns
t_{PHZ}, t_{PLZ}	3-state output disable time OE to QPn	see Figure 9					
		V_{CC} = 1.2 V		-	65	-	ns
		V_{CC} = 2.0 V		-	24	40	ns
		V_{CC} = 2.7 V		-	18	32	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	-	14	26	ns

Table 7. Dynamic characteristics *…continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 11.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_W	pulse width CP HIGH or LOW	see Figure 7					
		V_{CC} = 2.0 V		34	9	-	ns
		V_{CC} = 2.7 V		25	6	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	20	5	-	ns
t_W	pulse width STR HIGH	see Figure 8					
		V_{CC} = 2.0 V		34	9	-	ns
		V_{CC} = 2.7 V		25	6	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	20	5	-	ns
t_{su}	set-up time D to CP	see Figure 8					
		V_{CC} = 1.2 V		-	25	-	ns
		V_{CC} = 2.0 V		22	9	-	ns
		V_{CC} = 2.7 V		16	6	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	13	5	-	ns
t_{su}	set-up time CP to STR	see Figure 8					
		V_{CC} = 1.2 V		-	50	-	ns
		V_{CC} = 2.0 V		43	17	-	ns
		V_{CC} = 2.7 V		31	13	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	25	10	-	ns
t_h	hold time D to CP	see Figure 10					
		V_{CC} = 1.2 V		-	–10	-	ns
		V_{CC} = 2.0 V		5	–4	-	ns
		V_{CC} = 2.7 V		5	–3	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	5	–2	-	ns
t_h	hold time D to STR	see Figure 10					
		V_{CC} = 1.2 V		-	–25	-	ns
		V_{CC} = 2.0 V		5	–9	-	ns
		V_{CC} = 2.7 V		5	–6	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	5	–5	-	ns
f_{max}	maximum input clock frequency	see Figure 7					
		V_{CC} = 2.0 V		14	52	-	MHz
		V_{CC} = 2.7 V		19	70	-	MHz
		V_{CC} = 3.0 V to 3.6 V	[2]	24	87	-	MHz
		V_{CC} = 3.3 V; C_L = 15 pF		-	95	-	MHz
C_{PD}	power dissipation capacitance	V_{CC} = 3.3 V	[3][4]	-	83	-	MHz
T_{amb} = –40 °C to +125 °C							
t_{PHL}, t_{PLH}	propagation delay CP to QS1	see Figure 7					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.0 V		-	-	70	ns
		V_{CC} = 2.7 V		-	-	51	ns
		V_{CC} = 3.0 V to 3.6 V		-	-	41	ns

Table 7. Dynamic characteristics *…continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 11.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHL}, t_{PLH}	propagation delay CP to QS2	see Figure 7				
		V_{CC} = 1.2 V	-	-	-	ns
		V_{CC} = 2.0 V	-	-	61	ns
		V_{CC} = 2.7 V	-	-	45	ns
		V_{CC} = 3.0 V to 3.6 V	-	-	36	ns
t_{PHL}, t_{PLH}	propagation delay CP to QPn	see Figure 7				
		V_{CC} = 1.2 V	-	-	-	ns
		V_{CC} = 2.0 V	-	-	90	ns
		V_{CC} = 2.7 V	-	-	66	ns
		V_{CC} = 3.0 V to 3.6 V	-	-	53	ns
t_{PHL}, t_{PLH}	propagation delay STR to QPn	see Figure 8				
		V_{CC} = 1.2 V	-	-	-	ns
		V_{CC} = 2.0 V	-	-	82	ns
		V_{CC} = 2.7 V	-	-	60	ns
		V_{CC} = 3.0 V to 3.6 V	-	-	48	ns
t_{PZH}, t_{PZL}	3-state output enable time OE to QPn	see Figure 9				
		V_{CC} = 1.2 V	-	-	-	ns
		V_{CC} = 2.0 V	-	-	77	ns
		V_{CC} = 2.7 V	-	-	56	ns
		V_{CC} = 3.0 V to 3.6 V	-	-	45	ns
t_{PHZ}, t_{PLZ}	3-state output disable time OE to QPn	see Figure 9				
		V_{CC} = 1.2 V	-	-	-	ns
		V_{CC} = 2.0 V	-	-	49	ns
		V_{CC} = 2.7 V	-	-	37	ns
		V_{CC} = 3.0 V to 3.6 V	-	-	30	ns
t_W	pulse width CP HIGH or LOW	see Figure 7				
		V_{CC} = 2.0 V	41	-	-	ns
		V_{CC} = 2.7 V	30	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	24	-	-	ns
t_W	pulse width STR HIGH	see Figure 8				
		V_{CC} = 2.0 V	41	-	-	ns
		V_{CC} = 2.7 V	30	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	24	-	-	ns
t_{su}	set-up time D to CP	see Figure 8				
		V_{CC} = 1.2 V	-	-	-	ns
		V_{CC} = 2.0 V	26	-	-	ns
		V_{CC} = 2.7 V	19	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	15	-	-	ns

Table 7. Dynamic characteristics *…continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 11.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{su}	set-up time CP to STR	see Figure 8				
		V_{CC} = 1.2 V	-	-	-	ns
		V_{CC} = 2.0 V	51	-	-	ns
		V_{CC} = 2.7 V	38	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	30	-	-	ns
t_h	hold time D to CP	see Figure 10				
		V_{CC} = 1.2 V	-	-	-	ns
		V_{CC} = 2.0 V	5	-	-	ns
		V_{CC} = 2.7 V	5	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	5	-	-	ns
t_h	hold time D to STR	see Figure 10				
		V_{CC} = 1.2 V	-	-	-	ns
		V_{CC} = 2.0 V	5	-	-	ns
		V_{CC} = 2.7 V	5	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	5	-	-	ns
f_{max}	maximum input clock frequency	see Figure 7				
		V_{CC} = 2.0 V	12	-	-	MHz
		V_{CC} = 2.7 V	16	-	-	MHz
		V_{CC} = 3.0 V to 3.6 V	20	-	-	MHz

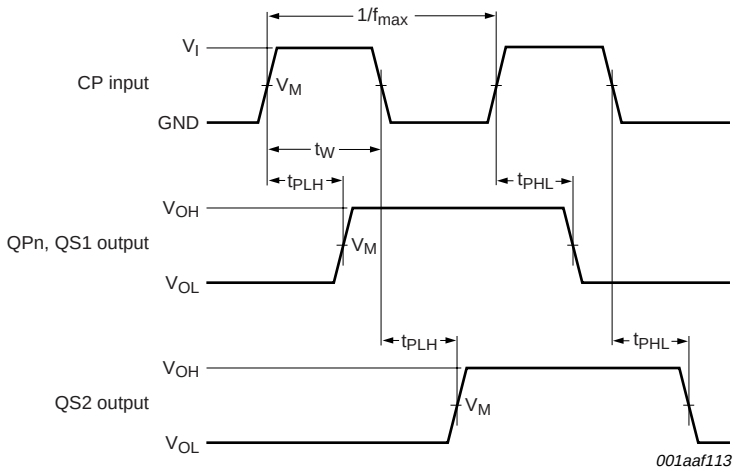
[1] All typical values are measured at T_{amb} = 25 °C.

[2] Typical value measured at V_{CC} = 3.3 V.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[4] The condition is V_I = GND to V_{CC}.

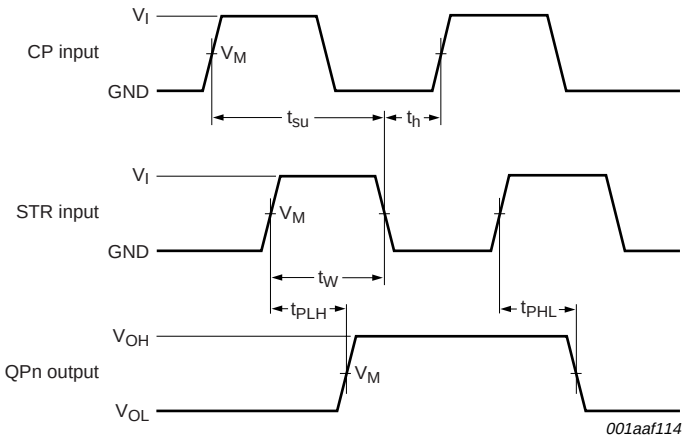
12. Waveforms



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

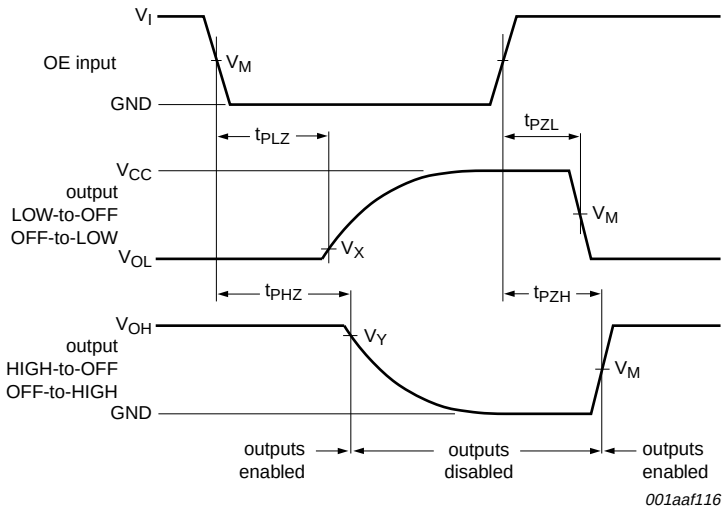
Fig 7. Propagation delay clock (CP) to output (QPn, QS1, QS2), clock pulse width and maximum clock frequency



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

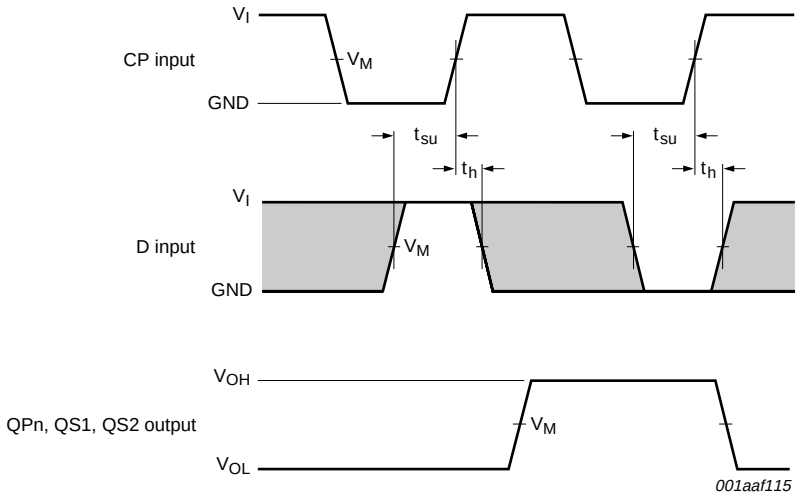
Fig 8. Strobe (STR) to output (QPn) propagation delays and the strobe pulse width and the clock set-up and hold times for strobe input



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig 9. 3-state output enable and disable times for input OE



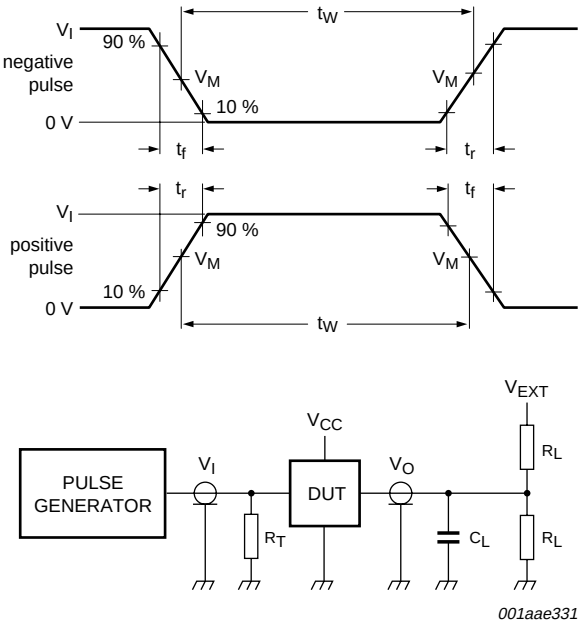
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig 10. Data set-up and hold times for the data input (D)

Table 8. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
1.2 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.1 \times V_{CC}$	$V_{OH} + 0.1 \times V_{CC}$
2.0 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.1 \times V_{CC}$	$V_{OH} + 0.1 \times V_{CC}$
2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} + 0.3 V
3.0 V to 3.6 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} + 0.3 V



Test data is given in Table 9.

Definitions test circuit:

R_L = load resistor.

C_L = load capacitance.

R_T = Termination resistance should be equal to output impedance of Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

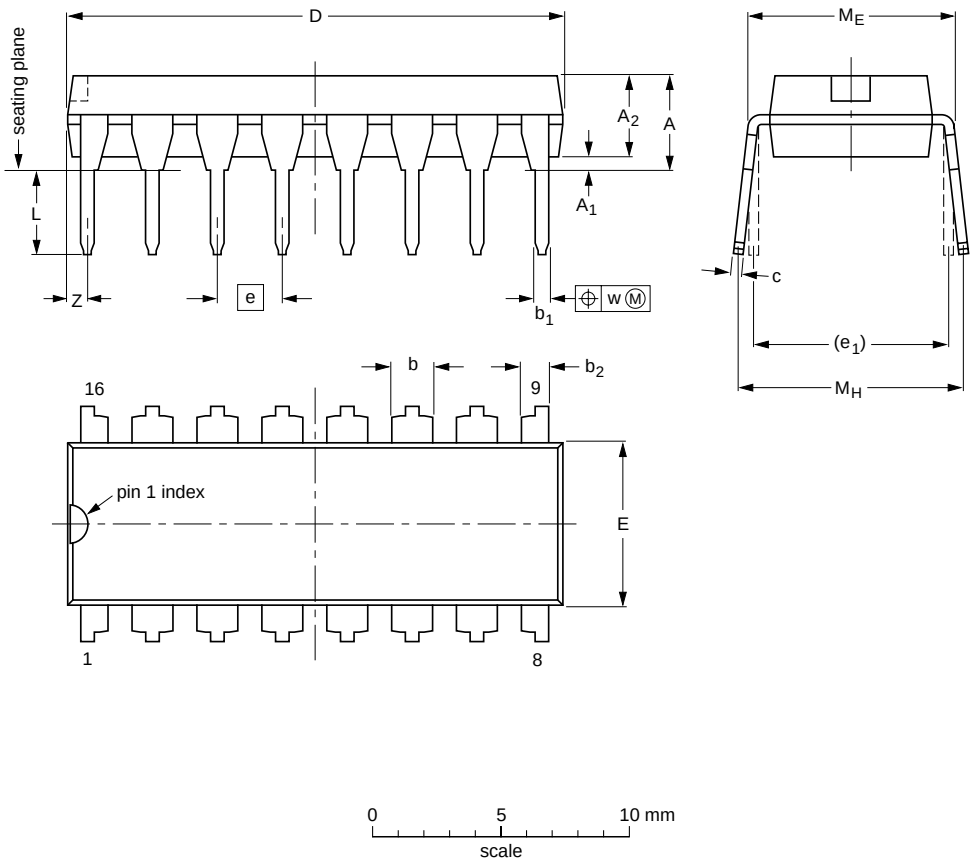
Fig 11. Load circuitry for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
< 2.7 V	V_{CC}	≤ 2.5 ns	50 pF	1 kΩ	GND	$2 \times V_{CC}$	open
2.7 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	1 kΩ	GND	$2 \times V_{CC}$	open

13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

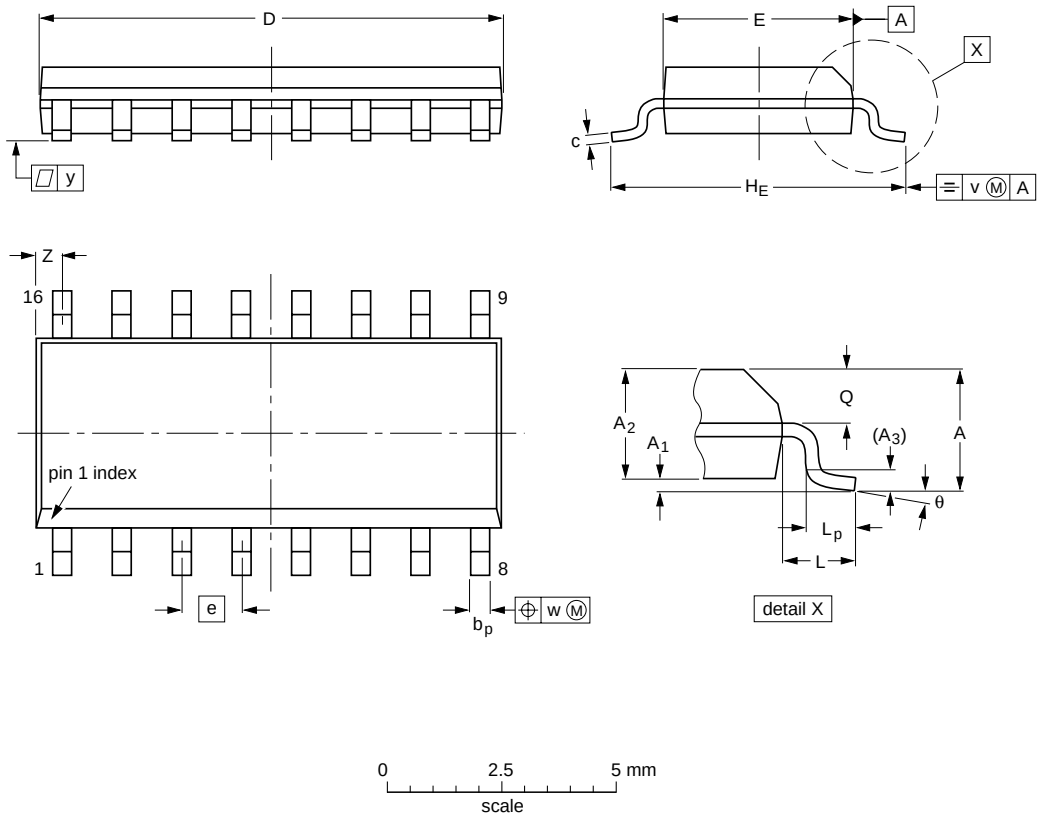
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						~~95-01-14~~ 03-02-13

Fig 12. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

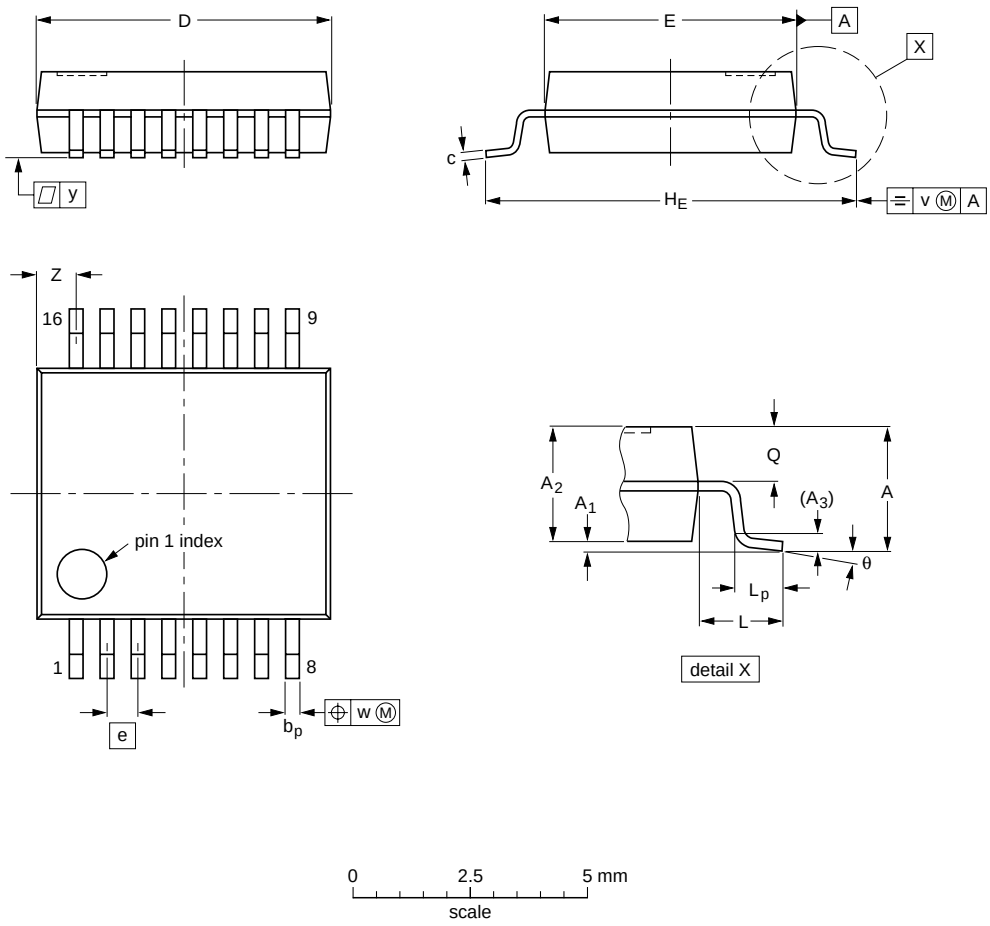
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 13. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

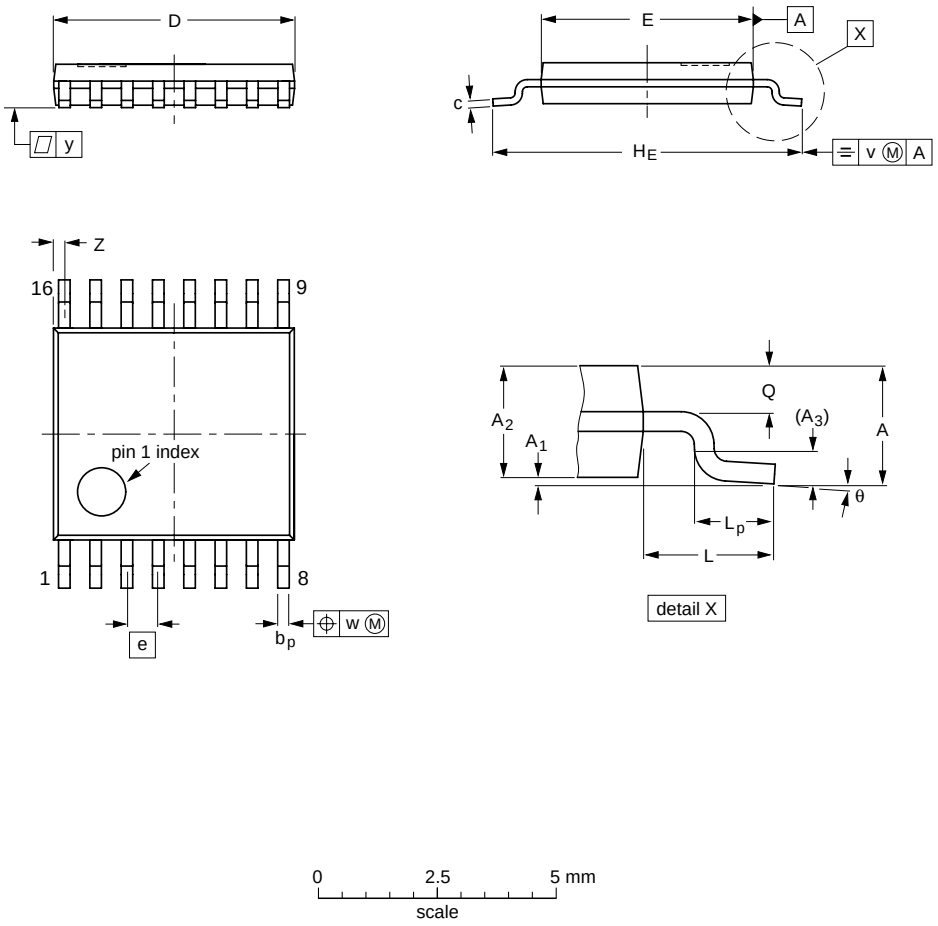
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 14. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 15. Package outline SOT403-1 (TSSOP16)

14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV4094_2	20060629	Product data sheet	-	74LV4094_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors • Section 4: Added type numbers 74LV4094DB and 74LV4094PW			
74LV4094_1	19980623	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.semiconductors.philips.com.

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